COL215 Software Assignment 2

Wiring-aware Gate Positioning

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Circuit:

Gates containing different pins on the left and right sides connected to other Gates

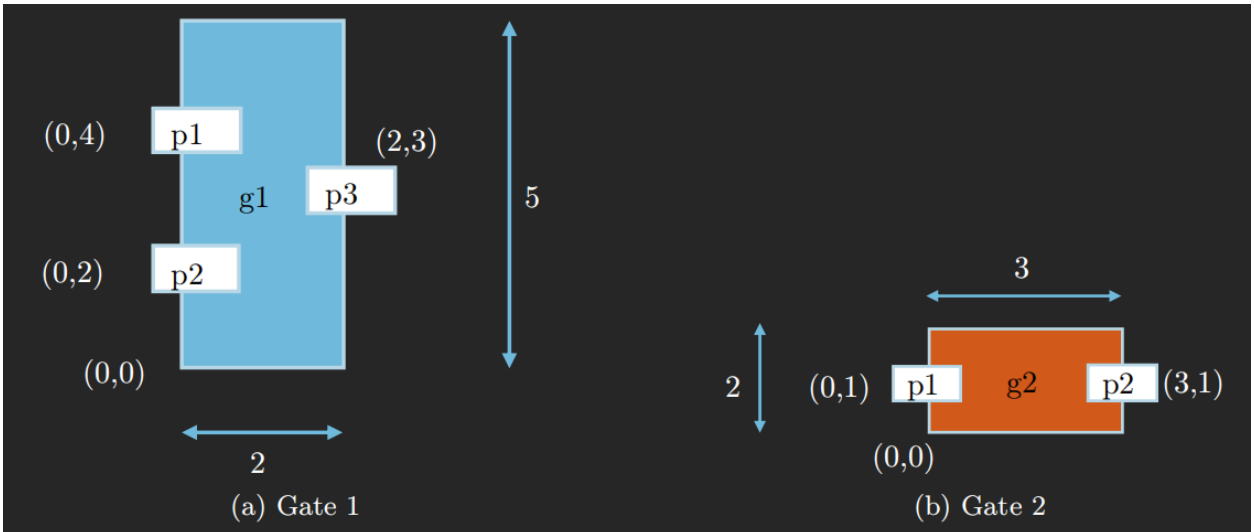


Figure 1: Gate pin specification example

Aim:

Minimize the sum of estimated wire length for all wires in the whole circuit.

Method:

Placing the gates by Brute Force to get the Minimum wire Length.

Procedure:

First, we count the number of connections between every pair of Gates and store and sorted those pairs in descending order of their number of connections.

Then we took out the first element from the list containing the maximum number of connections and called it say pivot and placed it and removed all gates containing this gate from the main list.

We maintain another list other than the main list that contains all the adjacent gates to the gates placed, again we sort this list in decreasing order of their number of connections.

And we choose the largest number of connections gate about the pivot from this second list.

After choosing we try placing the gate about the pivot in its surroundings.

For the up and down directions about the pivot we define a level, i.e. we place gates on a specific level.

After the gate is placed about the pivot, we calculate the wirelength between two gates by iterating over its pins and calculating the absolute distance, i.e. by the Manhattan distance between the coordinates of the two pins.

$$f(w_i) = |x_i^{(1)} - x_i^{(2)}| + |y_i^{(1)} - y_i^{(2)}|$$

Then we repeated the same task.

The way we iterated through every gate requires a connection between each other, so in-order to compensate for the part disconnected, we placed the gates on the right side of the previous part

At the end we calculated the total wire length by adding up all wire Lenths between each pair of Gates

Constraints on INPUT:

- **0 < Number of gates ≤ 1000**
- **0 < Width of gate ≤ 100**
- **0 < Height of gate ≤ 100**
- **0 < Number of pins on one side of a gate ≤ Height of Gate**
- **0 < Total Number of pins ≤ 40000**

Time and Space Complexity Analysis:

G=No. Of Gates, P = No. Of Pins, W = Wiringsq

Total Time Complexity:

- **Input parsing**: O(G+P+W)
- **Sorting gates**: O(GlogG)
- **Placing each gate:** O(G)+O(G)
- **Calculating total wire length**: O(W*G)
- **Bounding box calculation**: O(G)

Overall Time Complexity = O(G^2 + G*W)

Total Space Complexity:

- Storing gates and their connections: O(G+W)
- Storing pins: O(P)
- Temporary variables for sorting and placement: O(G)

Overall Space Complexity = O(G+P+W)

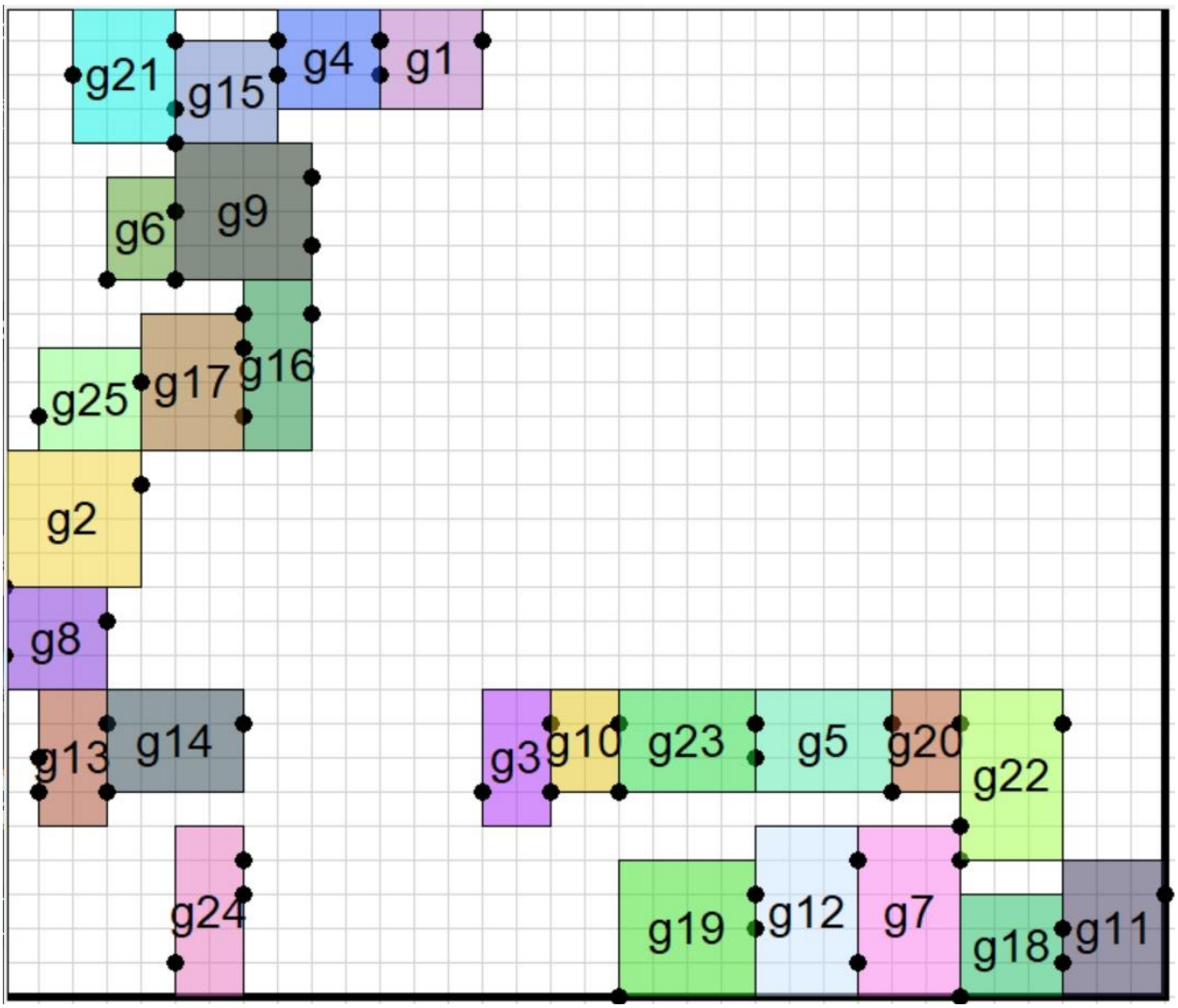
Testing Strategy:

- Will check for small cases, no overlapping should happen
- Will check for medium cases, for efficient working or not
- Will run the code for large gate values too, for confirming time complexity and space complexity
- Will check in each whether disconnected components are placed correctly where it should or not

Test Cases:

Tc 1:

```
g1 3 3
pins g1 0 1 3 2
g2 4 4
pins g2 0 0 4 3
g3 2 4
pins g3 0 1 2 3
g4 3 3
pins g4 0 1 3 2
g5 4 3
pins g5 0 1 4 2 0 2
g6 2 3
pins g6 0 0 2 2
g7 3 5
pins g7 0 1 3 4
g8 3 3
pins g8 0 1 3 2
g9 4 4
pins g9 0 0 4 3 4 1
g10 2 3
pins g10 0 0 2 2
g11 3 4
pins g11 0 1 3 3
g12 3 5
pins g12 0 2 3 4 3 1
g13 2 4
pins g13 0 1 2 3 0 2
g14 4 3
pins g14 0 0 4 2
g15 3 3
pins g15 0 1 3 2 3 3
g16 2 5
pins g16 0 1 2 4
g17 3 4
pins g17 0 2 3 3 3 4
g18 3 3
pins g18 0 0 3 1 3 2
g19 4 4
pins g19 0 0 4 3
g20 2 3
pins g20 0 0 2 2
g21 3 4
pins g21 0 2 3 3 3 0
g22 3 5
pins g22 0 1 3 4
g23 4 3
pins g23 0 0 4 2
g24 2 5
pins g24 0 1 2 4 2 3
g25 3 3
pins g25 0 1 3 2
wire g1.p1 g4.p2
wire g2.p1 g8.p1
wire g3.p2 g10.p1
wire g4.p1 g15.p2
wire g5.p2 g20.p1
wire g6.p2 g9.p1
wire g7.p1 g12.p3
wire g8.p2 g13.p2
wire g9.p3 g16.p1
wire g10.p2 g23.p1
wire g11.p1 g18.p2
wire g12.p1 g19.p2
wire g13.p3 g14.p1
wire g14.p2 g24.p1
wire g15.p3 g21.p2
wire g16.p2 g17.p3
wire g17.p1 g25.p2
wire g18.p3 g22.p1
wire g19.p1 g3.p1
wire g20.p2 g7.p2
wire g21.p3 g6.p2
wire g22.p2 g11.p2
wire g23.p2 g5.p3
wire g24.p3 g9.p2
wire g25.p2 g2.p2
```

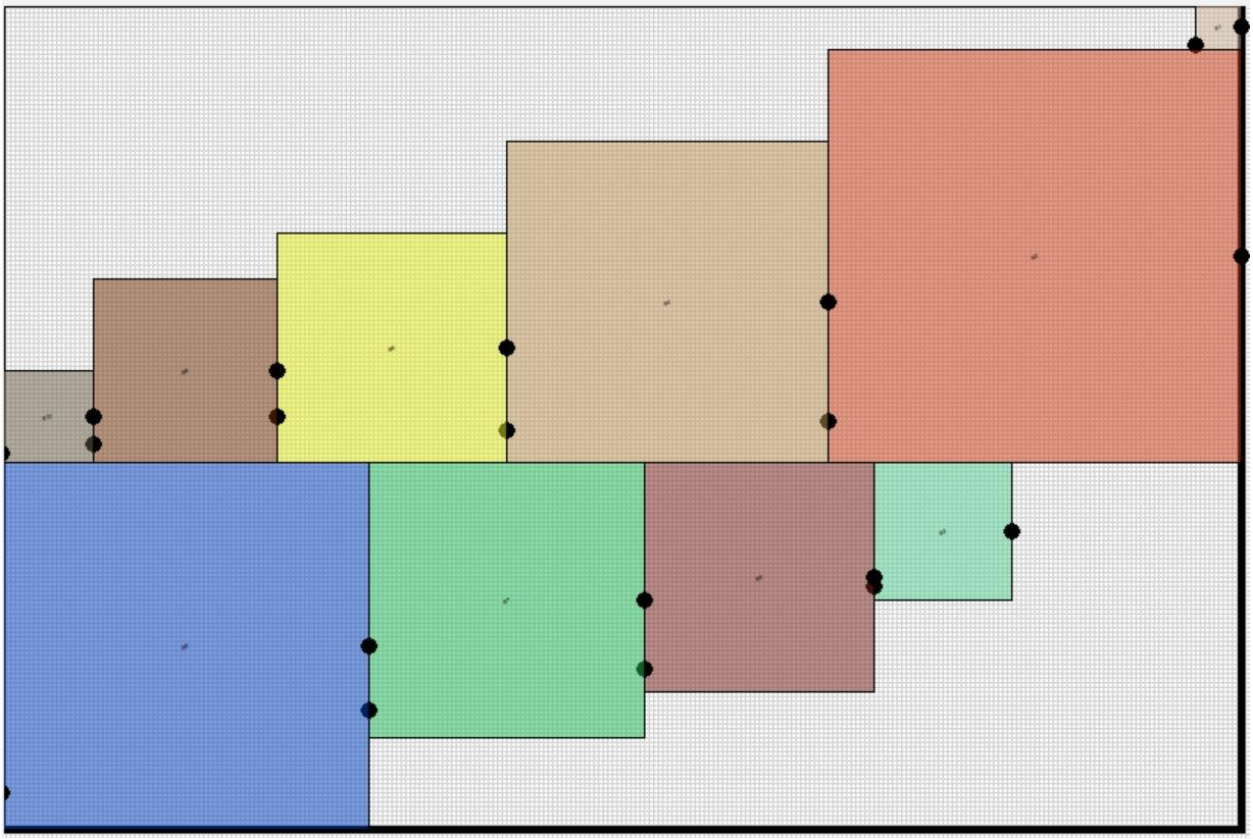


(tc-1)

Motivation: test case given in the Moodle itself, helps in working for disconnected wiring.

Tc 2:

```
g1 10 10
pins g1 0 1 10 5
g2 90 90
pins g2 0 9 90 45
g3 30 30
pins g3 0 3 30 15
g4 70 70
pins g4 0 7 70 35
g5 50 50
pins g5 0 5 50 25
g6 50 50
pins g6 0 10 50 25
g7 60 60
pins g7 0 6 60 30
g8 40 40
pins g8 0 4 40 20
g9 80 80
pins g9 0 8 80 40
g10 20 20
pins g10 0 2 20 10
wire g1.p1 g2.p2
wire g1.p2 g3.p2
wire g2.p1 g4.p2
wire g3.p1 g5.p2
wire g4.p1 g6.p2
wire g5.p1 g7.p2
wire g6.p1 g8.p2
wire g7.p1 g9.p2
wire g8.p1 g10.p2
wire g9.p1 g10.p1
```

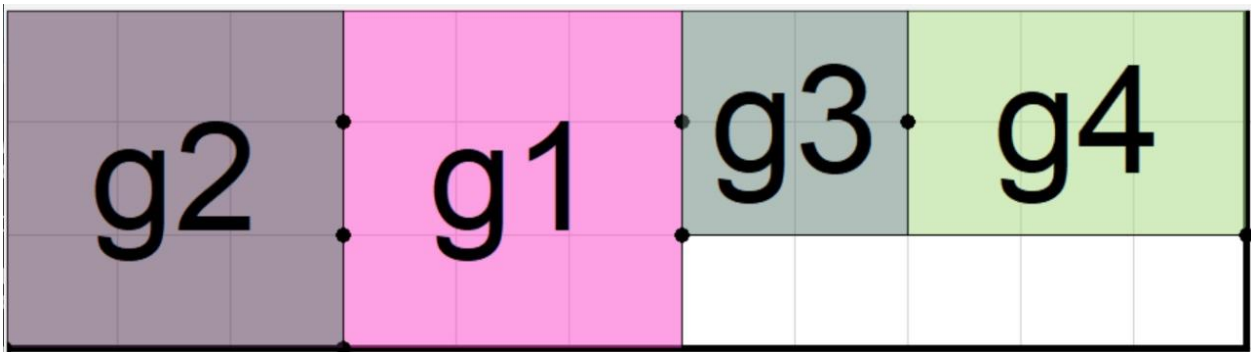


(tc-2)

Motivation: test case generated through AI

Tc 3:

```
g1 3 3
pins g1 0 0 0 1 3 2
g2 3 3
pins g2 0 0 3 1 3 2
g3 2 2
pins g3 0 0 2 1
g4 3 2
pins g4 0 1 3 0
wire g1.p1 g2.p1
wire g2.p2 g3.p1
wire g3.p2 g4.p1
wire g4.p2 g1.p2
```

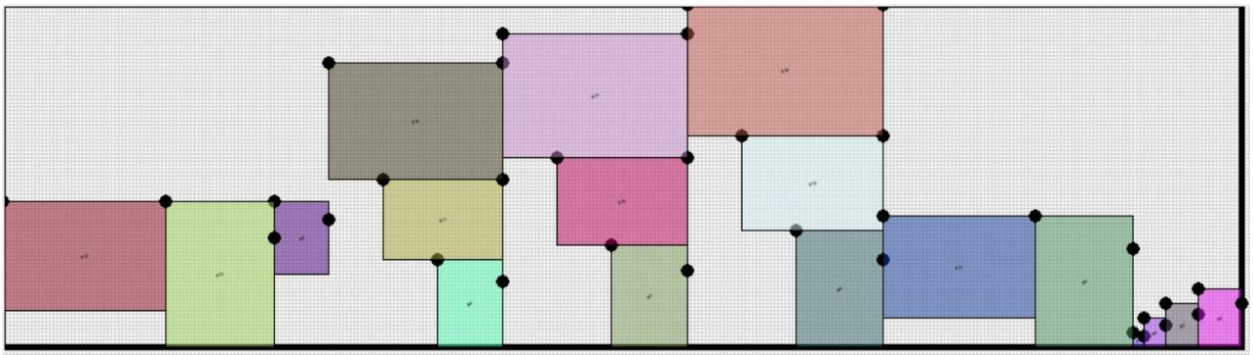


(tc-3)

Motivation: working for the small case and making sure that not overlapping

Tc 4:

```
g1 3 4
pins g1 0 4 3 3
g2 6 8
pins g2 0 8 6 6
g3 9 12
pins g3 0 12 9 9
g4 12 16
pins g4 0 16 12 12
g5 15 20
pins g5 0 20 15 15
g6 18 24
pins g6 0 24 18 18
g7 21 28
pins g7 0 28 21 21
g8 24 16
pins g8 0 16 24 16
g9 27 18
pins g9 0 18 27 18
g10 30 20
pins g10 0 20 30 20
g11 33 22
pins g11 0 22 33 22
g12 36 24
pins g12 0 24 36 24
g13 39 26
pins g13 0 26 39 26
g14 42 28
pins g14 0 28 42 28
g15 45 30
pins g15 0 30 45 30
g16 48 32
pins g16 0 32 48 32
g17 51 34
pins g17 0 34 51 34
g18 54 36
pins g18 0 36 54 36
g19 57 38
pins g19 0 38 57 38
g20 60 40
pins g20 0 40 60 40
g21 63 42
pins g21 0 42 63 42
g22 66 44
pins g22 0 44 66 44
wire g7.p1 g12.p2
wire g8.p1 g13.p2
wire g9.p1 g14.p2
wire g10.p1 g15.p2
wire g11.p1 g16.p2
wire g12.p1 g17.p2
wire g13.p1 g18.p2
wire g14.p1 g19.p2
wire g15.p1 g20.p2
wire g16.p1 g21.p2
wire g17.p1 g22.p2
```

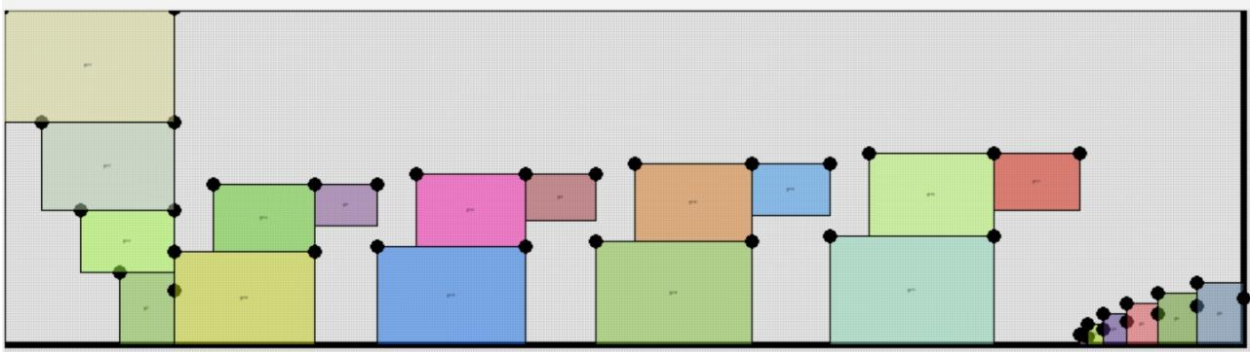


(tc-4)

Motivation: working for multiple symmetric cases and some disconnected components

Tc 5:

```
g1 3 4
pins g1 0 4 3 3
g2 6 8
pins g2 0 8 6 6
g3 9 12
pins g3 0 12 9 9
g4 12 16
pins g4 0 16 12 12
g5 15 20
pins g5 0 20 15 15
g6 18 24
pins g6 0 24 18 18
g7 21 28
pins g7 0 28 21 21
g8 24 16
pins g8 0 16 24 16
g9 27 18
pins g9 0 18 27 18
g10 30 20
pins g10 0 20 30 20
g11 33 22
pins g11 0 22 33 22
g12 36 24
pins g12 0 24 36 24
g13 39 26
pins g13 0 26 39 26
g14 42 28
pins g14 0 28 42 28
g15 45 30
pins g15 0 30 45 30
g16 48 32
pins g16 0 32 48 32
g17 51 34
pins g17 0 34 51 34
g18 54 36
pins g18 0 36 54 36
g19 57 38
pins g19 0 38 57 38
g20 60 40
pins g20 0 40 60 40
g21 63 42
pins g21 0 42 63 42
g22 66 44
pins g22 0 44 66 44
wire g7.p1 g12.p2
wire g8.p1 g13.p2
wire g9.p1 g14.p2
wire g10.p1 g15.p2
wire g11.p1 g16.p2
wire g12.p1 g17.p2
wire g13.p1 g18.p2
wire g14.p1 g19.p2
wire g15.p1 g20.p2
wire g16.p1 g21.p2
wire g17.p1 g22.p2
```



(tc-5)

Motivation: test case with medium number of gates covering different possibilities

Tc 6:

```
g1 3 4
pins g1 0 4 3 3
g2 6 8
pins g2 0 8 6 6
g3 9 12
pins g3 0 12 9 9
g4 12 16
pins g4 0 16 12 12
g5 15 20
pins g5 0 20 15 15
g6 18 24
pins g6 0 24 18 18
g7 21 28
pins g7 0 28 21 21
g8 24 32
pins g8 0 32 24 24
g9 27 36
pins g9 0 36 27 27
g10 30 40
pins g10 0 40 30 30
g11 33 44
pins g11 0 44 33 33
g12 36 48
pins g12 0 48 36 36
g13 39 52
pins g13 0 52 39 39
g14 42 56
pins g14 0 56 42 42
g15 45 60
pins g15 0 60 45 45
g16 48 64
pins g16 0 64 48 48
g17 51 68
pins g17 0 68 51 51
g18 54 72
pins g18 0 72 54 54
g19 57 76
pins g19 0 76 57 57
g20 60 80
pins g20 0 80 60 60
g21 63 42
pins g21 0 42 63 42
g22 66 44
pins g22 0 44 66 44
g23 69 46
pins g23 0 46 69 46
g24 72 48
pins g24 0 48 72 48
g25 75 50
pins g25 0 50 75 50
g26 78 52
pins g26 0 52 78 52
g27 81 54
pins g27 0 54 81 54
g28 84 56
pins g28 0 56 84 56
g29 87 58
pins g29 0 58 87 58
g30 90 60
pins g30 0 60 90 60
g31 93 62
pins g31 0 62 93 62
```

(tc-6)

Motivation: no wire connection between any of the gates, (whole output wasn't in the screen due to visualization file glitch but the working is as expected)

==========END==========