FPGA_TOP_ML505 Project Status (12/11/2013 - 17:40:41)			
Configuration File:	FPGA_TOP_ML505.xreport	**Parser Errors:**	
Module Name:	FPGA_TOP_ML505	**Implementation State:**	Programming File Generated
Target Device:	5vlx110tff1136-1	• **Errors:**	No Errors
Product Version:	ISE 14.6	• **Warnings:**	1028 Warnings (1028 new)
Design Goal:	data unavailable	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	data unavailable	• **Timing Constraints:**	All Constraints Met
Environment:	System Settings	• **Final Timing Score:**	0

Device Utilization Summary [-]				
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	7,006	69,120	10%	
Number used as Flip Flops	7,005			
Number used as Latches	1			
Number of Slice LUTs	14,442	69,120	20%	
Number used as logic	5,249	69,120	7%	
Number using O6 output only	4,606			
Number using O5 output only	419			
Number using O5 and O6	224			
Number used as Memory	9,108	17,920	50%	
Number used as Dual Port RAM	3,016			
Number using O6 output only	2,944			
Number using O5 and O6	72			
Number used as Shift Register	6,092			
Number using O6 output only	5,892			
Number using O5 output only	200			
Number used as exclusive route-thru	85			
Number of route-thrus	521			
Number using O6 output only	503			
Number using O5 output only	18			
Number of occupied Slices	5,273	17,280	30%	
Number of LUT Flip Flop pairs used	16,622			
Number with an unused Flip Flop	9,616	16,622	57%	
Number with an unused LUT	2,180	16,622	13%	
Number of fully used LUT-FF pairs	4,826	16,622	29%	
Number of unique control sets	381			
Number of slice register sites lost to control set restrictions	394	69,120	1%	
Number of bonded IOBs	126	640	19%	
Number of LOCed IOBs	126	126	100%	
IOB Flip Flops	46			
Number of BlockRAM/FIFO	13	148	8%	

Number using BlockRAM only	13			
Number of 18k BlockRAM used	15			
Total Memory used (KB)	270	5,328	5%	
Number of BUFG/BUFGCTRLs	2	32	6%	
Number used as BUFGs	2			
Number of DSP48Es	64	64	100%	
Number of PLL_ADVs	1	6	16%	
Average Fanout of Non-Clock Nets	4.24			

Performance Summary			[-]
Final Timing Score:	0 (Setup: 0, Hold: 0, Component Switching Limit: 0)	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints Met		

Detailed Reports (working directory="/home/cc/cs150/fa013/class/cs150-bn/fa13_team07/hardware/build/FPGA_TOP_ML505/")					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Fri Dec 6 14:09:51 2013	0	992 Warnings (992 new)	167 Infos (167 new)
Translation Report	Current	Fri Dec 6 14:10:20 2013	0	2 Warnings (2 new)	2 Infos (2 new)
Map Report	Current	Fri Dec 6 14:13:24 2013	0	3 Warnings (3 new)	8 Infos (8 new)
Place and Route Report	Current	Fri Dec 6 14:14:55 2013	0	30 Warnings (30 new)	0
Power Report					
Post-PAR Static Timing Report	Current	Fri Dec 6 14:16:28 2013	0	0	3 Infos (3 new)
Bitgen Report	Current	Fri Dec 6 14:15:55 2013	0	1 Warning (1 new)	0

Secondary Reports			[-]
Report Name	**Status**	**Generated**	
WebTalk Report	Current	Fri Dec 6 14:15:56 2013	
WebTalk Log File	Current	Fri Dec 6 14:15:57 2013	

Date Generated: 12/11/2013 - 17:40:42