UpsamplerWrap Project Status (12/06/2013 - 14:01:36)			
Configuration File:	UpsamplerWrap.xreport	**Parser Errors:**	
Module Name:	UpsamplerWrap	**Implementation State:**	Programming File Generated
Target Device:	5vlx110tff1136-1	• **Errors:**	No Errors
Product Version:	ISE 14.6	• **Warnings:**	6 Warnings (6 new)
Design Goal:	data unavailable	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	data unavailable	• **Timing Constraints:**	All Constraints Met
Environment:	System Settings	• **Final Timing Score:**	0

Device Utilization Summary [-]				
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	273	69,120	1%	
Number used as Flip Flops	273			
Number of Slice LUTs	587	69,120	1%	
Number used as logic	193	69,120	1%	
Number using O6 output only	155			
Number using O5 output only	16			
Number using O5 and O6	22			
Number used as Memory	392	17,920	2%	
Number used as Dual Port RAM	192			
Number using O6 output only	192			
Number used as Shift Register	200			
Number using O6 output only	200			
Number used as exclusive route-thru	2			
Number of route-thrus	18			
Number using O6 output only	18			
Number of occupied Slices	216	17,280	1%	
Number of LUT Flip Flop pairs used	702			
Number with an unused Flip Flop	429	702	61%	
Number with an unused LUT	115	702	16%	
Number of fully used LUT-FF pairs	158	702	22%	
Number of unique control sets	33			
Number of slice register sites lost to control set restrictions	23	69,120	1%	
Number of bonded IOBs	41	640	6%	
Number of BUFG/BUFGCTRLs	1	32	3%	
Number used as BUFGs	1			
Average Fanout of Non-Clock Nets	5.24			

Performance Summary [-]			
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report

Timing Constraints:	All Constraints Met		

Detailed Reports (working directory="/home/cc/cs150/fa013/class/cs150-bn/fa13_team07/hardware/build/UpsamplerWrap") [-]					
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Fri Dec 6 13:59:23 2013	0	5 Warnings (5 new)	0
Translation Report	Current	Fri Dec 6 13:59:30 2013	0	1 Warning (1 new)	0
Map Report	Current	Fri Dec 6 14:00:03 2013	0	0	8 Infos (8 new)
Place and Route Report	Current	Fri Dec 6 14:00:49 2013	0	0	3 Infos (3 new)
Power Report					
Post-PAR Static Timing Report	Current	Fri Dec 6 14:01:21 2013	0	0	4 Infos (4 new)
Bitgen Report	Current	Fri Dec 6 14:01:11 2013	0	0	0

Secondary Reports [-]		
Report Name	**Status**	**Generated**
WebTalk Report	Current	Fri Dec 6 14:01:12 2013
WebTalk Log File	Current	Fri Dec 6 14:01:12 2013

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