FPGA_TOP_ML505 Project Status (11/24/2013 - 02:56:01)			
Configuration File:	FPGA_TOP_ML505.xreport	**Parser Errors:**	
Module Name:	FPGA_TOP_ML505	**Implementation State:**	Programming File Generated
Target Device:	5vlx110tff1136-1	• **Errors:**	No Errors
Product Version:	ISE 14.6	• **Warnings:**	263 Warnings (0 new)
Design Goal:	data unavailable	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	data unavailable	• **Timing Constraints:**	All Constraints Met
Environment:	System Settings	• **Final Timing Score:**	0

Device Utilization Summary [-]				
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	2,269	69,120	3%	
Number used as Flip Flops	2,268			
Number used as Latches	1			
Number of Slice LUTs	5,814	69,120	8%	
Number used as logic	2,329	69,120	3%	
Number using O6 output only	1,977			
Number using O5 output only	218			
Number using O5 and O6	134			
Number used as Memory	3,454	17,920	19%	
Number used as Dual Port RAM	2,632			
Number using O6 output only	2,560			
Number using O5 and O6	72			
Number used as Shift Register	822			
Number using O6 output only	822			
Number used as exclusive route-thru	31			
Number of route-thrus	256			
Number using O6 output only	249			
Number using O5 output only	7			
Number of occupied Slices	2,080	17,280	12%	
Number of LUT Flip Flop pairs used	6,617			
Number with an unused Flip Flop	4,348	6,617	65%	
Number with an unused LUT	803	6,617	12%	
Number of fully used LUT-FF pairs	1,466	6,617	22%	
Number of unique control sets	220			
Number of slice register sites lost to control set restrictions	225	69,120	1%	
Number of bonded IOBs	126	640	19%	
Number of LOCed IOBs	126	126	100%	
IOB Flip Flops	46			
Number of BlockRAM/FIFO	15	148	10%	
Number using BlockRAM only	15			

Number of 18k BlockRAM used	15			
Total Memory used (KB)	270	5,328	5%	
Number of BUFG/BUFGCTRLs	2	32	6%	
Number used as BUFGs	2			
Number of DSP48Es	6	64	9%	
Number of PLL_ADVs	1	6	16%	
Average Fanout of Non-Clock Nets	5.43			

Performance Summary			[-]
Final Timing Score:	0 (Setup: 0, Hold: 0, Component Switching Limit: 0)	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints Met		

Detailed Reports (working directory="/home/cc/cs150/fa013/class/cs150-bn/fa13_team07/hardware/build/FPGA_TOP_ML505")					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Sun Nov 24 02:51:13 2013	0	223 Warnings (0 new)	27 Infos (0 new)
Translation Report	Current	Sun Nov 24 02:51:25 2013	0	1 Warning (0 new)	2 Infos (0 new)
Map Report	Current	Sun Nov 24 02:52:34 2013	0	3 Warnings (0 new)	8 Infos (0 new)
Place and Route Report	Current	Sun Nov 24 02:53:26 2013	0	35 Warnings (0 new)	0
Power Report					
Post-PAR Static Timing Report	Current	Sun Nov 24 02:54:20 2013	0	0	3 Infos (0 new)
Bitgen Report	Current	Sun Nov 24 02:54:03 2013	0	1 Warning (0 new)	0

Secondary Reports			[-]
Report Name	**Status**	**Generated**	
WebTalk Report	Current	Sun Nov 24 02:54:04 2013	
WebTalk Log File	Current	Sun Nov 24 02:54:05 2013	

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