```
This timing info can be found by running make report and then
selecting "Synthesis Report" under Detailed Reports. Then scroll
down to TIMING REPORT

Clock Information:
------------------
-----------------------------------------------------+------------------------------+-------+
Clock Signal                                         | Clock buffer(FF name)        | Load  |
-----------------------------------------------------+------------------------------+-------+
clk_10M_pre                                          | BUFG                         | 490   |
clk_50M_pre                                          | BUFG                         | 421   |
sram_arbiter/next2_or0000(sram_arbiter/next2_or00001:O)| NONE(*)(sram_arbiter/next2)| 1     |
-----------------------------------------------------+------------------------------+-------+
(*) This 1 clock signal(s) are generated by combinatorial logic,
and XST is not able to identify which are the primary clock signals.
Please use the CLOCK_SIGNAL constraint to specify the clock signal(s) generated by combinatorial logic.
INFO:Xst:2169 - HDL ADVISOR - Some clock signals were not automatically buffered by XST with BUFG/BUFR
resources. Please use the buffer_type constraint in order to insert these buffers to the clock signals to
help prevent skew problems.

Asynchronous Control Signals Information:
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No asynchronous control signals found in this design

Timing Summary:
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Speed Grade: -1

   Minimum period: 4.989ns (Maximum Frequency: 200.441MHz)
   Minimum input arrival time before clock: 3.586ns
   Maximum output required time after clock: 4.207ns
   Maximum combinational path delay: 3.723ns
```