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ROLL: 2024HT01123
SUBJECT: EMBEDDED SYSTEM DESIGN
LAB ASSIGNMENT: 1

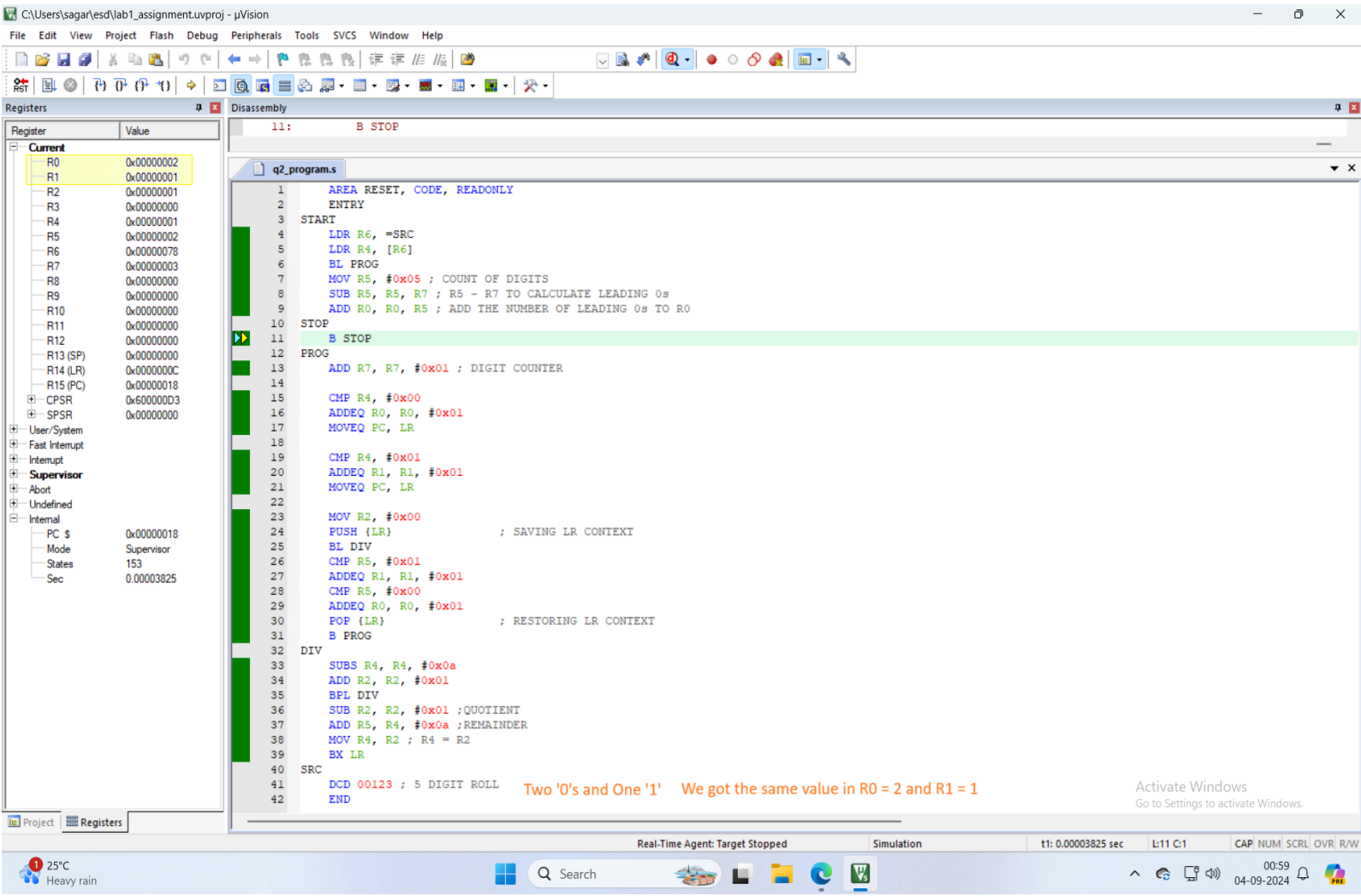
ANS 1:

a) On reset ARM7TDMI processor's **state is 0** and **mode is Supervisor**.
b) States taken to execute instructions:
    i) Arithmetic (ADR, ADD, SUB): 1
    ii) Load (LDR): 3
    iii) Store (STR): 2
c) Number of states taken for BGE "(1) if taken and (2) not taken" are the same in both cases.
    i) Number of states taken by BGE if branch:
        1) Taken: 1
        2) Not taken: 1
d) Performance of code-1 and code-2 for the following conditions:

Here we are taking a and b as first 2 values of DCD instruction, based on that I will be counting states:

Condition	**Code-1-States**	**Code-2-States**
a<b a=0x20 b=0x40	states=36 (if we execute `B stop` instruction) states=33 (if we do not execute `B stop` instruction)	states=33 (if we execute `B stop` instruction) states=30 (if we do not execute `B stop` instruction)
a>b a=0x40 b=0x20	states=32 (if we execute `B stop` instruction) states=29 (if we do not execute `B stop` instruction)	states=32 (if we execute `B stop` instruction) states=29 (if we do not execute `B stop` instruction)
a=b a=0x20 b=0x20	states=32 (if we execute `B stop` instruction) states=29 (if we do not execute `B stop` instruction)	states=32 (if we execute `B stop` instruction) states=29 (if we do not execute `B stop` instruction)

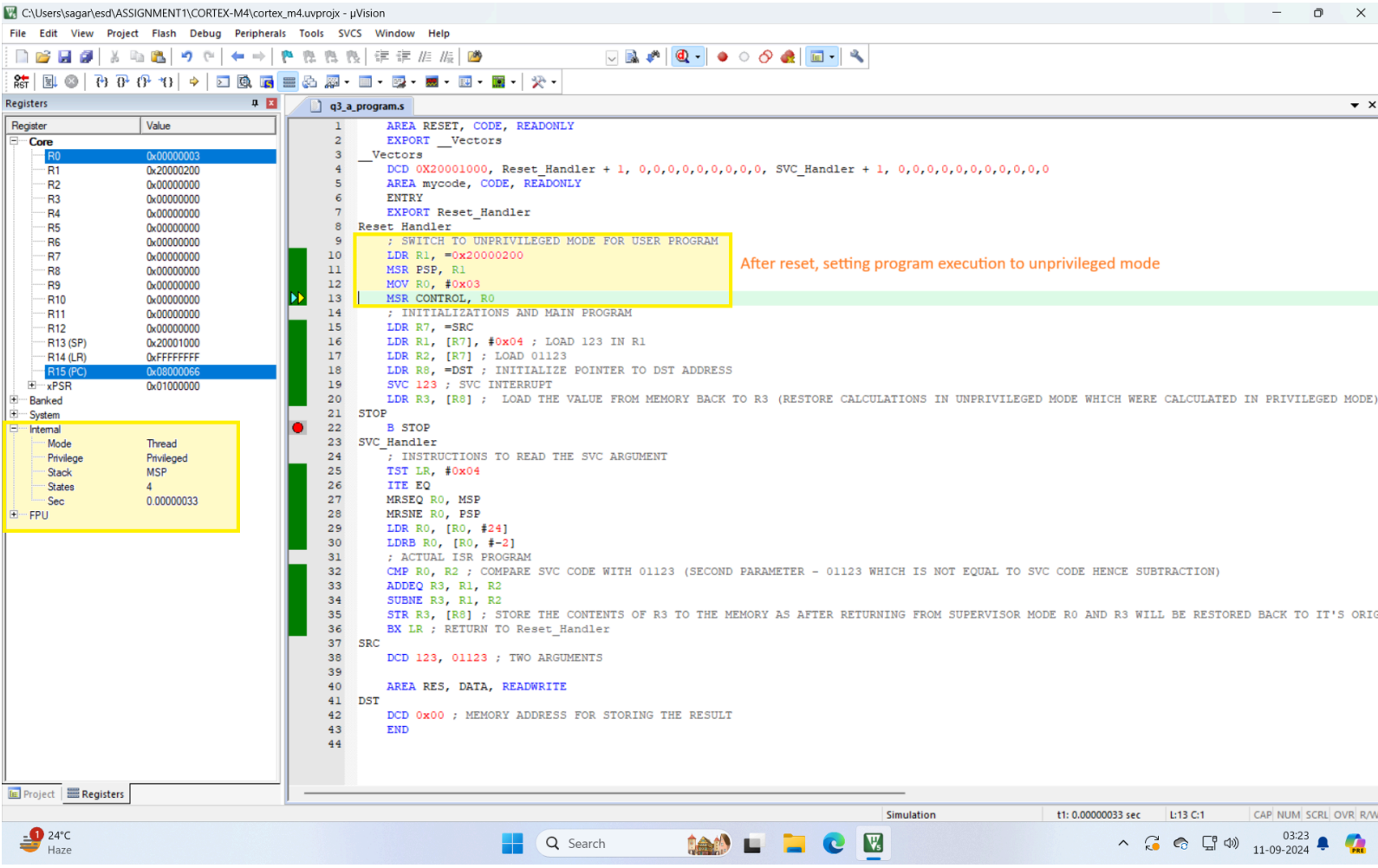
ANS 2:



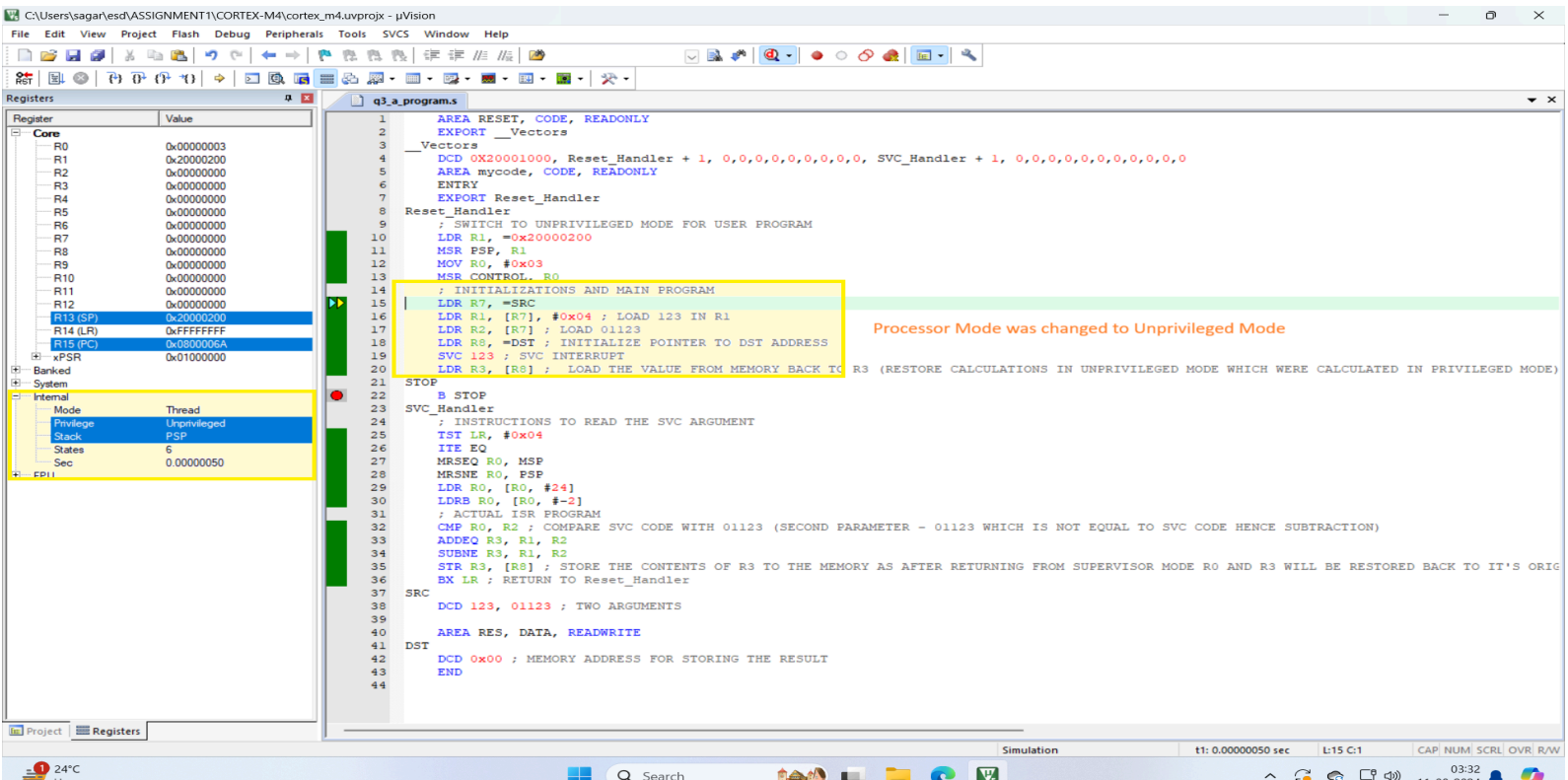
We have achieved the division (modulus) via repeated subtraction and breaked the loop once negative flag set to get the remainder (modulus)

ANS 3:

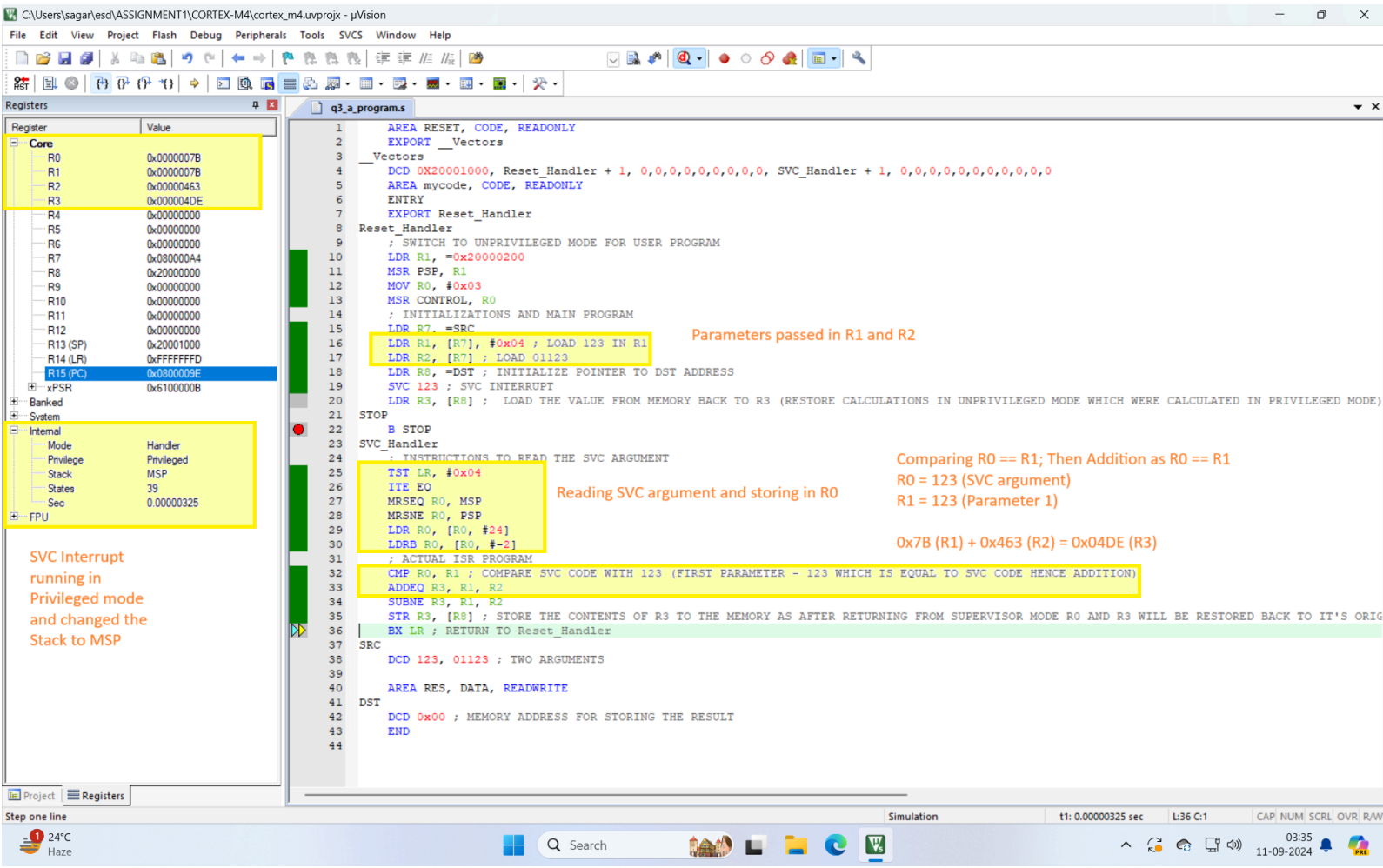
After RESET, setting program execution to unprivileged mode.



Processor Mode changed to Unprivileged Mode



CASE 1: WHEN SVC ARGUMENT AND ANY ONE PARAMETER MATCHES WITH BITS ID (ADDITION)



CASE 2: WHEN SVC ARGUMENT AND ANY ONE PARAMETER NOT MATCHES WITH BITS ID (SUBTRACTION)