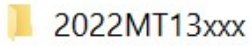
Lab Assignment-2

[Weightage - 10%]

Assignment Instructions:

1. Assignment should be solved individually.
2. No marks will be awarded if plagiarism is detected.
3. Question-1 must be performed in Remote lab.
4. It is mandatory to create a uVision Project folder in E:/ or D:/ or any other drive of Remote lab computer and give name to that folder as your BITS_ID e.g. 2022MT13xxx.

   Under this folder, you will save your assignment Keil project.
5. Please take complete (without cropping) screen shots of the KEIL IDE-in debug mode to demonstrate the desired output.
6. It is mandatory to ensure that the screenshot captures **system date & time**.
7. Screenshots must be clearly visible (good resolution).
8. For blur, adjusted, cropped and without system date and time screenshots, marks will be reduced.

Submission instructions:

Upload a single PDF document (named based on your BITS-ID number and name (**ID-No_Full-Name**)) which consist of answers of questions and relevant screenshots on Course Website (http://taxila-aws.bits-pilani.ac.in) during **17/09/2024-22/10/2024**.

Q.1. Write a C program for displaying your BITS ID on 1st Row and voltage difference between the terminals of the potentiometer, along with the date in the DD/M format, on 2nd row of LCD Display present in the LPC2378 kit. The Potentiometer is connected to AD0.0 pin (P0.23) of LPC2378. LCD connection details: DB4:P1.24, DB5:P1.25, DB6:P1.26, DB7:P1.27, RS:P1.28, RW:P1.29, E:P1.31.
This program is to be done using remote lab and Keil uV4/5.
Capture the screenshot of the LCD display showing your BITS ID, voltage value and date.
Give suitable screen shots of the KEIL IDE-in debug mode to demonstrate the desired outputs. Ensure that the screenshot captures system date & time.

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Q.2. Answer the following questions related to LPC2378:

a) What is the smallest change in input voltage that the ADC can detect? (+Vref =3.3 V) [2]

b) What is the maximum clock frequency needed by ADC of LPC2378? [2]

c) Give the steps to program timer for 2 second delay generation with calculation. Assume CCLK=48MHz. [4]