Lab 1: Introduction to Basic FPGA Design Concepts

Objective

Understand basic FPGA design concepts and tools by creating, synthesizing, implementing, and simulating a simple combinational logic circuit using the Vivado Design Suite.

Lab Overview

This lab introduces the essential steps involved in designing an FPGA-based circuit using the Vivado Design Suite. You will create a simple combinational logic circuit, simulate it to verify its functionality, and then implement the design on a ZYNQ FPGA board.

Equipment and Software

1. ZYNQ FPGA development board
2. USB programming cable
3. Computer with Vivado Design Suite installed
4. Basic understanding of digital logic design

Pre-Lab Preparation

Before starting the lab, ensure you have a working installation of the Vivado Design Suite on your computer. Familiarize yourself with basic digital logic gates and their truth tables.

Lab Activities

Activity 1: Introduction to the Vivado Design Suite

1. Launch Vivado:

- Open the Vivado Design Suite on your computer.

- Create a new project by selecting **File > New Project.

2. Create a New Project:

- Follow the wizard steps to create a new project.
- Name the project "BasicCombinationalCircuit" and choose a suitable location.
- Select **RTL Project** and check the option to **Do not specify sources at this time**.
- Choose the appropriate ZYNQ board or device for your setup.

3. Explore Vivado Interface:

- Familiarize yourself with the Project Manager, Flow Navigator, and Toolbars.
- Understand the different windows such as Sources, Properties, and Console.

Activity 2: Create a Simple Combinational Logic Circuit

1. Add Design Sources:

- In the Flow Navigator, click on **Add Sources.**
- Select **Add or Create Design Sources** and click **Next**.
- Click **Create File**, choose **Verilog** or **VHDL** as the file type, and name it **combinational_logic**.

2. Write the Design Code:

- Open the newly created file in the Vivado editor.
- Write the HDL code for a simple combinational circuit (e.g., an AND gate or OR gate).

Verilog Code for AND Gate:

```
module combinational_logic (
      input wire A,
      input wire B,
      output wire Y
```

```
);
    assign Y = A & B;
endmodule
```

---

3. Save the File:

- Save the code by clicking **File > Save** or pressing **Ctrl + S**.

Activity 3: Synthesize, Implement, and Simulate the Design

1. Create a Testbench:

- In the Flow Navigator, click on **Add Sources.**
- Select Add or **Create Simulation** Sources and **click Next**.
- Click **Create File**, choose **Verilog** or **VHDL** as the file type, and name it **tb_combinational_logic**.

2. Write the Testbench Code:

- Open the testbench file in the Vivado editor.
- Write the testbench code to apply test vectors and observe outputs.

Verilog Testbench Code:

```
`timescale 1ns / 1ps
module tb_combinational_logic;
    reg A;
    reg B;
    wire Y;
    // Instantiate the design under test (DUT)
    combinational_logic dut (
        .A(A),
```

```
        .B(B),
        .Y(Y)
    );

    initial begin
        // Initialize inputs
        A = 0; B = 0;
        #10; // Wait for 10 ns
        A = 0; B = 1;
        #10;
        A = 1; B = 0;
        #10;
        A = 1; B = 1;
        #10;
        $finish; // End the simulation
    end
    initial begin
        $monitor("At time %t: A = %b, B = %b, Y = %b", $time, A,
B, Y);
    end
endmodule
```

---

3. Simulate the Design:

- Click on **Run Simulation > Run Behavioral Simulation.**
- Use the Waveform window to observe the input and output signals.
- Verify that the output `Y` is correct for each combination of inputs `A` and `B`.

4. Synthesize the Design:

- In the Flow Navigator, click on **Run Synthesis**.

- Review any warnings or errors in the synthesis report.

5. **Implement the Design:**

- After successful synthesis, click on **Run Implementation**.

- Review the implementation report for any issues.

6. **Generate Bitstream:**

- Click on **Generate Bitstream** to create a bitstream file for programming the FPGA.

7. Program the FPGA:

- Connect your ZYNQ board to the computer using the USB programming cable.

- Click on **Open Hardware Manager** and connect to the board.

- Program the FPGA with the generated bitstream file.

8. Verify the Design:

- Use the onboard LEDs and switches (if available) to verify the functionality of your combinational circuit.

- Check the outputs for different input combinations.

Post-Lab Questions

1. Describe the steps involved in synthesizing and implementing a design in Vivado.

2. How can you verify the functionality of a combinational circuit using simulation?

3. What are the advantages of using FPGAs for implementing digital circuits?

Post-Lab Assignment

Use Vivado to design a 2-to-1 multiplexer in Verilog or VHDL, create a testbench to simulate and verify its functionality, and modify the design to implement a 4-to-1 multiplexer. Submit your design files and simulation results.

Conclusion

In this lab, you have learned the basic workflow of FPGA design using the Vivado Design Suite. You created, synthesized, implemented, and simulated a simple combinational logic circuit, gaining hands-on experience with FPGA design tools.