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SUBJECT: Hardware Software Co-Design

TITLE: RTL Code, design and implement the 4 x 1 multiplexer

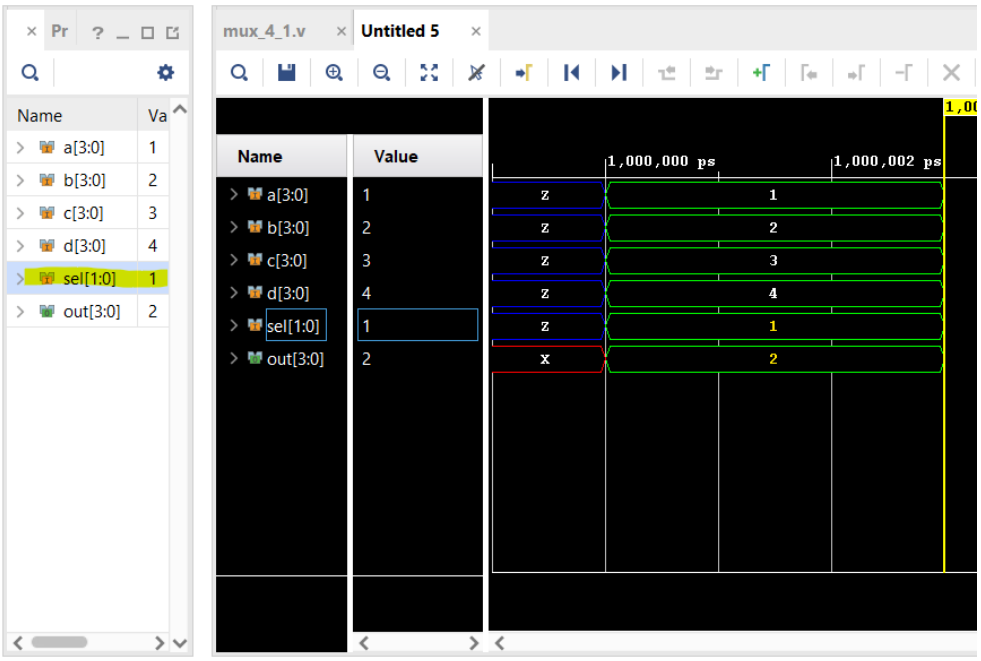
RTL code:

Project Summary | mux_4_1.v

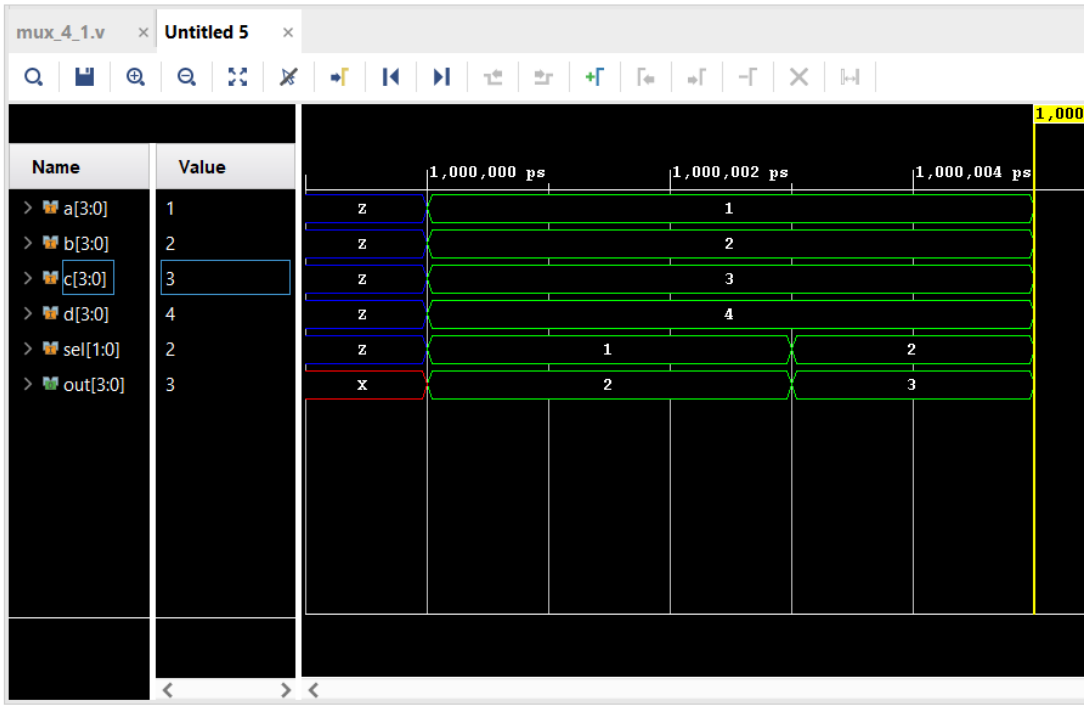
C:/Users/maina/fpga/multiplexers/multiplexers.srcs/sources_1/new/mux_4_1.v

```
19  //
20  //////////////////////////////////////////////////////////////////////////////////
21
22
23  module mux_4_1(
24      input [3:0] a,
25      input [3:0] b,
26      input [3:0] c,
27      input [3:0] d,
28      input [1:0] sel,
29      output reg [3:0] out);
30
31      always @ (a or b or c or d or sel) begin
32          case (sel)
33              2'b00 : out <= a;
34              2'b01 : out <= b;
35              2'b10 : out <= c;
36              2'b11 : out <= d;
37          endcase
38      end
39
40  endmodule
41
```

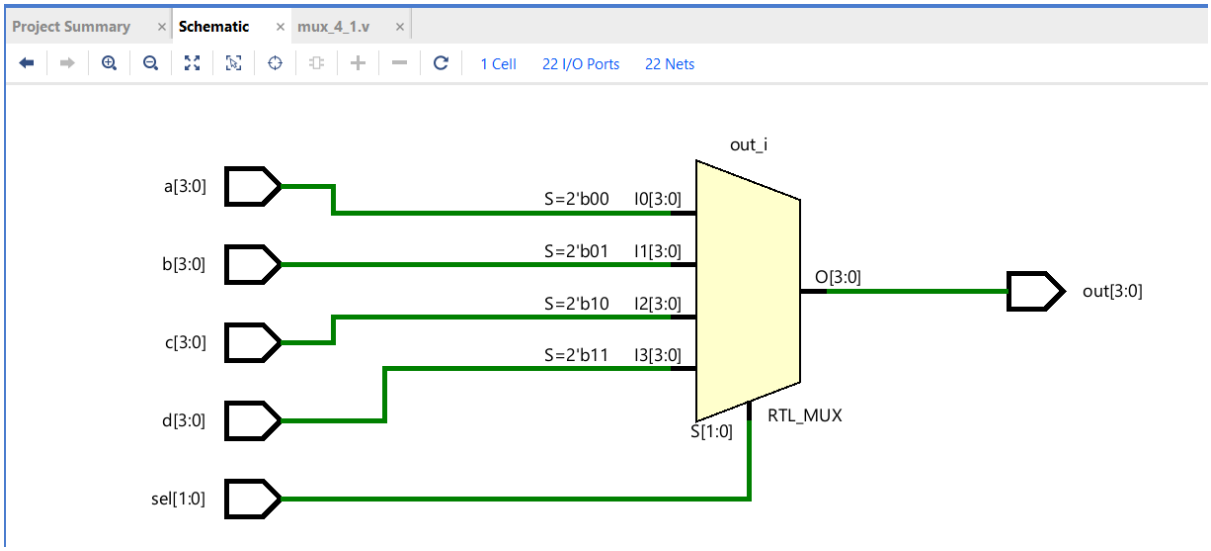
We have put the input values (a, b, c, d, sel) as (1, 2, 3, 4, 1th) which is giving us the output as 2 (which is at position 1st as mentioned in select line)



We have put the input values (a, b, c, d, sel) as (1, 2, 3, 4, 2) which is giving us the output as 3 (which is at position 2th as mentioned in select line)




Schematic elaborate design



4 x 1 MUX Schematic: