CS520 Project-2 | Fall 2019
Sample Test Case with Display Guidelines

Display Guidelines:

Your code should produce below states on standard display console for **EACH** Cycle:
Instruction at FETCH_STAGE
Instruction at DECODE_RF_STAGE
Details of RENAME TABLE State
Details of ARF State
Details of LSQ (Load-Store Queue) State
Details of ROB (Reorder Buffer) State
Details of IQ (Issue Queue) State
Instruction at INT1_FU_STAGE
Instruction at INT2_FU_STAGE
Instruction at MUL1_FU_STAGE
Instruction at MUL2_FU_STAGE
Instruction at MUL3_FU_STAGE
Instruction at BRANCH_FU_STAGE
Instruction at MEM_FU_STAGE
Details of ROB Retired Instructions
Default prediction in Fetch Stage for all branch instructions
Actual outcome in Branch FU for all branch instructions

Your code should produce outputs for below states at the end (only show allocated entries):
STATE OF ARCHITECTURAL REGISTER FILE
STATE OF DATA MEMORY

Please follow rest of the project-1 guidelines of command line arguments.

Instruction Sequence:

4000	I0	MOVC,R0,#0	R0 = 0	
4004	I1	MOVC,R3,#3	R3 = 3	
4008	I2	ADD,R4,R0,R3	R4 = 3	
4012	I3	MUL,R6,R4,R4	R6 = 9	
4016	I4	STORE,R6,R0,#4	D[4] <-- 9	
4020	I5	SUB,R5,R3,R4	R5 = 0	
4024	I6	BZ,#8	Taken Branch	
4028	I7	MOVC,R8,#32		Skipped
4032	I8	ADDL,R11,R5,#4		R11 = 4
4036	I9	SUBL,R10,R0,#8		R10 = -8
4040	I10	HALT		Simulation Finished

Expected Output:

Below output is manually created, so verify the output with required functionalities and if you find any discrepancies then do let us know.

```
#--#--#--#--#--#--#--#--#--#--#--#--#--#--#-- SIMULATION START #--#--#--#--#--#--#--#--#--#--#--#--#--#-
^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 1 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^
Instruction at FETCH_STAGE ---> (I0) MOVC,R0,#0
Instruction at DECODE_RF_STAGE ---> EMPTY
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Details of RENAME TABLE State --
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Details of ARF State --
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Details of IQ (Issue Queue) State --
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Details of LSQ (Load-Store Queue) State --
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Details of ROB (Reorder Buffer) State --
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Instruction at INT1_FU_STAGE ---> EMPTY
Instruction at INT2_FU_STAGE ---> EMPTY
Instruction at MUL1_FU_STAGE ---> EMPTY
Instruction at MUL2_FU_STAGE ---> EMPTY
Instruction at MUL3_FU_STAGE ---> EMPTY
Instruction at BRANCH_FU_STAGE ---> EMPTY
Instruction at MEM_FU_STAGE ---> EMPTY
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Details of ROB Retired Instructions --
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^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 2 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^
Instruction at FETCH_STAGE ---> (I1) MOVC,R3,#3
Instruction at DECODE_RF_STAGE ---> (I0) MOVC,R0,#0 [MOVC,P0,#0]
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Details of RENAME TABLE State –
R[00] --> P0
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Details of ARF State --
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Details of IQ (Issue Queue) State --
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Details of LSQ (Load-Store Queue) State --
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Details of ROB (Reorder Buffer) State --

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Instruction at INT1_FU_STAGE ---> EMPTY
Instruction at INT2_FU_STAGE ---> EMPTY
Instruction at MUL1_FU_STAGE ---> EMPTY
Instruction at MUL2_FU_STAGE ---> EMPTY
Instruction at MUL3_FU_STAGE ---> EMPTY
Instruction at BRANCH_FU_STAGE ---> EMPTY
Instruction at MEM_FU_STAGE ---> EMPTY

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Details of ROB Retired Instructions --

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^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 3 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^

Instruction at FETCH_STAGE ---> (I2) ADD,R4,R0,R3
Instruction at DECODE_RF_STAGE ---> (I1) MOVC,R3,#3 [MOVC,P1,#3]

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Details of RENAME TABLE State –
R[00] --> P0
R[03] --> P1

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Details of ARF State --

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Details of IQ (Issue Queue) State –
IQ[00] --> (I0) MOVC,R0,#0 [MOVC,P0,#0]

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Details of LSQ (Load-Store Queue) State --

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Details of ROB (Reorder Buffer) State –
ROB[00] --> (I0) MOVC,R0,#0 [MOVC,P0,#0]

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Instruction at INT1_FU_STAGE ---> EMPTY
Instruction at INT2_FU_STAGE ---> EMPTY
Instruction at MUL1_FU_STAGE ---> EMPTY
Instruction at MUL2_FU_STAGE ---> EMPTY
Instruction at MUL3_FU_STAGE ---> EMPTY
Instruction at BRANCH_FU_STAGE ---> EMPTY
Instruction at MEM_FU_STAGE ---> EMPTY

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Details of ROB Retired Instructions --

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^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 4 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^

Instruction at FETCH_STAGE ---> (I3) MUL,R6,R4,R4
Instruction at DECODE_RF_STAGE ---> (I2) ADD,R4,R0,R3 [ADD,P2,P0,P1]

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Details of RENAME TABLE State –
R[00] --> P0
R[03] --> P1
R[04] --> P2
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Details of ARF State --
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Details of IQ (Issue Queue) State –
IQ[00] --> (I1) MOVC,R3,#3 [MOVC,P1,#3]
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Details of LSQ (Load-Store Queue) State --
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Details of ROB (Reorder Buffer) State –
ROB[00] --> (I0) MOVC,R0,#0 [MOVC,P0,#0]
ROB[01] --> (I1) MOVC,R3,#3 [MOVC,P1,#3]
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Instruction at INT1_FU_STAGE ---> (I0) MOVC,R0,#0 [MOVC,P0,#0]
Instruction at INT2_FU_STAGE ---> EMPTY
Instruction at MUL1_FU_STAGE ---> EMPTY
Instruction at MUL2_FU_STAGE ---> EMPTY
Instruction at MUL3_FU_STAGE ---> EMPTY
Instruction at BRANCH_FU_STAGE ---> EMPTY
Instruction at MEM_FU_STAGE ---> EMPTY
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Details of ROB Retired Instructions --
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^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 5 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^

Instruction at FETCH_STAGE ---> (I4) STORE,R6,R0,#4
Instruction at DECODE_RF_STAGE ---> (I3) MUL,R6,R4,R4 [MUL,P3,P2,P2]
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Details of RENAME TABLE State –
R[00] --> P0
R[03] --> P1
R[04] --> P2
R[06] --> P3
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Details of ARF State --
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Details of IQ (Issue Queue) State –
IQ[00] --> (I2) ADD,R4,R0,R3 [ADD,P2,P0,P1]
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Details of LSQ (Load-Store Queue) State --
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Details of ROB (Reorder Buffer) State –
ROB[00] --> (I0) MOVC,R0,#0 [MOVC,P0,#0]
ROB[01] --> (I1) MOVC,R3,#3 [MOVC,P1,#3]
ROB[02] --> (I2) ADD,R4,R0,R3 [ADD,P2,P0,P1]
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Instruction at INT1_FU_STAGE ---> (I1) MOVC,R3,#3 [MOVC,P1,#3]
Instruction at INT2_FU_STAGE ---> (I0) MOVC,R0,#0 [MOVC,P0,#0]
Instruction at MUL1_FU_STAGE ---> EMPTY
Instruction at MUL2_FU_STAGE ---> EMPTY
Instruction at MUL3_FU_STAGE ---> EMPTY
Instruction at BRANCH_FU_STAGE ---> EMPTY
Instruction at MEM_FU_STAGE ---> EMPTY
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Details of ROB Retired Instructions --
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^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 6 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^

Instruction at FETCH_STAGE ---> (I5) SUB,R5,R3,R4
Instruction at DECODE_RF_STAGE ---> (I4) STORE,R6,R0,#4 [STORE,P3,P0,#4]
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Details of RENAME TABLE State –
R[00] --> P0
R[03] --> P1
R[04] --> P2
R[06] --> P3
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Details of ARF State –
R0 --> 0
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Details of IQ (Issue Queue) State –
IQ[00] --> (I2) ADD,R4,R0,R3 [ADD,P2,P0,P1]
IQ[01] --> (I3) MUL,R6,R4,R4 [MUL,P3,P2,P2]
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Details of LSQ (Load-Store Queue) State --
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Details of ROB (Reorder Buffer) State –
ROB[00] --> (I1) MOVC,R3,#3 [MOVC,P1,#3]
ROB[01] --> (I2) ADD,R4,R0,R3 [ADD,P2,P0,P1]
ROB[02] --> (I3) MUL,R6,R4,R4 [MUL,P3,P2,P2]
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Instruction at INT1_FU_STAGE ---> EMPTY
Instruction at INT2_FU_STAGE ---> (I1) MOVC,R3,#3 [MOVC,P1,#3]
Instruction at MUL1_FU_STAGE ---> EMPTY
Instruction at MUL2_FU_STAGE ---> EMPTY
Instruction at MUL3_FU_STAGE ---> EMPTY
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Instruction at BRANCH_FU_STAGE ---> EMPTY
Instruction at MEM_FU_STAGE ---> EMPTY
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Details of ROB Retired Instructions –
(I0) MOVC,R0,#0 [MOVC,P0,#0]
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^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 7 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^

Instruction at FETCH_STAGE ---> (I6) BZ,#8 => Default Prediction: Branch Not Taken
Instruction at DECODE_RF_STAGE ---> (I5) SUB,R5,R3,R4 [SUB,P4,P1,P2]
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Details of RENAME TABLE State –
R[00] --> P0
R[03] --> P1
R[04] --> P2
R[05] --> P4
R[06] --> P3
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Details of ARF State –
R0 --> 0
R3 --> 3
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Details of IQ (Issue Queue) State –
IQ[00] --> (I3) MUL,R6,R4,R4 [MUL,P3,P2,P2]
IQ[01] --> (I4) STORE,R6,R0,#4 [STORE,P3,P0,#4]
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Details of LSQ (Load-Store Queue) State –
LSQ[00] --> (I4) STORE,R6,R0,#4 [STORE,P3,P0,#4]
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Details of ROB (Reorder Buffer) State –
ROB[00] --> (I2) ADD,R4,R0,R3 [ADD,P2,P0,P1]
ROB[01] --> (I3) MUL,R6,R4,R4 [MUL,P3,P2,P2]
ROB[02] --> (I4) STORE,R6,R0,#4 [STORE,P3,P0,#4]
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Instruction at INT1_FU_STAGE ---> (I2) ADD,R4,R0,R3 [ADD,P2,P0,P1]
Instruction at INT2_FU_STAGE ---> EMPTY
Instruction at MUL1_FU_STAGE ---> EMPTY
Instruction at MUL2_FU_STAGE ---> EMPTY
Instruction at MUL3_FU_STAGE ---> EMPTY
Instruction at BRANCH_FU_STAGE ---> EMPTY
Instruction at MEM_FU_STAGE ---> EMPTY
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Details of ROB Retired Instructions –
(I1) MOVC,R3,#3 [MOVC,P1,#0]
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^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 8 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^

Instruction at FETCH_STAGE ---> (I7) MOVC,R8,#32
Instruction at DECODE_RF_STAGE ---> (I6) BZ,#8
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Details of RENAME TABLE State –
R[00] --> P0
R[03] --> P1
R[04] --> P2
R[05] --> P4
R[06] --> P3
~~~~~~

Details of ARF State –
R0 --> 0
R3 --> 3
~~~~~~

Details of IQ (Issue Queue) State –
IQ[00] --> (I3) MUL,R6,R4,R4 [MUL,P3,P2,P2]
IQ[01] --> (I5) SUB,R5,R3,R4 [SUB,P4,P1,P2]
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Details of LSQ (Load-Store Queue) State –
LSQ[00] --> (I4) STORE,R6,R0,#4 [STORE,P3,P0,#4]
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Details of ROB (Reorder Buffer) State –
ROB[00] --> (I2) ADD,R4,R0,R3 [ADD,P2,P0,P1]
ROB[01] --> (I3) MUL,R6,R4,R4 [MUL,P3,P2,P2]
ROB[02] --> (I4) STORE,R6,R0,#4 [STORE,P3,P0,#4]
ROB[03] --> (I5) SUB,R5,R3,R4 [SUB,P4,P1,P2]
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Instruction at INT1_FU_STAGE ---> (I4) STORE,R6,R0,#4 [STORE,P3,P0,#4]
Instruction at INT2_FU_STAGE ---> (I2) ADD,R4,R0,R3 [ADD,P2,P0,P1]
Instruction at MUL1_FU_STAGE ---> EMPTY
Instruction at MUL2_FU_STAGE ---> EMPTY
Instruction at MUL3_FU_STAGE ---> EMPTY
Instruction at BRANCH_FU_STAGE ---> EMPTY
Instruction at MEM_FU_STAGE ---> EMPTY
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Details of ROB Retired Instructions –
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^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 9 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^

Instruction at FETCH_STAGE ---> (I8) ADDL,R11,R5,#4
Instruction at DECODE_RF_STAGE ---> (I7) MOVC,R8,#32 [MOVC,P5,#32]
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Details of RENAME TABLE State –
R[00] --> P0
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R[03] --> P1
R[04] --> P2
R[05] --> P4
R[06] --> P3
R[08] --> P5
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Details of ARF State –
R0 --> 0
R3 --> 3
R4 --> 3
~~~~~~

Details of IQ (Issue Queue) State –
IQ[00] --> (I6) BZ,#8
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Details of LSQ (Load-Store Queue) State –
LSQ[00] --> (I4) STORE,R6,R0,#4 [STORE,P3,P0,#4]
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Details of ROB (Reorder Buffer) State –
ROB[00] --> (I3) MUL,R6,R4,R4 [MUL,P3,P2,P2]
ROB[01] --> (I4) STORE,R6,R0,#4 [STORE,P3,P0,#4]
ROB[02] --> (I5) SUB,R5,R3,R4 [SUB,P4,P1,P2]
ROB[03] --> (I6) BZ,#8
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Instruction at INT1_FU_STAGE ---> (I5) SUB,R5,R3,R4 [SUB,P4,P1,P2]
Instruction at INT2_FU_STAGE ---> (I4) STORE,R6,R0,#4 [STORE,P3,P0,#4]
Instruction at MUL1_FU_STAGE ---> (I3) MUL,R6,R4,R4 [MUL,P3,P2,P2]
Instruction at MUL2_FU_STAGE ---> EMPTY
Instruction at MUL3_FU_STAGE ---> EMPTY
Instruction at BRANCH_FU_STAGE ---> EMPTY
Instruction at MEM_FU_STAGE ---> EMPTY
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Details of ROB Retired Instructions –
(I2) ADD,R4,R0,R3 [ADD,P2,P0,P1]
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^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 10 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^

Instruction at FETCH_STAGE ---> (I9) SUBL,R10,R0,#8
Instruction at DECODE_RF_STAGE ---> (I8) ADDL,R11,R5,#4
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Details of RENAME TABLE State –
R[00] --> P0
R[03] --> P1
R[04] --> P2
R[05] --> P4
R[06] --> P3

R[08] --> P5
R[11] --> P6
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Details of ARF State –
R0 --> 0
R3 --> 3
R4 --> 3
~~~~~~

Details of IQ (Issue Queue) State –
IQ[00] --> (I6) BZ,#8
IQ[01] --> (I7) MOVC,R8,#32 [MOVC,P5,#32]
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Details of LSQ (Load-Store Queue) State –
LSQ[00] --> (I4) STORE,R6,R0,#4 [STORE,P3,P0,#4]
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Details of ROB (Reorder Buffer) State –
ROB[00] --> (I3) MUL,R6,R4,R4 [MUL,P3,P2,P2]
ROB[01] --> (I4) STORE,R6,R0,#4 [STORE,P3,P0,#4]
ROB[02] --> (I5) SUB,R5,R3,R4 [SUB,P4,P1,P2]
ROB[03] --> (I6) BZ,#8
ROB[03] --> (I7) MOVC,R8,#32 [MOVC,P5,#32]
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Instruction at INT1_FU_STAGE ---> EMPTY
Instruction at INT2_FU_STAGE ---> (I5) SUB,R5,R3,R4 [SUB,P4,P1,P2]
Instruction at MUL1_FU_STAGE ---> EMPTY
Instruction at MUL2_FU_STAGE ---> (I3) MUL,R6,R4,R4 [MUL,P3,P2,P2]
Instruction at MUL3_FU_STAGE ---> EMPTY
Instruction at BRANCH_FU_STAGE ---> EMPTY
Instruction at MEM_FU_STAGE ---> EMPTY
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Details of ROB Retired Instructions –
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^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 11 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^^

Instruction at FETCH_STAGE ---> (I10) HALT
Instruction at DECODE_RF_STAGE ---> (I9) SUBL,R10,R0,#8 [SUB,P7,P0,#8]
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Details of RENAME TABLE State –
R[00] --> P0
R[03] --> P1
R[04] --> P2
R[05] --> P4
R[06] --> P3
R[08] --> P5
R[10] --> P7

R[11] --> P6
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Details of ARF State –
R0 --> 0
R3 --> 3
R4 --> 3
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Details of IQ (Issue Queue) State –
IQ[00] --> (I8) ADDL,R11,R5,#4
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Details of LSQ (Load-Store Queue) State –
LSQ[00] --> (I4) STORE,R6,R0,#4 [STORE,P3,P0,#4]
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Details of ROB (Reorder Buffer) State –
ROB[00] --> (I3) MUL,R6,R4,R4 [MUL,P3,P2,P2]
ROB[01] --> (I4) STORE,R6,R0,#4 [STORE,P3,P0,#4]
ROB[02] --> (I5) SUB,R5,R3,R4 [SUB,P4,P1,P2]
ROB[03] --> (I6) BZ,#8
ROB[04] --> (I7) MOVC,R8,#32 [MOVC,P5,#32]
ROB[05] --> (I8) ADDL,R11,R5,#4
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Instruction at INT1_FU_STAGE ---> (I7) MOVC,R8,#32 [MOVC,P5,#32]
Instruction at INT2_FU_STAGE ---> EMPTY
Instruction at MUL1_FU_STAGE ---> EMPTY
Instruction at MUL2_FU_STAGE ---> EMPTY
Instruction at MUL3_FU_STAGE ---> (I3) MUL,R6,R4,R4 [MUL,P3,P2,P2]
Instruction at BRANCH_FU_STAGE ---> (I6) BZ,#8 => Actual Outcome: Branch Taken
Instruction at MEM_FU_STAGE ---> EMPTY
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Details of ROB Retired Instructions –
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^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 12 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^

Instruction at FETCH_STAGE ---> (I8) ADDL,R11,R5,#4
Instruction at DECODE_RF_STAGE ---> EMPTY
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Details of RENAME TABLE State –
R[00] --> P0
R[03] --> P1
R[04] --> P2
R[05] --> P4
R[06] --> P3
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Details of ARF State –
R0 --> 0
~~~~~~

R3 --> 3
R4 --> 3
R6 --> 9
~~~~~~

Details of IQ (Issue Queue) State –
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Details of LSQ (Load-Store Queue) State –
LSQ[00] --> (I4) STORE,R6,R0,#4 [STORE,P3,P0,#4]
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Details of ROB (Reorder Buffer) State –
ROB[00] --> (I4) STORE,R6,R0,#4 [STORE,P3,P0,#4]
ROB[01] --> (I5) SUB,R5,R3,R4 [SUB,P4,P1,P2]
ROB[02] --> (I6) BZ,#8
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Instruction at INT1_FU_STAGE ---> EMPTY
Instruction at INT2_FU_STAGE ---> EMPTY
Instruction at MUL1_FU_STAGE ---> EMPTY
Instruction at MUL2_FU_STAGE ---> EMPTY
Instruction at MUL3_FU_STAGE ---> EMPTY
Instruction at BRANCH_FU_STAGE ---> EMPTY
Instruction at MEM_FU_STAGE ---> (I4) STORE,R6,R0,#4 [STORE,P3,P0,#4] (CYCLE 1)
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Details of ROB Retired Instructions –
(I3) MUL,R6,R4,R4 [MUL,P3,P2,P2]
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^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 13 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^

Instruction at FETCH_STAGE ---> (I9) SUBL,R10,R0,#8
Instruction at DECODE_RF_STAGE ---> (I8) ADDL,R11,R5,#4 [ADDL,P5,P4,#4]
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Details of RENAME TABLE State –
R[00] --> P0
R[03] --> P1
R[04] --> P2
R[05] --> P4
R[06] --> P3
R[11] --> P5
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Details of ARF State –
R0 --> 0
R3 --> 3
R4 --> 3
R6 --> 9
~~~~~~

Details of IQ (Issue Queue) State –
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Details of LSQ (Load-Store Queue) State –
LSQ[00] --> (I4) STORE,R6,R0,#4 [STORE,P3,P0,#4]
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Details of ROB (Reorder Buffer) State –
ROB[00] --> (I4) STORE,R6,R0,#4 [STORE,P3,P0,#4]
ROB[01] --> (I5) SUB,R5,R3,R4 [SUB,P4,P1,P2]
ROB[02] --> (I6) BZ,#8
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Instruction at INT1_FU_STAGE ---> EMPTY
Instruction at INT2_FU_STAGE ---> EMPTY
Instruction at MUL1_FU_STAGE ---> EMPTY
Instruction at MUL2_FU_STAGE ---> EMPTY
Instruction at MUL3_FU_STAGE ---> EMPTY
Instruction at BRANCH_FU_STAGE ---> EMPTY
Instruction at MEM_FU_STAGE ---> (I4) STORE,R6,R0,#4 [STORE,P3,P0,#4] (CYCLE 2)
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Details of ROB Retired Instructions –
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^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 14 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^

Instruction at FETCH_STAGE ---> (I10) HALT
Instruction at DECODE_RF_STAGE ---> (I9) SUBL,R10,R0,#8 [SUBL,P6,P0,#8]
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Details of RENAME TABLE State –
R[00] --> P0
R[03] --> P1
R[04] --> P2
R[05] --> P4
R[06] --> P3
R[10] --> P6
R[11] --> P5
~~~~~~

Details of ARF State –
R0 --> 0
R3 --> 3
R4 --> 3
R6 --> 9
~~~~~~

Details of IQ (Issue Queue) State –
IQ[00] --> (I8) ADDL,R11,R5,#4 [ADDL,P5,P4,#4]
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Details of LSQ (Load-Store Queue) State –
LSQ[00] --> (I4) STORE,R6,R0,#4 [STORE,P3,P0,#4]
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Details of ROB (Reorder Buffer) State –
ROB[00] --> (I4) STORE,R6,R0,#4 [STORE,P3,P0,#4]
ROB[01] --> (I5) SUB,R5,R3,R4 [SUB,P4,P1,P2]
ROB[02] --> (I6) BZ,#8
ROB[03] --> (I8) ADDL,R11,R5,#4 [ADDL,P5,P4,#4]
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Instruction at INT1_FU_STAGE ---> EMPTY
Instruction at INT2_FU_STAGE ---> EMPTY
Instruction at MUL1_FU_STAGE ---> EMPTY
Instruction at MUL2_FU_STAGE ---> EMPTY
Instruction at MUL3_FU_STAGE ---> EMPTY
Instruction at BRANCH_FU_STAGE ---> EMPTY
Instruction at MEM_FU_STAGE ---> (I4) STORE,R6,R0,#4 [STORE,P3,P0,#4] (CYCLE 3)
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Details of ROB Retired Instructions –
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^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 15 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^

Instruction at FETCH_STAGE ---> EMPTY
Instruction at DECODE_RF_STAGE ---> (I10) HALT
~~~~~~

Details of RENAME TABLE State –
R[00] --> P0
R[03] --> P1
R[04] --> P2
R[05] --> P4
R[06] --> P3
R[10] --> P6
R[11] --> P5
~~~~~~

Details of ARF State –
R0 --> 0
R3 --> 3
R4 --> 3
R6 --> 9
~~~~~~

Details of IQ (Issue Queue) State –
IQ[00] --> (I9) SUBL,R10,R0,#8 [SUBL,P6,P0,#8]
~~~~~~

Details of LSQ (Load-Store Queue) State –
~~~~~~

Details of ROB (Reorder Buffer) State –
ROB[00] --> (I5) SUB,R5,R3,R4 [SUB,P4,P1,P2]
ROB[01] --> (I6) BZ,#8
ROB[02] --> (I8) ADDL,R11,R5,#4 [ADDL,P5,P4,#4]

ROB[03] --> (I9) SUBL,R10,R0,#8 [SUBL,P6,P0,#8]
~~~~~~
Instruction at INT1_FU_STAGE ---> (I8) ADDL,R11,R5,#4 [ADDL,P5,P4,#4]
Instruction at INT2_FU_STAGE ---> EMPTY
Instruction at MUL1_FU_STAGE ---> EMPTY
Instruction at MUL2_FU_STAGE ---> EMPTY
Instruction at MUL3_FU_STAGE ---> EMPTY
Instruction at BRANCH_FU_STAGE ---> EMPTY
Instruction at MEM_FU_STAGE ---> EMPTY
~~~~~~
Details of ROB Retired Instructions –
(I4) STORE,R6,R0,#4 [STORE,P3,P0,#4]
~~~~~~
^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 16 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^
Instruction at FETCH_STAGE ---> EMPTY
Instruction at DECODE_RF_STAGE ---> EMPTY
~~~~~~
Details of RENAME TABLE State –
R[00] --> P0
R[03] --> P1
R[04] --> P2
R[05] --> P4
R[06] --> P3
R[10] --> P6
R[11] --> P5
~~~~~~
Details of ARF State –
R0 --> 0
R3 --> 3
R4 --> 3
R5 --> 0
R6 --> 9
~~~~~~
Details of IQ (Issue Queue) State –
~~~~~~
Details of LSQ (Load-Store Queue) State –
~~~~~~
Details of ROB (Reorder Buffer) State –
ROB[00] --> (I6) BZ,#8
ROB[01] --> (I8) ADDL,R11,R5,#4 [ADDL,P5,P4,#4]
ROB[02] --> (I9) SUBL,R10,R0,#8 [SUBL,P6,P0,#8]
ROB[03] --> (I10) HALT
~~~~~~
Instruction at INT1_FU_STAGE ---> (I9) SUBL,R10,R0,#8
~~~~~~

Instruction at INT2_FU_STAGE ---> (I8) ADDL,R11,R5,#4 [ADDL,P5,P4,#4]
Instruction at MUL1_FU_STAGE ---> EMPTY
Instruction at MUL2_FU_STAGE ---> EMPTY
Instruction at MUL3_FU_STAGE ---> EMPTY
Instruction at BRANCH_FU_STAGE ---> EMPTY
Instruction at MEM_FU_STAGE ---> EMPTY
~~~~~~

Details of ROB Retired Instructions –
(I5) SUB,R5,R3,R4 [SUB,P4,P1,P2]
~~~~~~

^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 17 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^

Instruction at FETCH_STAGE ---> EMPTY
Instruction at DECODE_RF_STAGE ---> EMPTY
~~~~~~

Details of RENAME TABLE State –
R[00] --> P0
R[03] --> P1
R[04] --> P2
R[05] --> P4
R[06] --> P3
R[10] --> P6
R[11] --> P5
~~~~~~

Details of ARF State –
R0 --> 0
R3 --> 3
R4 --> 3
R5 --> 0
R6 --> 9
~~~~~~

Details of IQ (Issue Queue) State –
~~~~~~

Details of LSQ (Load-Store Queue) State –
~~~~~~

Details of ROB (Reorder Buffer) State –
ROB[00] --> (I8) ADDL,R11,R5,#4 [ADDL,P5,P4,#4]
ROB[01] --> (I9) SUBL,R10,R0,#8 [SUBL,P6,P0,#8]
ROB[02] --> (I10) HALT
~~~~~~

Instruction at INT1_FU_STAGE ---> EMPTY
Instruction at INT2_FU_STAGE ---> (I9) SUBL,R10,R0,#8 [SUBL,P6,P0,#8]
Instruction at MUL1_FU_STAGE ---> EMPTY
Instruction at MUL2_FU_STAGE ---> EMPTY
Instruction at MUL3_FU_STAGE ---> EMPTY

Instruction at BRANCH_FU_STAGE ---> EMPTY
Instruction at MEM_FU_STAGE ---> EMPTY
~~~~~~

Details of ROB Retired Instructions –
(I6) BZ,#8
~~~~~~

^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 18 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^

Instruction at FETCH_STAGE ---> EMPTY
Instruction at DECODE_RF_STAGE ---> EMPTY
~~~~~~

Details of RENAME TABLE State –
R[00] --> P0
R[03] --> P1
R[04] --> P2
R[05] --> P4
R[06] --> P3
R[10] --> P6
R[11] --> P5
~~~~~~

Details of ARF State –
R0 --> 0
R3 --> 3
R4 --> 3
R5 --> 0
R6 --> 9
R11 --> 4
~~~~~~

Details of IQ (Issue Queue) State –
~~~~~~

Details of LSQ (Load-Store Queue) State –
~~~~~~

Details of ROB (Reorder Buffer) State –
ROB[00] --> (I9) SUBL,R10,R0,#8 [SUBL,P6,P0,#8]
ROB[01] --> (I10) HALT
~~~~~~

Instruction at INT1_FU_STAGE ---> EMPTY
Instruction at INT2_FU_STAGE ---> EMPTY
Instruction at MUL1_FU_STAGE ---> EMPTY
Instruction at MUL2_FU_STAGE ---> EMPTY
Instruction at MUL3_FU_STAGE ---> EMPTY
Instruction at BRANCH_FU_STAGE ---> EMPTY
Instruction at MEM_FU_STAGE ---> EMPTY
~~~~~~

Details of ROB Retired Instructions –
~~~~~~

(I8) ADDL,R11,R5,#4 [ADDL,P5,P4,#4]
~~~~~~

^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 19 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^

Instruction at FETCH_STAGE ---> EMPTY
Instruction at DECODE_RF_STAGE ---> EMPTY
~~~~~~

Details of RENAME TABLE State –
R[00] --> P0
R[03] --> P1
R[04] --> P2
R[05] --> P4
R[06] --> P3
R[10] --> P6
R[11] --> P5
~~~~~~

Details of ARF State –
R0 --> 0
R3 --> 3
R4 --> 3
R5 --> 0
R6 --> 9
R10 --> -8
R11 --> 4
~~~~~~

Details of IQ (Issue Queue) State –
~~~~~~

Details of LSQ (Load-Store Queue) State –
~~~~~~

Details of ROB (Reorder Buffer) State –
ROB[00] --> (I10) HALT
~~~~~~

Instruction at INT1_FU_STAGE ---> EMPTY
Instruction at INT2_FU_STAGE ---> EMPTY
Instruction at MUL1_FU_STAGE ---> EMPTY
Instruction at MUL2_FU_STAGE ---> EMPTY
Instruction at MUL3_FU_STAGE ---> EMPTY
Instruction at BRANCH_FU_STAGE ---> EMPTY
Instruction at MEM_FU_STAGE ---> EMPTY
~~~~~~

Details of ROB Retired Instructions –
(I9) SUBL,R10,R0,#8 [SUBL,P6,P0,#8]
~~~~~~

#--#--#--#--#--#--#--#--#--#--#--#--#--#-- SIMULATION FINISHED #--#--#--#--#--#--#--#--#--#--#--#--#--
~~~~~~

```
================= STATE OF ARCHITECTURAL REGISTER FILE ====================
-----------------------------------------------------------------------------------------------------
| ARF[00] | Value = 00 |
| ARF[03] | Value = 03 |
| ARF[04] | Value = 03 |
| ARF[05] | Value = 00 |
| ARF[06] | Value = 09 |
| ARF[10] | Value = - 8 |
| ARF[11] | Value = 04 |
-----------------------------------------------------------------------------------------------------
================= STATE OF DATA MEMORY ================================
-----------------------------------------------------------------------------------------------------
| MEM[04] | Value = 09 |
-----------------------------------------------------------------------------------------------------
```