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ECE 25
Section: A52
Wednesday, 7p-10p, WLH 2211

Lab 1: Using Vivado

Introduction: The purpose of this lab is to become familiar with Xilinx Vivado, the main design tool we will be using for the following labs. After completing this lab, we will become acquainted with the software and using basic Hardware Description Language (HDL) to design circuits. We are also expected to know how to simulate circuits and downloading circuit designs onto the FPGA BASYS3 board's programming chip.

Procedure:

- Create a project on Vivado by giving it a name, file location. Select the port and BASYS3 board
- Then, program the BASYS3 board by first creating a source file to design code and specifying the ports in the module definition with three inputs and one output
- Generate a schematic by inserting code to add "wires" and "gates" to connect individual circuit parts
- Then, simulate the design to test the circuit by adding a simulation course file using Post Order Conventions
- Initiate all inputs to zero, set all inputs to generate eight possible input conventions (2^3 = 8), and set the timescale, then run the simulation
- Download verified design into BASYS3 programmable chip by assigning corresponding pins for inputs and output to the computer.
- Use switches on board to verify circuit is correct and the same as simulation

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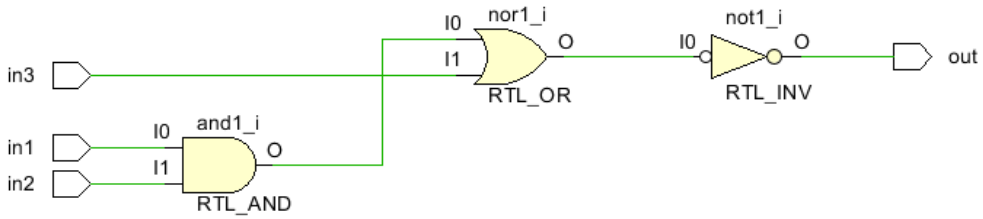
Circuit Diagrams:

Figure 1:



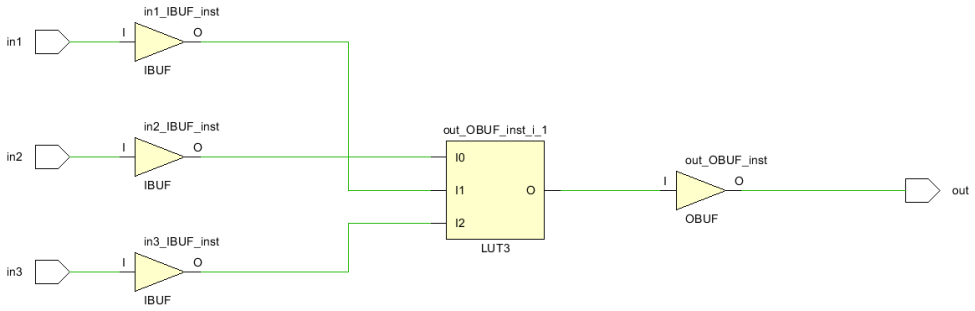


Figure 2:

Data:

ECE25_Lab_1 File

```
module first (input in1, input in2, input in3, output out);

wire wire1, wire2;

and and1(wire1, in1, in2);
nor nor1(wire2, wire1, in3);
not not1(out, wire2);

endmodule
```

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Lab1_Simulation File

```
`timescale 1ns/1ps

module simulation ();

reg in1, in2, in3;
wire out;

//instantiate the module
first first1(in1, in2, in3, out);

initial
begin
//initialize inputs

in1 = 0; in2 = 0; in3 = 0;

#10 in1 = 0; in2 = 0; in3 =1;
#10 in1 = 0; in2 = 1; in3 =0;
#10 in1 = 0; in2 = 1; in3 =1;
#10 in1 = 1; in2 = 0; in3 = 0;
#10 in1 = 1; in2 = 0; in3 = 1;
#10 in1 = 1; in2 = 1; in3 = 0;
#10 in1 = 1; in2 = 1; in3 = 1;

end

Endmodule
```

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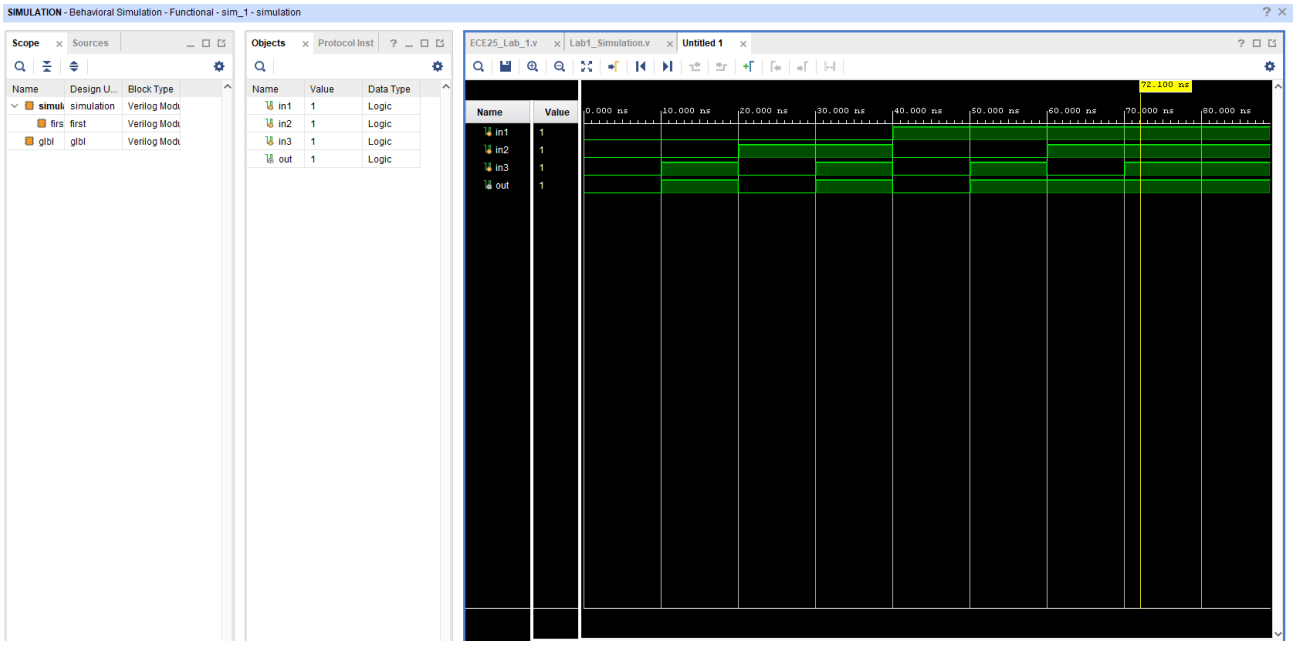

Figure 3:

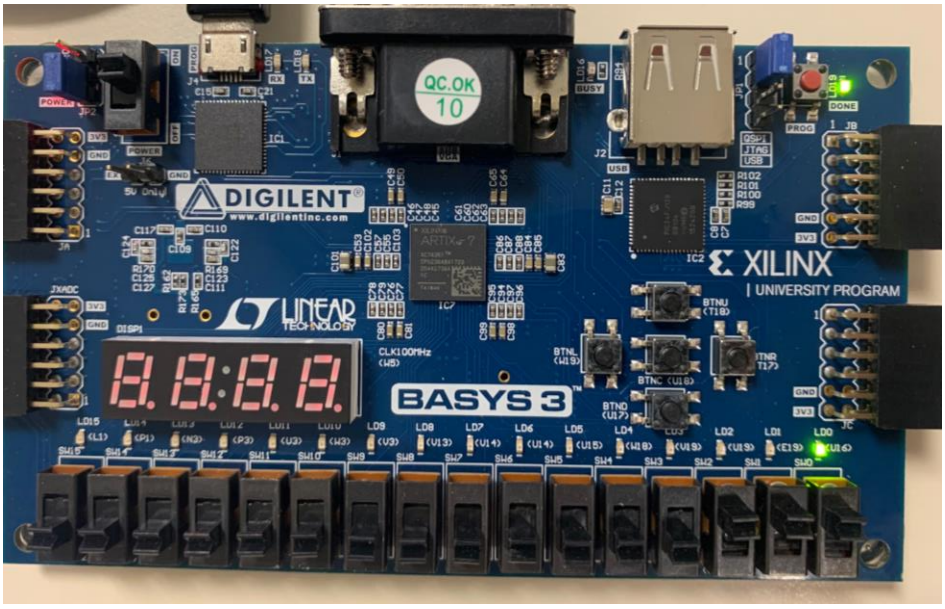

Figure 4:
LD0 lights up, displaying a true result when all inputs are switched on as true.

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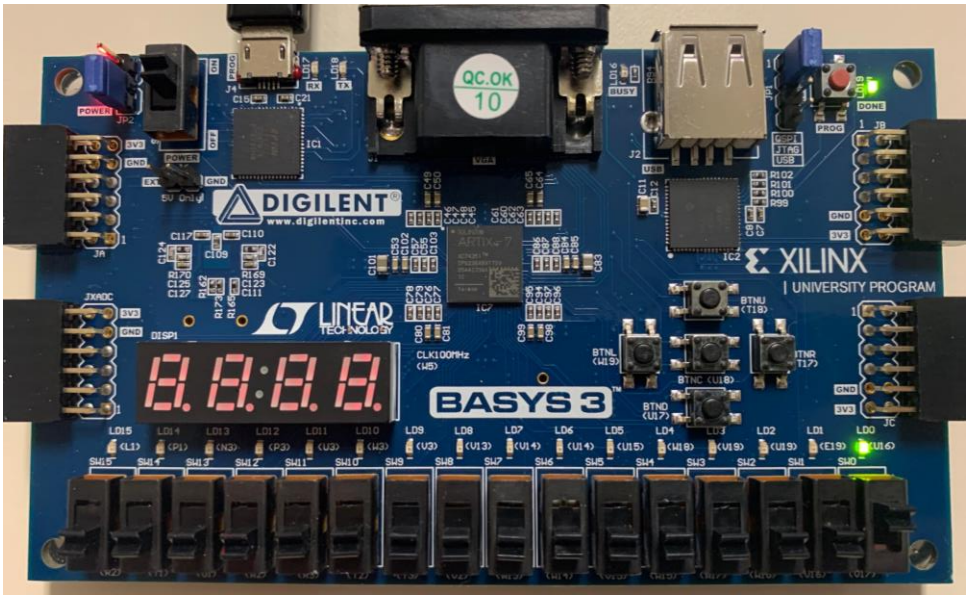

Figure 5:
LD0 lights up displaying a true result when only in3 is true. In3, bottom right, is switch SW0 which the computer reads as V17.

Truth Table:

In1 W16	In2 V16	In3 V17	out U16
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

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Analysis:

Xilinx Vivado allows the user to use Hardware Designer Language (HDL) to design circuits and simulate them. We used a BASYS3 board and its programmable chip to program and generate a schematic using Hardware Description Language, simulate its design with a simulation source, and download a verified design onto the programmable chip using assigned pins on the chip. By flipping the three switches on and off in accordance with the eight different possibilities, we verified that our downloaded circuit was correct and the LED (LD0) turned on when the output was true. Referring to the green waveforms and our truth table proved useful in checking if our circuit was correct.

We generated our schematic on Vivaldo with three inputs using an AND gate, NOR gate, and NOT gate (inverter) by specifying ports in the module definitions as seen in the code above. After downloading the design to the chip, we assigned switches SW2, SW1, and SW0 as inputs to in1, in2, and in3 respectively. LD0, the LED, was assigned as the output. The computer, however, reads these switches as W16, V16, V17 as in1, in2, and in3, and LD0 as U16. SW2, SW1, SW0, and LD0 are only for readable code.

Conclusion:

So we can check the digital circuit and stimulate through the HDL from the logic gate and truth table. We have tested the output by programming the wire to HDL; then, we connect it to a Schematic file to simulate and test the data after flipping the digit (0 and 1). The result of the actual tables is related to the Data in Figure 2. We did double-checking to load the system onto the circuit, and we are investigating the following truth table.

In the end, the lab made us familiar with Electrical Engineering related to Digital Circuits and Programing as an introductory course. This lab is an introduction to the future lab based on the software and integration of hardware such (HDL and Verilog). It is a combination of physical circuits and digital circuits to make devices and work with the operating systems in class. Basically, it makes us familiar with the circuit and programming languages for the future course and a career.