1. Description

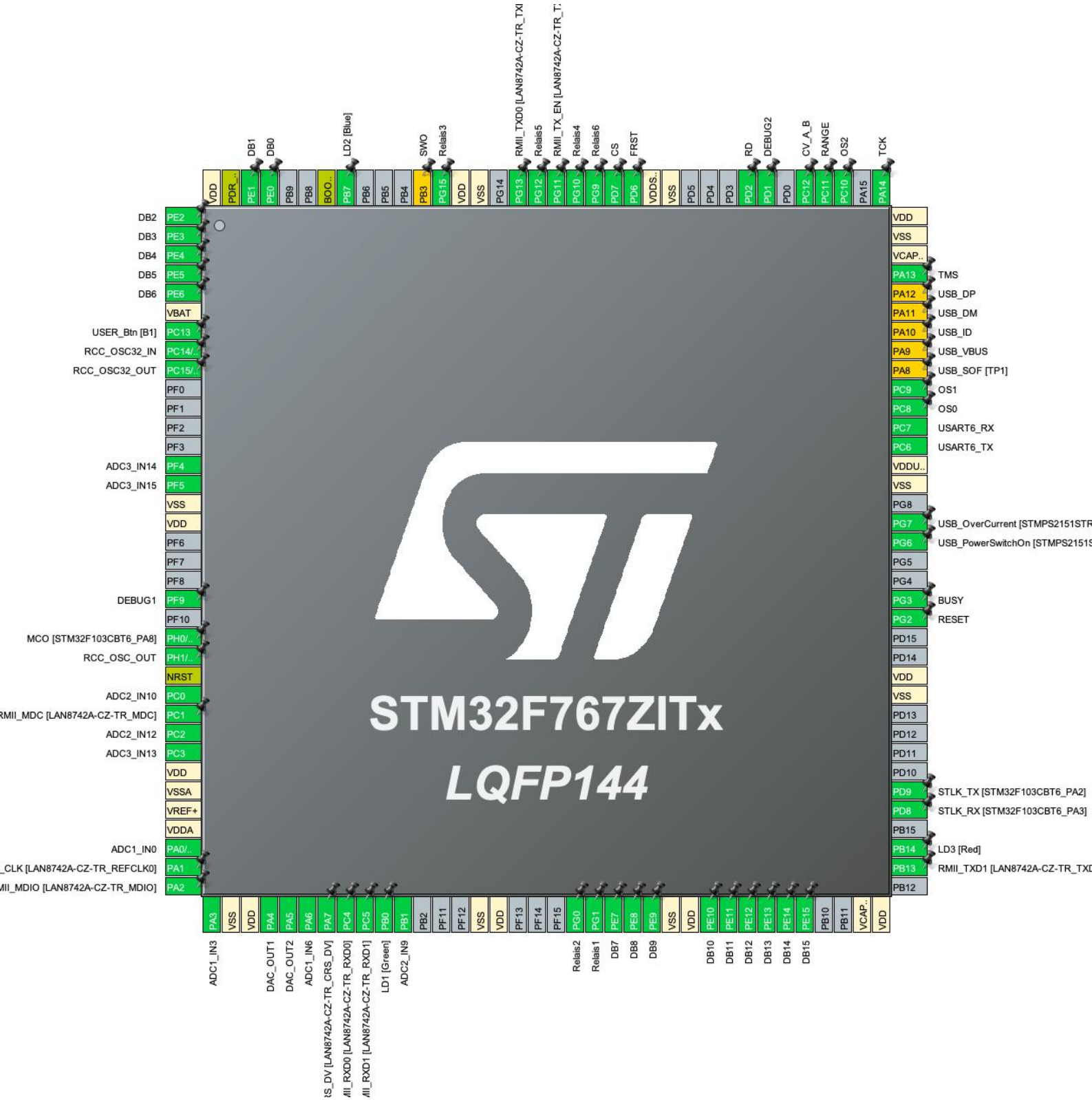
1.1. Project

Project Name	MotherEnigine
Board Name	NUCLEO-F767ZI
Generated with:	STM32CubeMX 5.4.0
Date	12/15/2019

1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x7
MCU name	STM32F767ZITx
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Input	DB2
2	PE3 *	I/O	GPIO_Input	DB3
3	PE4 *	I/O	GPIO_Input	DB4
4	PE5 *	I/O	GPIO_Input	DB5
5	PE6 *	I/O	GPIO_Input	DB6
6	VBAT	Power		
7	PC13	I/O	GPIO_EXTI13	USER_Btn [B1]
8	PC14/OSC32_IN	I/O	RCC_OSC32_IN	
9	PC15/OSC32_OUT	I/O	RCC_OSC32_OUT	
14	PF4	I/O	ADC3_IN14	
15	PF5	I/O	ADC3_IN15	
16	VSS	Power		
17	VDD	Power		
21	PF9 *	I/O	GPIO_Output	DEBUG1
23	PH0/OSC_IN	I/O	RCC_OSC_IN	MCO [STM32F103CBT6_PA8]
24	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
25	NRST	Reset		
26	PC0	I/O	ADC2_IN10	
27	PC1	I/O	ETH_MDC	RMII_MDC [LAN8742A-CZ-TR_MDC]
28	PC2	I/O	ADC2_IN12	
29	PC3	I/O	ADC3_IN13	
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
34	PA0/WKUP	I/O	ADC1_IN0	
35	PA1	I/O	ETH_REF_CLK	RMII_REF_CLK [LAN8742A-CZ-TR_REFCLK0]
36	PA2	I/O	ETH_MDIO	RMII_MDIO [LAN8742A-CZ-TR_MDIO]
37	PA3	I/O	ADC1_IN3	
38	VSS	Power		
39	VDD	Power		
40	PA4	I/O	DAC_OUT1	

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
41	PA5	I/O	DAC_OUT2	
42	PA6	I/O	ADC1_IN6	
43	PA7	I/O	ETH_CRS_DV	RMII_CRS_DV [LAN8742A-CZ-TR_CRS_DV]
44	PC4	I/O	ETH_RXD0	RMII_RXD0 [LAN8742A-CZ-TR_RXD0]
45	PC5	I/O	ETH_RXD1	RMII_RXD1 [LAN8742A-CZ-TR_RXD1]
46	PB0 *	I/O	GPIO_Output	LD1 [Green]
47	PB1	I/O	ADC2_IN9	
51	VSS	Power		
52	VDD	Power		
56	PG0 *	I/O	GPIO_Output	Relais2
57	PG1 *	I/O	GPIO_Output	Relais1
58	PE7 *	I/O	GPIO_Input	DB7
59	PE8 *	I/O	GPIO_Input	DB8
60	PE9 *	I/O	GPIO_Input	DB9
61	VSS	Power		
62	VDD	Power		
63	PE10 *	I/O	GPIO_Input	DB10
64	PE11 *	I/O	GPIO_Input	DB11
65	PE12 *	I/O	GPIO_Input	DB12
66	PE13 *	I/O	GPIO_Input	DB13
67	PE14 *	I/O	GPIO_Input	DB14
68	PE15 *	I/O	GPIO_Input	DB15
71	VCAP_1	Power		
72	VDD	Power		
74	PB13	I/O	ETH_TXD1	RMII_TXD1 [LAN8742A-CZ-TR_TXD1]
75	PB14 *	I/O	GPIO_Output	LD3 [Red]
77	PD8	I/O	USART3_TX	STLK_RX [STM32F103CBT6_PA3]
78	PD9	I/O	USART3_RX	STLK_TX [STM32F103CBT6_PA2]
83	VSS	Power		
84	VDD	Power		
87	PG2 *	I/O	GPIO_Output	RESET
88	PG3 *	I/O	GPIO_Output	BUSY
91	PG6 *	I/O	GPIO_Output	USB_PowerSwitchOn [STMPS2151STR_EN]

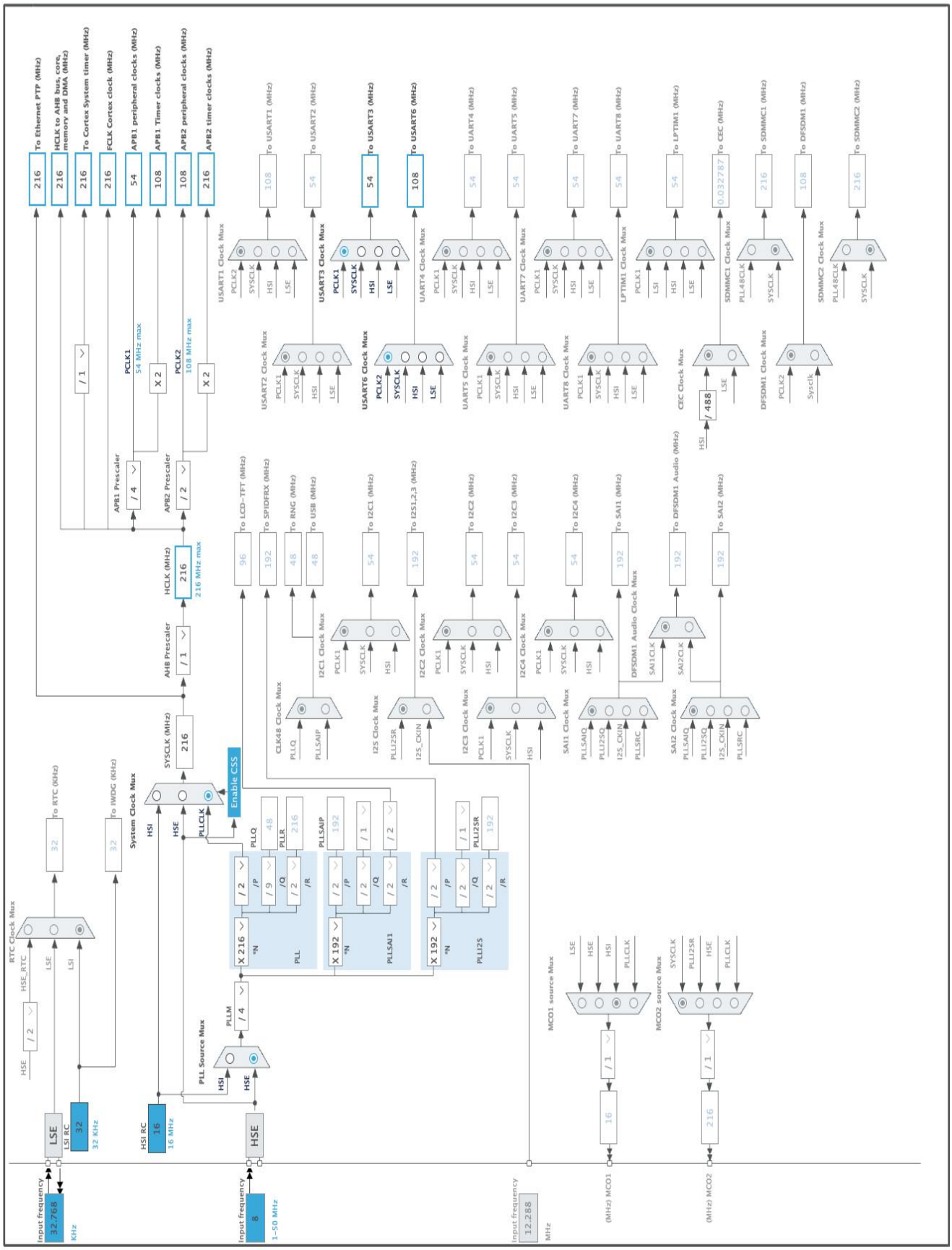
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
92	PG7 *	I/O	GPIO_Input	USB_OverCurrent [STMPS2151STR_FAULT]
94	VSS	Power		
95	VDDUSB	Power		
96	PC6	I/O	USART6_TX	
97	PC7	I/O	USART6_RX	
98	PC8 *	I/O	GPIO_Output	OS0
99	PC9 *	I/O	GPIO_Output	OS1
100	PA8 **	I/O	USB_OTG_FS_SOF	USB_SOF [TP1]
101	PA9 **	I/O	USB_OTG_FS_VBUS	USB_VBUS
102	PA10 **	I/O	USB_OTG_FS_ID	USB_ID
103	PA11 **	I/O	USB_OTG_FS_DM	USB_DM
104	PA12 **	I/O	USB_OTG_FS_DP	USB_DP
105	PA13	I/O	SYS_JTMS-SWDIO	TMS
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14	I/O	SYS_JTCK-SWCLK	TCK
111	PC10 *	I/O	GPIO_Output	OS2
112	PC11 *	I/O	GPIO_Output	RANGE
113	PC12 *	I/O	GPIO_Output	CV_A_B
115	PD1 *	I/O	GPIO_Output	DEBUG2
116	PD2 *	I/O	GPIO_Output	RD
120	VSS	Power		
121	VDDSDMMC	Power		
122	PD6 *	I/O	GPIO_Input	FRST
123	PD7 *	I/O	GPIO_Output	CS
124	PG9 *	I/O	GPIO_Output	Relais6
125	PG10 *	I/O	GPIO_Output	Relais4
126	PG11	I/O	ETH_TX_EN	RMII_TX_EN [LAN8742A-CZ-TR_TXEN]
127	PG12 *	I/O	GPIO_Output	Relais5
128	PG13	I/O	ETH_TXD0	RMII_TXD0 [LAN8742A-CZ-TR_TXD0]
130	VSS	Power		
131	VDD	Power		
132	PG15 *	I/O	GPIO_Output	Relais3
133	PB3 **	I/O	SYS_JTDO-SWO	SWO
137	PB7 *	I/O	GPIO_Output	LD2 [Blue]
138	BOOT0	Boot		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
141	PE0 *	I/O	GPIO_Input	DB0
142	PE1 *	I/O	GPIO_Input	DB1
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	MotherEnigine
Project Folder	/Users/christiansager/klanghabitat_quantum/firmware/STM32_Workspace/Mother
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_F7 V1.15.0

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x7
MCU	STM32F767ZITx
Datasheet	029041_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.6

7. IPs and Middleware Configuration

7.1. ADC1

mode: IN0

mode: IN3

mode: IN6

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	**8 bits (11 ADC Clock cycles) ***
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	**EOC flag at the end of all conversions ***

ADC_Regular_ConversionMode:

Number Of Conversion	**2 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 0
Sampling Time	**84 Cycles ***
Rank	**2 ***
Channel	**Channel 3 ***
Sampling Time	**112 Cycles ***

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.2. ADC2

mode: IN9
mode: IN10
mode: IN12
7.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	**8 bits (11 ADC Clock cycles) ***
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	**EOC flag at the end of all conversions ***

ADC_Regular_ConversionMode:

Number Of Conversion	**2 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 9
Sampling Time	**84 Cycles ***
Rank	**2 ***
Channel	Channel 9
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.3. ADC3
mode: IN13
mode: IN14
mode: IN15
7.3.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 13
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.4. CORTEX_M7

7.4.1. Parameter Settings:

Cortex Interface Settings:

Flash Interface	AXI Interface
ART ACCLERATOR	Disabled
Instruction Prefetch	Disabled
CPU ICache	**Enabled ***
CPU DCache	**Enabled ***

Cortex Memory Protection Unit Control Settings:

MPU Control Mode	MPU NOT USED

7.5. DAC

mode: OUT1 Configuration

mode: OUT2 Configuration

7.5.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	Enable
Trigger	None

DAC Out2 Settings:

Output Buffer	Enable
Trigger	None

7.6. ETH

Mode: RMII

7.6.1. Parameter Settings:

Advanced : Ethernet Media Configuration:

Auto Negotiation	Enabled

General : Ethernet Configuration:

Ethernet MAC Address	00:80:E1:00:00:00
PHY Address	**0 ***

Ethernet Basic Configuration:

Rx Mode	Interrupt Mode
TX IP Header Checksum Computation	By hardware

7.6.2. Advanced Parameters:

External PHY Configuration:

PHY	LAN8742A_PHY_ADDRESS
PHY Address Value	0
PHY Reset delay these values are based on a 1 ms Systick interrupt	**0x000000FF ***
PHY Configuration delay	**0x00000FFF ***
PHY Read TimeOut	**0x0000FFFF ***
PHY Write TimeOut	**0x0000FFFF ***

Common : External PHY Configuration:

Transceiver Basic Control Register	**0x00 ***

Transceiver Basic Status Register	**0x01 ***
PHY Reset	**0x8000 ***
Select loop-back mode	**0x4000 ***
Set the full-duplex mode at 100 Mb/s	**0x2100 ***
Set the half-duplex mode at 100 Mb/s	**0x2000 ***
Set the full-duplex mode at 10 Mb/s	**0x0100 ***
Set the half-duplex mode at 10 Mb/s	**0x0000 ***
Enable auto-negotiation function	**0x1000 ***
Restart auto-negotiation function	**0x0200 ***
Select the power down mode	**0x0800 ***
Isolate PHY from MII	**0x0400 ***
Auto-Negotiation process completed	**0x0020 ***
Valid link established	**0x0004 ***
Jabber condition detected	**0x0002 ***

Extended : External PHY Configuration:

PHY special control/status register Offset	**0x1F ***
PHY Speed mask	**0x0004 ***
PHY Duplex mask	**0x0010 ***
PHY Interrupt Source Flag register Offset	**0x001D ***
PHY Link down inturrupt	**0x000B ***

7.7. GFXSIMULATOR

7.7.1. Simulator Graphic:

7.8. GPIO

7.9. RCC

High Speed Clock (HSE): BYPASS Clock Source

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.9.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	7 WS (8 CPU cycle)

RCC Parameters:

HSI Calibration Value	16

TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Over Drive	Enabled
Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

7.10. SYS

Debug: Serial Wire

Timebase Source: TIM1

7.11. TIM5

mode: Clock Source

7.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**216 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**1000 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	**Update Event ***

7.12. TIM6

mode: Activated

7.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**107 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**65535 ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.13. TIM7

mode: Activated

7.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**107 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**65535 ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.14. USART3

Mode: Asynchronous

7.14.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.15. USART6

Mode: Asynchronous

7.15.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.16. FREERTOS

Interface: CMSIS_V1

7.16.1. Config parameters:

API:

FreeRTOS API	CMSIS v1

Versions:

FreeRTOS version	10.0.1
CMSIS-RTOS version	1.02

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000

MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled

Memory management settings:

Memory Allocation	Dynamic / Static
TOTAL_HEAP_SIZE	15360
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Disabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Disabled

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	**1 ***

7.16.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Disabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled

7.17. LWIP

mode: Enabled

Advanced parameters are not listed except if modified by user.

7.17.1. General Settings:

LwIP Version:

LwIP Version (Version of LwIP supported by CubeMX ** CubeMX specific **)	2.0.3

IPv4 - DHCP Options:

LWIP_DHCP (DHCP Module)	**Disabled ***

IP Address Settings:

IP_ADDRESS (IP Address)	**192.168.001.205 ***
NETMASK_ADDRESS (Netmask Address)	**255.255.255.000 ***
GATEWAY_ADDRESS (Gateway Address)	**192.168.001.001 ***

RTOS Dependency:

WITH_RTOS (Use FREERTOS ** CubeMX specific **)	Enabled
CMSIS_VERSION (CMSIS API Version used)	CMSIS v1

Protocols Options:

LWIP_ICMP (ICMP Module Activation)	Enabled
LWIP_IGMP (IGMP Module)	Disabled

LWIP_DNS (DNS Module)	Disabled
LWIP_UDP (UDP Module)	Enabled
MEMP_NUM_UDP_PCB (Number of UDP Connections)	4
LWIP_TCP (TCP Module)	Enabled
MEMP_NUM_TCP_PCB (Number of TCP Connections)	5

7.17.2. Key Options:

Infrastructure - OS Awarness Option:

NO_SYS (OS Awarness)	OS Used

Infrastructure - Timers Options:

LWIP_TIMERS (Use Support For sys_timeout)	Enabled

Infrastructure - Core Locking and MPU Options:

SYS_LIGHTWEIGHT_PROT (Memory Functions Protection)	Enabled

Infrastructure - Heap and Memory Pools Options:

MEM_SIZE (Heap Memory Size)	1600

Infrastructure - Internal Memory Pool Sizes:

MEMP_NUM_PBUF (Number of Memory Pool struct Pbufs)	16
MEMP_NUM_RAW_PCB (Number of Raw Protocol Control Blocks)	4
MEMP_NUM_TCP_PCB_LISTEN (Number of Listening TCP Connections)	8
MEMP_NUM_TCP_SEG (Number of TCP Segments simultaneously queued)	16
MEMP_NUM_LOCALHOSTLIST (Number of Host Entries in the Local Host List)	1

Pbuf Options:

PBUF_POOL_SIZE (Number of Buffers in the Pbuf Pool)	16
PBUF_POOL_BUFSIZE (Size of each pbuf in the pbuf pool)	592

IPv4 - ARP Options:

LWIP_ARP (ARP Functionality)	Enabled

Callback - TCP Options:

TCP_TTL (Number of Time-To-Live Used by TCP Packets)	255
TCP_WND (TCP Receive Window Maximum Size)	2144
TCP_QUEUE_OOSEQ (Allow Out-Of-Order Incoming Packets)	Enabled
TCP_MSS (Maximum Segment Size)	536
TCP_SND_BUF (TCP Sender Buffer Space)	1072
TCP_SND_QUEUELEN (Number of Packet Buffers Allowed for TCP Sender)	9

Network Interfaces Options:

LWIP_NETIF_STATUS_CALLBACK (Callback Function on Interface Status Changes)	Disabled
LWIP_NETIF_LINK_CALLBACK (Callback Function on Interface Link Changes)	Disabled

NETIF - Loopback Interface Options:

LWIP_NETIF_LOOPBACK (NETIF Loopback)	Disabled

Infrastructure - Threading Options:

TCPIP_THREAD_NAME (TCPIP Thread Name)	"tcpip_thread"
TCPIP_THREAD_STACKSIZE (TCPIP Thread Stack Size)	1024
TCPIP_THREAD_PRIO (TCPIP Thread Priority Level)	3
TCPIP_MBOX_SIZE (TCPIP Mailbox Size)	6
DEFAULT_THREAD_NAME (Default LwIP Thread Name)	"lwIP"
DEFAULT_THREAD_STACKSIZE (Default LwIP Thread Stack Size)	1024
DEFAULT_THREAD_PRIO (Default LwIP Thread Priority Level)	3
DEFAULT_RAW_RECVMBOX_SIZE (Default Mailbox Size on a NETCONN Raw)	0
DEFAULT_TCP_RECVMBOX_SIZE (Default Mailbox Size on a NETCONN TCP)	6
DEFAULT_ACCEPTMBOX_SIZE (Default Mailbox Size for Incoming Connections)	6

Thread Safe APIs - Netconn Options:

LWIP_NETCONN (NETCONN API)	Enabled

Thread Safe APIs - Socket Options:

LWIP_SOCKET (Socket API)	Enabled
LWIP_COMPAT_SOCKETS (BSD-style Socket Functions Names)	1
LWIP_SOCKET_OFFSET (Socket Offset Number)	0

7.17.3. PPP:

PPP Options:

PPP_SUPPORT (PPP Module)	Disabled

7.17.4. IPv6:

IPv6 Options:

LWIP_IPV6 (IPv6 Protocol)	Disabled

7.17.5. HTTPD:

HTTPD Options:

LWIP_HTTPD (LwIP HTTPD Support ** CubeMX specific **)	**Enabled ***

7.17.6. SNMP:

SNMP Options:

LWIP_SNMP (LwIP SNMP Agent)	Disabled

7.17.7. SNTP:

SNTP Options:

LWIP_SNTP (LWIP SNTP Support ** CubeMX specific **)	Disabled

7.17.8. MDNS/TFTP:

MDNS Options:

LWIP_MDNS (Multicast DNS Support ** CubeMX specific **)	Disabled

TFTP Options:

LWIP_TFTP (TFTP Support ** CubeMX specific **)	Disabled

7.17.9. Perf/Checks:

Sanity Checks:

LWIP_DISABLE_TCP_SANITY_CHECKS (TCP Sanity Checks)	Disabled
LWIP_DISABLE_MEMP_SANITY_CHECKS (MEMP Sanity Checks)	Disabled

Performance Options:

LWIP_PERF (Performace Testing for LwIP)	Disabled

7.17.10. Statistics:

Debug - Statistics Options:

LWIP_STATS (Statictics Collection)	Disabled

7.17.11. Checksum:

Infrastructure - Checksum Options:

CHECKSUM_BY_HARDWARE (Hardware Checksum ** CubeMX specific **)	Disabled
LWIP_CHECKSUM_CTRL_PER_NETIF (Generate/Check Checksum per Netif)	Disabled
CHECKSUM_GEN_IP (Generate Software Checksum for Outgoing IP Packets)	Disabled
CHECKSUM_GEN_UDP (Generate Software Checksum for Outgoing UDP Packets)	Disabled
CHECKSUM_GEN_TCP (Generate Software Checksum for Outgoing TCP Packets)	Disabled
CHECKSUM_GEN_ICMP (Generate Software Checksum for Outgoing ICMP Packets)	Disabled
CHECKSUM_GEN_ICMP6 (Generate Software Checksum for Outgoing ICMP6 Packets)	Disabled
CHECKSUM_CHECK_IP (Generate Software Checksum for Incoming IP Packets)	Disabled
CHECKSUM_CHECK_UDP (Generate Software Checksum for Incoming UDP Packets)	Disabled
CHECKSUM_CHECK_TCP (Generate Software Checksum for Incoming TCP Packets)	Disabled
CHECKSUM_CHECK_ICMP (Generate Software Checksum for Incoming ICMP Packets)	Disabled
CHECKSUM_CHECK_ICMP6 (Generate Software Checksum for Incoming ICMP6 Packets)	Disabled

7.17.12. Debug:

LwIP Main Debugging Options:

LWIP_DBG_MIN_LEVEL (Minimum Level)	All

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0/WKUP	ADC1_IN0	Analog mode	No pull-up and no pull-down	n/a	
	PA3	ADC1_IN3	Analog mode	No pull-up and no pull-down	n/a	
	PA6	ADC1_IN6	Analog mode	No pull-up and no pull-down	n/a	
ADC2	PC0	ADC2_IN10	Analog mode	No pull-up and no pull-down	n/a	
	PC2	ADC2_IN12	Analog mode	No pull-up and no pull-down	n/a	
	PB1	ADC2_IN9	Analog mode	No pull-up and no pull-down	n/a	
ADC3	PF4	ADC3_IN14	Analog mode	No pull-up and no pull-down	n/a	
	PF5	ADC3_IN15	Analog mode	No pull-up and no pull-down	n/a	
	PC3	ADC3_IN13	Analog mode	No pull-up and no pull-down	n/a	
DAC	PA4	DAC_OUT1	Analog mode	No pull-up and no pull-down	n/a	
	PA5	DAC_OUT2	Analog mode	No pull-up and no pull-down	n/a	
ETH	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	RMII_MDC [LAN8742A-CZ-TR_MDC]
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	RMII_REF_CLK [LAN8742A-CZ-TR_REFCLK0]
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	RMII_MDIO [LAN8742A-CZ-TR_MDIO]
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	RMII_CRS_DV [LAN8742A-CZ-TR_CRS_DV]
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	RMII_RXD0 [LAN8742A-CZ-TR_RXD0]
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	RMII_RXD1 [LAN8742A-CZ-TR_RXD1]
	PB13	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	RMII_TXD1 [LAN8742A-CZ-TR_TXD1]
	PG11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	RMII_TX_EN [LAN8742A-CZ-TR_TXEN]
	PG13	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	RMII_TXD0 [LAN8742A-CZ-TR_TXD0]
RCC	PC14/OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15/OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0/OSC_I	RCC_OSC_IN	n/a	n/a	n/a	MCO

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	N					[STM32F103CBT6_PA8]
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	TCK
USART3	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	STLK_RX [STM32F103CBT6_PA3]
	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	STLK_TX [STM32F103CBT6_PA2]
USART6	PC6	USART6_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC7	USART6_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
Single Mapped Signals	PA8	USB_OTG_FS_SOF	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USB_SOF [TP1]
	PA9	USB_OTG_FS_VBUS	Input mode	No pull-up and no pull-down	**n/a**	USB_VBUS
	PA10	USB_OTG_FS_ID	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USB_ID
	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USB_DM
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USB_DP
	PB3	SYS_JTDO-SWO	n/a	n/a	**n/a**	SWO
GPIO	PE2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DB2
	PE3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DB3
	PE4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DB4
	PE5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DB5
	PE6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DB6
	PC13	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	USER_Btn [B1]
	PF9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DEBUG1
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD1 [Green]
	PG0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Relais2
	PG1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Relais1
	PE7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DB7
	PE8	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DB8

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PE9	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DB9
	PE10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DB10
	PE11	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DB11
	PE12	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DB12
	PE13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DB13
	PE14	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DB14
	PE15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DB15
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD3 [Red]
	PG2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RESET
	PG3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	BUSY
	PG6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USB_PowerSwitchOn [STMPS2151STR_EN]
	PG7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	USB_OverCurrent [STMPS2151STR_FAULT]
	PC8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OS0
	PC9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OS1
	PC10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OS2
	PC11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RANGE
	PC12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CV_A_B
	PD1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DEBUG2
	PD2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RD
	PD6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	FRST
	PD7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CS
	PG9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Relais6
	PG10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Relais4
	PG12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Relais5
	PG15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Relais3
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [Blue]
	PE0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DB0
	PE1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DB1

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA2_Stream0	Peripheral To Memory	**Medium ***
ADC2	DMA2_Stream2	Peripheral To Memory	**Medium ***
USART6_RX	DMA2_Stream1	Peripheral To Memory	Low
USART6_TX	DMA2_Stream6	Memory To Peripheral	Low

ADC1: DMA2_Stream0 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	**Word ***

ADC2: DMA2_Stream2 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	**Word ***

USART6_RX: DMA2_Stream1 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART6_TX: DMA2_Stream6 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
ADC1, ADC2 and ADC3 global interrupts	true	1	0
TIM1 update interrupt and TIM10 global interrupt	true	0	0
TIM5 global interrupt	true	1	0
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	true	1	0
TIM7 global interrupt	true	1	0
DMA2 stream0 global interrupt	true	1	0
DMA2 stream1 global interrupt	true	1	0
DMA2 stream2 global interrupt	true	1	0
Ethernet global interrupt	true	1	0
DMA2 stream6 global interrupt	true	1	0
USART6 global interrupt	true	1	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
USART3 global interrupt	unused		
EXTI line[15:10] interrupts	unused		
Ethernet wake-up interrupt through EXTI line 19	unused		
FPU global interrupt	unused		

*** User modified value**

9. Software Pack Report