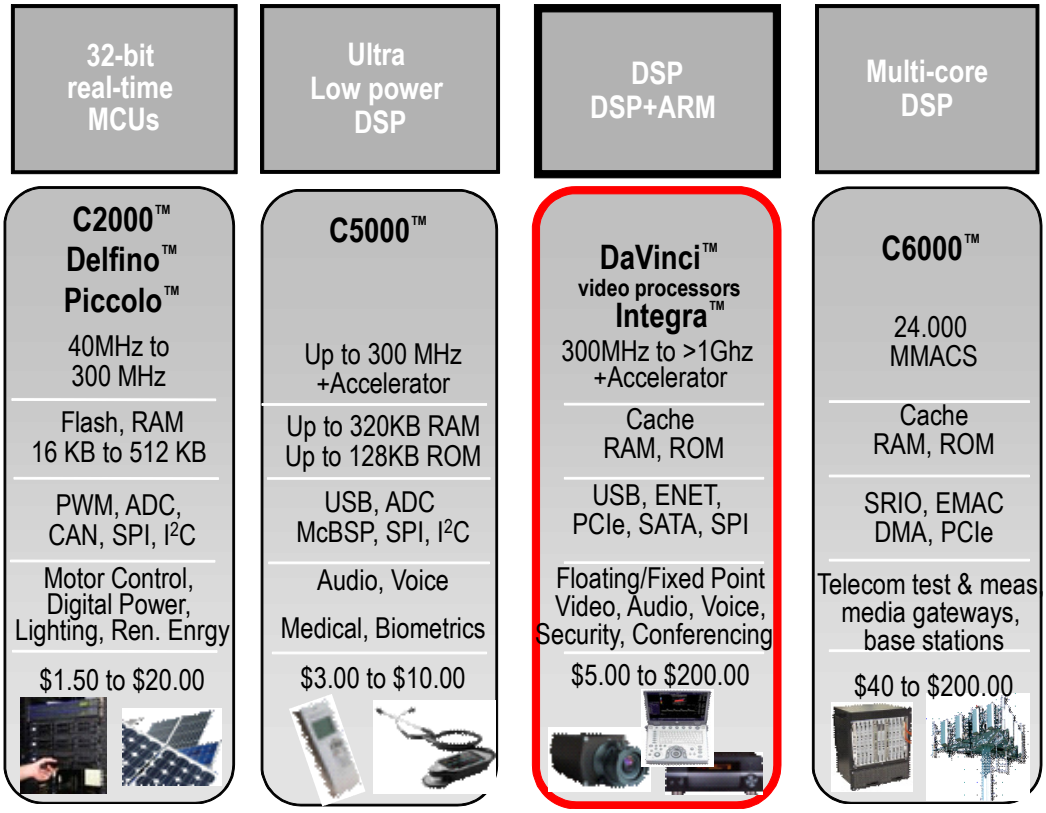
Chapter 2

The TMS320C6x Family: Hardware and Software

Introduction

In this chapter the DSPS of primary focus for the course, the TMS320C6x, will be introduced and explained in terms of hardware, software, and development environments found in the laboratory. The specific C6x family member of most interest is the C6748.

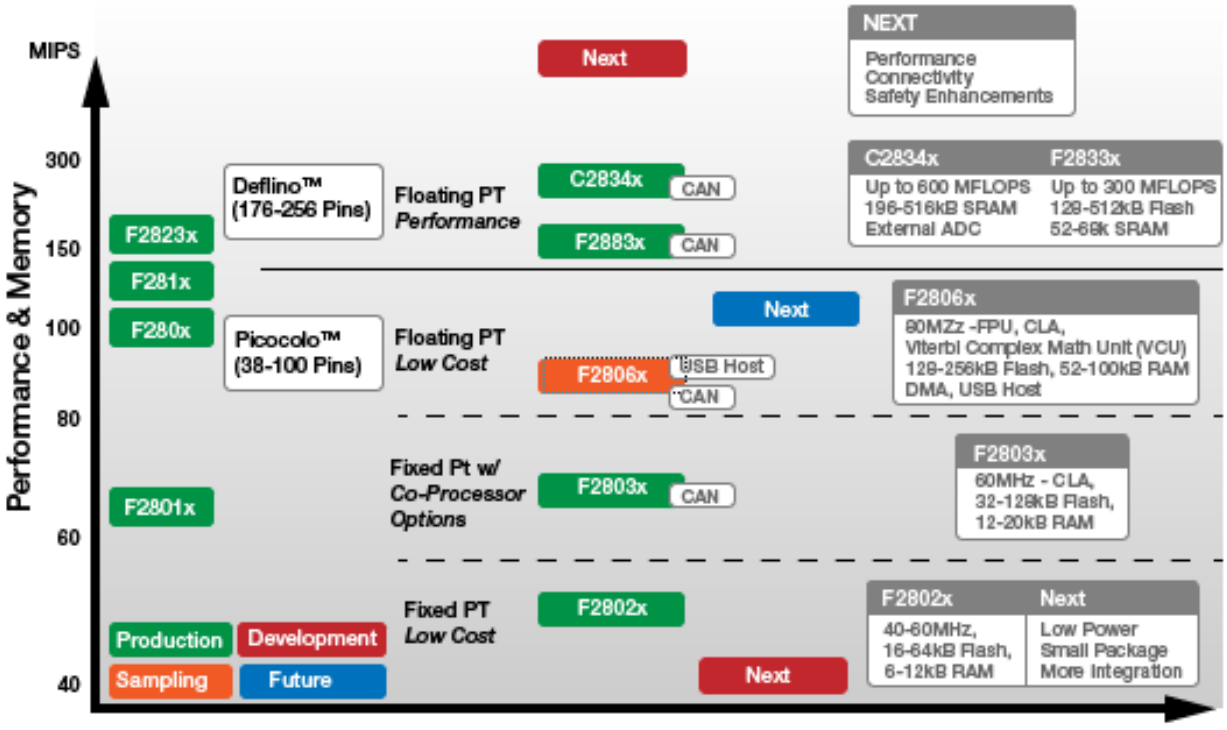
The Family of TI DSP Processors (ordered by price/performance)

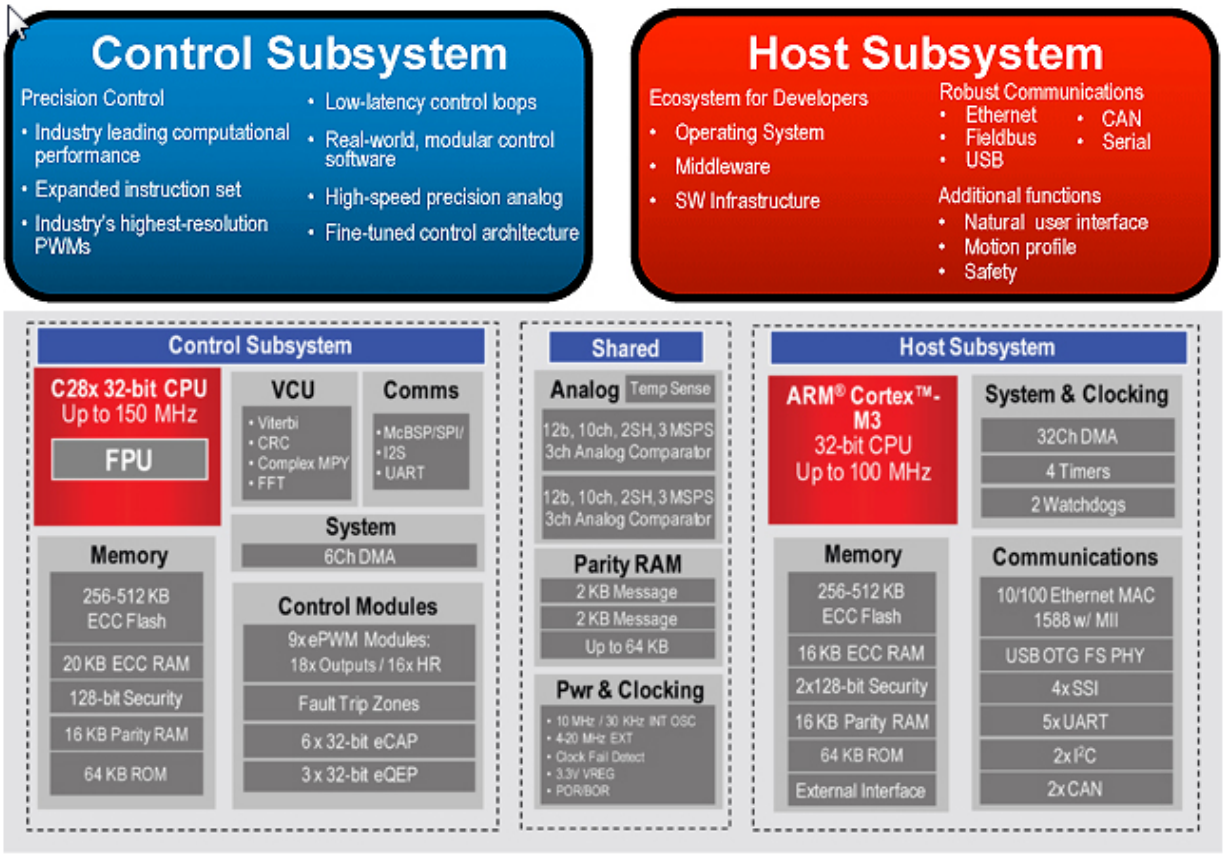


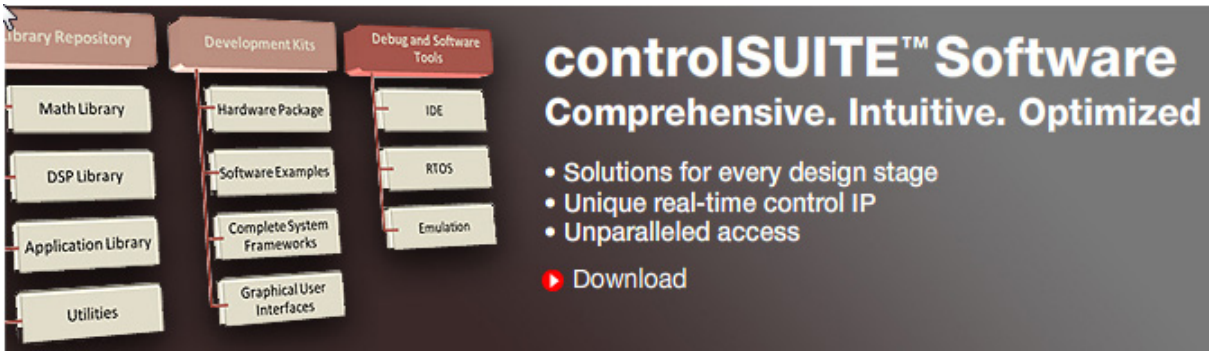
DSP Devices Overview

- TI has four classes of DSP processors
  - *C2000 Defino and Piccolo*: Devices are 32-bit microcontrollers with high performance integrated peripherals designed for real-time control applications. Its math-optimized core gives designers the means to improve system efficiency, reliability, and flexibility. Powerful integrated peripherals make C2000 devices the perfect single-chip control solution. C2000's development tools strategy and software (controlSUITE) create an open platform with the goal of maximizing usability and minimizing development time.

Product Portfolio

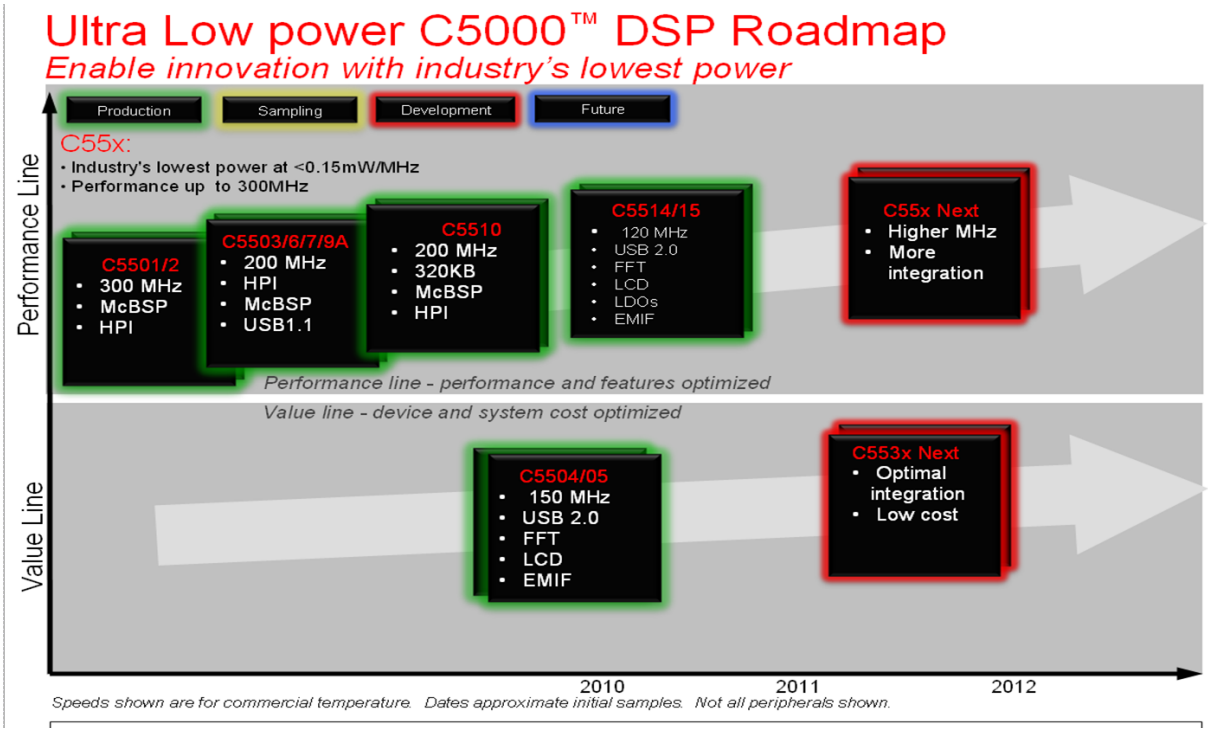






Featured Application – Digital Power Conversion

– *TMS320C5000™ Power Efficient DSPs*: Very low standby power and advanced power management, for personal and portable products; GPS receivers and medical (a short intro to the VC5505 eZDSP at the end of the chapter)



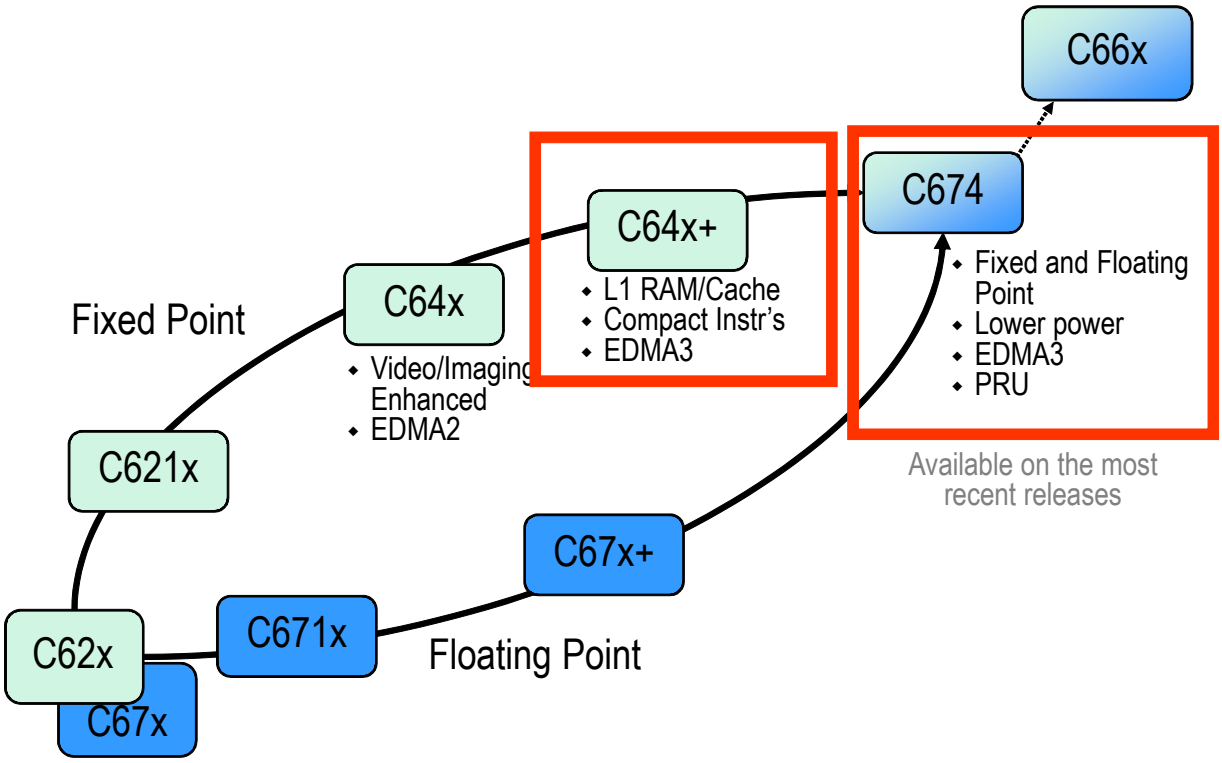
– *TMS320C6000™ DSPs*: (see below)

The C6x Families

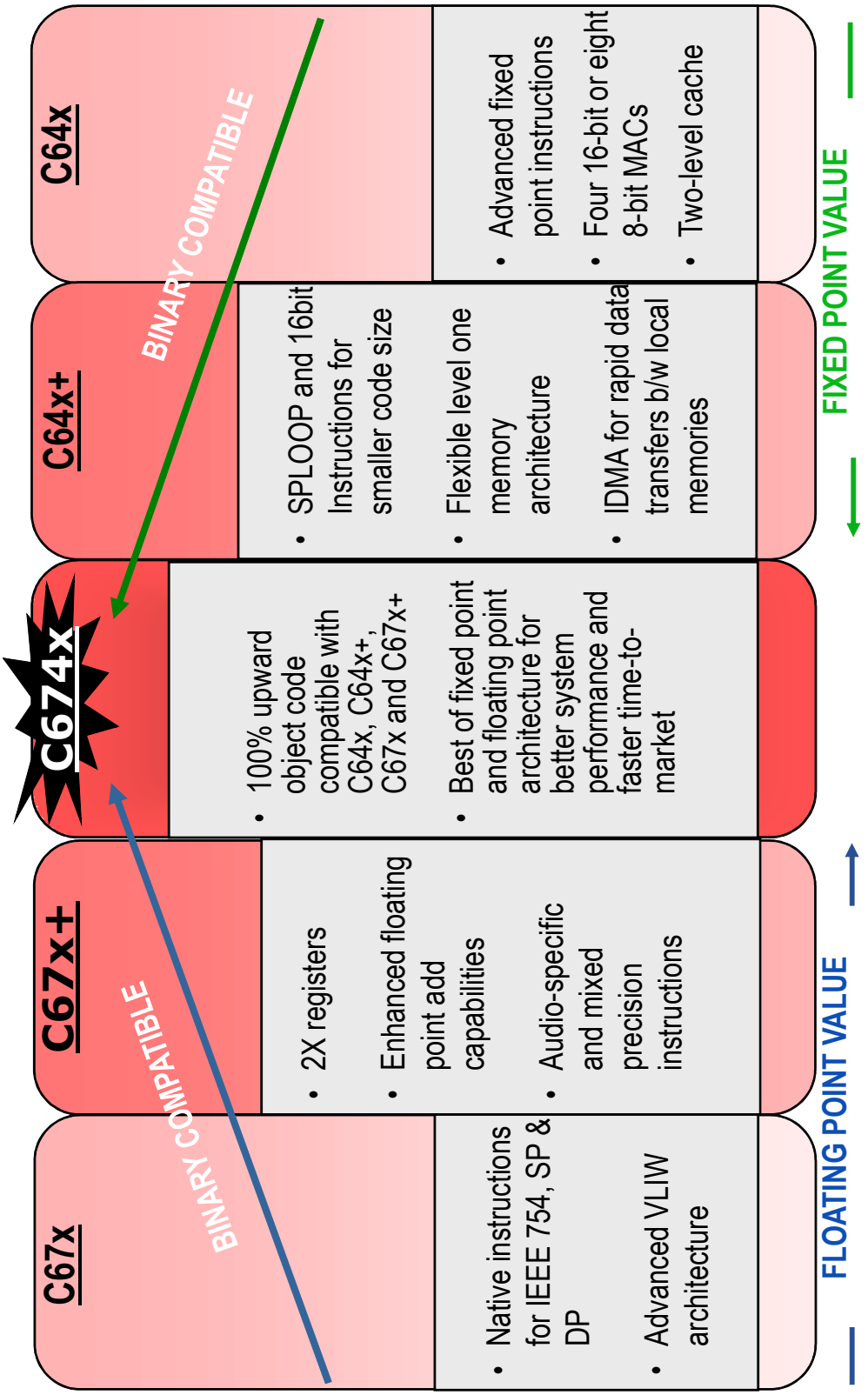
- *C64x High Performance DSPs*: Very fast fixed-point processing, with up to 1.2 GHz clock speed (9600 MMACs on C6455-1200, 24000 MMACs on CC6474-1000 with 3 cores)
- *C62x Performance Value DSPs*: High performance and high cost efficiency; optimized for wireless infrastructure, telecom infrastructure, and imaging applications (5760 MMACs on C6412-720)

- *C67x Floating Point DSPs*: The most advanced DSP C compiler and assembly optimizer for efficiency and performance; high performance audio applications (e.g., C6748 375/456-MHz Fixed/Floating point, up to 3648/2746 MIPS/MFLOPS)

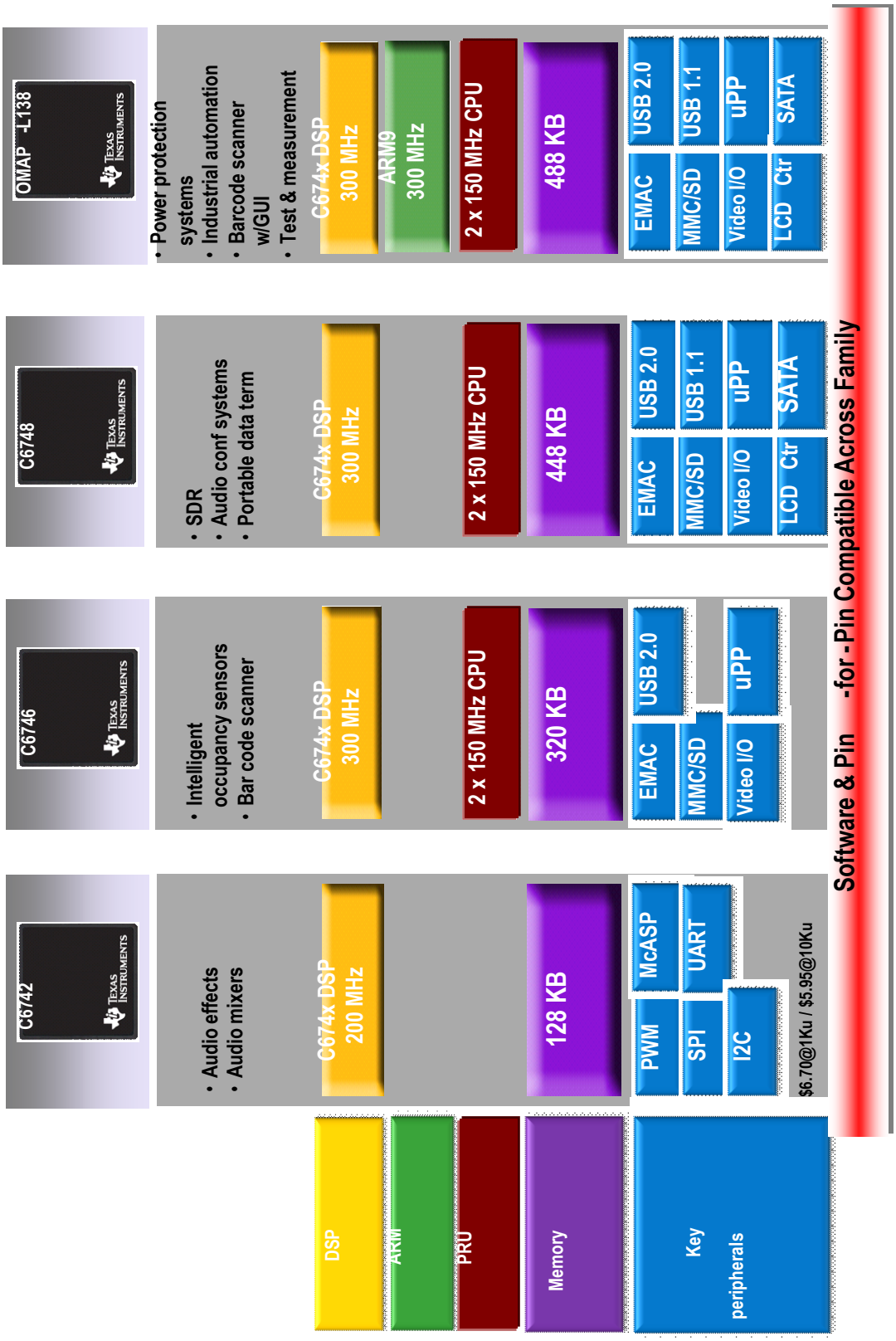
C6000 DSP Platform Roadmap



Binary Compatability



Peripheral Options



C6x Family Feature Overview

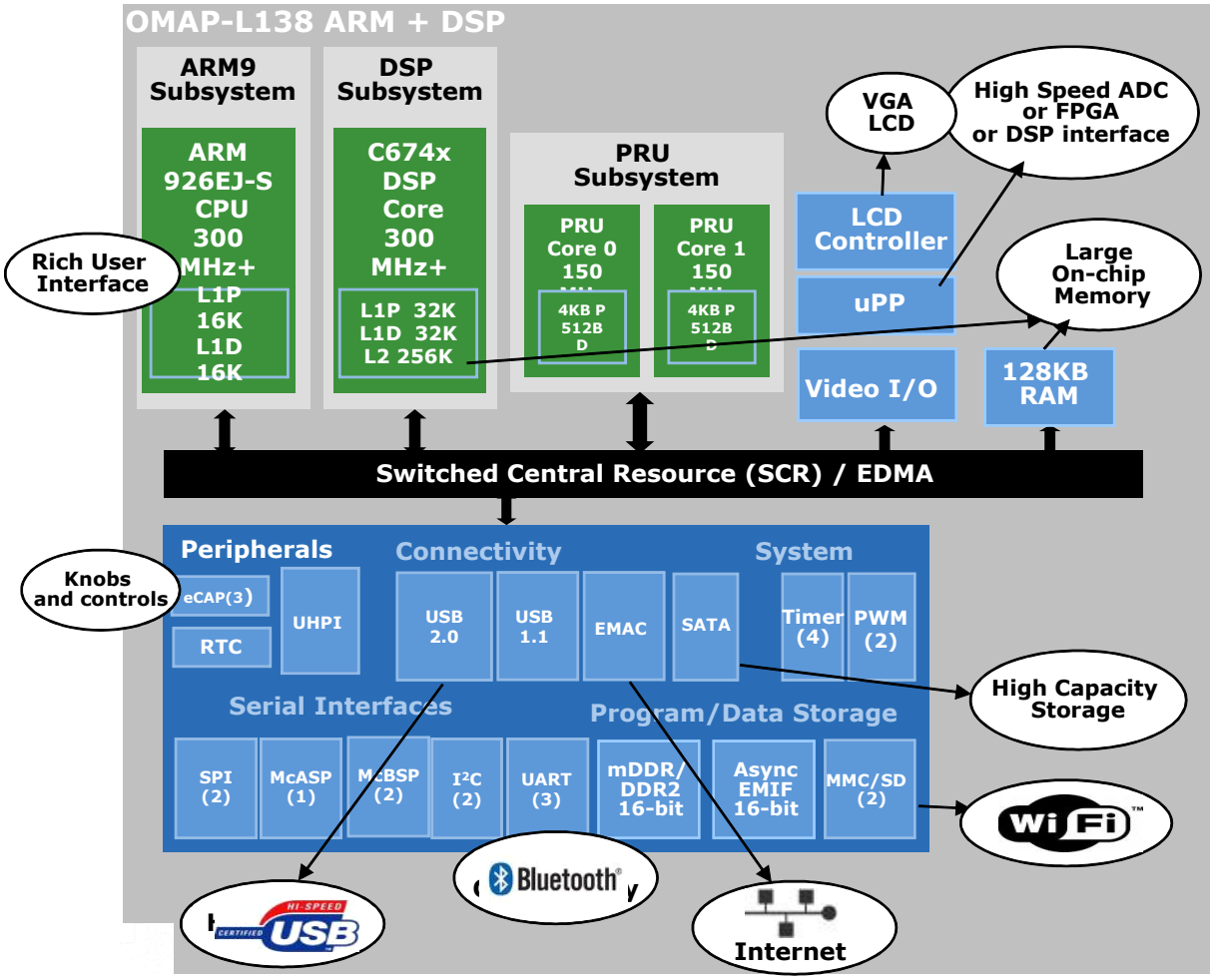
- To appreciate the C6x family consider a little history first
- The first of TI's high performance floating point processors was the C3x
- In 1988 the first of the TMS320C3x's began shipping at a cost of $1,300 each
- At the present time development of the C3x family has slowed, but a core of users still exists in the market place
- In 2000 TI introduced the C33 which is capable of 150 MFLOPS
  - This new processor featured two 1k and two 16k dual access RAM blocks
  - Consumes 0.2 W and costs $5-8 in 100KU
  - The pilot offering of this course, in 1998, used the C31 which comes in low cost 60 ns, lowers cost 74 ns, highest speed 40 ns (used in the C31 DSK), and other single-cycle execution time versions
- Today the C6x family, first announced in 1Q97, continues the high performance traditions of the C3x family, but offers much more in terms of both hardware and software
- Features of the C6x family include:
  - Code compatible fixed- and floating-point
  - Widely adopted by broad-band infrastructure vendors

- Highly parallel VelociTI™ advanced very long instruction word (VLIW) architecture
- RISC-like instructions
- Claim industry's most efficient C compiler to ease high level language (HLL) development
- Low price points ~ C6738-300 (300 MHz) is $15.75 in 1ku

Comparison Matrix

Product Attributes	Floating Pt C671x	Floating Pt C672x	Fixed Pt C6410	Fixed Pt C6421-400	NEW C6743	NEW C6745	NEW C6747	NEW C6742	NEW C6746	NEW C6748
DSP Frequency (MHz)	300	350	400	400	300/200	300/200	300/200	200	300	300
ARM Frequency (MHz)										
Peak MFLOP/MMACs	1800	2100	3200	3200	1800/2400	1800/2400	1800/2400	1800/2400	1800/2400	1800/2400
Total Power (25°C)	1.6W[1]	977mW[2]	973mW[2]	555mW[2]	470mW[3]	470mW[3]	470mW[3]	420mW[4]	420mW[4]	420mW[4]
Standby Power (25°C)	1.1W	230mW	471mW	136mW	60mW	60mW	60mW	11mW	11mW	11mW
Memory (L1 Cache)	8KB	32KB (Prog)	32 KB	64 KB	64KB	64KB	64KB	64KB	64KB	64KB
Memory (L2 Cache)	256KB	256KB	128 KB	64 KB	128 KB	256KB	256KB	64KB	256KB	256KB
Memory (L3)							128KB			128KB
EDR Memory		32/16-bit	32/16-bit		16/8-bit	16/8-bit	32/16-bit	32/16-bit	32/16-bit	32/16-bit
DDR Memory				16/8-bit				32/16-bit	32/16-bit	32/16-bit
McASP	2	3	2	1	2	2	3	1	1	1
McBSP			2	1				1	2	2
EMAC				1	1	1	1		1	1
USB 2.0						1	1		1	1
USB 1.1							1			1
VHPI	1	1	1	1			1	1	1	1
HPP									1	1
UART				2	2	3	3	1	3	3
SATA										1
PWM				3	3	3	3	3	3	3
MMC/SD					1	1	1		2	2
LCDc							1			1
Package (mm)	27x27 (BGA) 28x28 (PYP)	17x17 (BGA) 20x20 (QFP)	23x23 (BGA)	16x16 (BGA)	17x17 (BGA) 24x24 (QFP)	24x24 (QFP)	17x17 (BGA)		16x16 (BGA) 13x13 (nFPGA)	
Pricing (1ku)	$36.60	$32.50	$19.58	$11.73	$9.00	$11.25	$12.95	$6.70	$13.50	$15.20

C6x Architecture Overview



CPU Cores
- ARM926EJ-S™ (MPU) 300MHz+
- C674x DSP Core 300MHz+
- 2 PRU Cores upto 150 MHz each

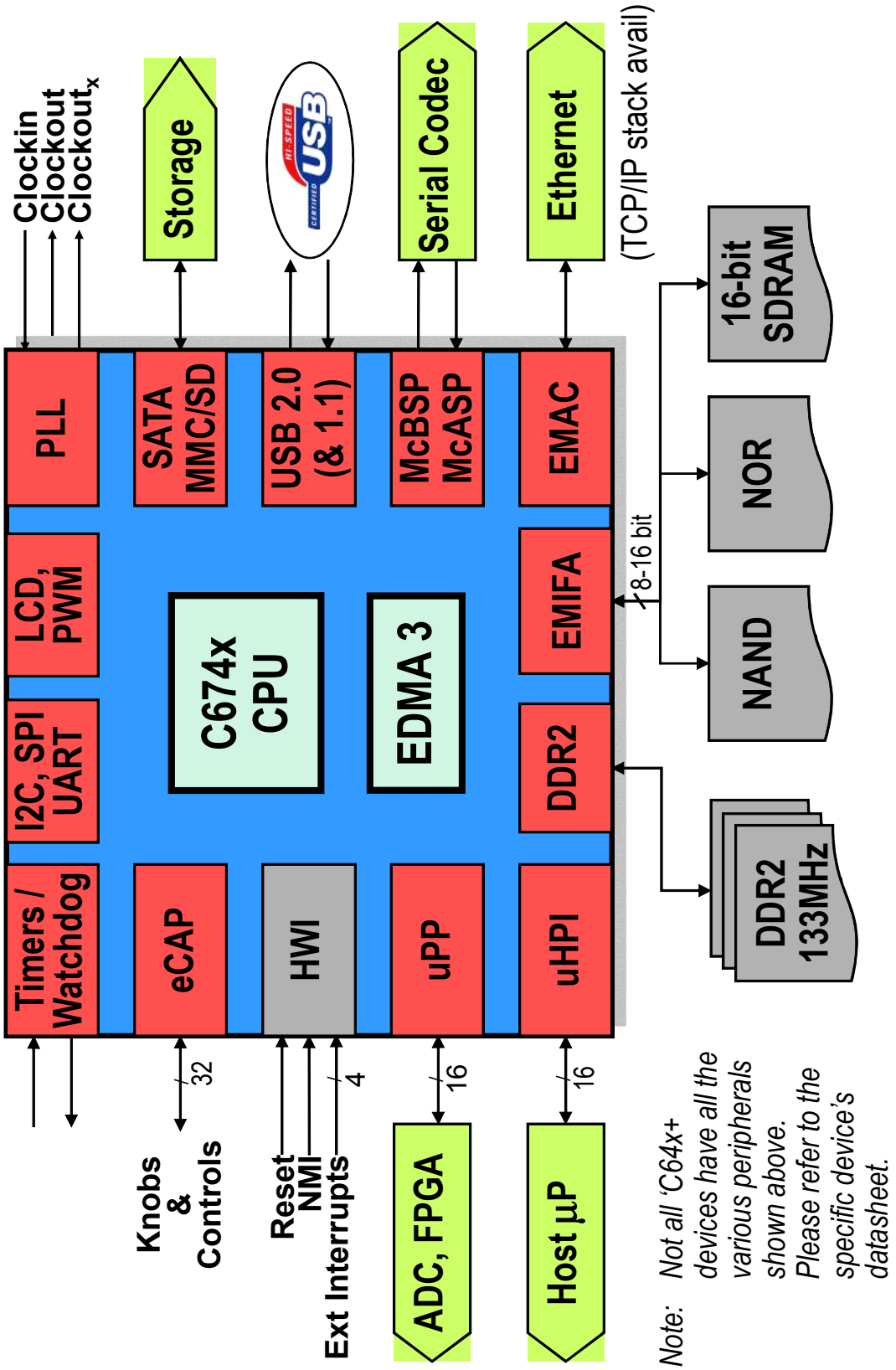
Peripherals (1.8/ 3.3V IOs)
- 10/100 Ethernet MAC
- EMIFA - SDRAM/NAND Flash
- EMIFB – DDR (mDDR/DDR2)
- Video Port I/F, SATA, uPP, LCDC

Power (1.0-1.2V Core, 1.8/3.3V IOs)
- Total Power < 440 mW @ 300Mhz, 1.2V, 25C
  For DSP at 70% loading, ARM at 50% loading; mDDR 50% active at 135MHz
- Standby Power
  < 9mW @ 1.2V/ 25C

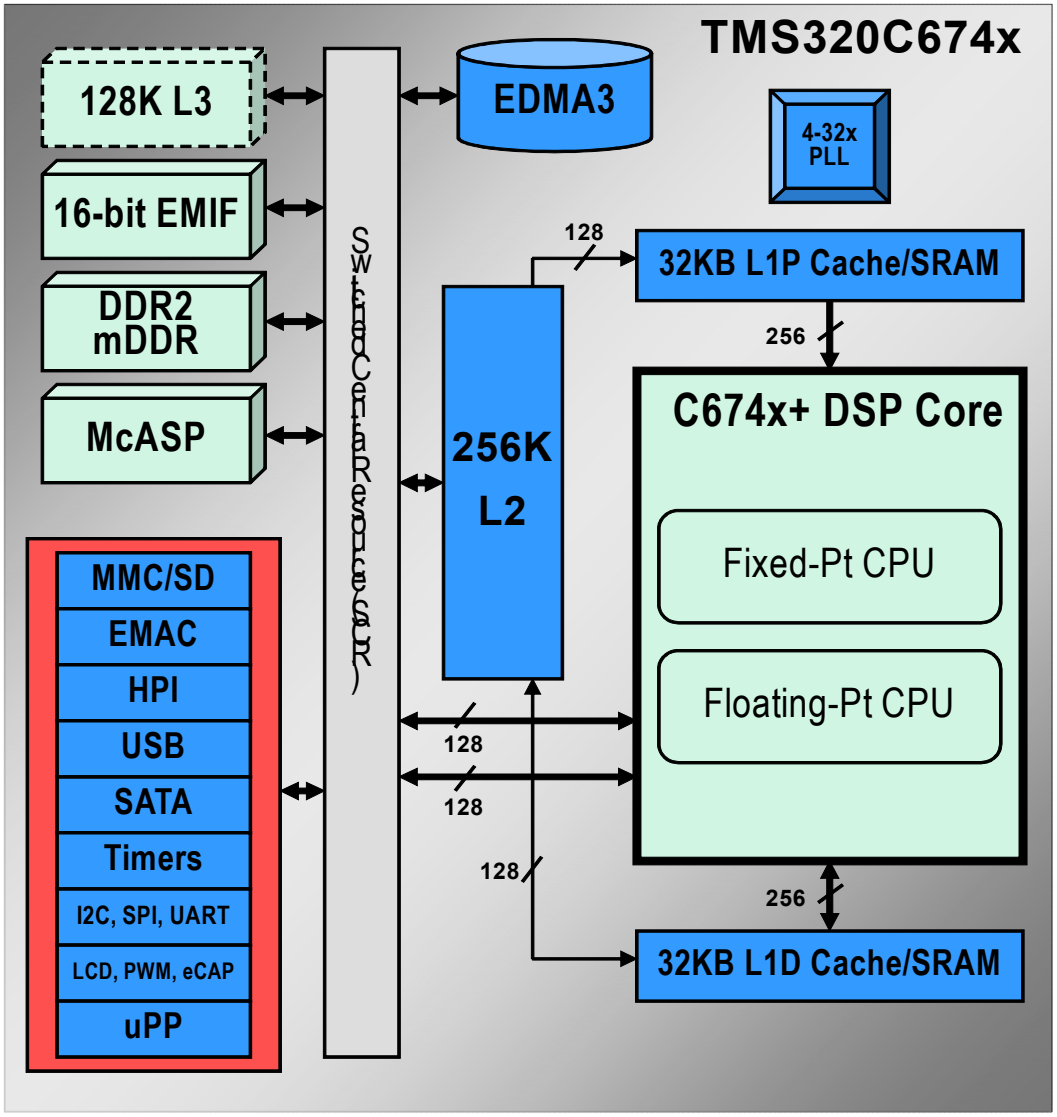
Package
- 13 x13mm nFBGA (0.65mm), 16x16mm BGA (0.8mm)
- Pin to pin compatible with C6748/6/2, AM1808/6

Applications
- Power Protection Systems, Test & Measurement, SDR, Bar Code Scanners, Portable Communications, Portable Medical, Portable Audio

Connectivity



High Level Architecture



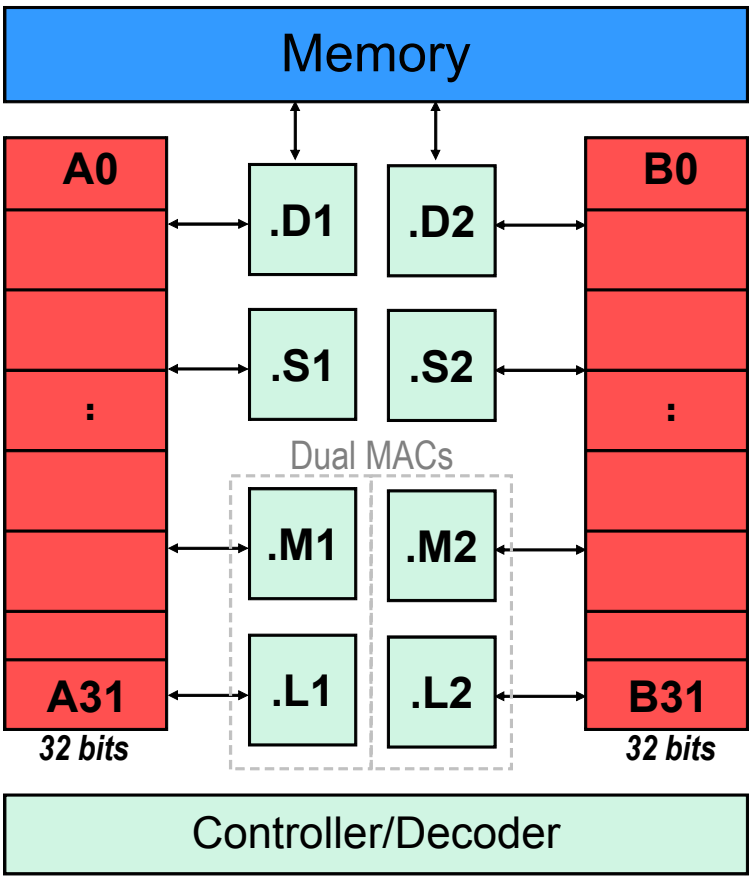
Performance & Memory

- Up to 300MHz
- 256K L2 (up to 64K cache)
- 32K L1P & L1D Cache/SRAM
- 32-bit DDR2-266
- 16-bit EMIF (NAND Flash)

Communications

- 64-Channel EDMA 3.0
- 10/100 EMAC
- USB 1.1 & 2.0
- SATA

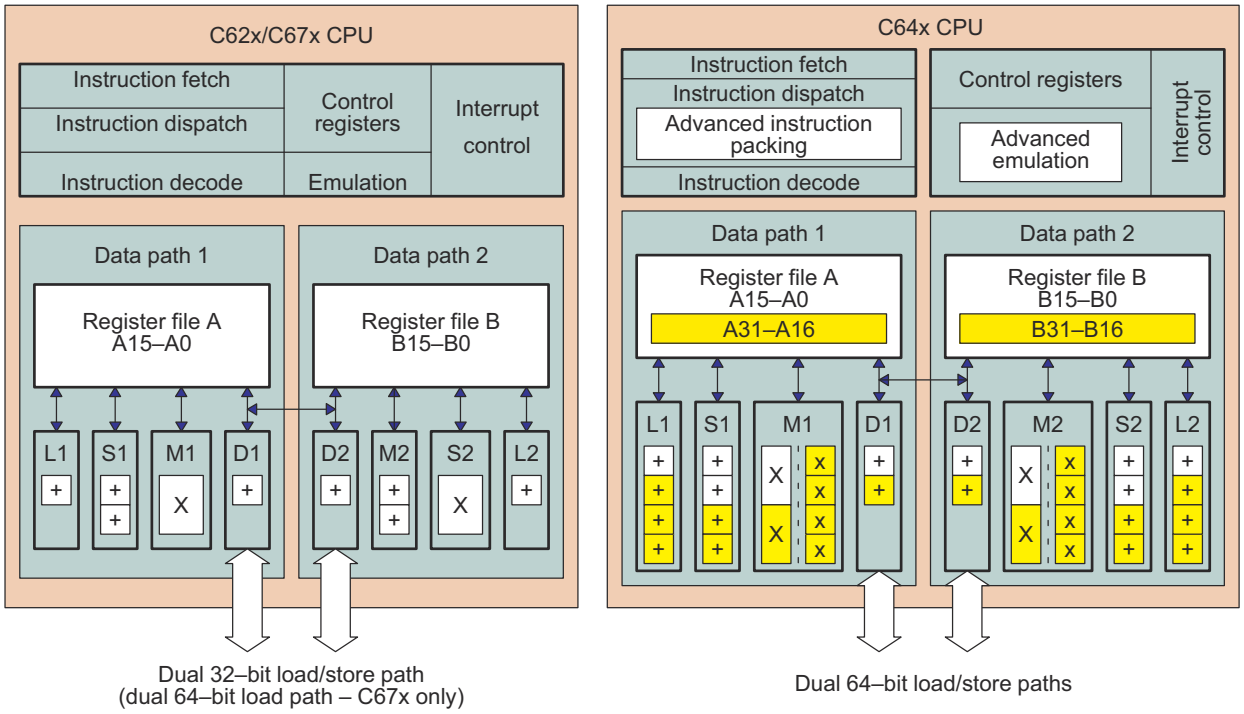
C6000 Core Architecture



- While the dual-MAC speeds math intensive algorithms, the flexibility of 8 independent functional units allows the compiler to quickly perform other types of processing
- Can dispatch up to 8 32-bit instructions every cycle
- All instructions are conditional – allowing efficient hardware pipelining
- The core contains 64 32-bit general purpose registers with few restrictions (aids compiler in generating more efficient code)
- Can perform up to EIGHT 16x16 multiplies/ACC per clk cycle

- MAU is 8 bits for program/data
- Compiler excels at natural C
- Data types: char = 8 bits, short = 16 bits, int = 32 bits, long = 40 bits, long long = 64 bits

Older C6713 Versus the Newer C674 & C64 (not C64+):

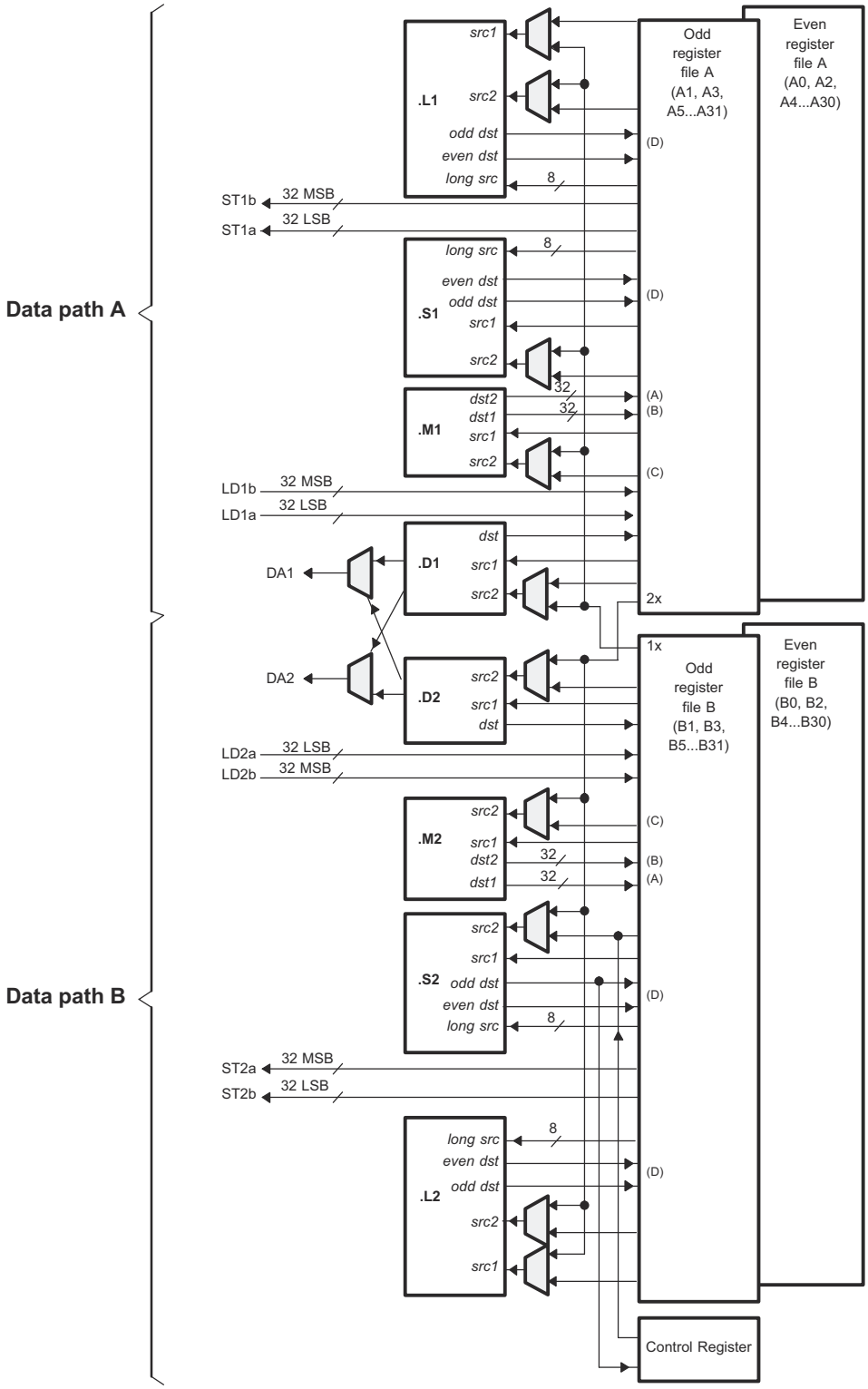


Functional Unit Operations

Functional Unit	Fixed–Point Operations	Floating–Point Operations
.L unit (.L1, .L2)	32/40-bit arithmetic and compare operations 32-bit logical operations Leftmost 1 or 0 counting for 32 bits Normalization count for 32 and 40 bits **Byte shifts** **Data packing/unpacking** **5-bit constant generation** **Dual 16-bit arithmetic operations** **Quad 8-bit arithmetic operations** **Dual 16-bit min/max operations** **Quad 8-bit min/max operations**	Arithmetic operations DP → SP, INT → DP, INT → SP conversion operations
.S unit (.S1, .S2)	32-bit arithmetic operations 32/40-bit shifts and 32-bit bit-field operations 32-bit logical operations Branches Constant generation Register transfers to/from control register file (.S2 only) **Byte shifts** **Data packing/unpacking** **Dual 16-bit compare operations** **Quad 8-bit compare operations** **Dual 16-bit shift operations** **Dual 16-bit saturated arithmetic operations** **Quad 8-bit saturated arithmetic operations**	Compare Reciprocal and reciprocal square–root operations Absolute value operations SP → DP conversion operations
.M unit (.M1, .M2)	16 x 16 multiply operations **16 x 32 multiply operations** **Quad 8 x 8 multiply operations** **Dual 16 x 16 multiply operations** **Dual 16 x 16 multiply with add/subtract operations** **Quad 8 x 8 multiply with add operation** **Bit expansion** **Bit interleaving/de-interleaving** **Variable shift operations** **Rotation** **Galois Field Multiply**	32 X 32–bit fixed–point multiply operations Floating–point multiply operations
.D unit (.D1, .D2)	32-bit add, subtract, linear and circular address calculation Loads and stores with 5-bit constant offset Loads and stores with 15-bit constant offset (.D2 only) **Load and store double words with 5-bit constant** **Load and store non-aligned words and double words** **5-bit constant generation** **32-bit logical operations**	Load doubleword with 5–bit constant offset

Note: Fixed-point operations are available on all three devices. Floating-point operations and 32 x 32-bit fixed-point multiply are available only on the 'C67x. Additonal 'C64x functions are shown in bold.

C6748 Data Paths



A. On .M unit, *dst2* is 32 MSB.
B. On .M unit, *dst1* is 32 LSB.
C. On C64x CPU .M unit, *src2* is 32 bits; on C64x+ CPU .M unit, *src2* is 64 bits.
D. On .L and .S units, *odd dst* connects to odd register files and *even dst* connects to even register files.

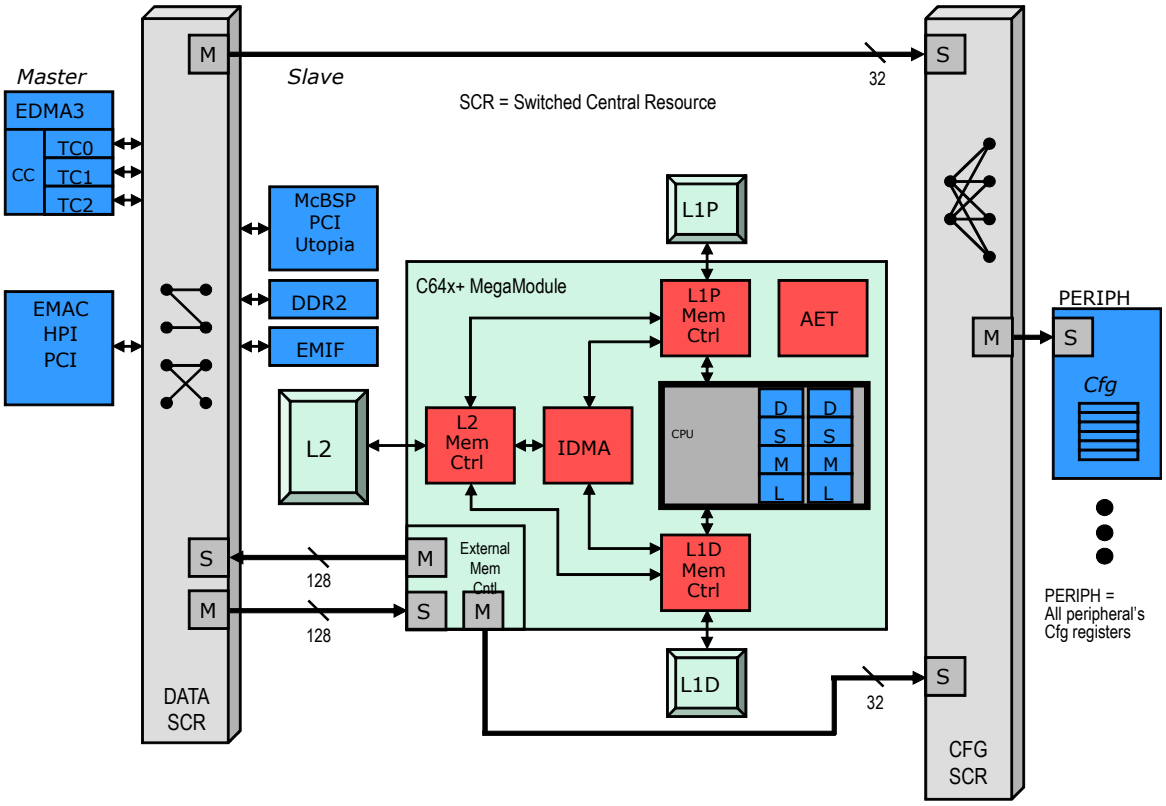
- Each C64x+ .M unit can perform one of the following each clock cycle:
  - one 32 x 32 bit multiply, one 16 x 32 bit multiply, two 16 x 16 bit multiplies, two 16 x 32 bit multiplies, two 16 x 16 bit multiplies with add/subtract capabilities, four 8 x 8 bit multiplies, four 8 x 8 bit multiplies with add operations, and four 16 x 16 multiplies with add/subtract capabilities (including a complex multiply)
  - There is also support for Galois field multiplication for 8-bit and 32-bit data
  - The complex multiply (CMPY) instruction takes for 16-bit inputs and produces a 32-bit real and a 32-bit imaginary output
  - There are also complex multiplies with rounding capability that produces one 32-bit packed output that contain 16-bit real and 16-bit imaginary values
  - The 32 x 32 bit multiply instructions provide the extended precision necessary for audio and other high-precision algorithms on a variety of signed and unsigned 32-bit data types
- The .L or (Arithmetic Logic Unit) now incorporates the ability to do parallel add/subtract operations on a pair of common inputs
  - Versions of this instruction exist to work on 32-bit data or on pairs of 16-bit data performing dual 16-bit add and sub-

tracts in parallel

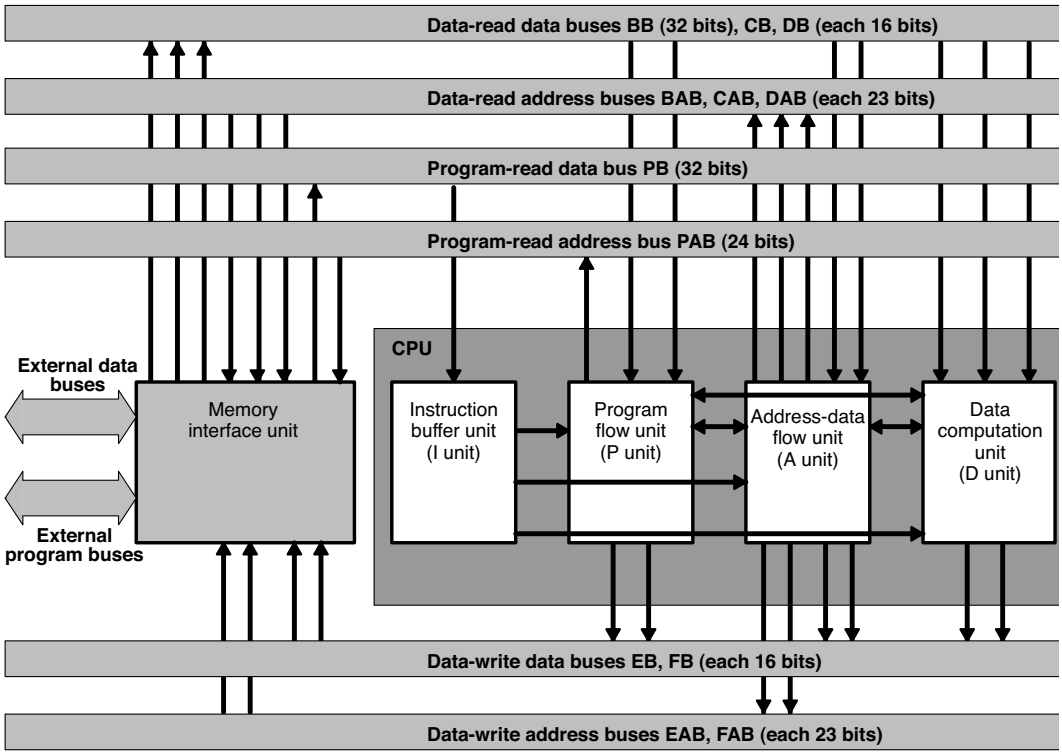
  - There are also saturated forms of these instructions

- The C64x+ core enhances the .S unit in several ways
  - In the C64x core, dual 16-bit MIN2 and MAX2 comparisons were only available on the .L units
  - On the C64x+ core they are also available on the .S unit which increases the performance of algorithms that do searching and sorting
  - Finally, to increase data packing and unpacking throughput, the .S unit allows sustained high performance for the quad 8-bit/16-bit and dual 16-bit instructions
  - Unpack instructions prepare 8-bit data for parallel 16-bit operations
  - Pack instructions return parallel results to output precision including saturation support

The Internal Bus Structure: SCR & Megamodule



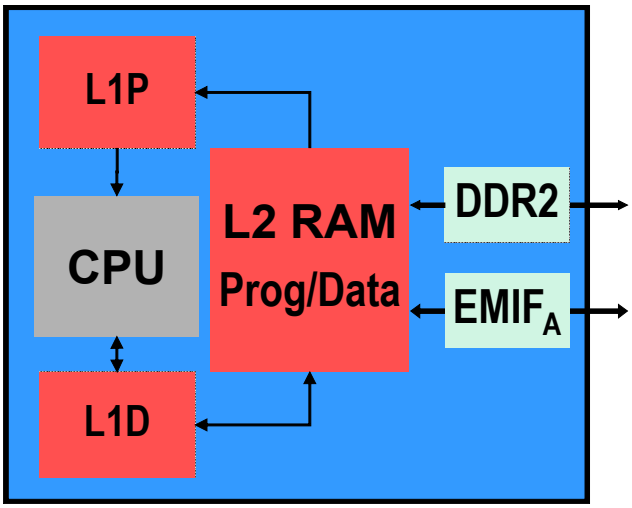
C55x Low Power DSP Quick Compare



- Although not immediately obvious from the above figures, a distinctive feature of the C6x and C55 over conventional microprocessors, is the *Harvard architecture*, that is separate buses for program and data
  - Instructions can be fetched *while* data is being accessed

C6748 Internal Memory

- **Level 1 Memory (32KB each)**
  - **Cache or RAM**
  - **L1P (prog), L1D (data)**
- **Level 2 Memory (256KB)**
  - **RAM (prog or data)**
  - **Up to 256KB can be cache**
- **Level 3 Memory (128KB)**
  - **Shared RAM**



Level 1 Memory

- **Single-cycle access**
- **L2 accessed on miss**
- **L1P: direct mapped**
- **L1D: 2-way set associative**

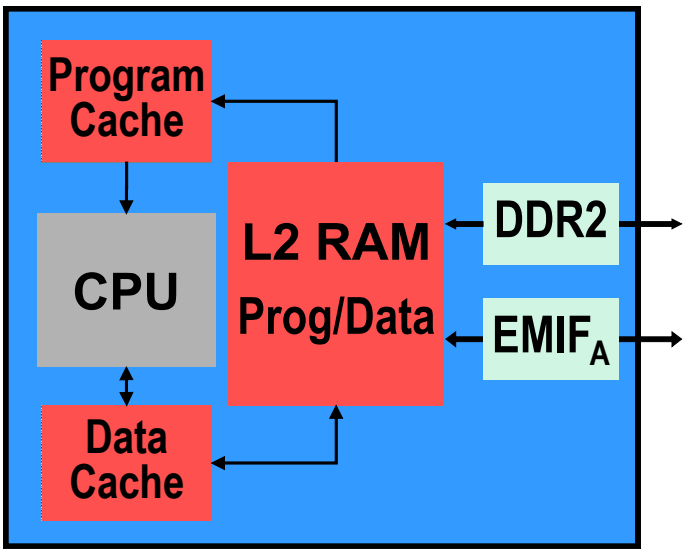
Level 2 Memory

- **Unified: Prog or Data**
- **4-way cache support**

L1/L2 Shared Features

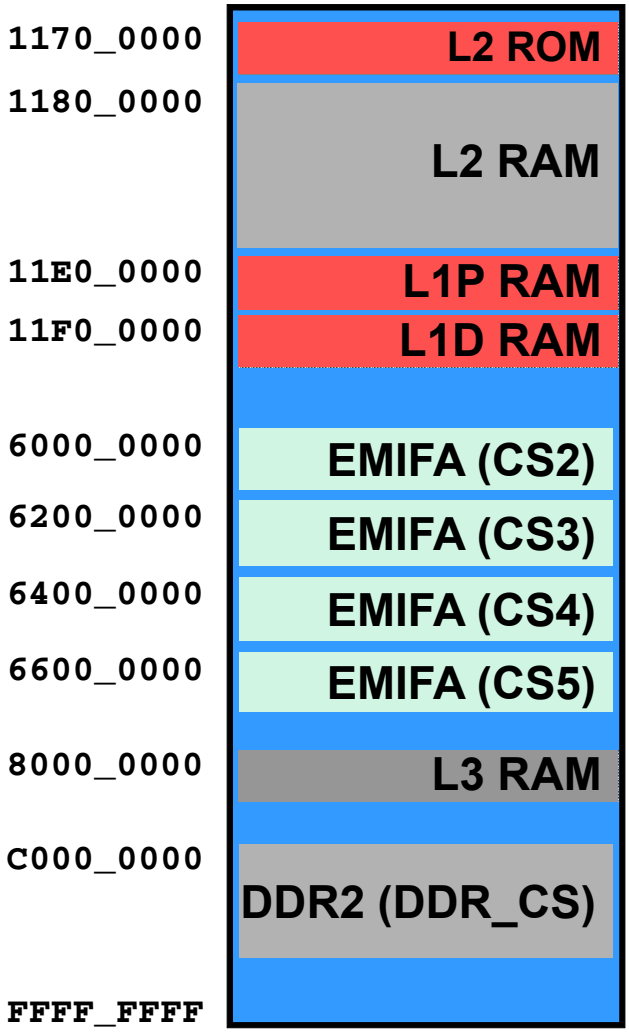
- **Configure each memory as cache or addressable RAM (or combination)**
- **Cache Freeze**

C6748 External Memory

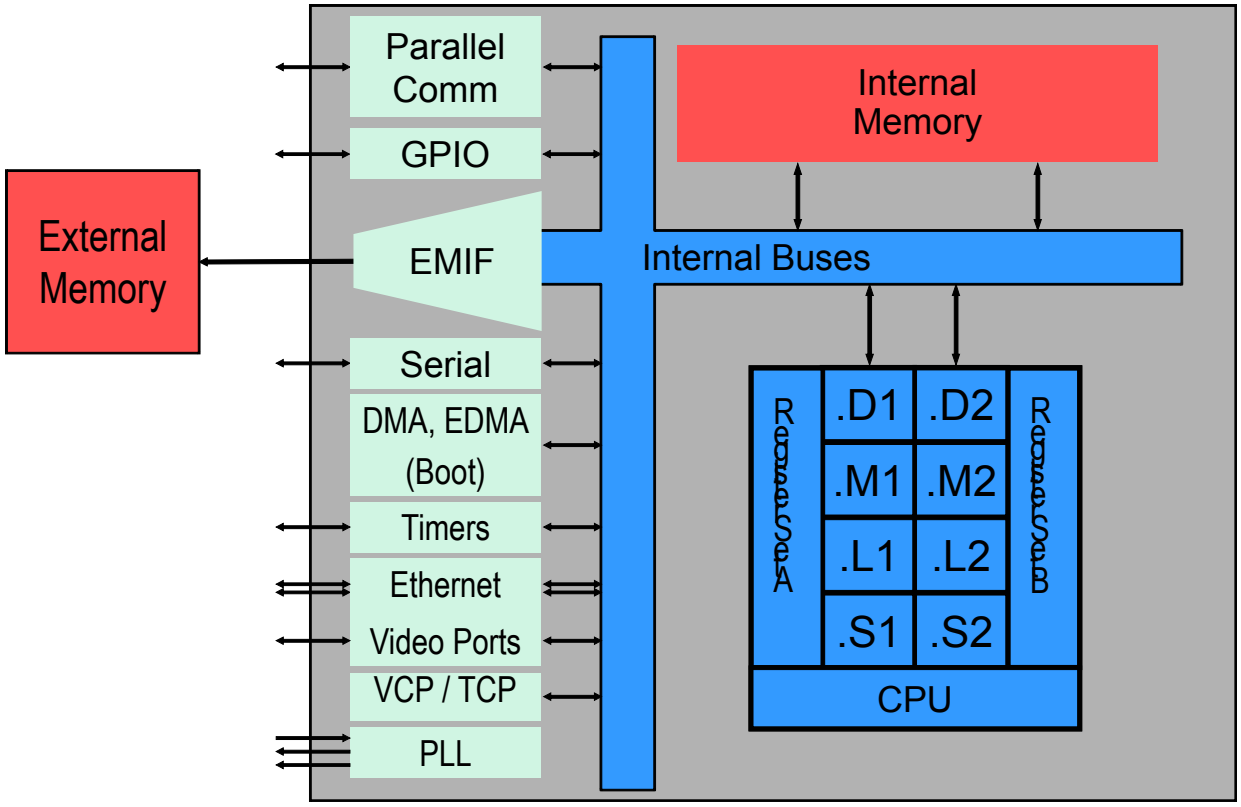


- EMIFA has four ranges (8MB each):
- Program or Data
- Named: ACE2, ACE3, ACE4, ACE5
- DDR2 is 512MB

Remaining memory is unused



'C6000 Peripherals Summary

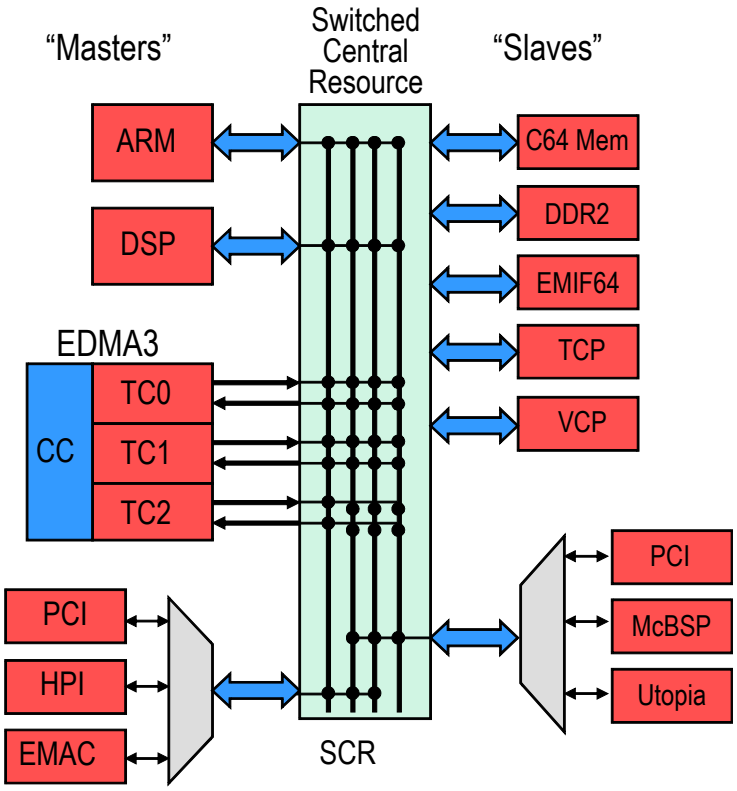


Host Port

- A dedicated bus for connection to a micro or external host
- Bootloading can occur via HPI

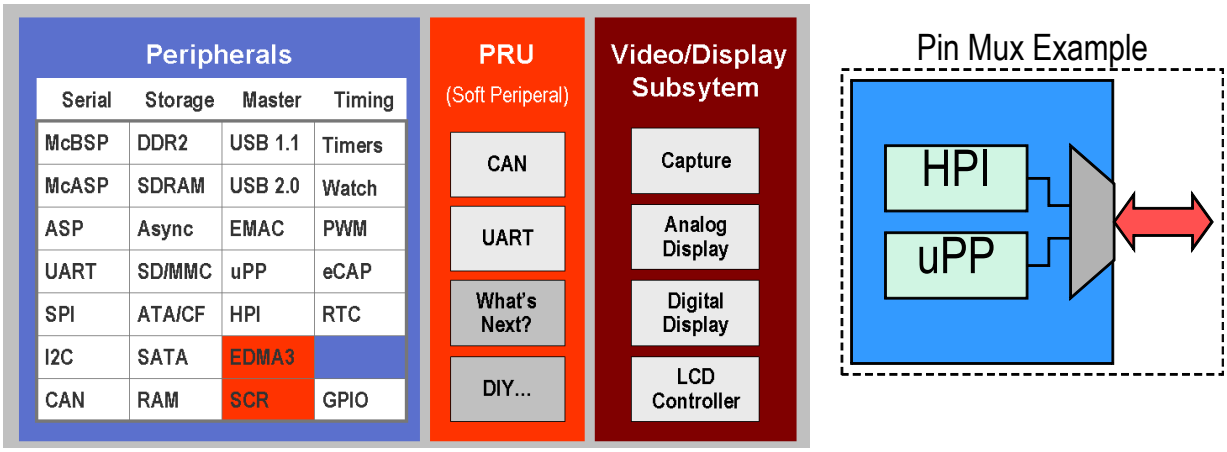
System Architecture – SCR/EDMA

Note: this picture is the "general idea". Every device has a different scheme for SCRs and peripheral muxing. In other words "check your data sheet".



- SCR – Switched Central Resource
- Masters initiate accesses to/fromslaves via the SCR
- Most Masters (requestors) and Slaves(resources) have their own port to the SCR
- Lower bandwidth masters (HPI,PCI66, etc) share a port
- There is a default priority (0 to 7) toSCR resources that can be modified.

What is Pin Multiplexing?



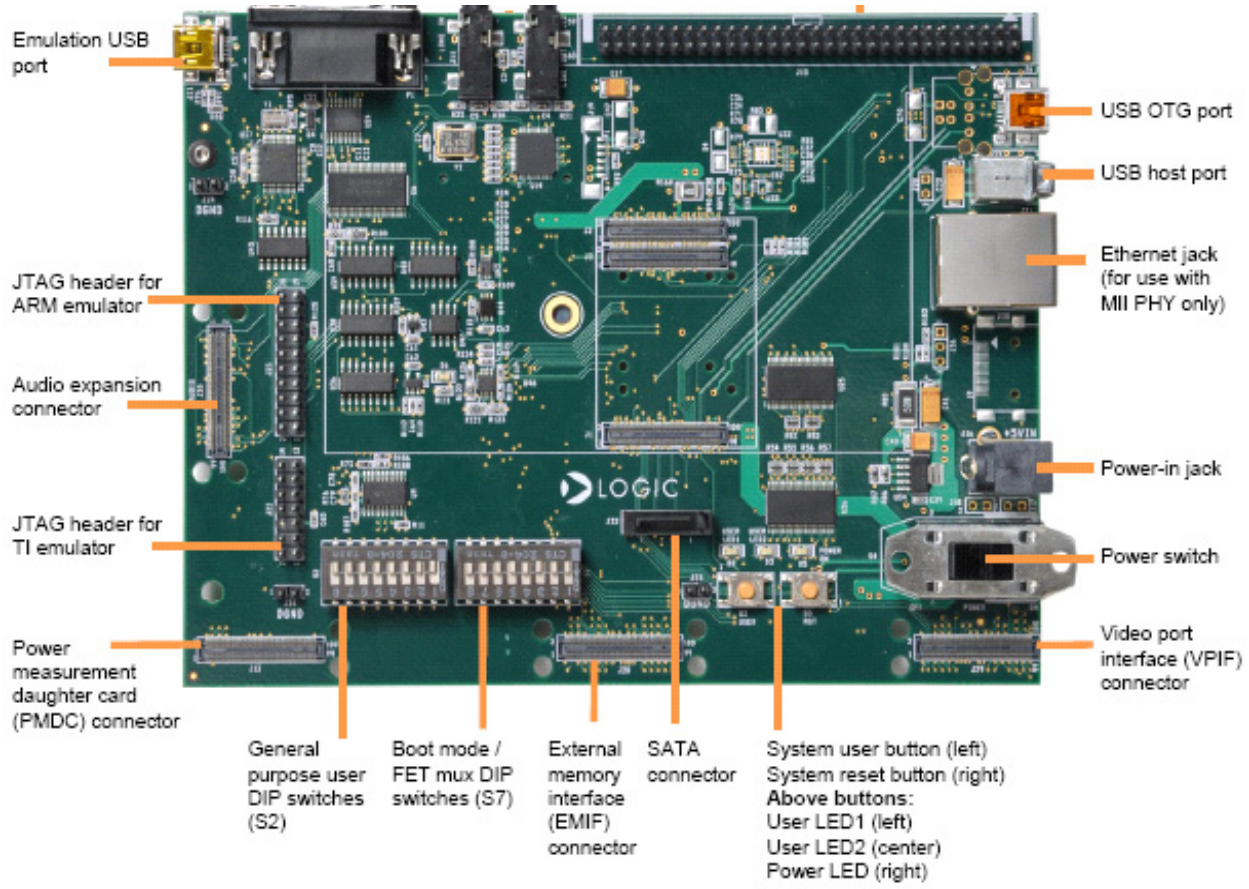
- How many pins is on your device?
- How many pins would all your peripheral require?
- Pin Multiplexing is the answer – only so many peripherals can be used at the same time … in other words, to reduce costs, peripherals must share available pins
- Which ones can you use simultaneously?
  - Designers examine app use cases when deciding best muxing layout
  - Read datasheet for final authority on how pins are muxed
  - Graphical utility can assist with figuring out pin-muxing…

Laboratory Hardware Targets

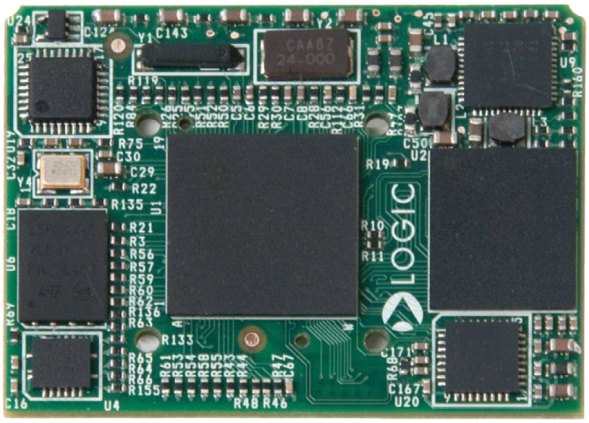
- There are many C6x development systems or hardware targets available from third parties
- TI itself supplies:

  - The OMAL-L138 eXperimenters Board $495
  - The C6713-225 based DSK $395, with bundled DSK specific software, and USB host interface; 2M x 32 on board SDRAM, 512K bytes on board flash
  - The C6416-600 based DSK $395, with bundled DSK specific software, and USB host interface
  - The VC5505-100 based eZDSP USB Stick $49, with bundled CCS4 for XDS100 class JTAG emulators
- Full versions of the software tools are running in the lab
  - Full Code Composer Studio Platinum version 4.2
  - Full Code Composer Studio Platinum version 5.1

The OMAP-L138 (C6748) eXperimenters Board

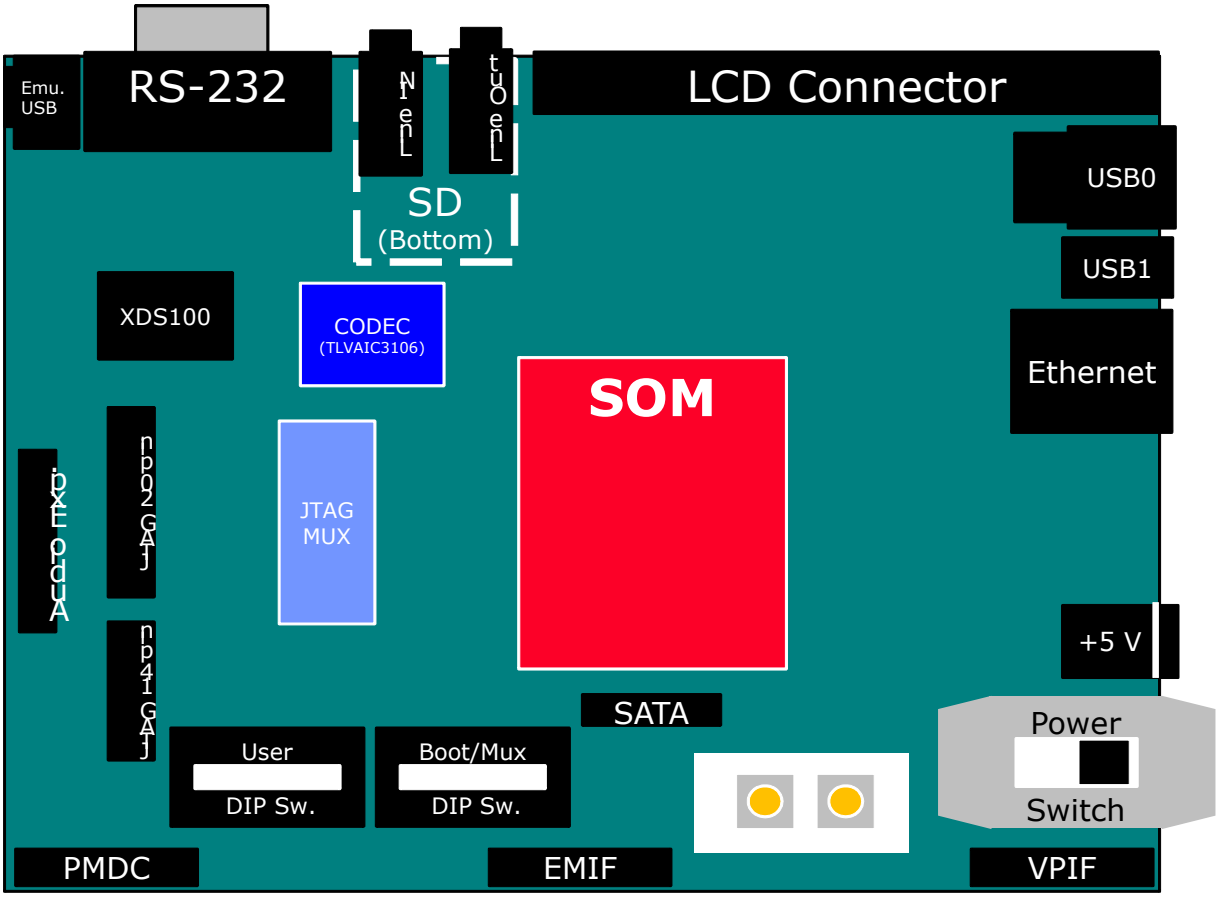


The System on Module (SOM) Board

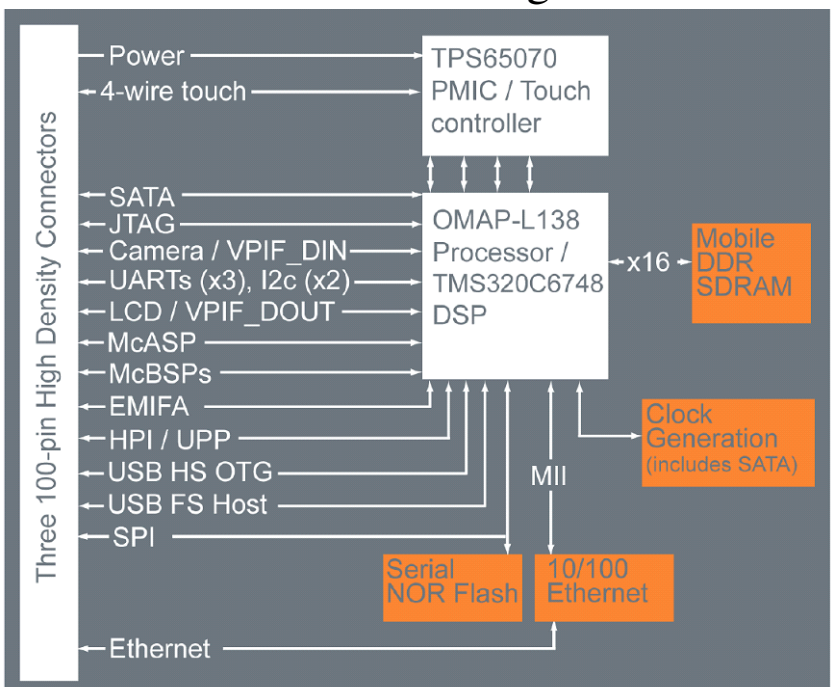


- Product-ready System on Module with a TI OMAP-L138 processor or TMS320C6748 DSP running at 375 MHz

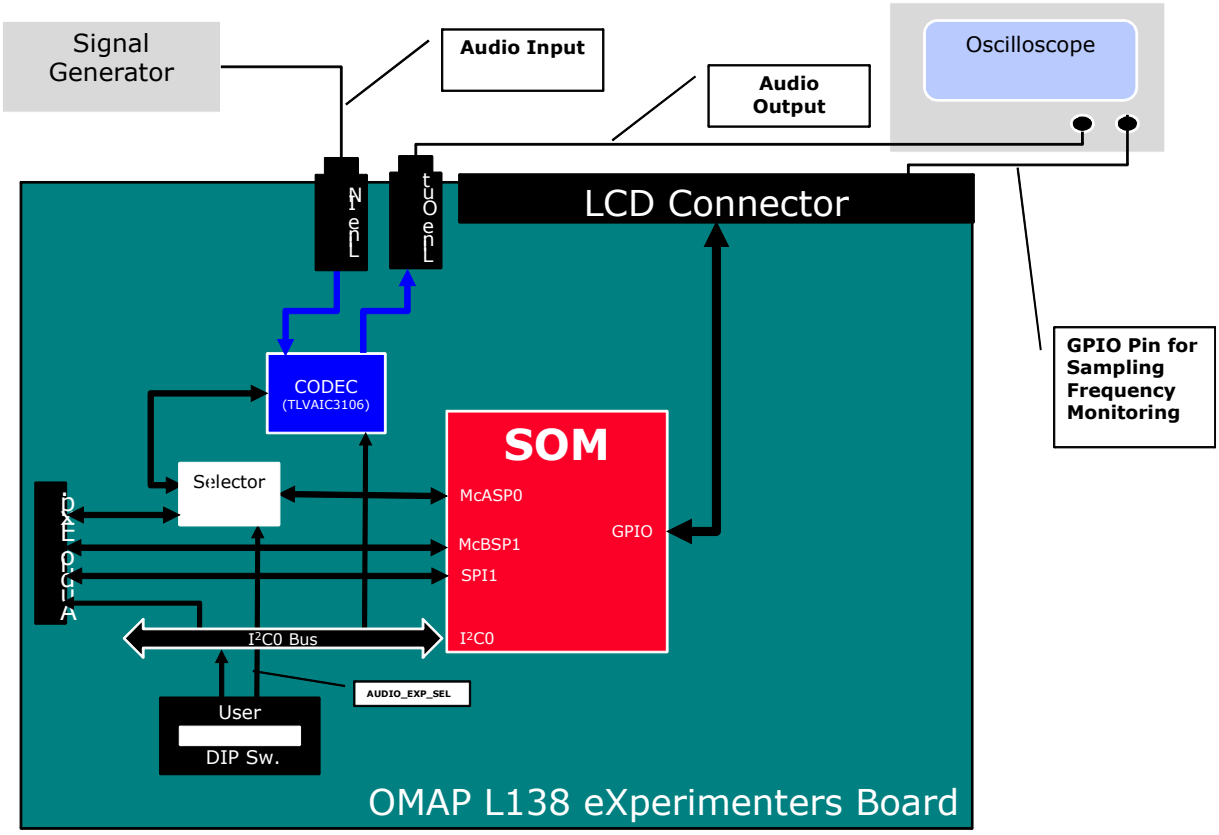
- The Card (Top View)



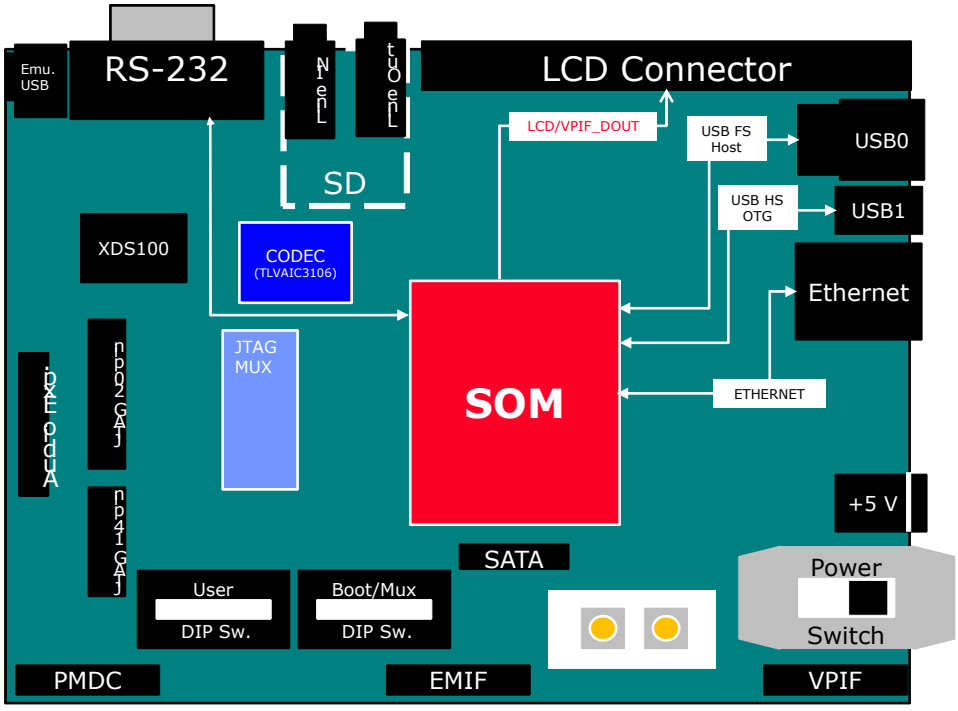
- OMAP-L138 SOM-M1 Block Diagram



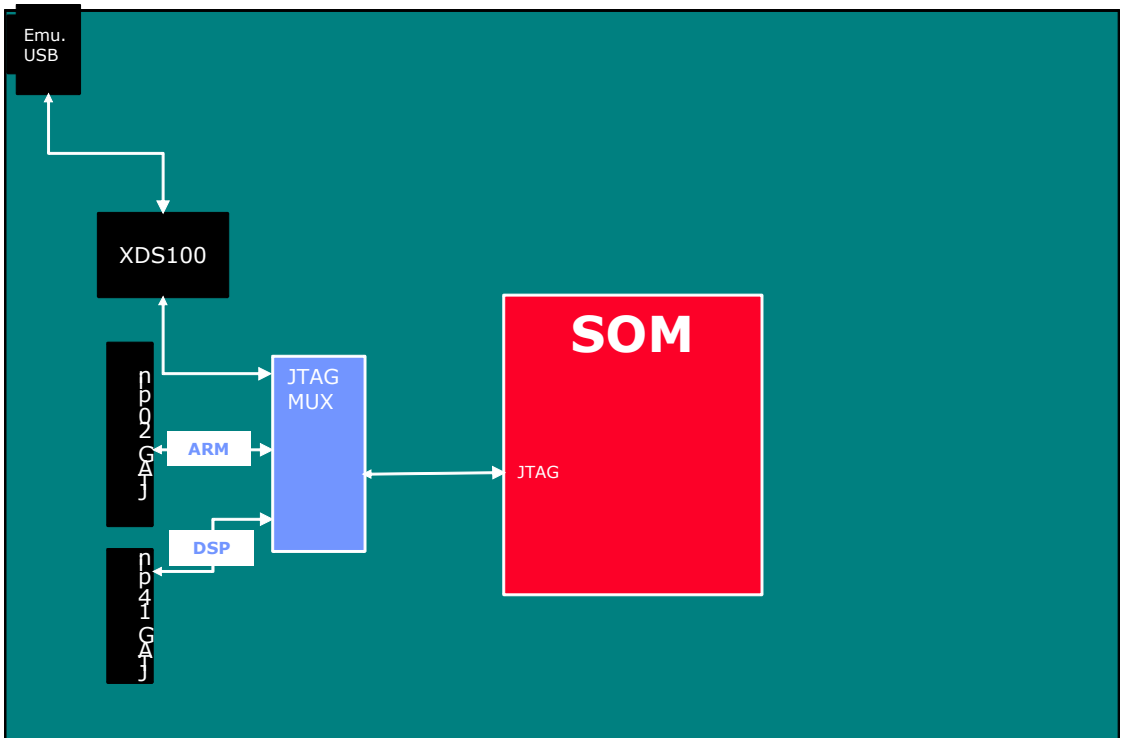
- Audio Interface



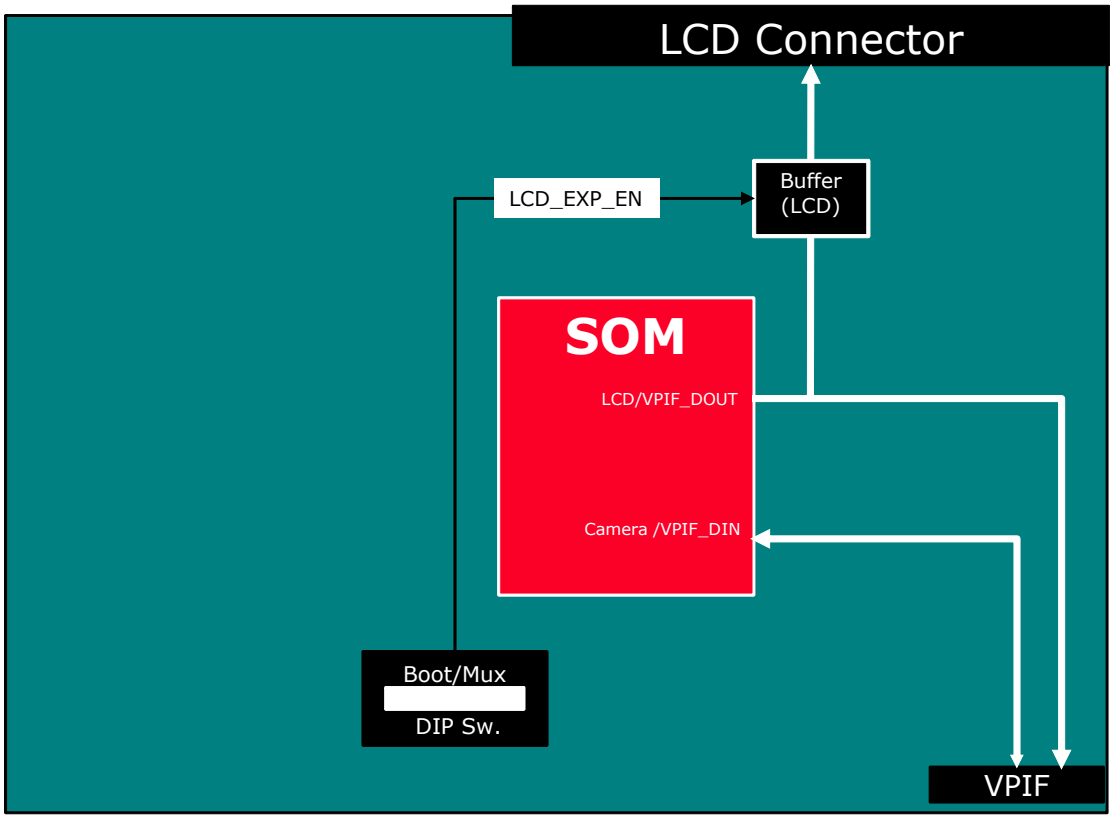
- Communication Interfaces



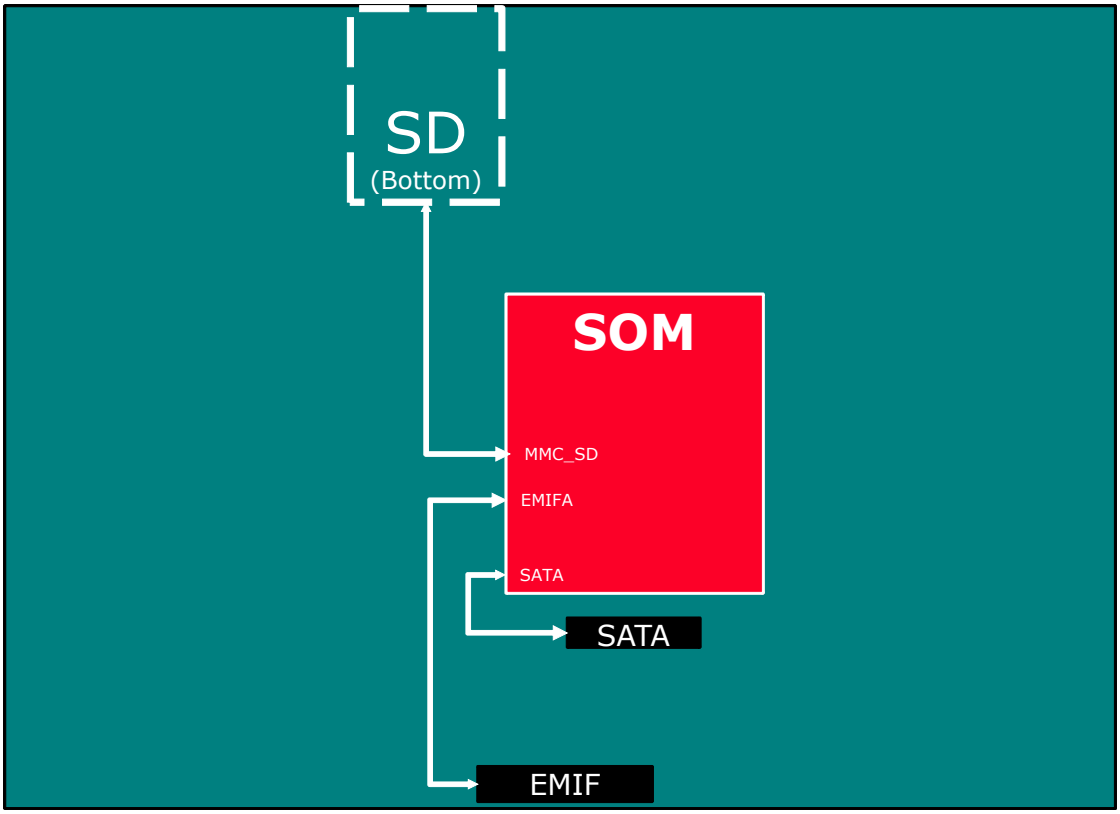
- Emulation Interfaces



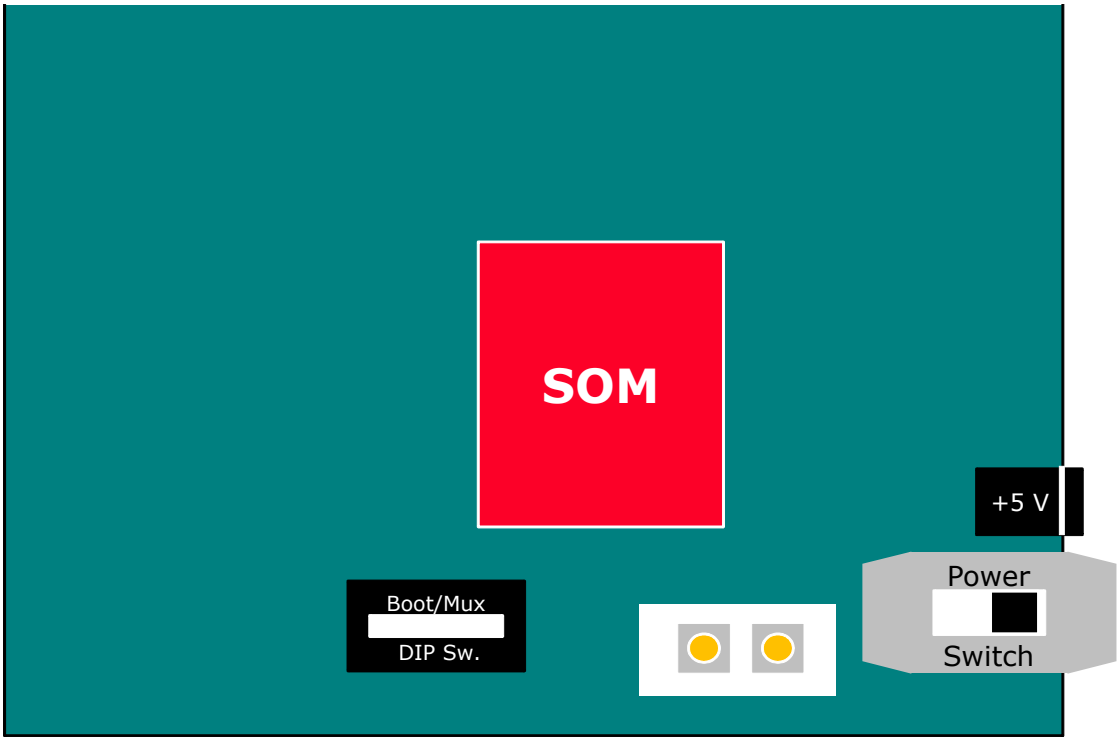
- Video and LCD Interfaces



- Memory Interfaces



- Boot and Power Management



The C6748 Memory Map

Table 2-4. C6748 Top Level Memory Map

Start Address	End Address	Size	DSP Mem Map	EDMA Mem Map	PRUSS Mem Map	Master Peripheral Mem Map	LCDC Mem Map
0x0000 0000	0x0000 0FFF	4K			PRUSS Local Address Space		
0x0000 1000	0x006F FFFF						
0x0070 0000	0x007F FFFF	1024K	DSP L2 ROM (1)				
0x0080 0000	0x0083 FFFF	256K	DSP L2 RAM				
0x0084 0000	0x00DF FFFF						
0x00E0 0000	0x00E0 7FFF	32K	DSP L1P RAM				
0x00E0 8000	0x00EF FFFF						
0x00F0 0000	0x00F0 7FFF	32K	DSP L1D RAM				
0x00F0 8000	0x017F FFFF						
0x0180 0000	0x0180 FFFF	64K	DSP Interrupt Controller				
0x0181 0000	0x0181 0FFF	4K	DSP Powerdown Controller				
0x0181 1000	0x0181 1FFF	4K	DSP Security ID				
0x0181 2000	0x0181 2FFF	4K	DSP Revision ID				
0x0181 3000	0x0181 FFFF	52K					
0x0182 0000	0x0182 FFFF	64K	DSP EMC				
0x0183 0000	0x0183 FFFF	64K	DSP Internal Reserved				
0x0184 0000	0x0184 FFFF	64K	DSP Memory System				
0x0185 0000	0x01BF FFFF						
0x01C0 0000	0x01C0 7FFF	32K	EDMA3 CC				
0x01C0 8000	0x01C0 83FF	1K	EDMA3 TC0				
0x01C0 8400	0x01C0 87FF	1K	EDMA3 TC1				
0x01C0 8800	0x01C0 FFFF						
0x01C1 0000	0x01C1 0FFF	4K	PSC 0				
0x01C1 1000	0x01C1 1FFF	4K	PLL Controller 0				
0x01C1 2000	0x01C1 3FFF						
0x01C1 4000	0x01C1 4FFF	4K	SYSCFG0				
0x01C1 5000	0x01C1 FFFF						
0x01C2 0000	0x01C2 0FFF	4K	Timer0				
0x01C2 1000	0x01C2 1FFF	4K	Timer1				
0x01C2 2000	0x01C2 2FFF	4K	I2C 0				
0x01C2 3000	0x01C2 3FFF	4K	RTC				
0x01C2 4000	0x01C3 FFFF						
0x01C4 0000	0x01C4 0FFF	4K	MMC/SD 0				
0x01C4 1000	0x01C4 1FFF	4K	SPI 0				
0x01C4 2000	0x01C4 2FFF	4K	UART 0				
0x01C4 3000	0x01CF FFFF						
0x01D0 0000	0x01D0 0FFF	4K	McASP 0 Control				
0x01D0 1000	0x01D0 1FFF	4K	McASP 0 AFIFO Ctrl				
0x01D0 2000	0x01D0 2FFF	4K	McASP 0 Data				
0x01D0 3000	0x01D0 BFFF						

(1) The DSP L2 ROM is used for boot purposes and cannot be programmed with application code

Table 2-4. C6748 Top Level Memory Map (continued)

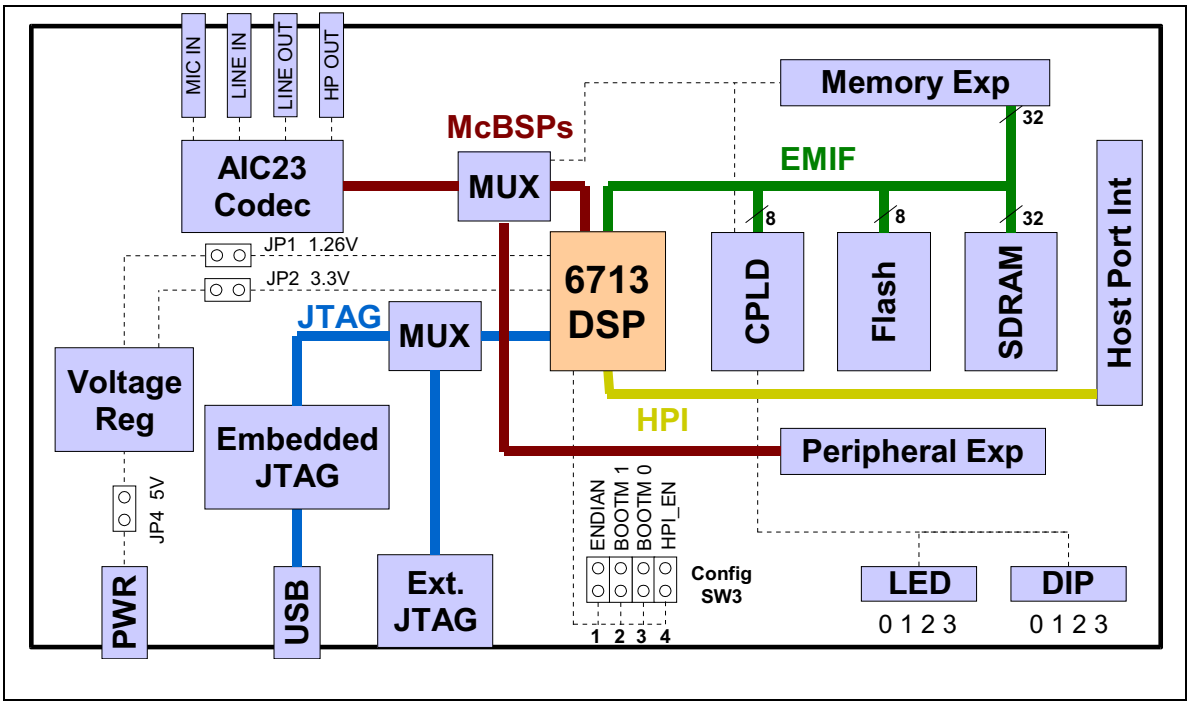
Start Address	End Address	Size	DSP Mem Map	EDMA Mem Map	PRUSS Mem Map	Master Peripheral Mem Map	LCDC Mem Map
0x01D0 C000	0x01D0 CFFF	4K	UART 1				
0x01D0 D000	0x01D0 DFFF	4K	UART 2				
0x01D0 E000	0x01D0 FFFF						
0x01D1 0000	0x01D1 07FF	2K	McBSP0				
0x01D1 0800	0x01D1 0FFF	2K	McBSP0 FIFO Ctrl				
0x01D1 1000	0x01D1 17FF	2K	McBSP1				
0x01D1 1800	0x01D1 1FFF	2K	McBSP1 FIFO Ctrl				
0x01D1 2000	0x01DF FFFF						
0x01E0 0000	0x01E0 FFFF	64K	USB0				
0x01E1 0000	0x01E1 0FFF	4K	UHPI				
0x01E1 1000	0x01E1 2FFF						
0x01E1 3000	0x01E1 3FFF	4K	LCD Controller				
0x01E1 4000	0x01E1 4FFF	4K	Memory Protection Unit 1 (MPU 1)				
0x01E1 5000	0x01E1 5FFF	4K	Memory Protection Unit 2 (MPU 2)				
0x01E1 6000	0x01E1 6FFF	4K	UPP				
0x01E1 7000	0x01E1 7FFF	4K	VPIF				
0x01E1 8000	0x01E1 9FFF	8K	SATA				
0x01E1 A000	0x01E1 AFFF	4K	PLL Controller 1				
0x01E1 B000	0x01E1 BFFF	4K	MMCSD1				
0x01E1 C000	0x01E1 FFFF						
0x01E2 0000	0x01E2 1FFF	8K	EMAC Control Module RAM				
0x01E2 2000	0x01E2 2FFF	4K	EMAC Control Module Registers				
0x01E2 3000	0x01E2 3FFF	4K	EMAC Control Registers				
0x01E2 4000	0x01E2 4FFF	4K	EMAC MDIO port				
0x01E2 5000	0x01E2 5FFF	4K	USB1				
0x01E2 6000	0x01E2 6FFF	4K	GPIO				
0x01E2 7000	0x01E2 7FFF	4K	PSC 1				
0x01E2 8000	0x01E2 8FFF	4K	I2C 1				
0x01E2 9000	0x01E2 BFFF						
0x01E2 C000	0x01E2 CFFF	4K	SYSCFG1				
0x01E2 D000	0x01E2 FFFF						
0x01E3 0000	0x01E3 7FFF	32K	EDMA3 CC1				
0x01E3 8000	0x01E3 83FF	1K	EDMA3 TC2				
0x01E3 8400	0x01EF FFFF						
0x01F0 0000	0x01F0 0FFF	4K	eHRPWM 0				
0x01F0 1000	0x01F0 1FFF	4K	HRPWM 0				
0x01F0 2000	0x01F0 2FFF	4K	eHRPWM 1				
0x01F0 3000	0x01F0 3FFF	4K	HRPWM 1				
0x01F0 4000	0x01F0 5FFF						
0x01F0 6000	0x01F0 6FFF	4K	ECAP 0				
0x01F0 7000	0x01F0 7FFF	4K	ECAP 1				
0x01F0 8000	0x01F0 8FFF	4K	ECAP 2				
0x01F0 9000	0x01F0 BFFF						
0x01F0 C000	0x01F0 CFFF	4K	Timer2				
0x01F0 D000	0x01F0 DFFF	4K	Timer3				
0x01F0 E000	0x01F0 EFFF	4K	SPI1				

Table 2-4. C6748 Top Level Memory Map (continued)

Start Address	End Address	Size	DSP Mem Map	EDMA Mem Map	PRUSS Mem Map	Master Peripheral Mem Map	LCDC Mem Map
0x01F0 F000	0x01F0 FFFF						
0x01F1 0000	0x01F1 0FFF	4K	McBSP0 FIFO Data				
0x01F1 1000	0x01F1 1FFF	4K	McBSP1 FIFO Data				
0x01F1 2000	0x116F FFFF						
0x1170 0000	0x117F FFFF	1024K	DSP L2 ROM (2)				
0x1180 0000	0x1183 FFFF	256K	DSP L2 RAM				
0x1184 0000	0x11DF FFFF						
0x11E0 0000	0x11E0 7FFF	32K	DSP L1P RAM				
0x11E0 8000	0x11EF FFFF						
0x11F0 0000	0x11F0 7FFF	32K	DSP L1D RAM				
0x11F0 8000	0x3FFF FFFF						
0x4000 0000	0x5FFF FFFF	512M	EMIFA SDRAM data (CS0)				
0x6000 0000	0x61FF FFFF	32M	EMIFA async data (CS2)				
0x6200 0000	0x63FF FFFF	32M	EMIFA async data (CS3)				
0x6400 0000	0x65FF FFFF	32M	EMIFA async data (CS4)				
0x6600 0000	0x67FF FFFF	32M	EMIFA async data (CS5)				
0x6800 0000	0x6800 7FFF	32K	EMIFA Control Regs				
0x6800 8000	0x7FFF FFFF						
0x8000 0000	0x8001 FFFF	128K	On-chip RAM				
0x8002 0000	0xAFFF FFFF						
0xB000 0000	0xB000 7FFF	32K	DDR2 Control Regs				
0xB000 8000	0xBFFF FFFF						
0xC000 0000	0xDFFF FFFF	512M	DDR2 Data				
0xE000 0000	0xFFFF FFFF						

(2) The DSP L2 ROM is used for boot purposes and cannot be programmed with application code

The C6713 DSK



- The C6713 DSK was introduced summer 2003
- The 6713 is an enhanced version of the 6711, including
- McBSP1 is used as a bi-directional data channel
- McBSP0 is used as a unidirectional codec control channel in SPI format (operative normally only when first configuring the codec)
- The AIC codec uses a 12 MHz clock (popular USB clock rate)
- Through division common audio sample rate frequencies available are: 48 KHz, 44.1 KHz, and 8 KHz

C6713 DSK Board Layout

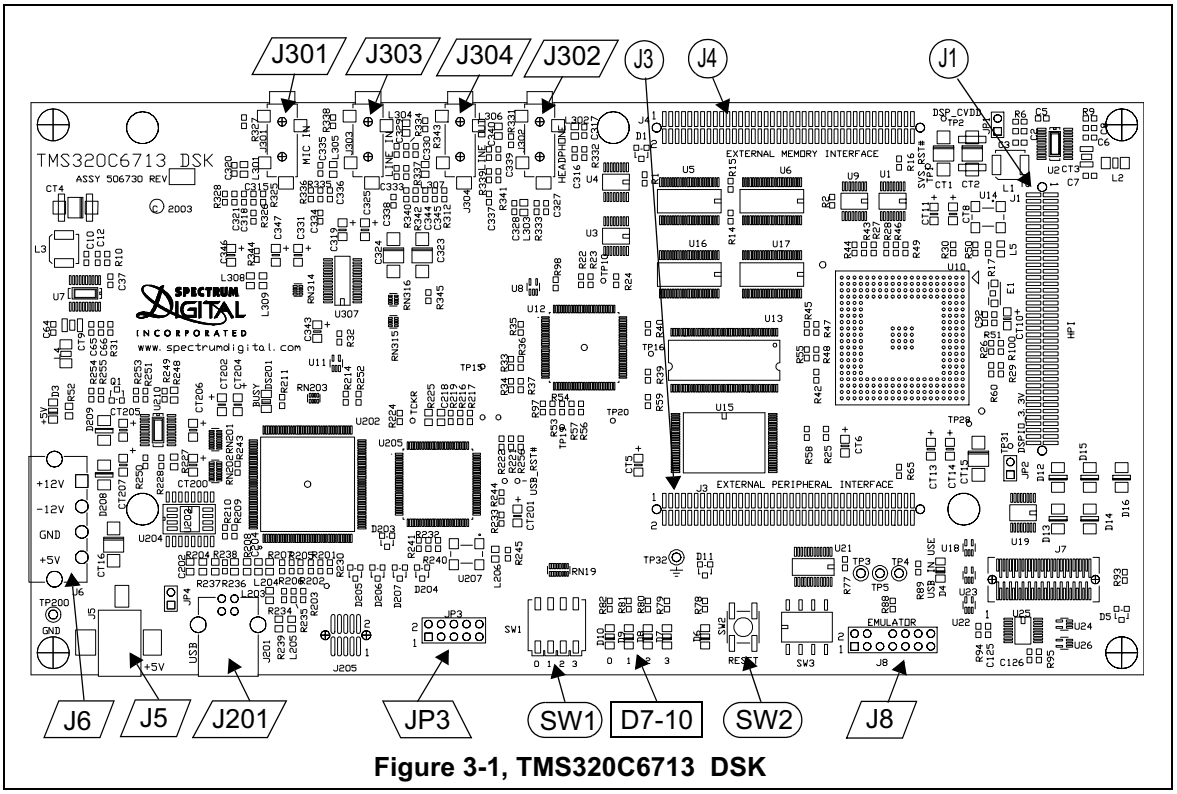
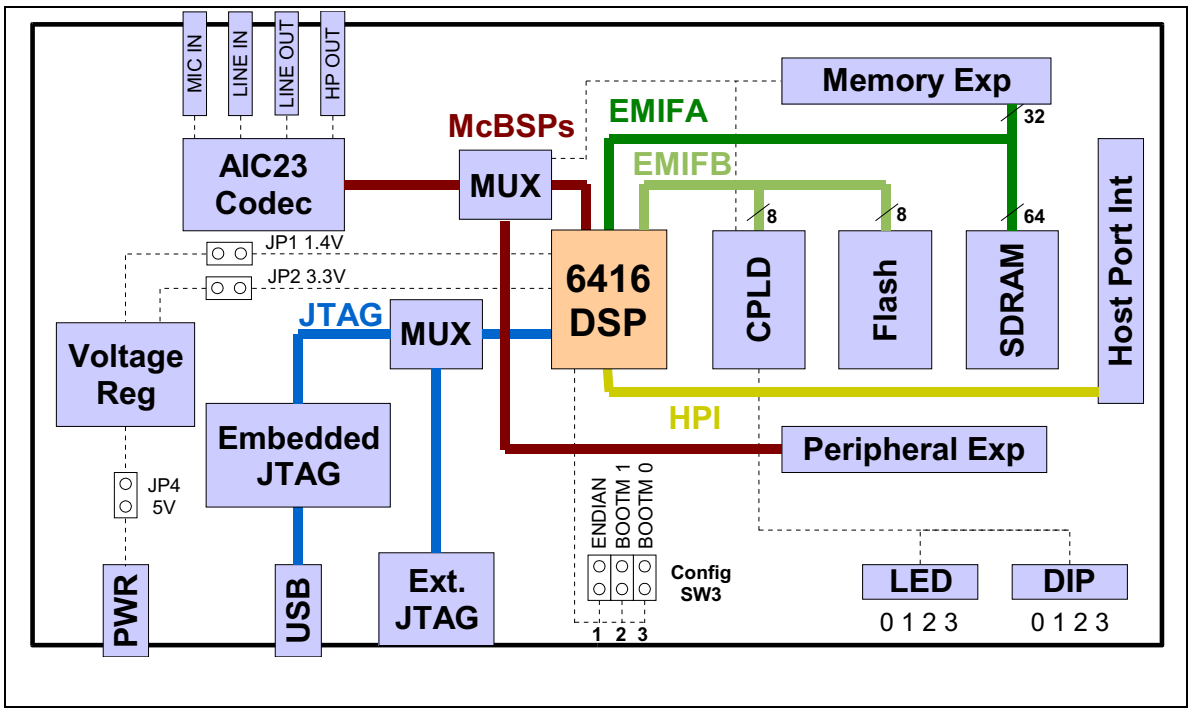


Figure 3-1, TMS320C6713 DSK

Connector	# Pins	Function
J4	80	Memory
J3	80	Peripheral
J1	80	HPI
J301	3	Microphone
J303	3	Line In
J304	3	Line Out
J303	3	Headphone
J5	2	+5 Volt
J6 *	4	Optional Power Connector
J8	14	External JTAG
J201	5	USB Port
JP3	10	CPLD Programming
SW3	8	DSP Configuration Jumper

The C6416 DSK Block Diagram



- The 6416 DSK is very similar to the 6713 DSK, except the 6416 is a high performance fixed point device having:
  - 600 MHz CPU clock (1.67 ns cycle time yielding 4800 MIPS)
  - Only fixed-point hardware
  - Viterbi decoder co-processor for comm applications
  - Turbo decoder co-processor for comm applications (3GPP)
- The external memory and codec configurations are identical
-

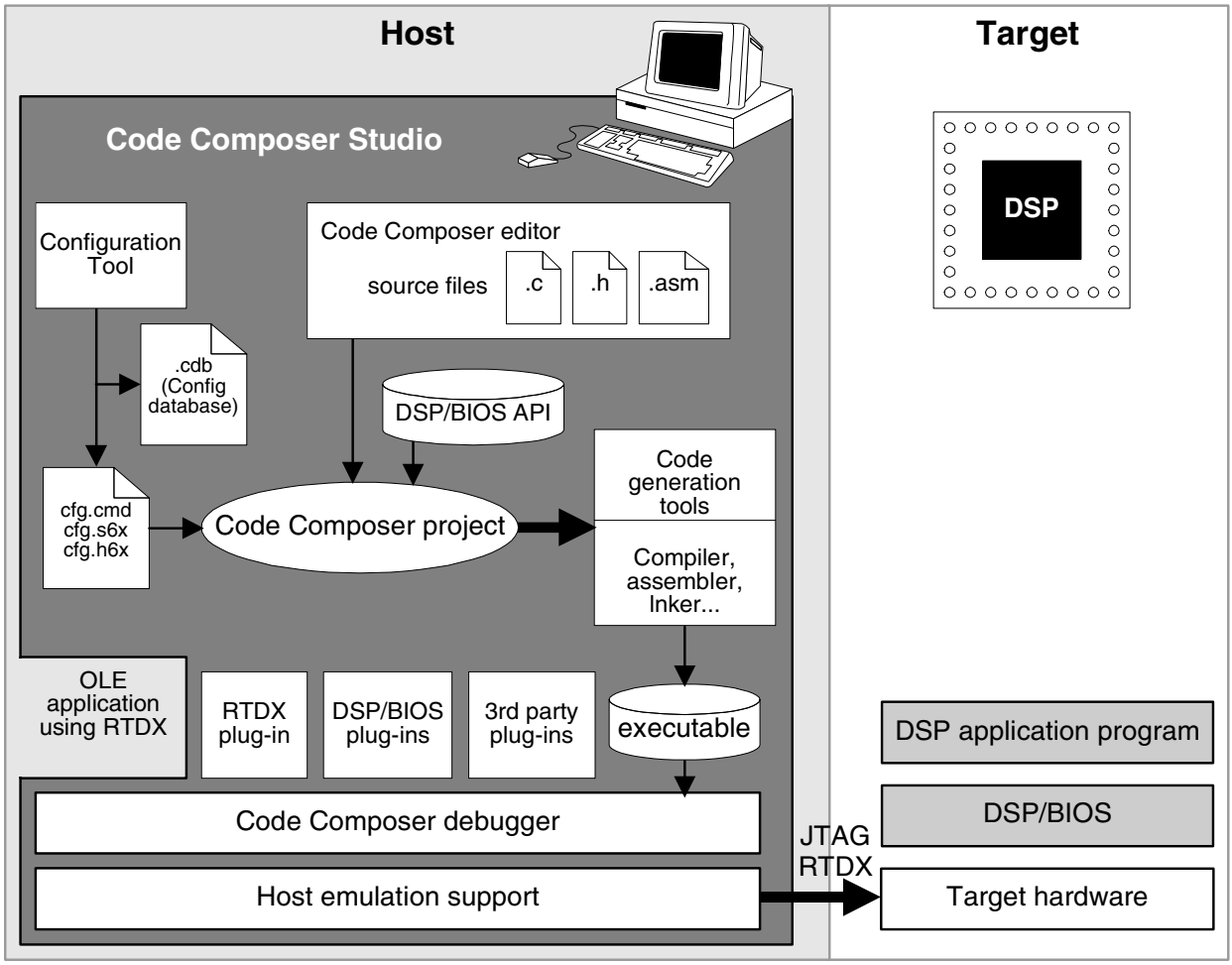
Memory Mapping for the DSK's

- Memory map details can be found in the TI documentation
- We are most interested in the memory addresses locations for storing programs and data on DSK
- The *linker command file*, `*.cmd` is used to handle the differences in memory mapping between the two platform, and in general across all TI DSP processors

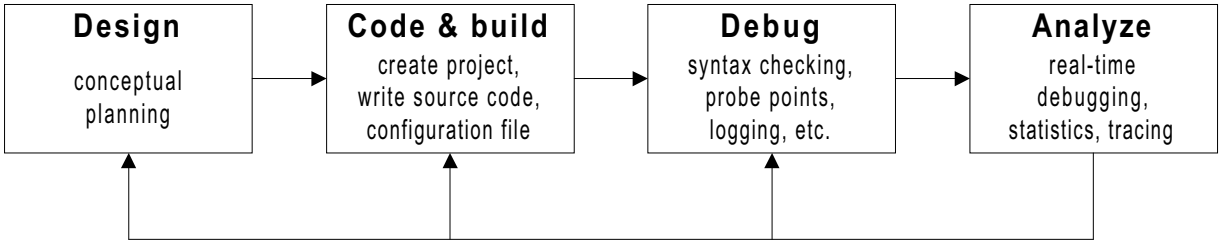
Software Development Overview

Code Composer Studio (CCS) is the primary development environment on all of TI's DSP platforms

- At a high level CCS consists of the following:

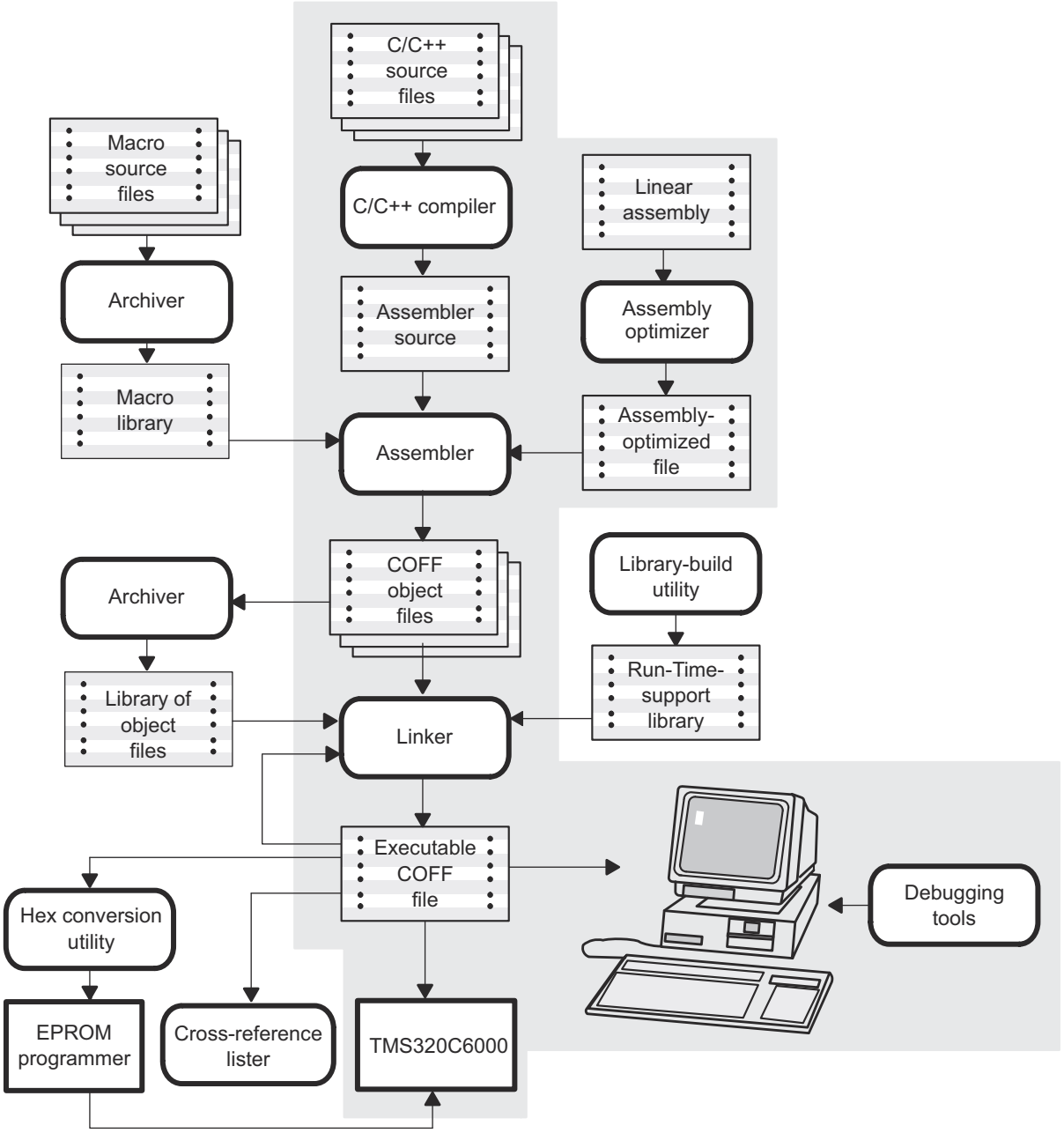


- The phases of code development in CCS can be viewed as follows:

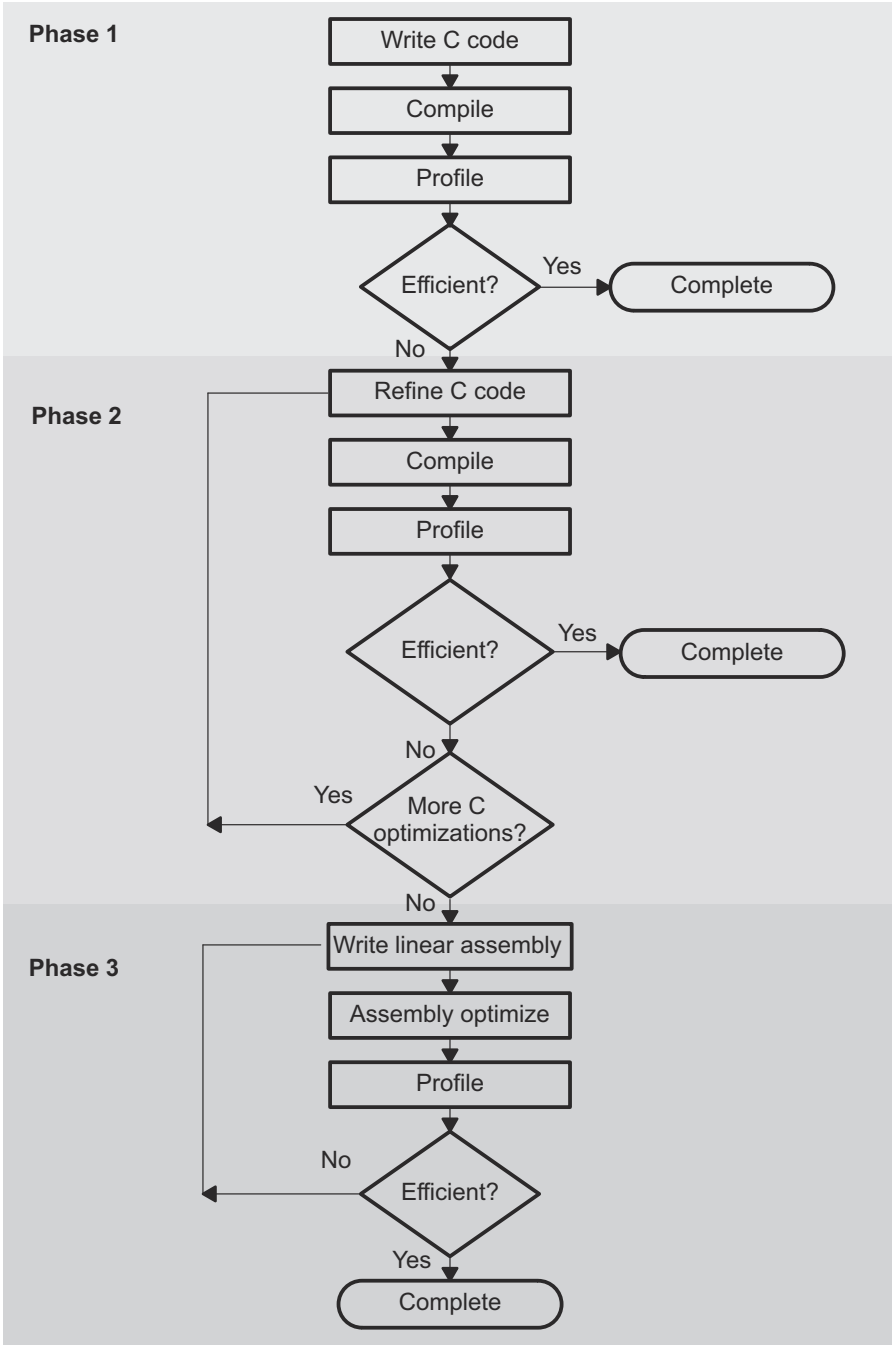


- Irrespective of the development environment employed, command-line or IDE, the generation of machine code in the form of an executable common object file format (`coff`) file follows a common flow

C6x Code Generation Overview



Code Development Flow Chart



DSP/BIOS

- Built-in instrumentation capability
  - `printf` stops the DSP to send a string back to the debugger
- BIOS can automatically log events back to CCS using `LOG_printf()`
- The DSP/BIOS API contains user specified functions to send event information back to CCS
- View real-time statistics that are passed back during non-critical times
- This capability comes about via *Real-Time Data Exchange* (RTDX)

Traditional Start/Stop Data Transfer

Continuous Run Data Transfer with RTDX

- DSP/BIOS can also be used to view system events
- All of this is controlled/defined via the CCS *configuration tool*, and the associated configuration file, which replaces the `.cmd` file
- How do we manage/synchronize real-world events?
- Hardware events are driven by hardware interrupts
- With BIOS hardware interrupts are transformed to software interrupts (SWI)
- Each SWI can be managed via prioritization in a scheduler that is part of the DSP/BIOS configuration tool

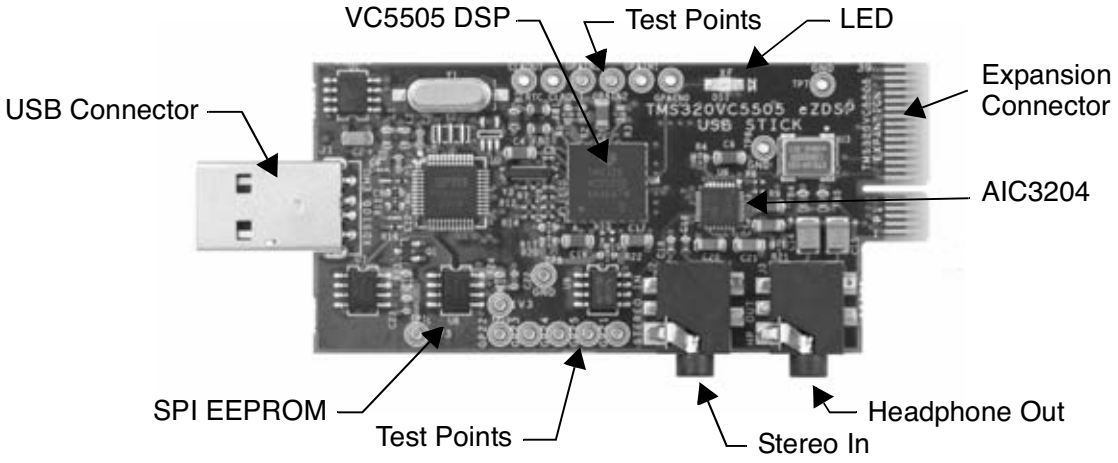
DSP/BIOS Summary for Now

A real-time kernel that consists of:

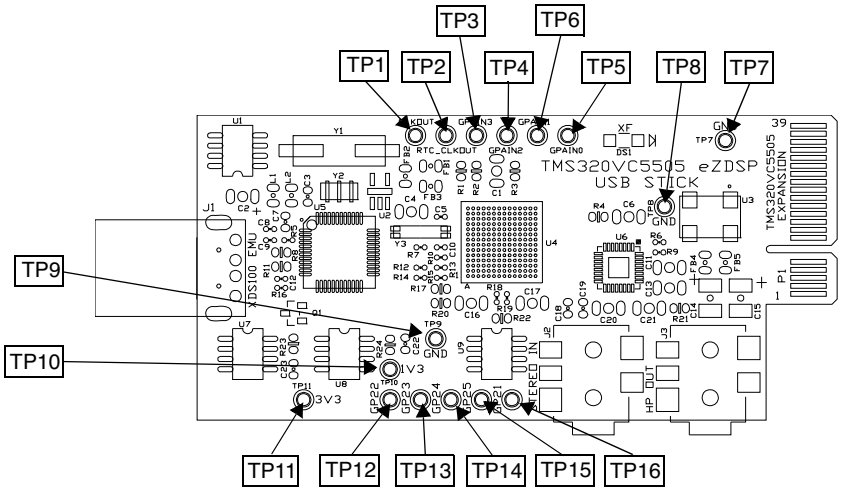
- real-time scheduling
- real-time capture
- real-time I/O

VC5505 *eZDSP USB Stick*

- Exposure to the new low-cost DSP platform from the fixed-point c55x family is also planned
- The board

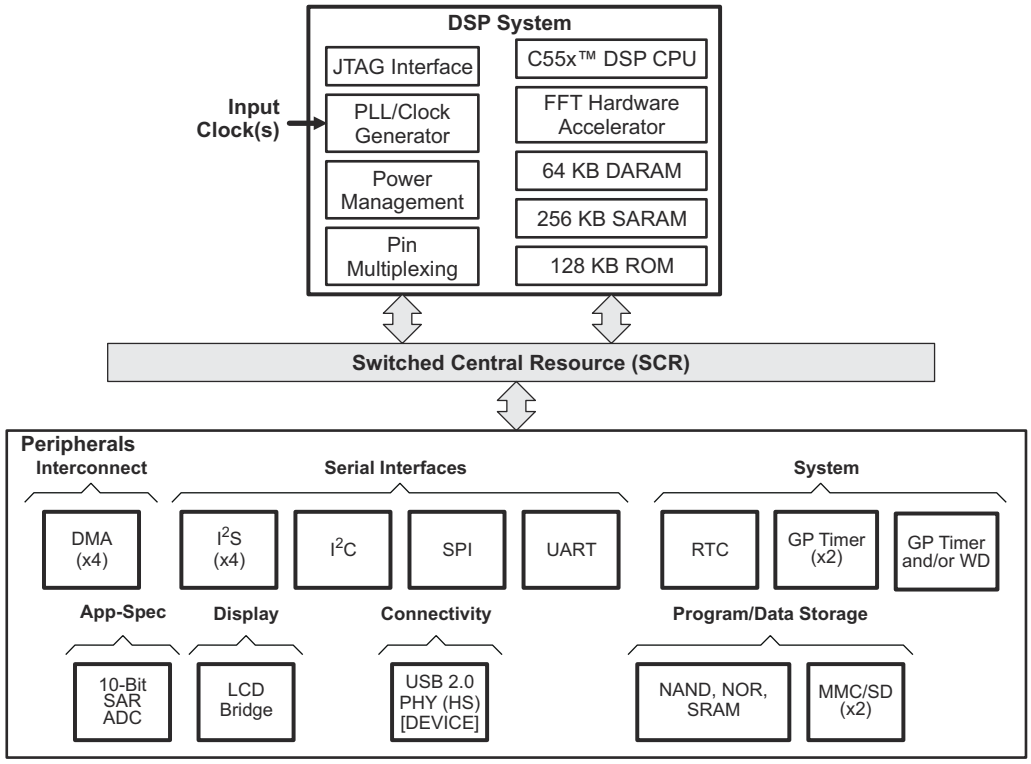


- Test points



TP #	Schematic Page	Signal Name
TP1	3	CLKOUT, Pin A7, VC5505
TP2	3	RTC_CLKOUT, Pin D8, VC5505
TP3	2	GPAIN3, Pin C11, VC5505
TP4	2	GPAIN2, Pin B11, VC5505
TP5	2	GPAIN1, Pin A11, VC5505
TP6	2	GPAIN0, Pin D10, VC5505
TP7	3	GND
TP8	7	GND
TP9	5	GND
TP10	6	Vcore, VCC_1V3, Pin 7,8 U8
TP11	6	3V3, VCC_3V3, Pin 7,8 U7
TP12	4	GPIO22, Pin E2, VC5505
TP13	4	GPIO23, Pin F2, VC5505
TP14	4	GPIO24, Pin G2, VC5505
TP15	4	GPIO25, Pin G4, VC5505
TP16	4	GPIO21, Pin N1, VC5505

- Block diagram

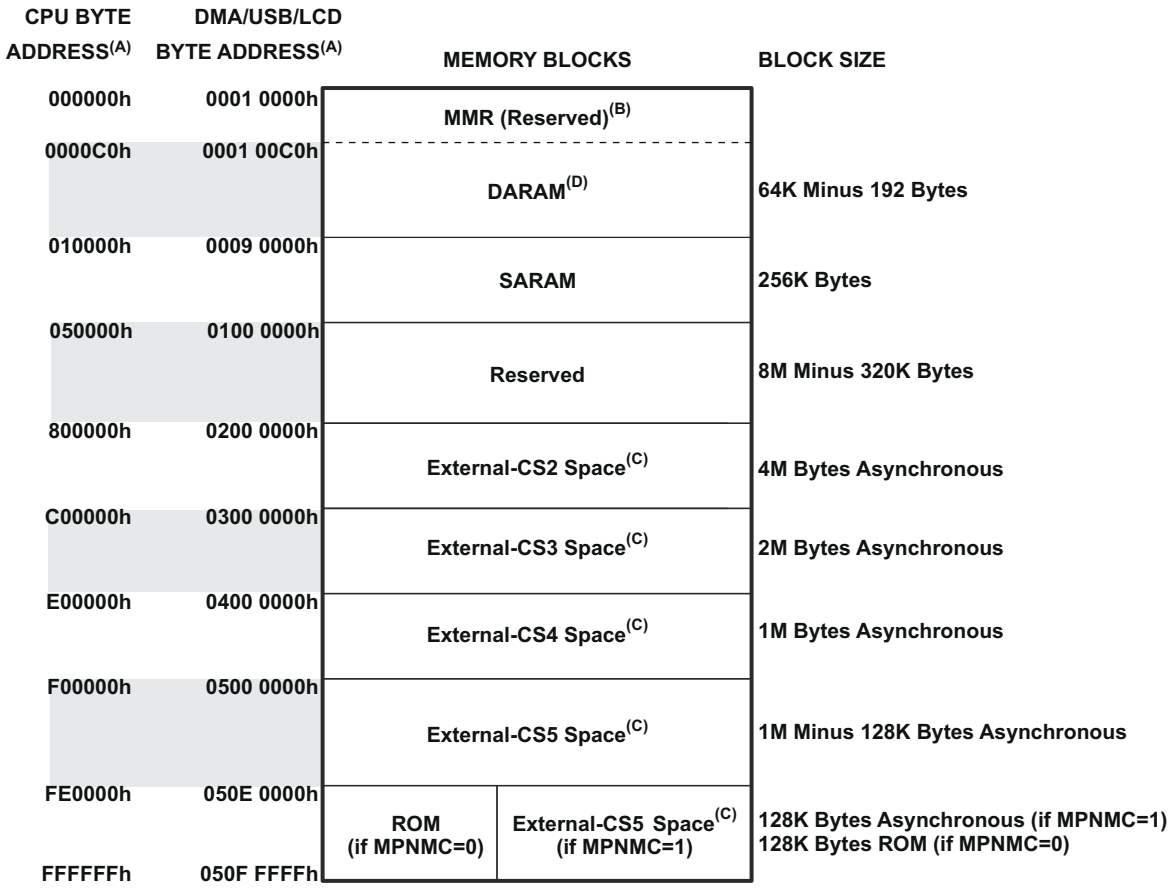


• Features

1.1 TMS320VC5505 Features

- **High-Performance, Low-Power, TMS320C55x™ Fixed-Point Digital Signal Processor**
  - **16.67-, 10-ns Instruction Cycle Time**
  - **60-, 100-MHz Clock Rate**
  - **One/Two Instruction(s) Executed per Cycle**
  - **Dual Multipliers [Up to 200 Million Multiply-Accumulates per Second (MMACS)]**
  - **Two Arithmetic/Logic Units (ALUs)**
  - **Three Internal Data/Operand Read Buses and Two Internal Data/Operand Write Buses**
  - **Fully Software-Compatible With C55x Devices**
  - **Industrial Temperature Devices Available**
- **320K Bytes Zero-Wait State On-Chip RAM, Composed of:**
  - **64K Bytes of Dual-Access RAM (DARAM), 8 Blocks of 4K x 16-Bit**
  - **256K Bytes of Single-Access RAM (SARAM), 32 Blocks of 4K x 16-Bit**
- **128K Bytes of Zero Wait-State On-Chip ROM (4 Blocks of 16K x 16-Bit)**
- **16-/8-Bit External Memory Interface (EMIF) with Glueless Interface to:**
  - **8-/16-Bit NAND Flash, 1- and 4-Bit ECC**
  - **8-/16-Bit NOR Flash**
  - **Asynchronous Static RAM (SRAM)**
- **Direct Memory Access (DMA) Controller**
  - **Four DMA With 4 Channels Each (16-Channels Total)**
- **Three 32-Bit General-Purpose Timers**
  - **One Selectable as a Watchdog and/or GP**
- **Two MultiMedia Card/Secure Digital (MMC/SD) Interfaces**
- **Universal Asynchronous Receiver/Transmitter (UART)**
- **Serial-Port Interface (SPI) With Four Chip-Selects**
- **Master/Slave Inter-Integrated Circuit (I^2C Bus™)**
- **Four Inter-IC Sound (I^2S Bus™) for Data Transport**
- **Device USB Port With Integrated 2.0 High-Speed PHY that Supports:**
  - **USB 2.0 Full- and High-Speed Device**
- **LCD Bridge With Asynchronous Interface**
- **Tightly-Coupled FFT Hardware Accelerator**
- **10-Bit 4-Input Successive Approximation (SAR) ADC**
- **Real-Time Clock (RTC) With Crystal Input, With Separate Clock Domain, Separate Power Supply**
- **Four Core Isolated Power Supply Domains: Analog, RTC, CPU and Peripherals, and USB**
- **Four I/O Isolated Power Supply Domains: RTC I/O, EMIF I/O, USB PHY, and DV_{DDIO}**
- **Low-Power S/W Programmable Phase-Locked Loop (PLL) Clock Generator**
- **On-Chip ROM Bootloader (RBL) to Boot From NAND Flash, NOR Flash, SPI EEPROM, or I2C EEPROM**
- **IEEE-1149.1 (JTAG™) Boundary-Scan-Compatible**
- **Up to 26 General-Purpose I/O (GPIO) Pins (Multiplexed With Other Device Functions)**
- **196-Terminal Pb-Free Plastic BGA (Ball Grid Array) (ZCH Suffix)**
- **1.05-V Core (60 MHz), 1.8-V, 2.5-V, 2.8-V, or 3.3-V I/Os**
- **1.3-V Core (100 MHz), 1.8-V, 2.5-V, 2.8-V, or 3.3-V I/Os**
- **Applications:**
  - **Wireless Audio Devices (e.g., Headsets, Microphones, Speakerphones, etc.)**
  - **Echo Cancellation Headphones**
  - **Portable Medical Devices**
  - **Voice Applications**
  - **Industrial Controls**
  - **Fingerprint Biometrics**
  - **Software Defined Radio**

- Memory Map



A. Address shown represents the first byte address in each block.

B. The first 192 bytes are reserved for memory-mapped registers (MMRs).

C. Out of the four DMA controllers, *only* DMA controller 3 has access to the external memory space.

D. The USB and LCD controllers do not have access to DARAM.

- For more details on the C55 architecture in general see Section 4.4 of the Kuo text
- Since the C55 follows in the line of the C54, Section 4.3 of the Kuo text covers this family of processors