CSE350: Digital Electronics & Pulse Techniques

Lecture 01: ADC Intro, Flash ADC, Dual Slope ADC

Course Instructor:

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Inspiring Excellence

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Analog: Information or data that can be any real value at any instant of time. Physical world signals are of analog nature.

Analog Signal

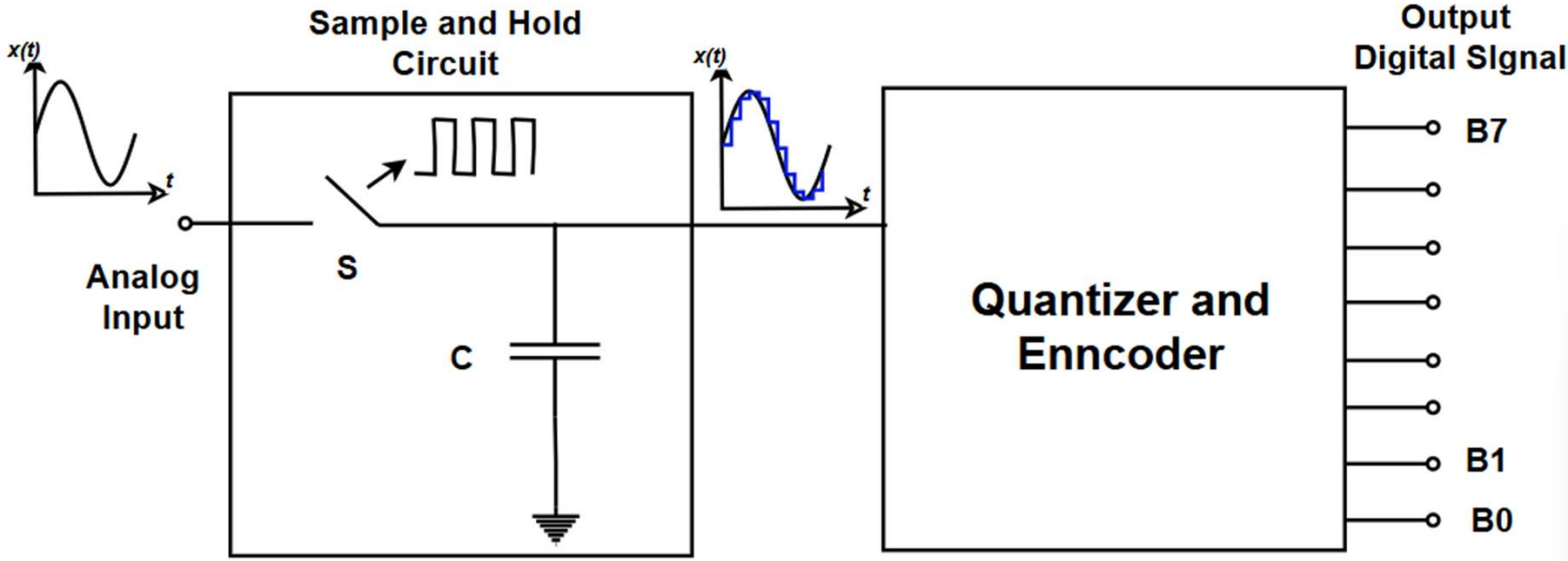
Digital: Information in the form of binary bit streams. Computers & all digital devices need digital signals to operate.

Digital data means binary bit of strings.

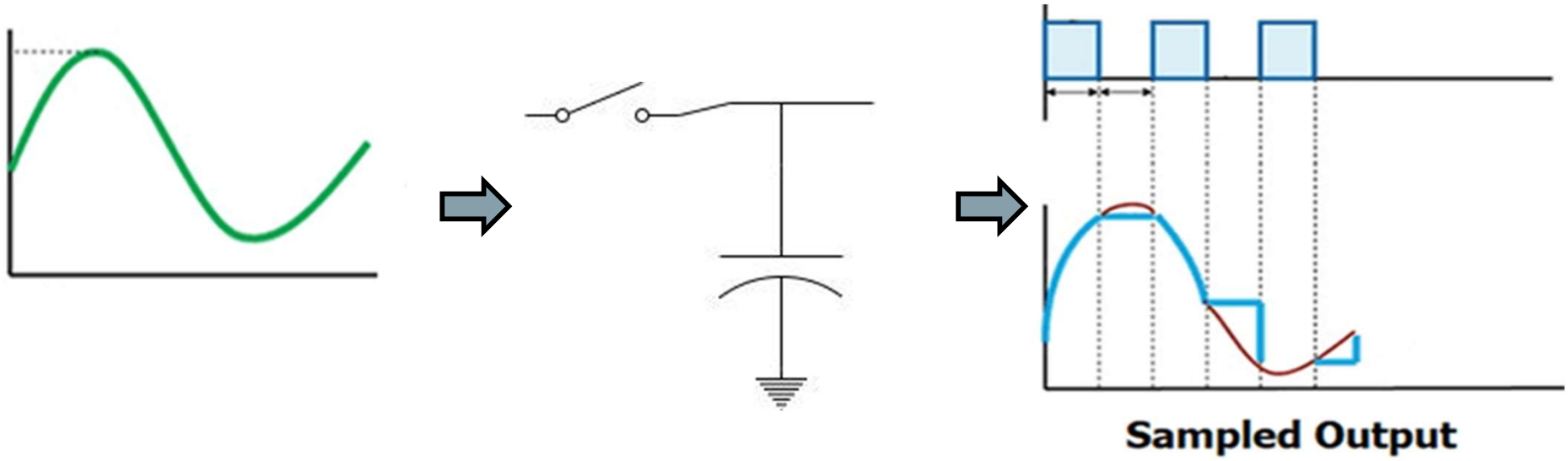
Digital Signal

***ADC** is the process of converting analog signals to digital signals.* It can be summarized as below:

A/D conversion process



Sample & Hold: The analog signal is sampled at regular intervals of a clock pulse. A capacitor is used to hold the peak value of the preceding interval until next one arrives. Thus, instead of all the real values of the original signal, we get a signal that has reduced specific values, i.e. a discrete signal.



Quantization

Quantization is a process by which we assign sampled and hold signal data to some fixed preassigned values.

Depending on the method used to assign analog values to these levels, quantization can be of the following **two** types:

1. Midrise Quantization
2. Midtread Quantization

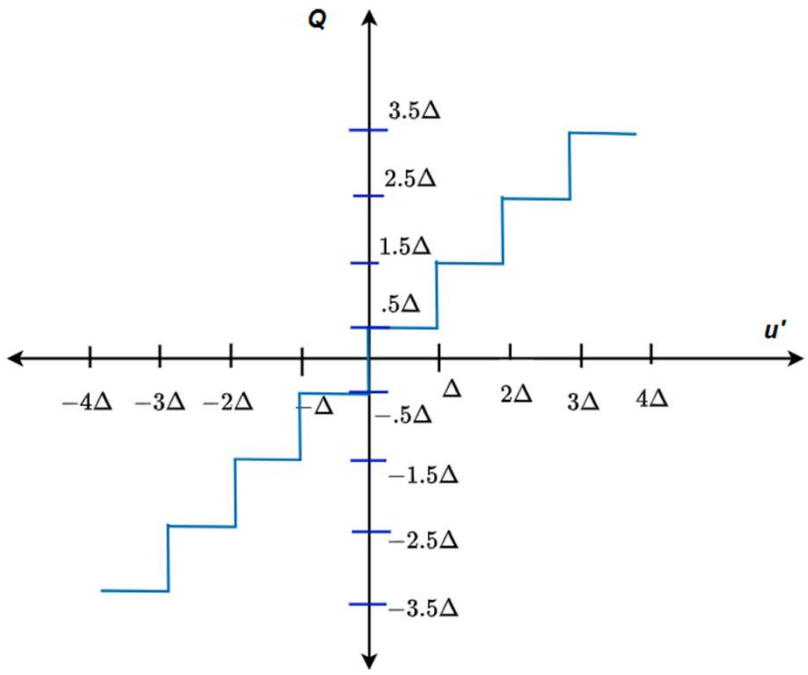
$N = Number\ \ of\ bits$
$2^N = Number\ of\ Quantization\ levels$

The difference between any two consecutive levels are equal and called the **resolution of quantization**. This can be expressed as, $\Delta = \text{resolution} = \frac{V_{max} - Vmin}{2^N}$

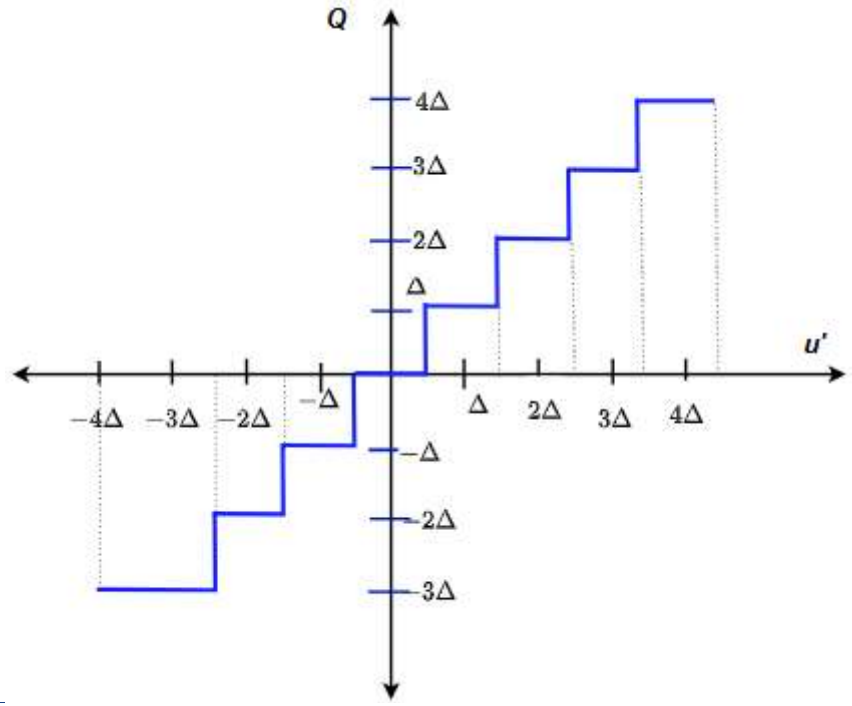
Mid-rise Quantization: A type of quantization scheme used in digital signal processing, where the range of the input signal is divided into a set of equal-sized intervals, and the output levels are assigned to the midpoints of these intervals.

The quantization levels are symmetric about zero but do not include a quantization level at zero (midpoint between minimum & maximum). For a signal quantized into 8 levels with a range from -4 to 4:

- Quantization intervals: $[-4,-3),[-3,-2),\ldots,[3,4)$
- Midpoints (output levels): $-3.5, -2.5, -1.5, -0.5, 0.5, 1.5, 2.5, 3.5$



Mid-tread Quantization: A type of quantization scheme used in signal processing, where the range of the input signal is divided into intervals, and the output levels are assigned to the midpoints of these intervals, with one of the levels located exactly at zero(midpoint between minimum & maximum).



For a signal quantized into 8 levels with a range from -4 to 4:

- Quantization intervals: [−4,−2.5),[−3.5,−2.5),…, [3.5,4.5)
- Midpoints (output levels): -4, -3, -2, -1, 0, 1, 2, 3

Encoding: This is the process of assigning binary bit streams to the quantization levels.

For example, the mid-rise quantization levels as showed in previous slide, will be assigned the following 3-bit values:

-3.5: 000 (0)

-2.5: 001 (1)

-1.5: 010 (2)

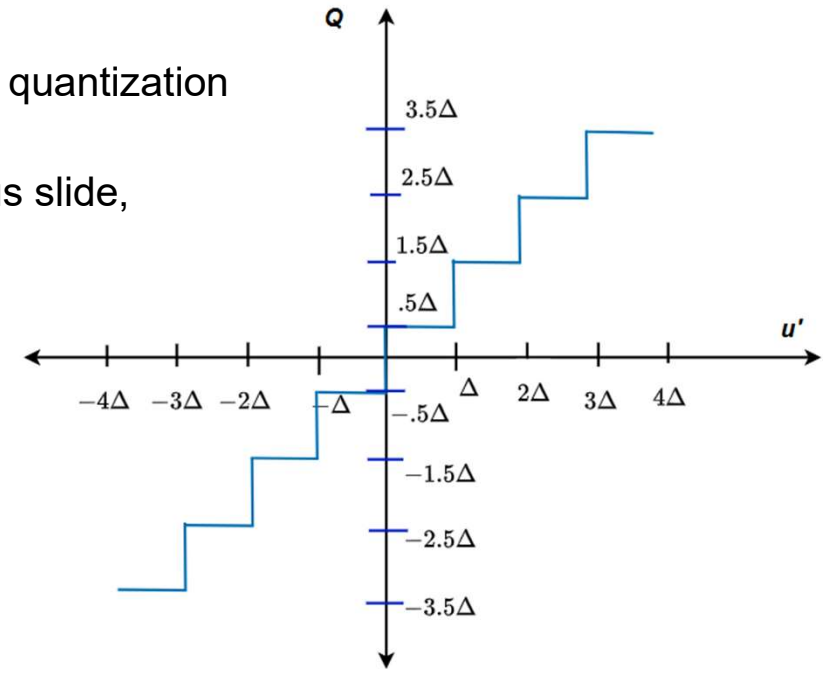
-0.5: 011 (3)

0.5: 100 (4)

1.5: 101 (5)

2.5: 110 (6)

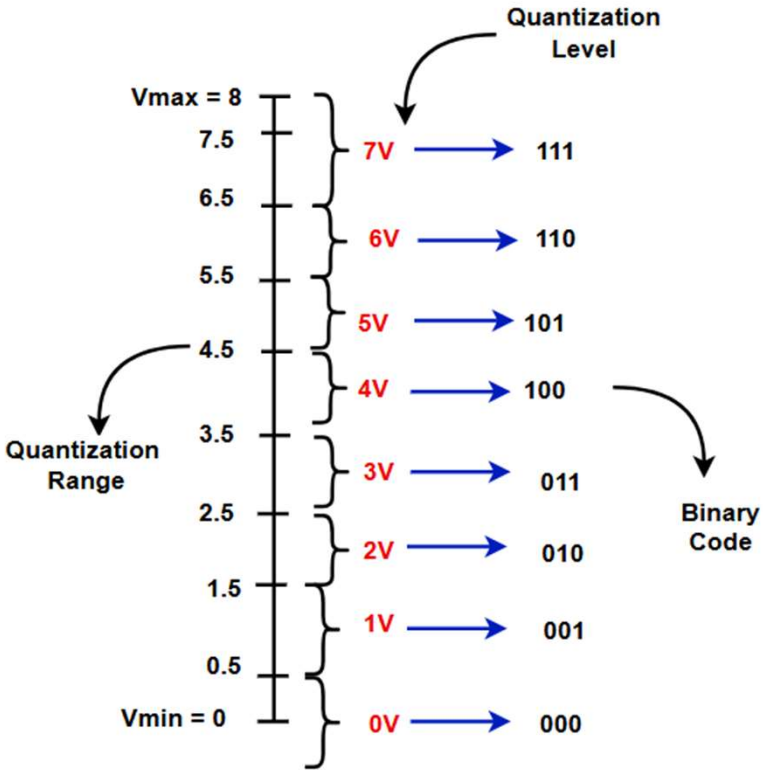
3.5: 111 (7)

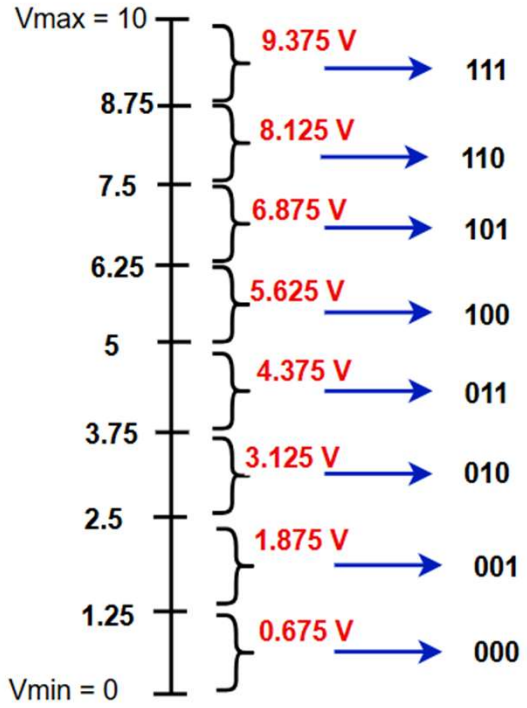


Example: Identify which one is Mid rise and Mid tread.

1. $V_{max} = 8$ and $V_{min} = 0$

2. $V_{max} = 10$ and $V_{min} = 0$





(i) Here,

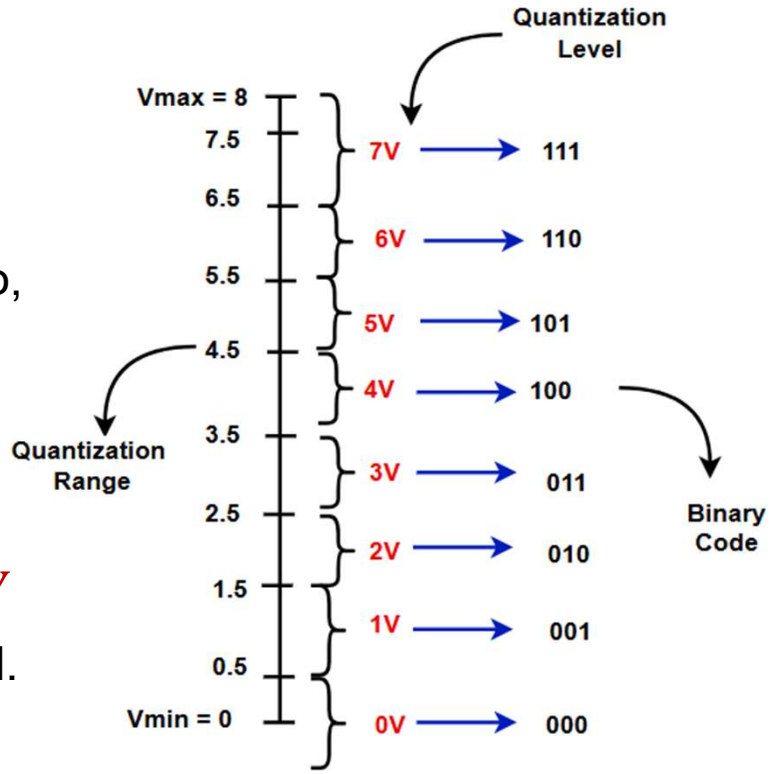
$$\frac{Vmax + Vmin}{2} = \frac{8 + 0}{2} = 4\ V$$

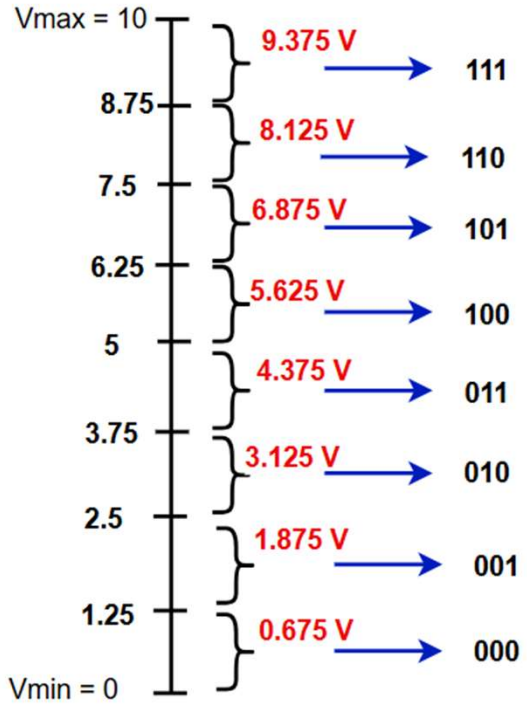
As 4 V is a Quantization level. So, it is a **mid tread quantization**

(ii) Here,

$$\frac{Vmax + Vmin}{2} = \frac{10 + 0}{2} = 5\ V$$

As 5 V is not a Quantization level. So, it is a **mid rise quantization**





Flash A/D converter

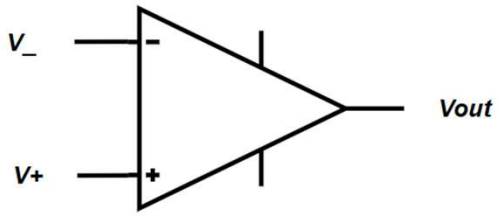
Features of the Flash A/D converter:

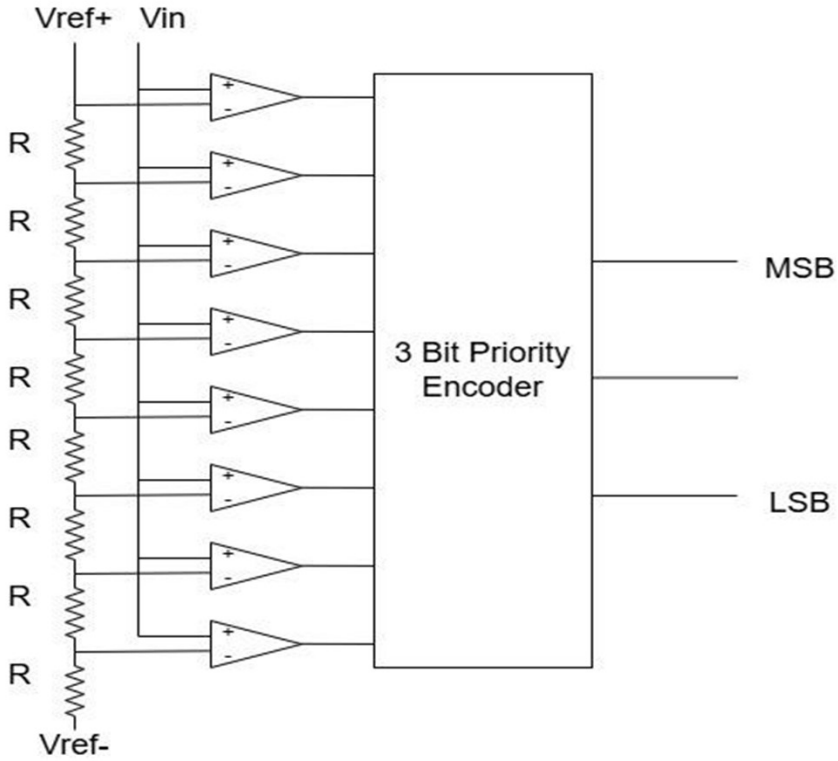
- ✓ This converter is very fast. (adv)
- ✓ It requires one clock cycle to convert the analog to digital data. (adv)
- ✓ It requires a lot components. (dis-adv)

We know, For open loop comparator

$If\ V_+ > V_-\ , V_{out} = High\ (logic\ 1\ )$

$If\ V_+ < V_-\ , V_{out} = Low\ (logic\ 0\ )$





Flash ADC design

Suppose you have a signal with V_{max} = 10 V and V_{min} = 0V. Design a simple flash ADC converter. Use 3 bits for designing. Provide your encoder truth table.

Design:
Here,

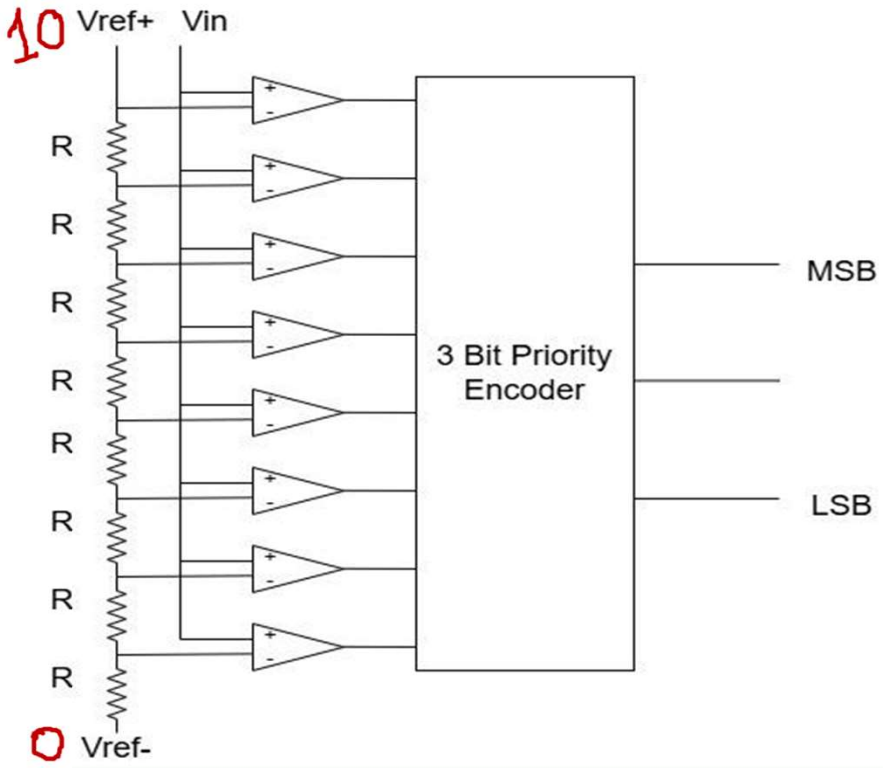
$N = 3$

$\#Number\ of\ registor = 2^3 = 8$

$\#Number\ of\ comparator = 2^3 - 1 = 7$

$V_{+ref} = Vmax = 10\ V$

$V_{-ref} = Vmin = 0\ V$



Flash ADC design

(V+ of the comparator is connected to the input.)

The following is the Circuit of a 3 bits Flash ADC,

$$I = \frac{10 - 0}{8R} = \frac{10}{8R}$$

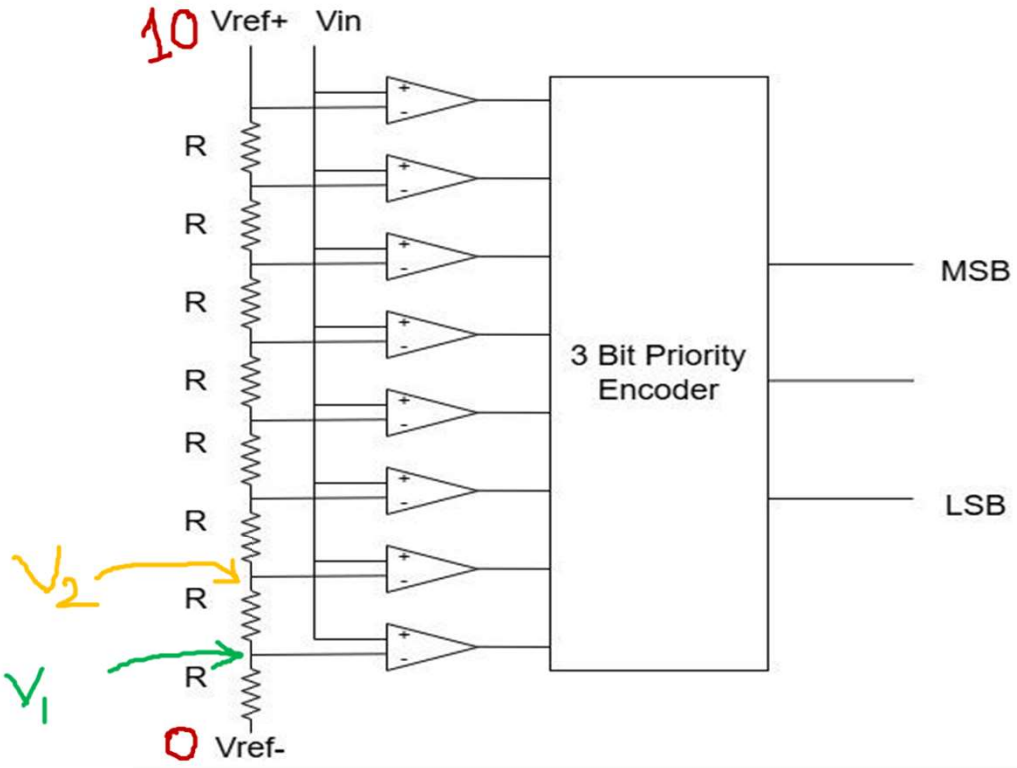
$$I = \frac{V1 - V_{-ref}}{R}$$

$$V1 = V_{-ref} + IR = 0 + \frac{10}{8R} * R = 1.25\ V$$

Similarly, $I = \frac{V2 - V1}{R} \Rightarrow V2 = V1 + IR$

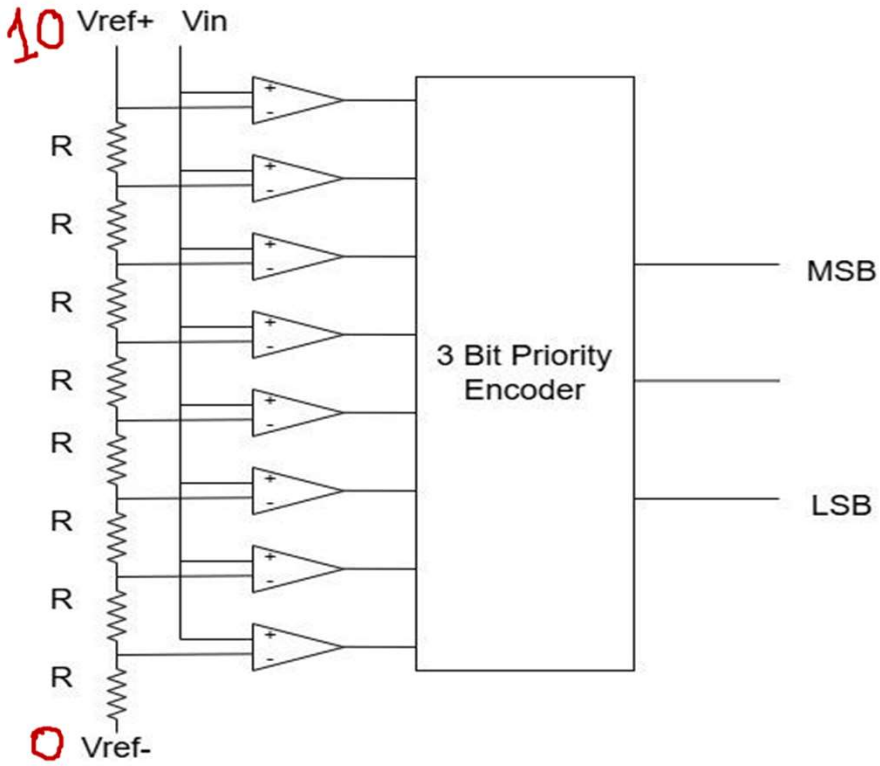
$$\Rightarrow \quad V2 = 1.25 + \frac{10}{8R} * R = 2.5\ V$$

You can find other voltage in this way.



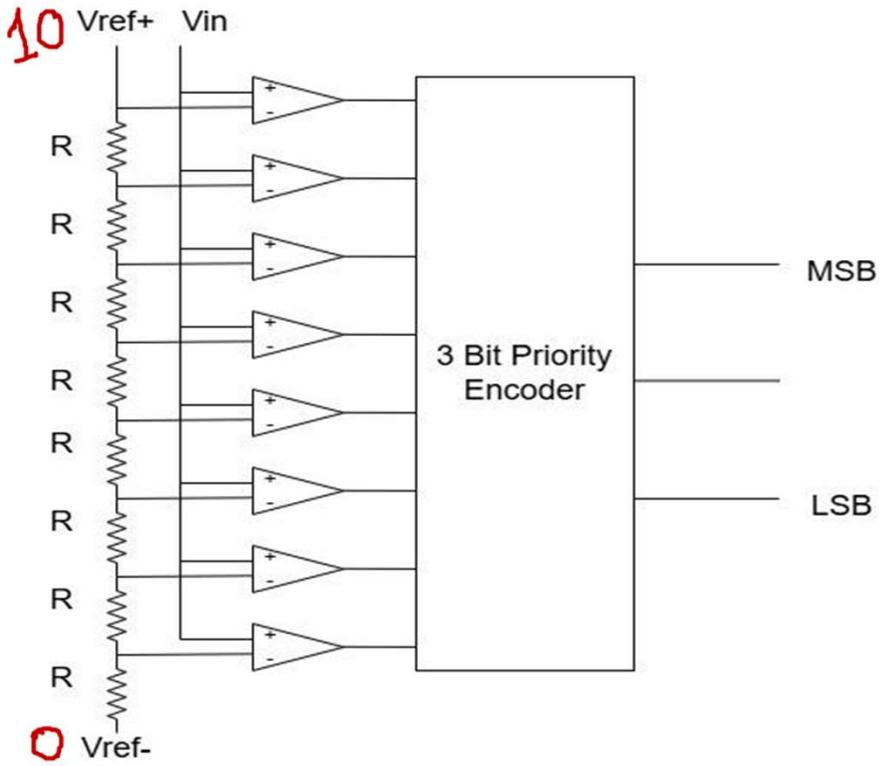
(V+ of the comparator is connected to the input.)

Q Range	Q level	I7I6I5I4I3I2I1|	Binary (B2B1B0)
0 - 1.25	0.675	000 000 0	000
1.25 - 2.5	1.875	000 000 1	001
2.5 - 3.75	3.125	000 001 1	010
3.75 – 5	4.375	000 011 1	011
5 – 6.25	5.625	000 111 1	100
6.25 – 7.5	6.875	001 111 1	101
7.5 – 8.75	8.125	011 111 1	110
8.75 - 10	9.375	111 111 1	111



(V- of the comparator is connected to the input.)

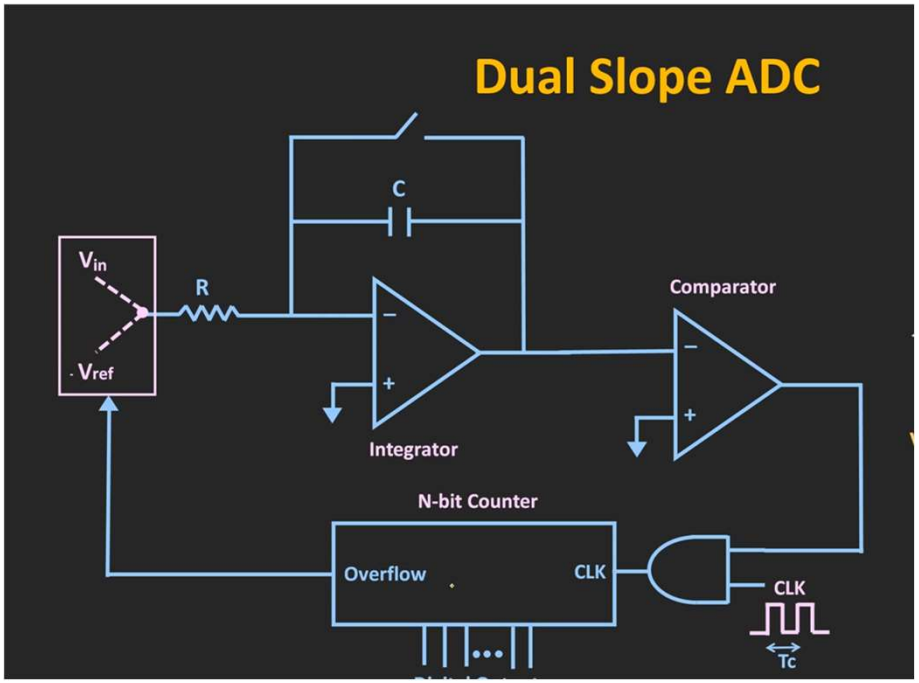
I7I6I5I4I3I2I1	Binary (B2B1B0)
111 111 1	000
111 111 0	001
111 110 0	010
111 100 0	011
111 000 0	100
110 000 0	101
1 000 000	110
000 000 0	111

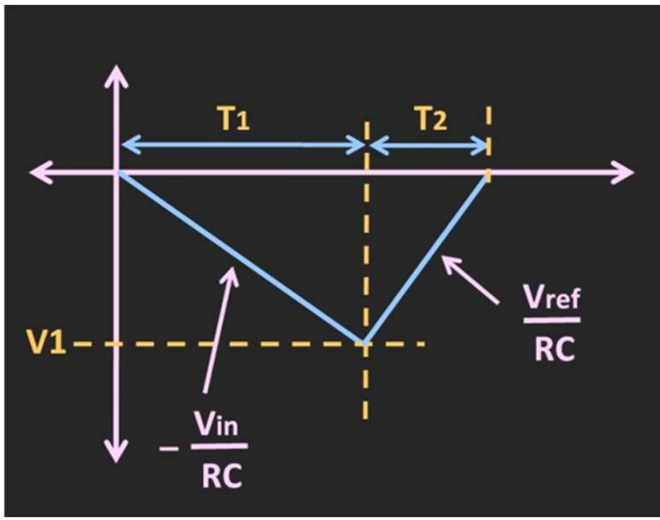


Dual Slope ADC:

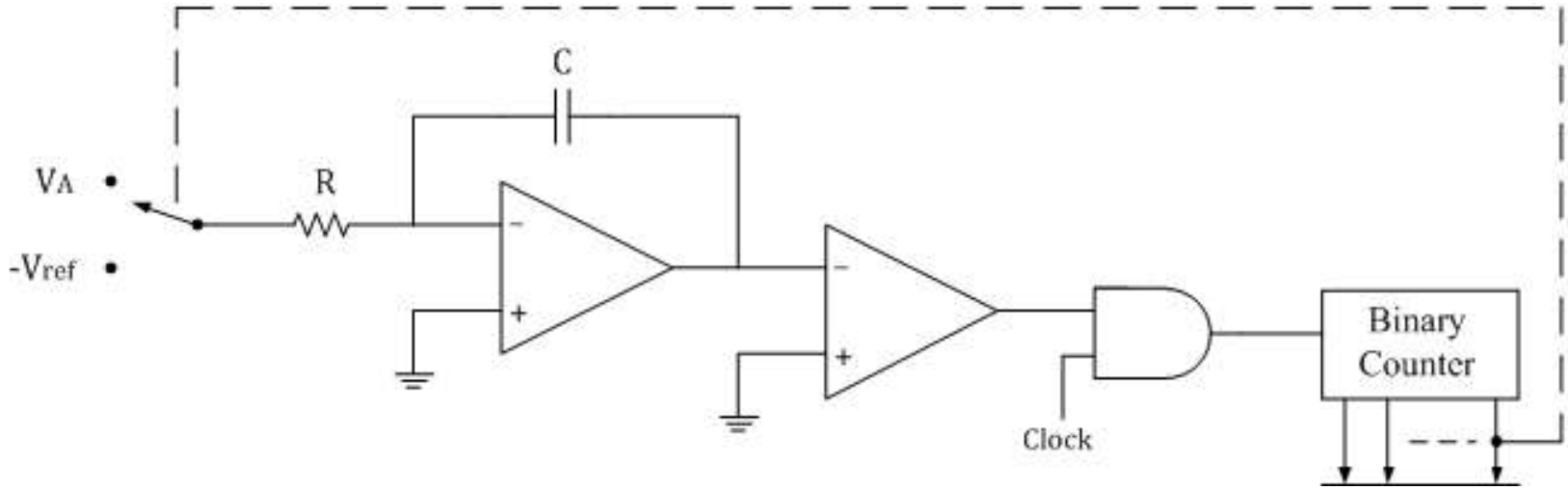
Advantages: Requires less components, high resolution (number of quantization levels or bits can be high).

Disadvantages: Too slow conversion.





Dual slope ADC



A dual slope ADC uses an integrator for conversion. This provides high resolution with good accuracy but it has a very slow conversion time. So, they are not used to gather data but preferred in places where the signal changes slowly.

Additional Reference - https://www.youtube.com/watch?v=2gF_nfaBV_0

- Case 1: When connected to V_A/ V_{in}, from time t<0 to t= T1

$$V_o = -\frac{1}{RC}\int_0^{T1} Vin\ dt$$

$$V_o = -\frac{Vin*T1}{RC}$$

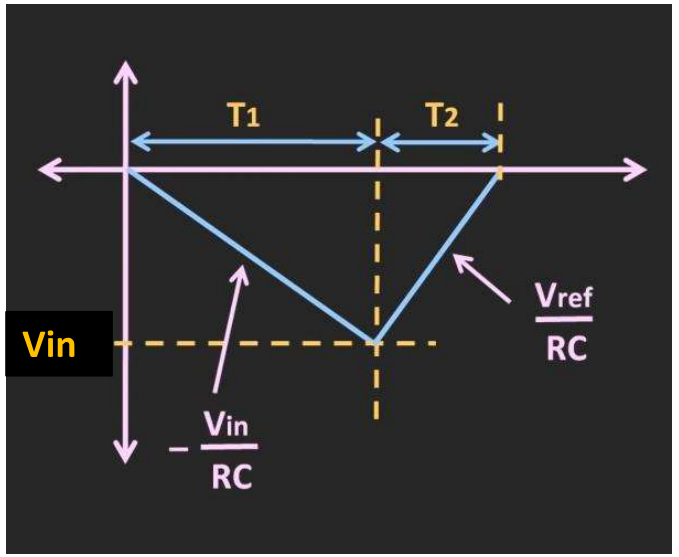
From time t=0 to t= T1, the counter counts from 0-2^n and after reaching 2^n, a control signal is sent to the switch and the switch connects to –Vref so the capacitor starts discharging.

$$V_o = -\frac{1}{RC}\int_{t1}^{t2} -Vref\ dt + Vinitial$$

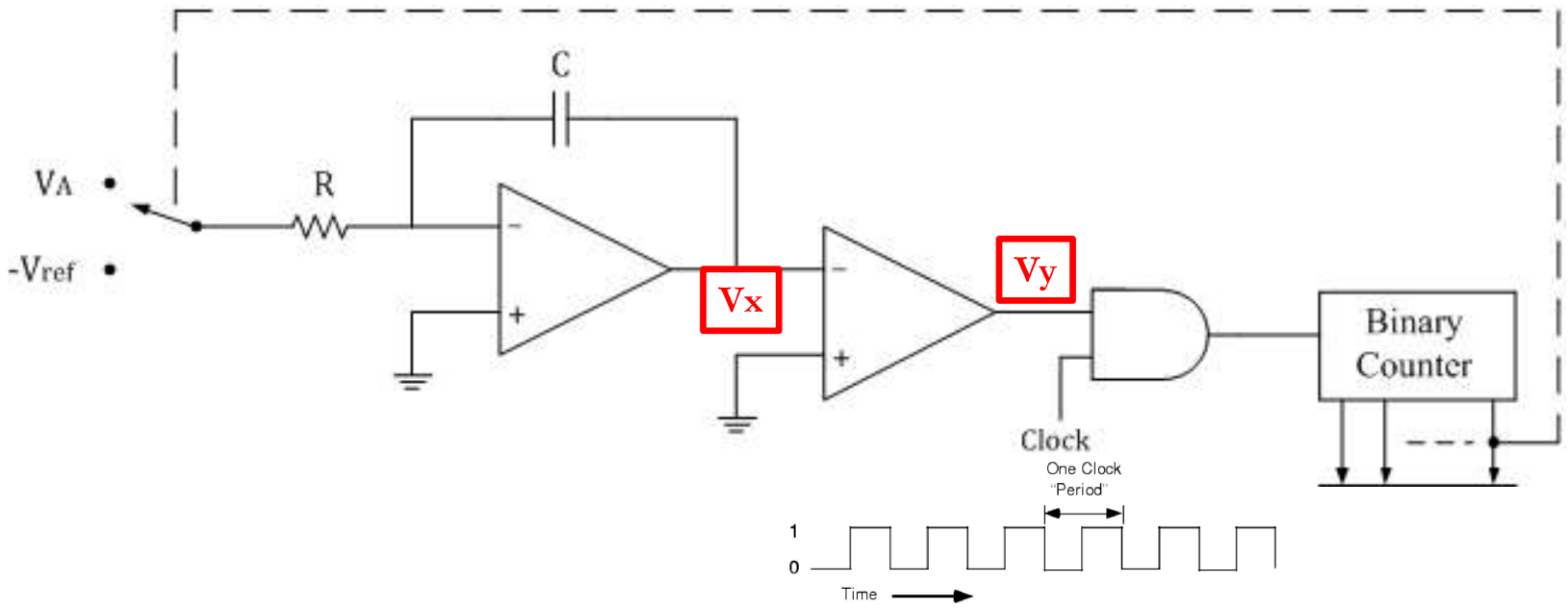
$$V_o = \frac{Vref*T2}{RC} - \frac{Vin*T1}{RC} = 0$$

So, $$\frac{Vref*T2}{RC} = \frac{Vin*T1}{RC}$$

$$T2 = \frac{Vin*T1}{Vref}$$



Case 1: When connected to V_A/ V_{in} , from time t<0 to t= T1

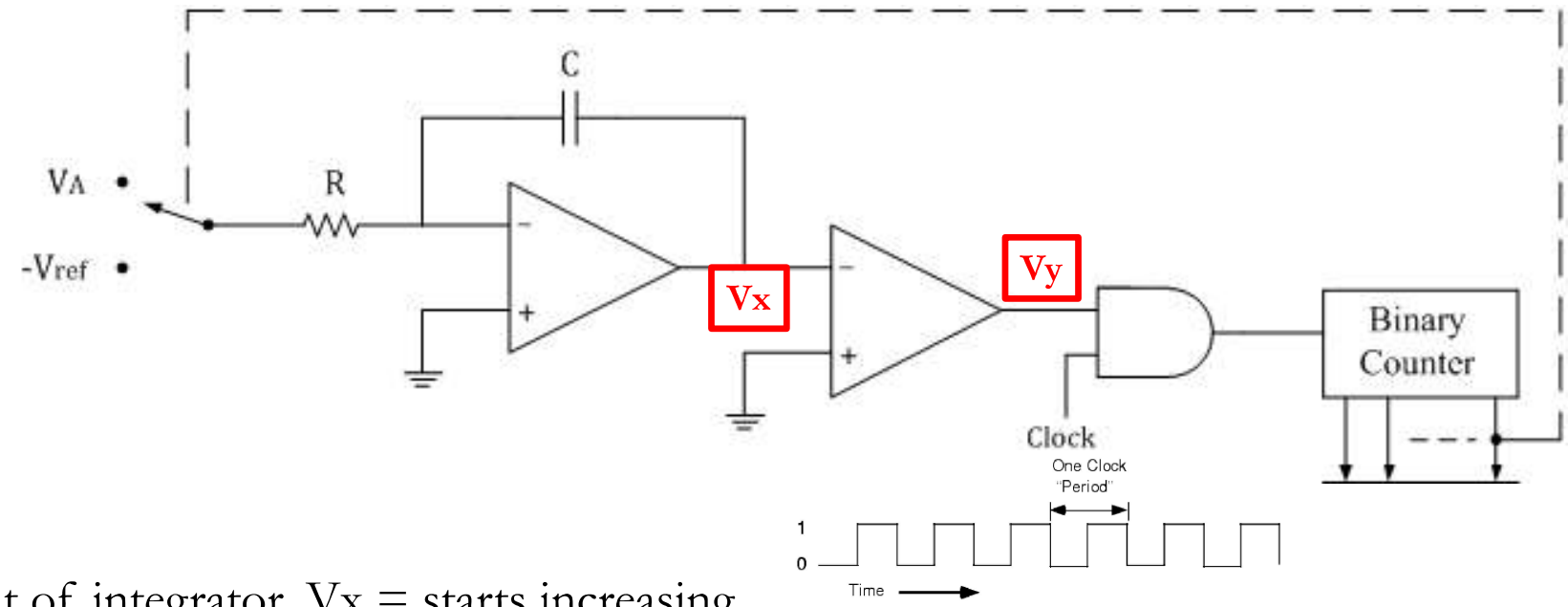


Output of integrator, Vx = -ve

So, the output of comparator, Vy = "1"

So the AND gate gives the clock pulse. And our counter starts counting from 0-2^n. After that, the overflow bit causes the integrator to switch to -Vref

Case 2: When connected to -Vref



Output of integrator, Vx = starts increasing

So, the output of comparator, Vy = Becomes "0" as soon as integrator output reaches positive value.

So the AND gate output becomes "0" and the counter stops counting after T2 time.

$T1 = 2^n * Tc$ and $T2 = N * Tc$

$$Vin = \frac{N}{2^n} * Vref$$