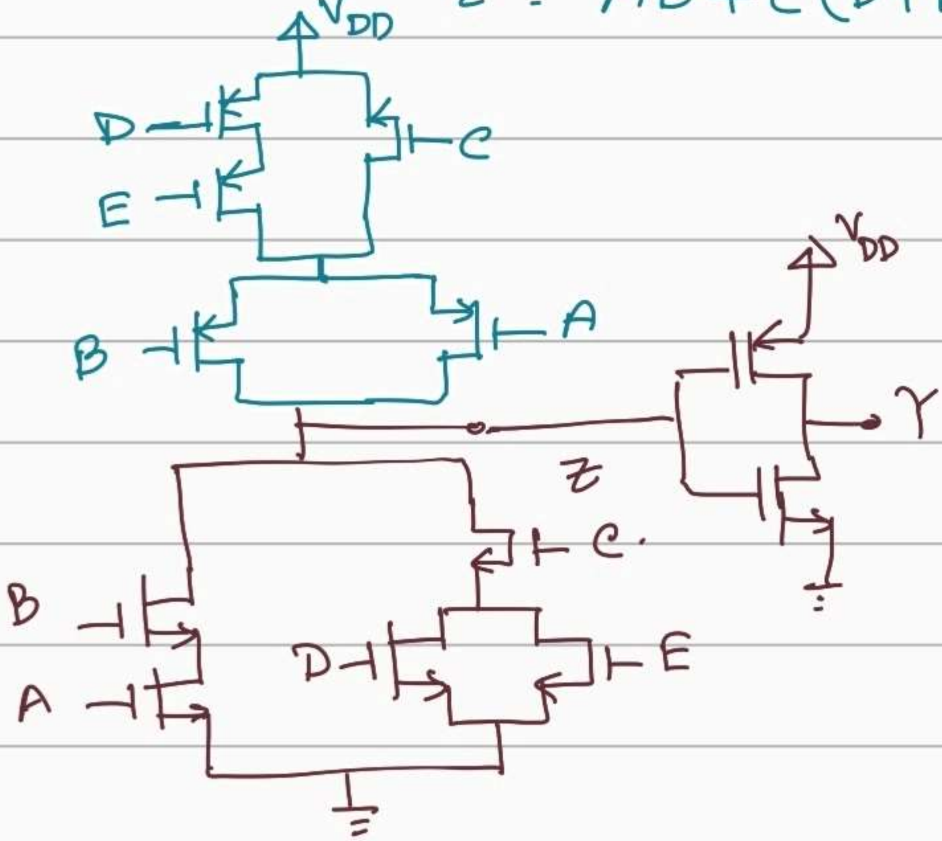
Example: 16·11

$$Y = AB + C(D+E)$$

$$Y = \overline{Z}$$

$$Z = \overline{AB + C(D+E)}$$



\# Switching up series connections doesn't change output.

April - 16, Quiz 4. Question has been announced.

"NMOS NOR gate with DEPLETION LOAD"

Lecture 16: $\boxed{\text{ADC and DAC}}$

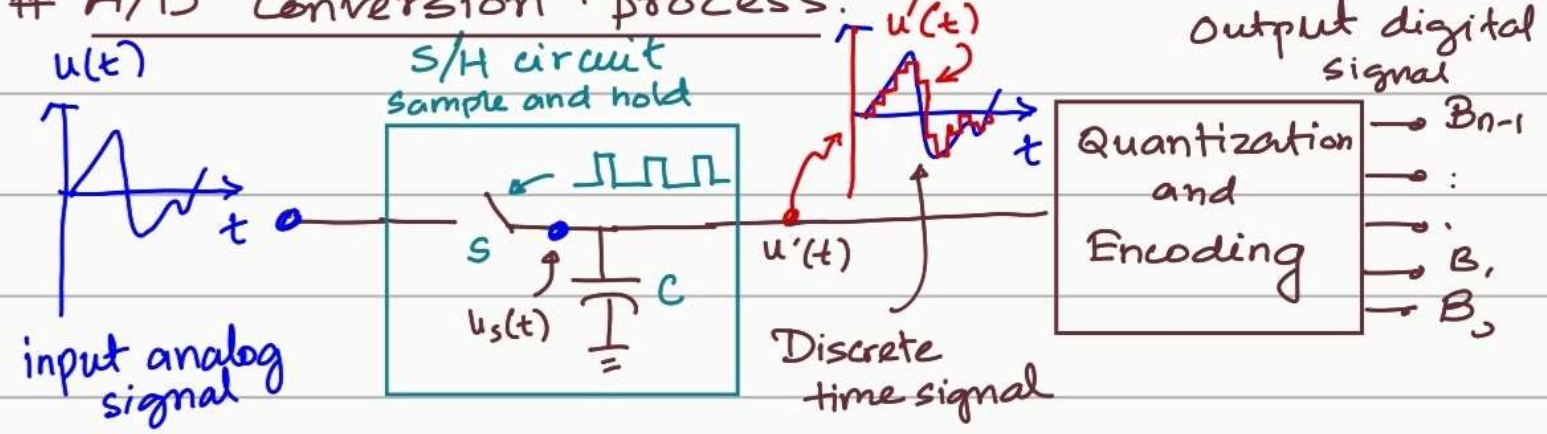
\# Physical world's informations are analog. Analog means data could take any real value at each instant of time.

\# In order to store/process we use digital data in our computers and microprocessor. Digital data means binary bit of strings.

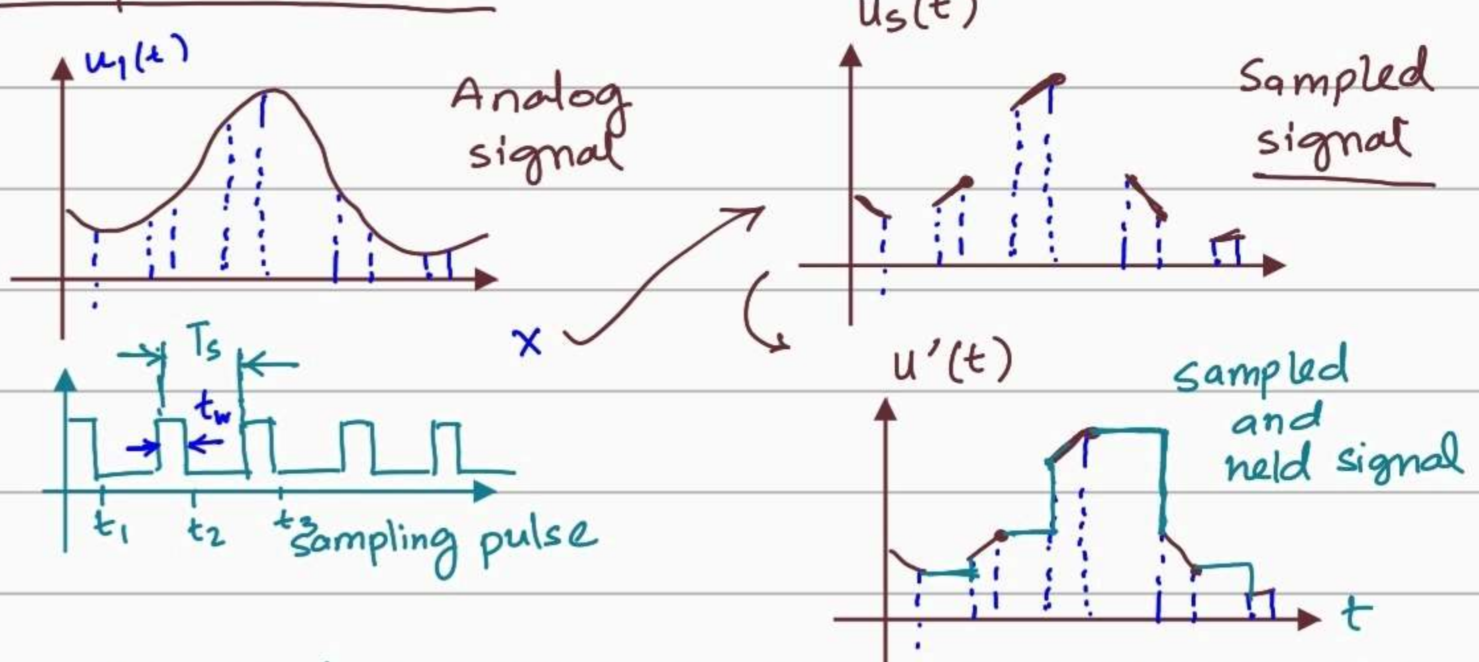
Environment → Transducer → Computer → speaker

$\boxed{A/D}$ $\boxed{D/A}$

A/D Conversion Process



Sample and Hold:

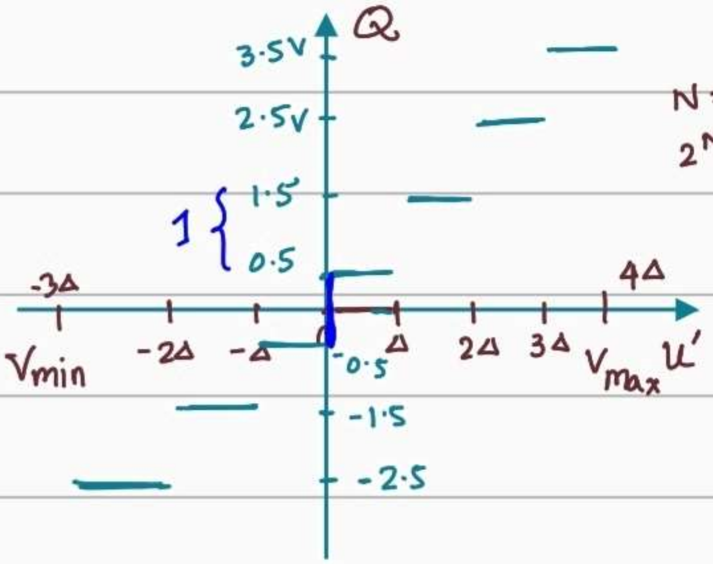


This hold operation is done using the capacitor.

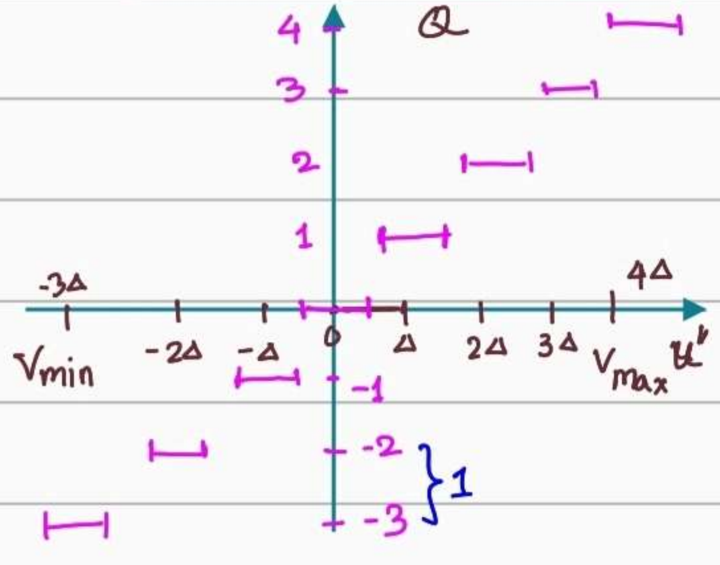
Quantization:

Quantization is process by which we assign sampled and hold signal data to some fixed preassigned values.

Midrise quantization



Mid tread quantization



N = number bits we want as digital output

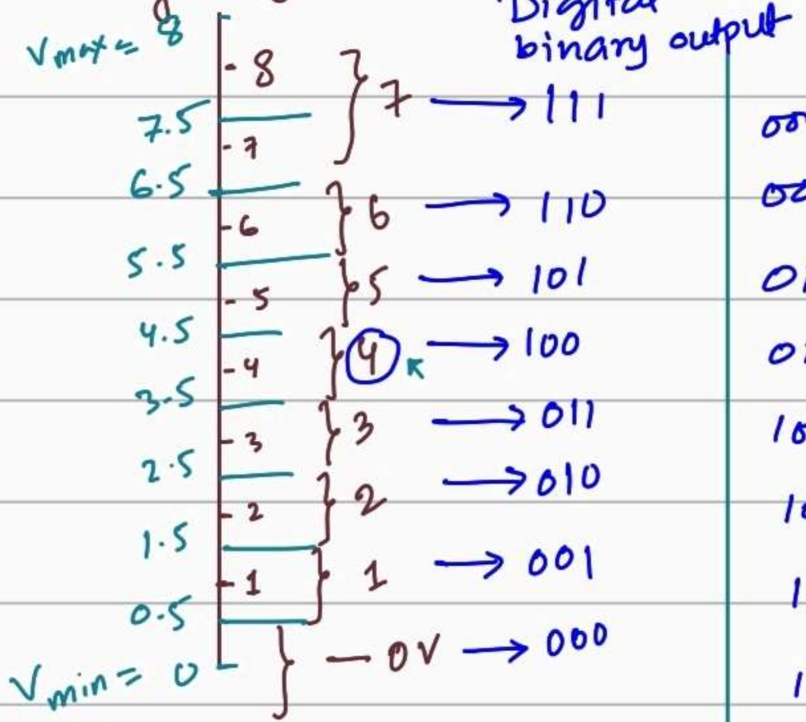
$$\Delta = \text{resolution} = \frac{V_{max} - V_{min}}{2^N}$$

2^N = number of levels.

V_{max} / V_{min} = maximum/minimum possible value of analog signal.

Encoding: We can choose binary values for each quantized levels.

Analog signal.



$$\frac{V_{max} + V_{min}}{2} = 4$$

4 v is a quantization level so it is actually midtread quantization.

$N = 3,\ 2^N = 8$

Midrise quantization

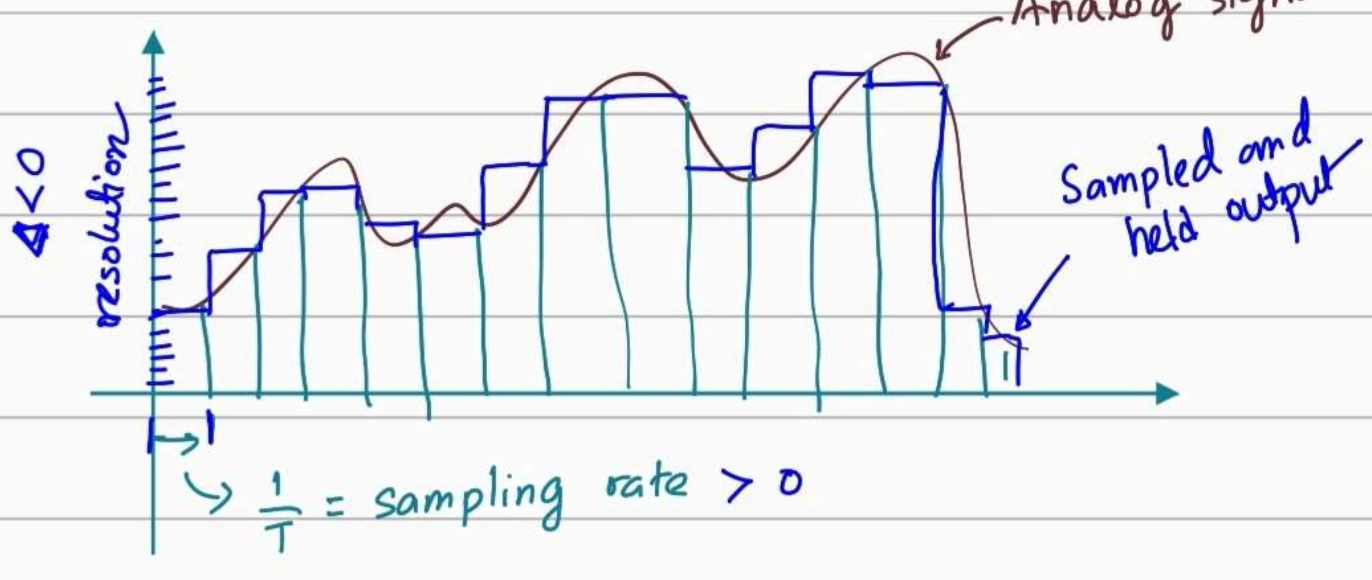
$V_{max} = 10V$, $V_{min} = 0V$

000 ←	0 – 1.25V	→	0.675
001	1.25 – 2.5	→	1.875
010	2.5 – 3.75	→	3.125
011	3.75 – 5.0	→	4.375
100	5.0 – 625	→	5.625
101	6.25 – 7.5	→	6.875
110	7.5 – 8.75	→	8.125
111	8.75 – 10.0	→	9.375

Δ 1.25

$$\frac{V_{min} + V_{max}}{2} = 5V$$

Voltage levels



Flash A/D Converter:

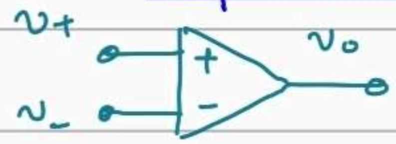
Ad. # This converter is very fast. It requires one clock cycle to convert the analog to digital data.

Dis. # It requires a lot component.

$N = 3. \; 2^N = 8$

Midrise quantization:

comparators



$v_+ > v_-$, v_o = High ✓

$v_+ < v_-$, v_o = low ✓

$V^+_{ref} = 9.375\,V$

$V^-_{ref} = -0.675\,V$

$I = \left(\frac{V^+_{ref} - V^-_{ref}}{8R}\right) = \frac{10}{8R}$

1.25V

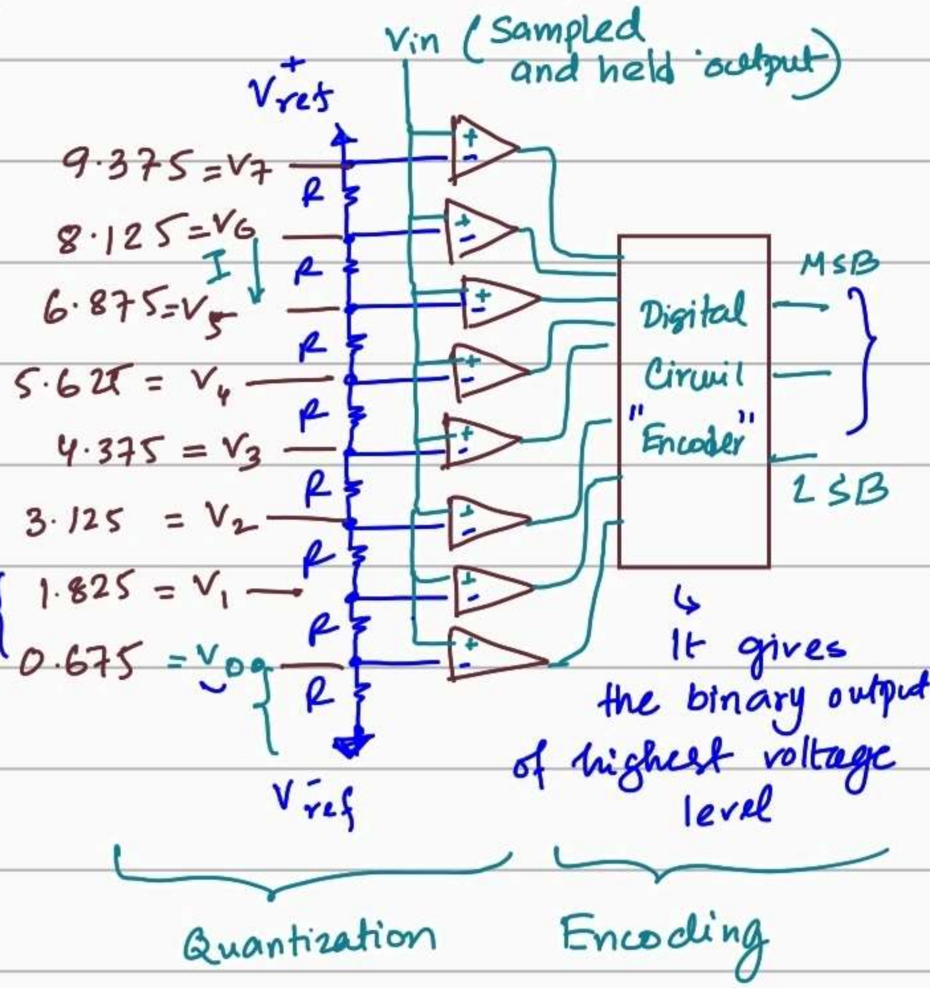
$IR = V_0 - V^-_{ref}$

$\Rightarrow V_0 = V^-_{ref} + IR$

$= -0.675 + \frac{10}{8}$

$= 0.675$

$V_1 = V_0 + IR = 1.825\,V$



Dual Slope converter:

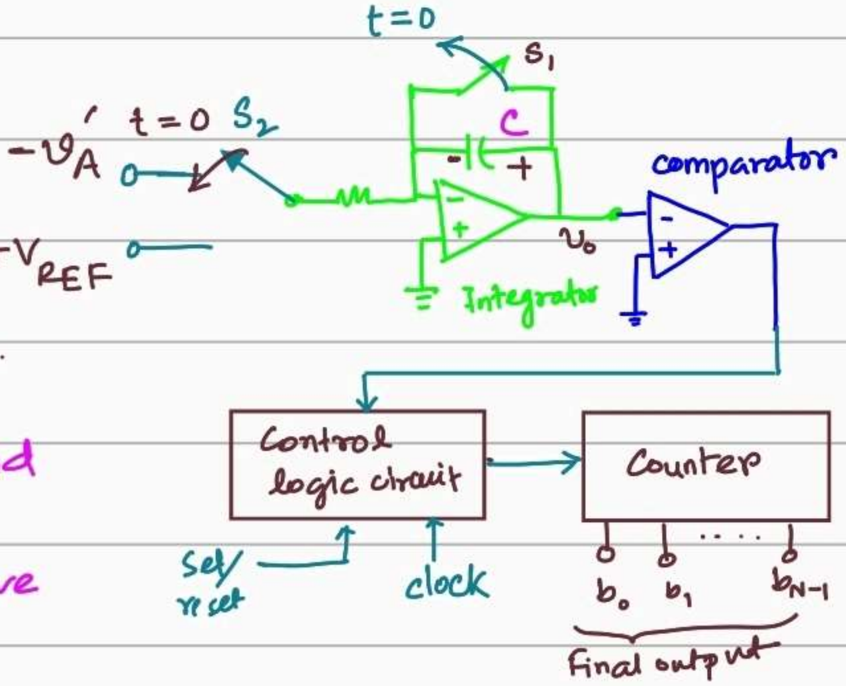
Adv: It requires small amount of circuit components. We can use many levels for quantization.

Disadvantage: Relatively slow.

Circuit:

v_A' = Sampled and held signal

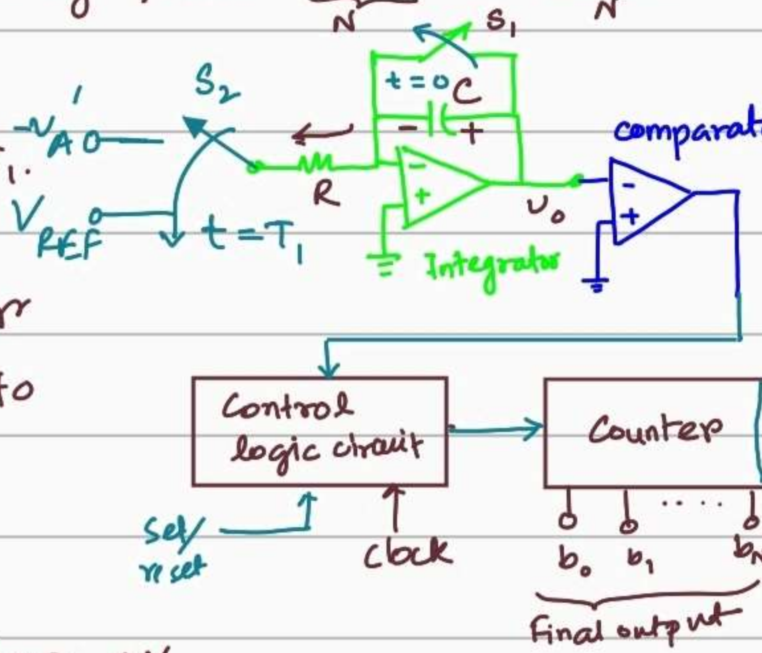
V_{REF} = preassigned value.



- (t < 0) S_1 is closed and S_2 is open.
  - \# Capacitor doesn't have any charge.

- t = 0, S_1 is open. S_2 is now connected to v_A'.
  capacitor is charging in a way that v_o increases.
  counter starts counting from $\underbrace{000..0}_{N}$ to $\underbrace{1111\,1}_{N}$.

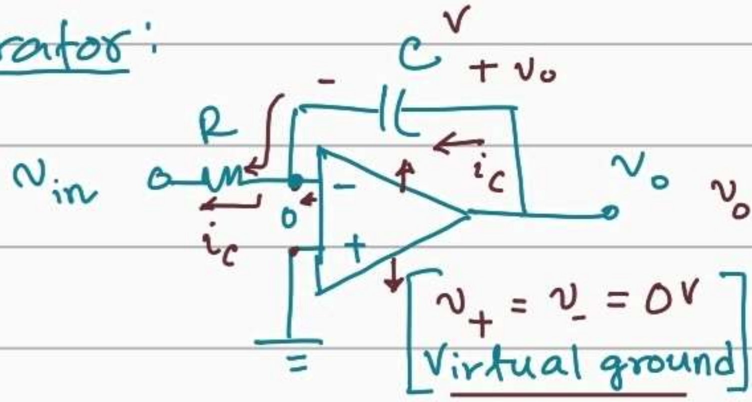
- $t \geq T_1$. Counter finishes counting from 0 to 2^N-1. at $t = T_1$.
  S_2 is now connected to V_{REF}. From then capacitor discharges and v_o starts to decline.



- $t = T_2$ (not fixed time)

v_o output level decreases below 0V.
Now comparator output changes from low to high.
At that moment control circuit stops the counter.
Then the output of the counter is the digital output we want.

Integrator:



Q = stored charge in capacitor.

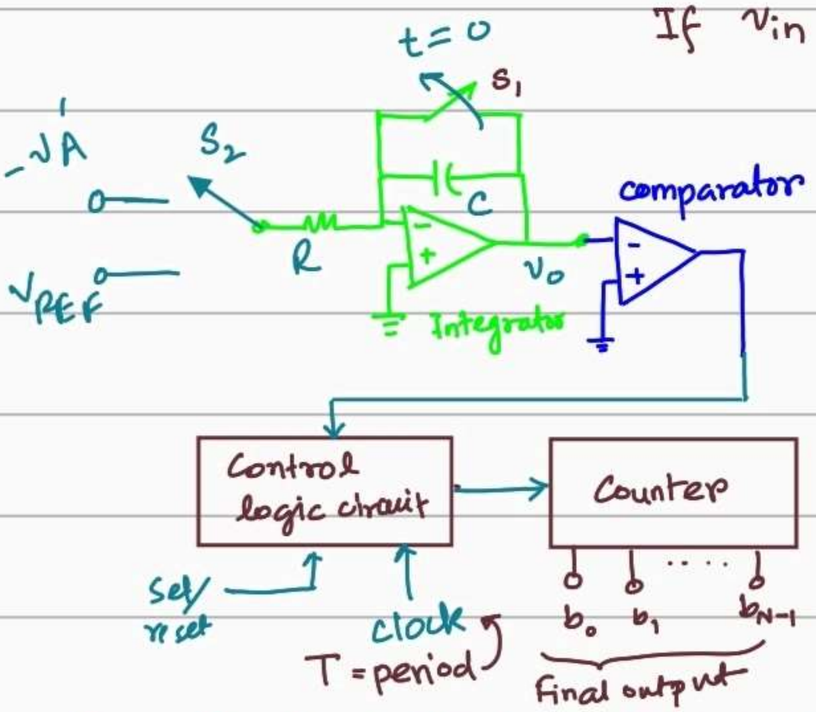
$v_o = V =$ voltage across the capacitor.

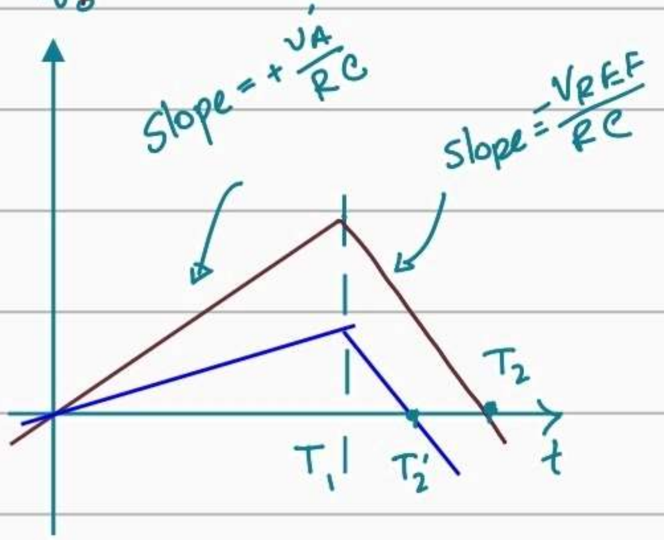
$Q = CV$

$$\therefore \frac{dQ}{dt} = \text{current through the capacitor}$$

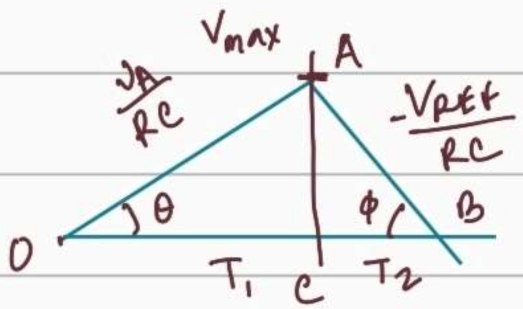
$$= C \cdot \frac{dV_o}{dt} = i_c = \frac{0 - v_{in}}{R} \Rightarrow \boxed{\frac{dV_o}{dt} = -\frac{v_{in}}{RC}}$$

If v_{in} is constant then $\frac{dv_o}{dt}$ is constant.





Say final output is binary representation of the number n.



$$\tan\theta = \frac{V_A}{RC} = \frac{AC}{OC} = \frac{V_{max}}{T_1}$$

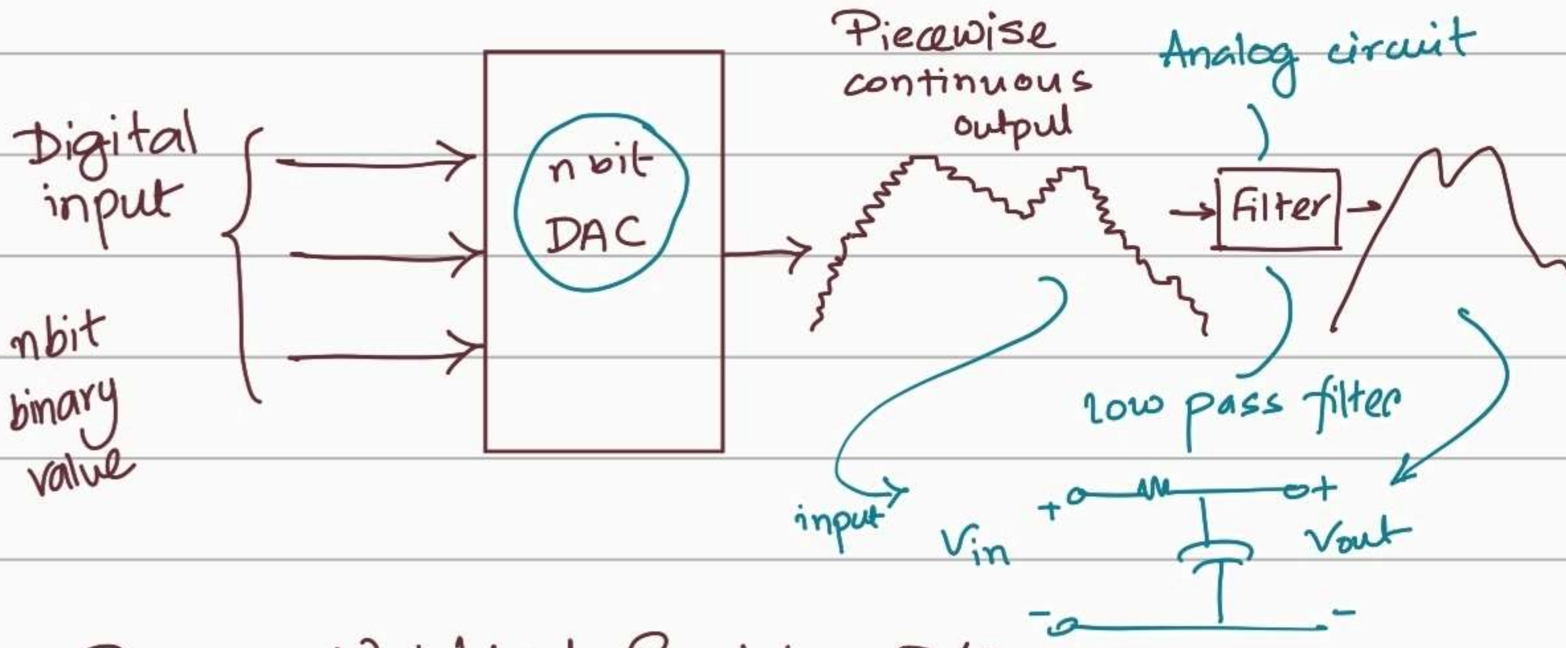
$$\tan\phi = \frac{V_{REF}}{RC} = \frac{AC}{BC} = \frac{V_{max}}{T_2}$$

$$\frac{V_{max}/T_1}{V_{max}/T_2} = \frac{V_A}{V_{REF}} = \frac{T_2}{T_1} = \frac{nT}{2^N T}$$

$$\boxed{n = V_A \frac{2^N}{V_{REF}}} \Leftarrow \boxed{V_A = \frac{n}{2^N} V_{REF}}$$

Lecture 17: D/A and A/D converter

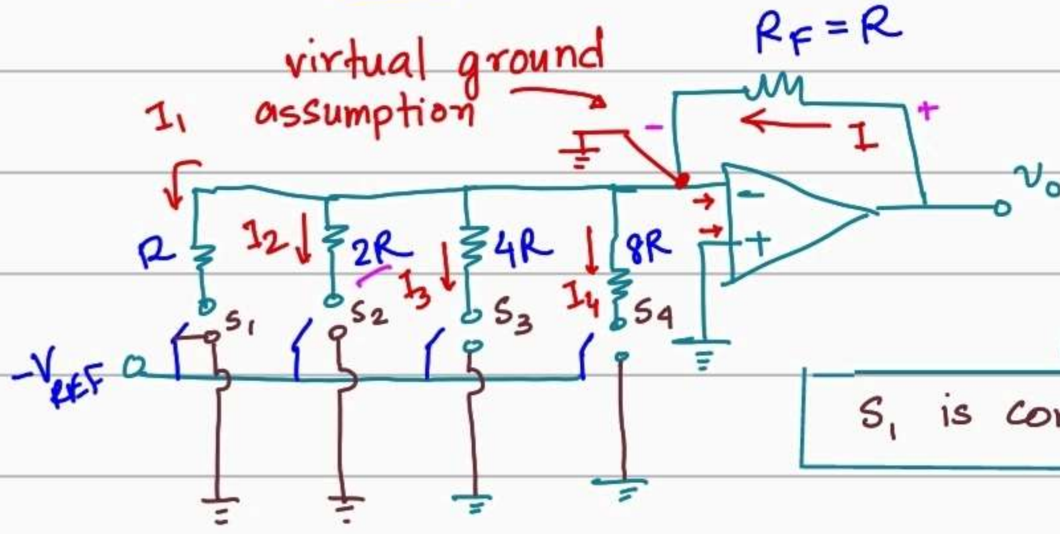
Digital to Analog Conversion



Binary Weighted Resistor D/A

Inverting summer

4 bit



Input: $b_1 b_2 b_3 b_4$
4 bit string

If b_1 is 1, S_1 is connected to the resistor, if b_1 is 0, S_1 is connected to ground.

Same rules applies to S_2, S_3 and S_4.

$$I = I_1 + I_2 + I_3 + I_4 = \frac{v_o - 0}{R_F} = \frac{v_o}{R_F}$$

	I_1	I_2	I_3	I_4
switch is connected to resistor	$\frac{0-(-V_{REF})}{R} = \frac{V_{REF}}{R}$	$\frac{V_{REF}}{2R}$	$\frac{V_{REF}}{4R}$	$\frac{V_{REF}}{8R}$
switch is connected to ground	0 because the path is open	0	0	0

$$\frac{v_o}{R_F} = b_1 \frac{V_{REF}}{R} + b_2 \frac{V_{REF}}{2R} + b_3 \frac{V_{REF}}{4R} + b_4 \frac{V_{REF}}{8R}$$

$$\Rightarrow \boxed{v_o = V_{REF}\left(b_1 + b_2/2 + b_3/4 + b_4/8\right)}$$