# Chapter 2

# DAC (Digital to Analog Conversion)

DAC is the process of converting a digital signal or bit stream to an analog signal. The whole DAC process can be summarized as follows:

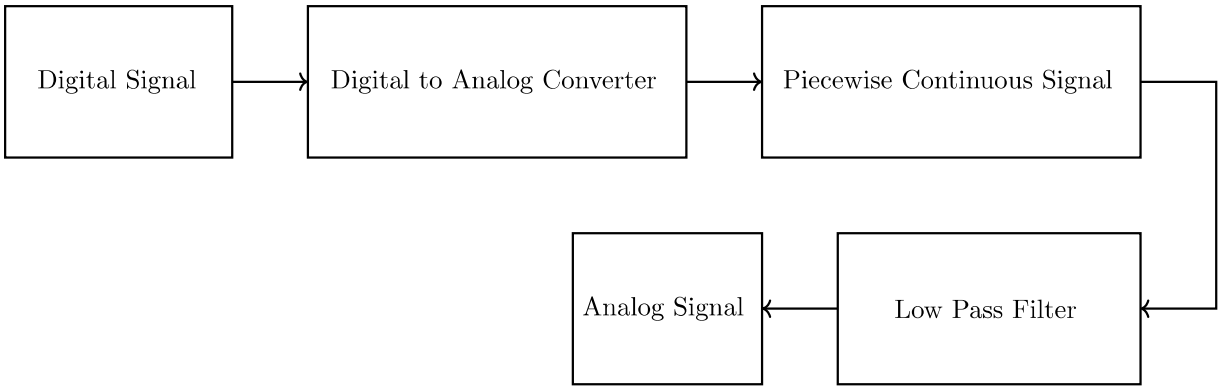



Figure 2.1: A flow chart of DAC process

As like ADC, we will be studying the Digital to Analog Converter in this course. We discuss the following two DACs.

## Binary Weighted Resistors DAC

A 3-bit Binary Weighted Resistors DAC looks like this:

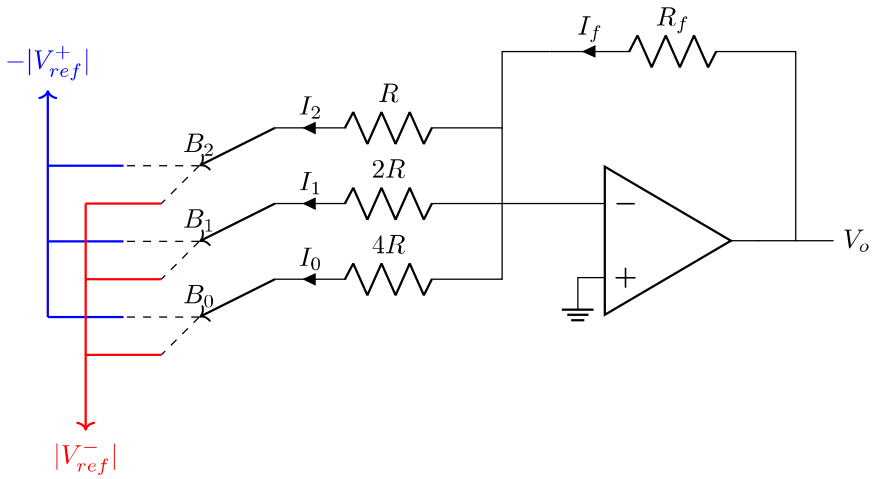



Figure 2.2: A 3-bit Binary Weighted Resistor DAC

As we can see, it is effectively a 3-input *inverting adder*, with different gains on each branches, and the input can switch between two separate reference voltages.

**Analysis of Operation:** The conversion from digital to analog follows a simple concept of binary to decimal number conversion. We know, that to convert a binary number to its decimal equivalent, we need to multiply each bit with the appropriate power of 2 and then sum the products. The circuit in figure 2.2, is implementing this through its input branches with successively doubled resistors. The switches of the input branches connect to the appropriate reference voltage according to the bit of the digital input signal they represent.

Here, $B_2$ is the MSB & $B_0$ is the LSB. Let the currents through the input branches be $I_2$, $I_1$ & $I_0$. While, the current through the feedback resistor, $R_f$ be $I_f$. As the Op Amp's input terminals are virtually shorted and the non-inverting terminal is grounded, voltage at the inverting terminal, $V_- = 0$ V. Applying KCL at $V_-$ and expressing the currents using Ohm's law,

$$I_f = I_2 + I_1 + I_0 \Rightarrow \frac{V_o - V_-}{R_f} = \frac{V_- - V_{B_2}}{R} + \frac{V_- - V_{B_1}}{2R} + \frac{V_- - V_{B_0}}{4R}$$

$$\Rightarrow V_0 = -\frac{R_f}{R}(V_{B_2} + \frac{V_{B_1}}{2} + \frac{V_{B_0}}{4})$$

As we can see, the contributions to the output voltage of the input branches doubles from LSB to MSB, just like in binary to decimal conversion.

Now, the switches at the inputs function like this— when the input bit is high, it connects to $-|V_{ref}^{+}|$, and when the bit is low, it connects to $|V_{ref}^{-}|$. The idea of two reference voltages for the

two bits (1 & 0) comes from the fact that, each bit represent a certain voltage. As the 3 input branches can all have either 1 or 0 as inputs, we can convert $2^3$ digital inputs to analog voltage ($V_o$). Well, the question is, how do we select these reference voltages?

Let's consider two extreme inputs two answer this. The lowest member of the possible $2^3$ input bit streams is the one with all bits set to 0, "000". So, all input branches will connect to $|V_{ref}^-|$. The output voltage for this case is,

$$V_{o_{000}} = -\frac{R_f}{R} \times |V_{ref}^-|(1 + \frac{1}{2} + \frac{1}{4}) = -\frac{R_f}{R} \times |V_{ref}^-| \times \frac{7}{4}$$

Similarly, the other extreme input is when all bits are set to 1, "111". The output voltage for this case can be found in a same manner,

$$V_{o_{111}} = -\frac{R_f}{R} \times -|V_{ref}^+| \times \frac{7}{4}$$

If we recall our knowledge on ADC, "000" was used to encode the lowest quantization level, and "111" for the highest level. Thus, we select reference voltages, feedback resistance & branch resistances in accordance with the highest & lowest quantization levels, such that $V_{o_{000}}$ & $V_{o_{111}}$ are equal to them. The outputs of the other inputs then automatically matches with the respective quantization levels.

Some important terminologies & facts of Binary Weighted Resistors DAC:

1. **LSB Voltage or Step Size:** LSB voltage is the output voltage when only the LSB is set to 1 and all other bits are set to 0.

$$V_{LSB} = V_{o_{001}} = -\frac{R_f}{R}(|V_{ref}^-| + \frac{|V_{ref}^-|}{2} + \frac{-|V_{ref}^+|}{4}) \tag{2.1}$$

   This matches the step size, since step size is the difference between two successive quantization levels. We see,

$$\Delta = V_{o_{001}} - V_{o_{000}} = -\frac{R_f}{R}\frac{-|V_{ref}^+| - |V_{ref}^-|}{4} = \frac{R_f}{R}\frac{|V_{ref}^+| + |V_{ref}^-|}{4} \tag{2.2}$$

2. This DAC only matches the quantization levels for an encoding using *mid-rise* quantization, since the step size is uniform throughout. Try it yourself and verify that any two successive input bit streams' output voltage differ by the same amount.

3. **MSB Voltage:** Just like LSB voltage, MSB voltage is the output voltage when only the MSB is set to 1.

$$V_{MSB} = V_{o_{100}} = -\frac{R_f}{R}(-|V_{ref}^+| + \frac{|V_{ref}^-}{2} + \frac{|V_{ref}^-|}{4}) \tag{2.3}$$

4. One of the disadvantages of Binary Weighted Resistors is that, a lot of different resistors are used. Hence, fluctuations in their values can cause errors in output voltage.

# R2R Ladder DAC

## Variant 1

To overcome the problem of too many different resistors of the previous DAC, we bring in the R2R Ladder. For a 3-bit input the circuit is shown below:

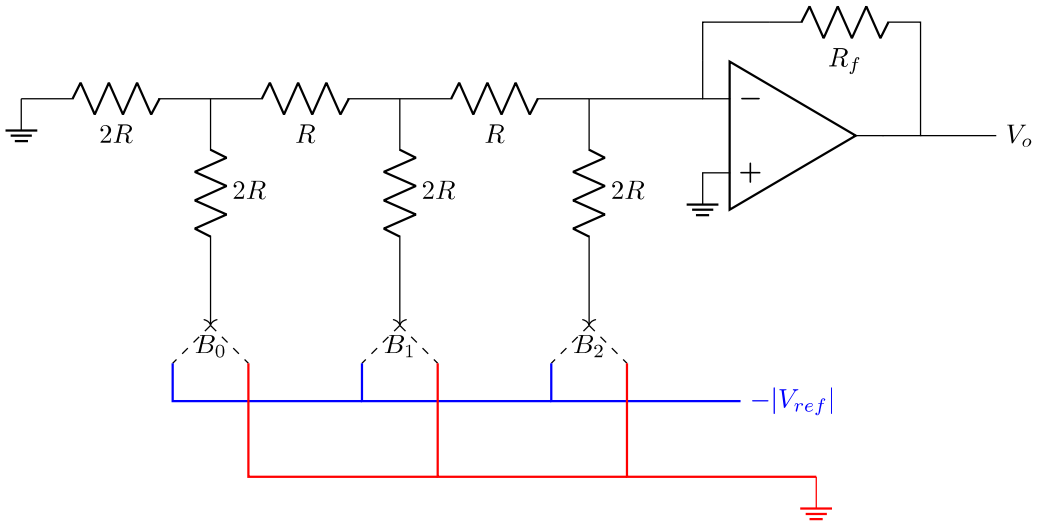



Figure 2.3: A 3-bit R2R Ladder DAC (Variant 1)

**Analysis of Operation:** A lot of things in figure 2.3 looks familiar, don't they? They function actually the same for this DAC too, as in Binary Weighted Resistors. The main difference here is that the input branches have *the same* resistance, 2R each. Also, there are resistors of value R in between input branches. Finally, after the LSB branch, the ladder ends with a 2R resistor, to the ground. The input branches are like the steps of the ladder like structure. Let's now get mathematical.

To determine the output voltage, we will first find the effects of each input bit branch to the output and then use *superposition* to get their combined effect. Let's start with $B_0$.

Consider the case when $B_0 = 1$, and the other two bits are 0. The $B_0$ switch connects to $-|V_{ref}|$, and the other two switches to the ground. Refer to figure 2.4. Since $V_- = 0$ V, the voltage across the 2R resistance in the $B_2$ branch is 0-0 = 0 V. Thus, no current will flow. Let's perform Node Analysis on nodes $n_1$ & $n_0$. For $n_0$,

$$\frac{V_{n_0} - (-|V_{ref}|)}{2R} + \frac{V_{n_0} - 0}{2R} + \frac{V_{n_0} - V_{n_1}}{R} = 0 \Rightarrow \frac{V_{n_0}}{2} + \frac{V_{n_0} + |V_{ref}|}{2} + V_{n_0} - V_{n_1} = 0$$

For $n_1$,

$$\frac{V_{n_1} - 0}{2R} + \frac{V_{n_1} - 0}{R} + \frac{V_{n_1} - V_{n_0}}{R} = 0 \Rightarrow \frac{V_{n_1}}{2} + V_{n_1} + V_{n_1} - V_{n_0} = 0$$

Solving the two equations, $V_{n_0} = -\frac{5}{16}|V_{ref}|$, $V_{n_1} = -\frac{1}{8}|V_{ref}|$

Now applying KCL at the inverting terminal,

$$\frac{V_o^0 - 0}{R_f} = \frac{0 - V_{n_1}}{R} \Rightarrow V_o^0 = R_f \times \frac{|V_{ref}|}{8R}$$

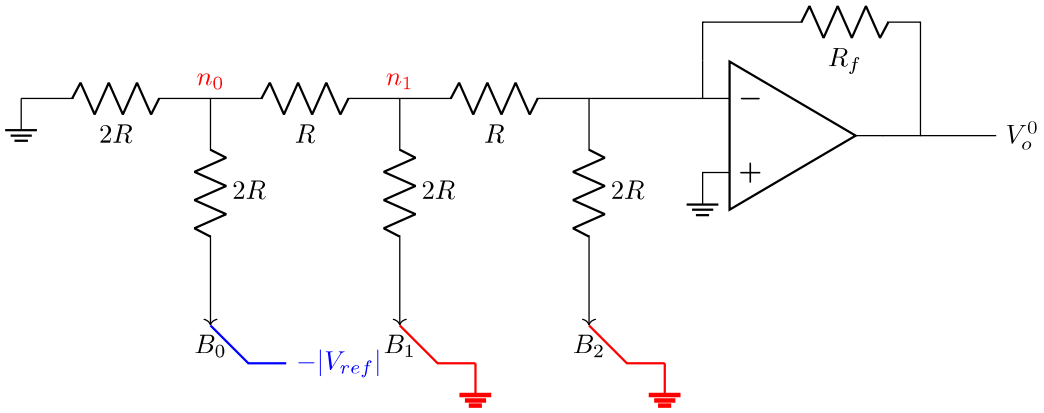



Figure 2.4: Case 001

Similarly for the case when only $B_1$ is 1:

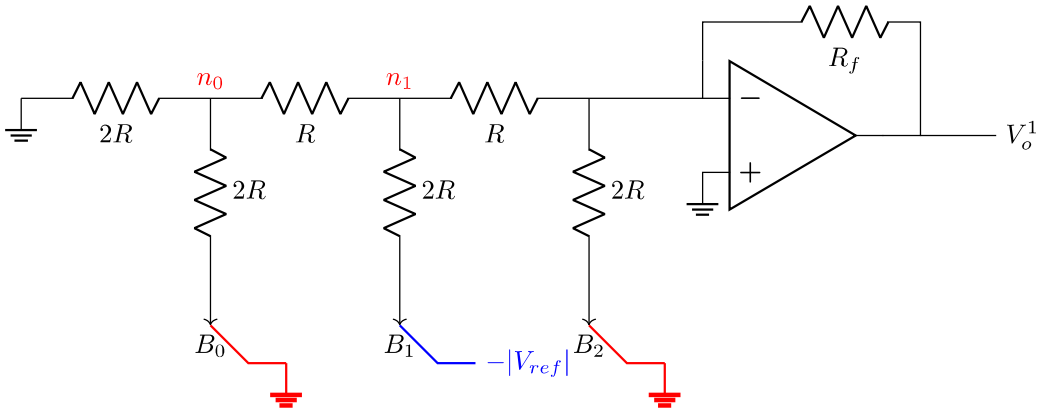



Figure 2.5: Case 010

Again, applying Node Analysis to $n_0$ & $n_1$ in figure 2.5, for $n_0$,

$$\frac{V_{n_0} - 0}{2R} \times 2 + \frac{V_{n_0} - V_{n_1}}{R} = 0$$

For $n_1$,

$$\frac{V_{n_1} - (-|V_{ref}|)}{2R} + \frac{V_{n_1} - 0}{R} + \frac{V_{n_1} - V_{n_0}}{R} = 0$$

Solving, $V_{n_0} = -\frac{1}{8}|V_{ref}|$, $V_{n_1} = -\frac{1}{4}|V_{ref}|$. Now, applying KCL at the inverting terminal,

$$\frac{V_o^1 - 0}{R_f} = \frac{0 - V_{n_1}}{R} \Rightarrow V_o^1 = R_f \times \frac{|V_{ref}|}{4}$$

Finally for the case when $B_2 = 1$:

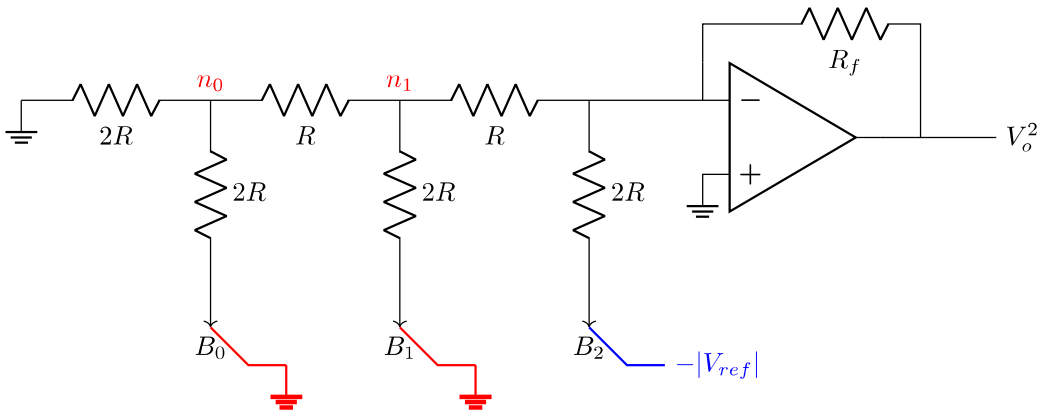



Figure 2.6: Case 100

Node Analysis gives,

$$\frac{V_{n_0} - 0}{2R} \times 2 + \frac{V_{n_0} - V_{n_1}}{R} = 0$$

$$\frac{V_{n_1} - V_{n_0}}{R} + \frac{V_{n_1} - 0}{2R} + \frac{V_{n_1} - 0}{R} = 0$$

Solving, $V_{n_0} = V_{n_1} = 0$. Now applying KCL at the inverting terminal,

$$\frac{V_o^2 - 0}{R_f} = \frac{0 - (-|V_{ref}|)}{2R} \Rightarrow V_o^2 = R_f \times \frac{|V_{ref}|}{2R}$$

One thing to note for this case is that the current through the $B_2$ branch is not 0 this time since the $B_2$ switch is connected to $-|V_{ref}|$ instead of ground.

Let's now combine the results using superposition,

$$V_o = V_o^0 + V_o^1 + V_o^2 = \frac{R_f|V_{ref}|}{2R}(B_2 + \frac{B_1}{2} + \frac{B_0}{4})$$

As we can see, the effect of doubled weightage for higher order bits is also effective for this DAC circuit. So, it follows the similar concept of binary to decimal conversion.

### Variant 2

Another possible variant of the R2R DAC is shown below:

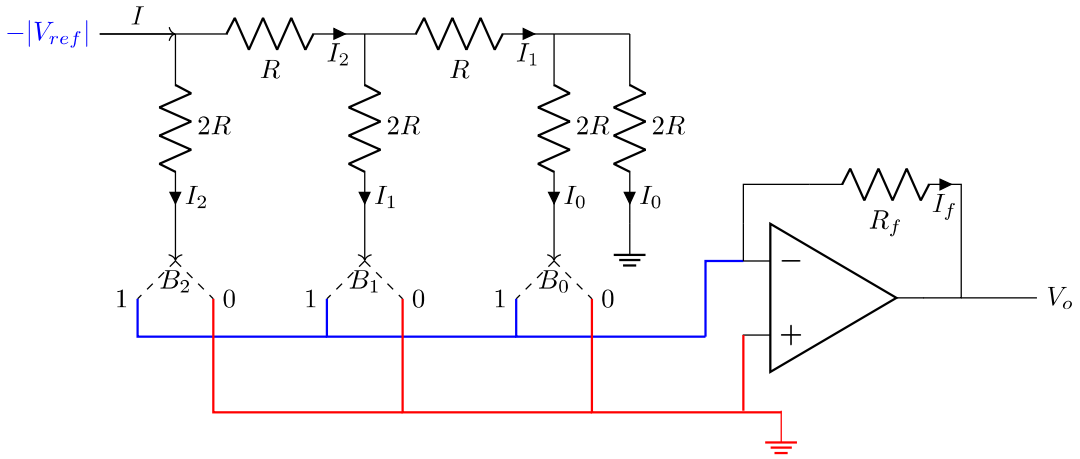



Figure 2.7: A 3-bit R2R Ladder DAC (Variant 2)

One of the main differences of this variant is that the switches connect to ground for both bits (1 & 0). However, these two grounds connect to the two different terminals of the Op Amp. The reference voltage this time is applied in between an R & a 2R valued resistance.

**Analysis of Operation:** Since the input branches & the rightmost 2R resistance are always grounded at one end irrespective of the inputs to the switches— we can derive the configuration of the resistances in the ladder. Let's start with the rightmost two 2R resistances. They are in parallel combination and their equivalent resistance (let $R_{P_1}$) is R. Now, $R_{P_1}$ is in series with the rightmost R. Their equivalent will be R+R=2R (let $R_{S_1}$). $R_{S_2}$ is in parallel with the 2R resistance of input branch $B_1$. Their equivalent will again be R (let $R_{P_2}$). The leftmost R & $R_{P_2}$ are in series. For the same reason, their equivalent (let $R_{S_2}$) will be 2R. Finally, $R_{S_2}$ & the leftmost 2R (of branch $B_2$) are in parallel.

Now let's verify the currents marked on different branches. We start by assigning notations for the currents of the input branches ($I_0$ to $I_2$). Since the two rightmost 2R resistances are in parallel, they will get the same currents through them ($I_0$). For this very logic the current through ($R$+$R_{S_1}$) will also be $I_1$. And finally, the current through ($R$+$R_{S_2}$) will be $I_2$. Tracing back from the rightmost node using KCL, $I_1 = I_0 + I_0 = 2I_0$. Then, $I_2 = I_1 + I_1 = 2I_1 = 4I_0$. Finally, $I = I_2 + I_2 = 2I_2 = 4I_1 = 8I_0$.

Consider the case when all input bits are high. All the input switches are connected to the inverting terminal of the Op Amp. So, applying KCL at this terminal,

$$I_f = I_2 + I_1 + I_0 = I_2 + \frac{I_2}{2} + \frac{I_2}{4} = \frac{-|V_{ref}| - 0}{2R}(1 + \frac{1}{2} + \frac{1}{4})$$

But $I_f = \frac{0-V_o}{R_f}$. So,

$$-\frac{V_o}{R_f} = -\frac{|V_{ref}|}{2R}(1 + \frac{1}{2} + \frac{1}{4}) \Rightarrow V_o = R_f \frac{|V_{ref}|}{2R}(1 + \frac{1}{2} + \frac{1}{4})$$

Generalizing for both the bits,

$$V_o = R_f \frac{|V_{ref}|}{2R}(B_2 + \frac{B_1}{2} + \frac{B_0}{4}) \tag{2.4}$$

So, we got the same formula for the output voltage. The difference is thus in the structure, not the result.

Important terminologies & facts of R2R Ladder DAC:

1. Uses only two values of resistors— easy and accurate fabrication is possible.
2. Easily scalable to desired number of bits.
3. Unable to convert to bipolar analog signals. Thus requires offset addition after conversion, to achieve bipolarity.
4. **MSB & LSB Voltages:**

$$V_{MSB} = V_{o_{100}} = \frac{R_f|V_{ref}|}{2R}(1 + 0 + 0) = \frac{R_f|V_{ref}|}{2R} \tag{2.5}$$

$$V_{LSB} = V_{o_{001}} = \frac{R_f|V_{ref}|}{2R}(0 + 0 + \frac{1}{4}) = \frac{R_f|V_{ref}|}{8R} \tag{2.6}$$

   The LSB voltage is also the *step size* or $\Delta$.

5. One disadvantage of *variant 2* is that there is always a current flowing through the resistors even if the input bits are 0. This causes more power dissipation.

# Problems Roster

## Problem 1:

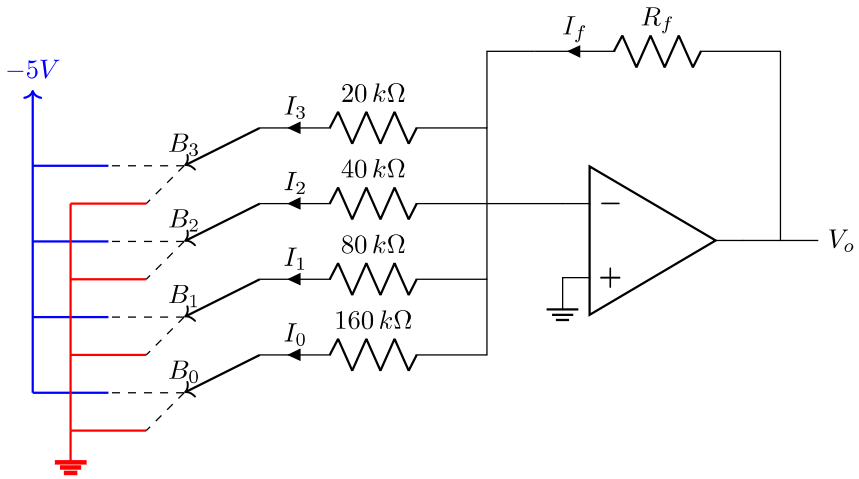



Figure 2.8: A 3-bit Binary Weighted Resistor DAC

For the 4-bit DAC circuit shown in figure 2.8, assume $R_f = 5\,k\Omega$

| | |
|---|---|
| (a) | Determine the output voltage for the inputs— (i) 1100 (ii) 1010. |
| (b) | Find the *MSB* & *LSB* voltages. What is the maximum possible output from the DAC? |
| (c) | What are the values of the input branch currents when they conduct? |

## Solution:

(a)

(i)

$$V_{o_{1100}} = -\frac{R_f}{R}(-|V_{ref}^{+}| + \frac{-|V_{ref}^{+}|}{2} + \frac{|V_{ref}|^{-}}{4} + \frac{|V_{ref}|^{-}}{8}) = -\frac{5}{20}(-5 + \frac{-5}{2} + \frac{0}{4} + \frac{0}{8}) = 1.875\,V$$

(ii)

$$V_{o_{1010}} = -\frac{5}{20}(-5 + 0 + \frac{-5}{4} + 0) = 1.5625\,V$$

(b)

$$V_{MSB} = V_{o_{1000}} = -\frac{5}{20}(-5 + 0 + 0 + 0) = 1.25\,V$$

$$V_{LSB} = V_{o_{0001}} = -\frac{5}{20}(0 + 0 + 0 + \frac{-5}{8}) = 0.15625\,V$$

(c) The input branches conduct whenever their respective bits are "1". Thus,

$$I_3 = \frac{0-(-5)}{20} = 0.25\,mA$$

$$I_2 = \frac{0-(-5)}{40} = 0.125\,mA$$

$$I_1 = \frac{0-(-5)}{80} = 0.0625\,mA$$

$$I_0 = \frac{0-(-5)}{160} = 0.03125\,mA$$

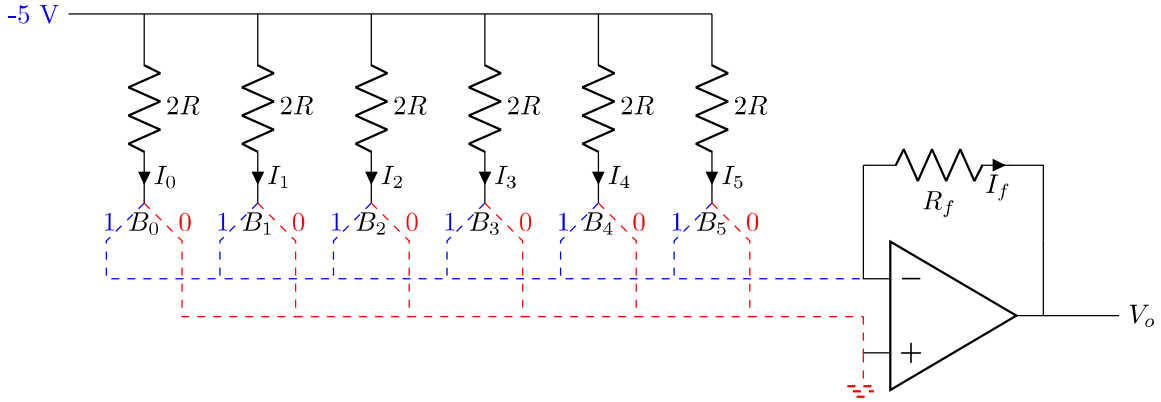
**Problem 2:**

Consider a 6-bit R2R DAC (variant 2). Assume $R_f = R = 5\,k\Omega$ & $|V_{ref}|$=5 V.

| | |
|---|---|
| (a) | Draw the DAC circuit with proper labelings. |
| (b) | Find the input branch currents $I_0$ to $I_5$. |
| (c) | What is the output for the input "010011"? What is the change in output voltage if the input changes from "101010" to "010101". |

**Solution:**

(a)




(b)

$$I_5 = \frac{0-(-5)}{2\times 5} = 0.5\,mA$$

$$I_4 = \frac{1}{2}I_5 = 0.25\,mA$$

$$I_3 = \frac{1}{2} I_4 = 0.125\, mA$$

$$I_2 = \frac{1}{2} I_3 = 0.0625\, mA$$

$$I_1 = \frac{1}{2} I_2 = 0.03125\, mA$$

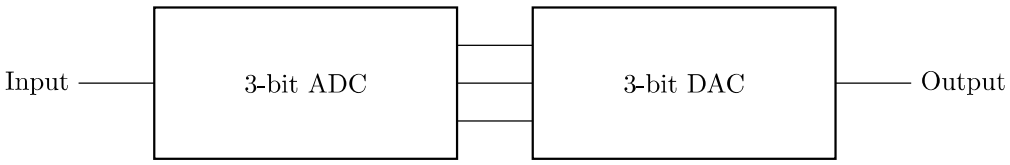
$$I_0 = \frac{1}{2} I_1 = 0.15625\, mA$$

(c)

$$V_{o_{010011}} = \frac{R_f |V_{ref}|}{2R}(0 + \frac{1}{2} + 0 + 0 + \frac{1}{16} + \frac{1}{32}) = \frac{5 \times 5}{2 \times 5} \times \frac{19}{32} = 1.484375\, V$$

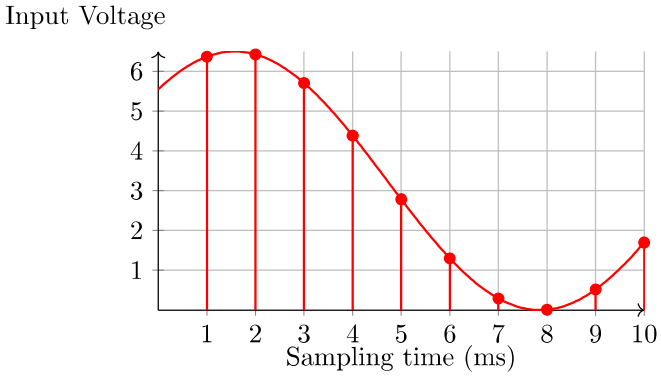
$$\Delta V_o = V_{o_{101010}} - V_{o_{010101}} = \frac{R_f |V_{ref}|}{2R}[(1+0+\frac{1}{4}+0+\frac{1}{16}+0)-(0+\frac{1}{2}+0+\frac{1}{8}+0+\frac{1}{32})] = \frac{5 \times 5}{2 \times 5} \times \frac{21}{32} = 1.640625\, V$$

**Problem 3:**




| ADC Input Voltage | Encoding | DAC Output Voltage |
|---|---|---|
| 0-1 | 000 | 0.5 |
| 1-2 | 001 | 1.5 |
| 2-3 | 010 | 2.5 |
| 3-4 | 011 | 3.5 |
| 4-5 | 100 | 4.5 |
| 5-6 | 101 | 5.5 |
| 6-7 | 110 | 6.5 |
| 7-8 | 111 | 7.5 |

| | |
|---|---|
| (a) | For the following input waveshape, draw the reconstructed output by the DAC. The sampling instances are marked on the input waveshape. |
| (b) | Comment on the quality of the reconstructed signal and how the quality would be affected if additional bits were used for both the ADC and DAC. |

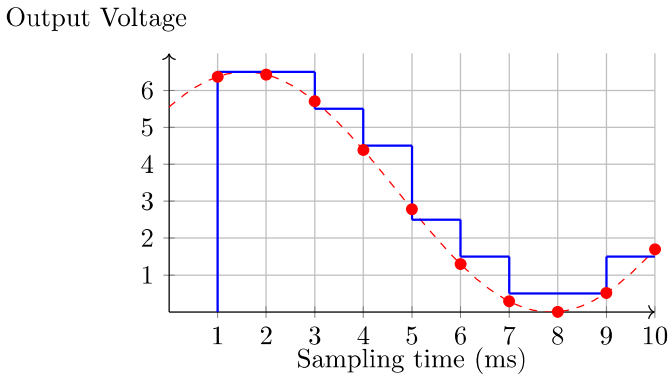



**Solution:**

(a) Using the table given, let's first find the output voltages for the sampled inputs.

| Sampling Instances | Sampled Input | Encoding | DAC Output Voltage |
|---|---|---|---|
| 1 | 6.3 | 110 | 6.5 |
| 2 | 6.4 | 110 | 6.5 |
| 3 | 5.7 | 101 | 5.5 |
| 4 | 4.4 | 100 | 4.5 |
| 5 | 2.8 | 010 | 2.5 |
| 6 | 1.3 | 001 | 1.5 |
| 7 | 0.3 | 000 | 0.5 |
| 8 | 0 | 000 | 0.5 |
| 9 | 0.5 | 000 | 0.5 |
| 10 | 1.7 | 001 | 1.5 |

Reconstructed Signal (in blue):




(b) Reconstructed signal roughly estimates the original input, and the quality is not very good.

Using higher number of bits for both the ADC and DAC will give a better voltage resolution. The reconstructed voltage levels would be closer to that of the originally sampled value.