

MULTIVIBRATOR

Multivibrators:

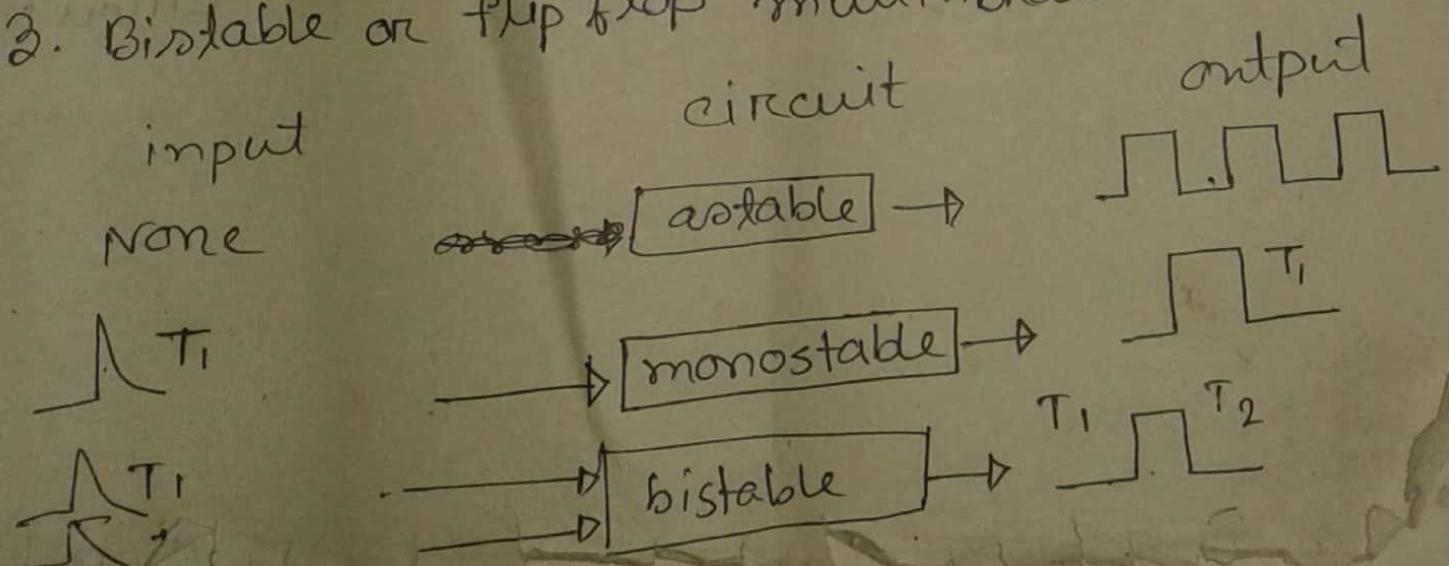
A **electronic** circuit that generates **square** waves (or other **non** sinusoidal such as rectangular, sawtooth waves) known as multivibrators.

The name multivibrator is derived from the fact that a **square wave** actually consists of a large number of **sinusoidal** of different frequencies.

It is basically two stage amplifier with output of one is feedback, to the input of other.

Depending upon the manner in which the two stages interchange their wa states,

1. AStable or free running multivibrator
2. monostable or one shot multivibrator.
3. Bistable or flip flop multivibrator.



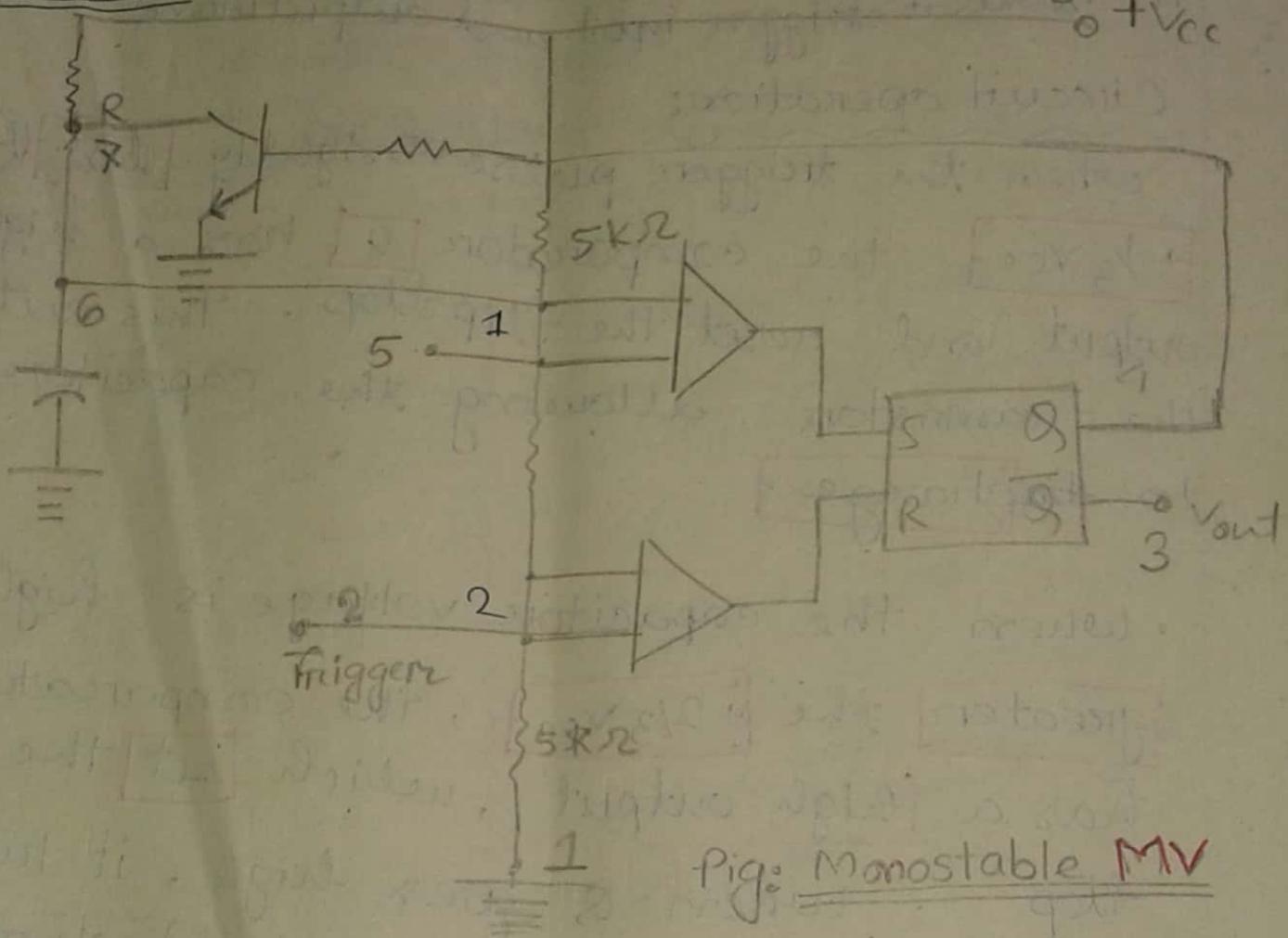
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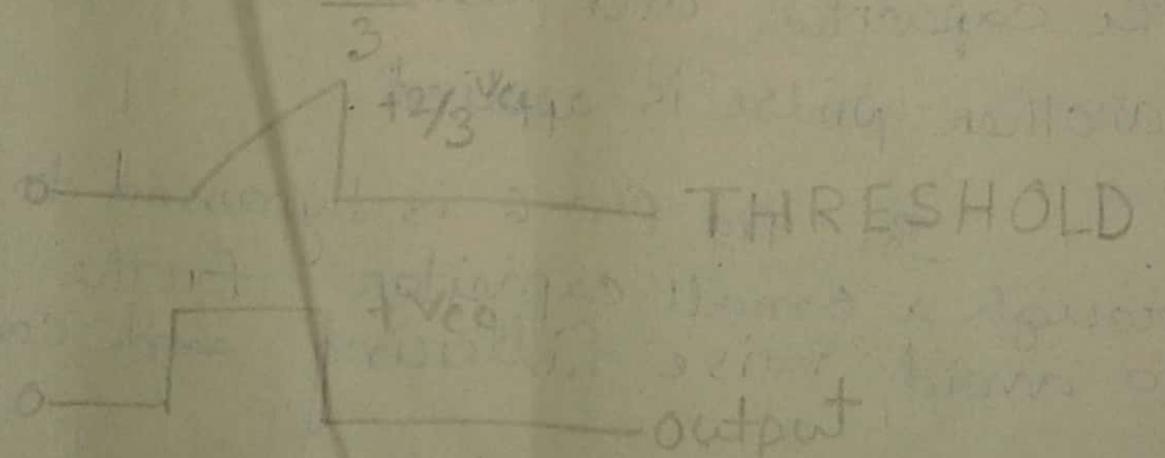
Comparison between three types of multivibrator

	Astable	Monostable	Bistable
Absolute stable State	has no absolute stable state	has one absolute stable state	has two stable state
Quasi stable state	has two quasi stable state	has one quasi stable state	has no quasi stable state
Triggering	It doesn't need any triggering	Needs triggering to go back to its original state	Needs triggering
Uses	It is used as a source of clock pulse in sequential circuit	It is used to generate new pulses and regenerate old and worn out pulses	It is used in timing circuit as a frequency driver. Also used in computer memory circuit

(1) # Draw and explain Astable and monostable MV by using 555 IC
monostable



+V_{CC} Trigger i.e. (trigger input)



Output

(threshold output wave)

fig(a) shows the 555 timer connected for monostable operation.

(b) shows its IC connection

(c) shows its trigger input and output wave.

Circuit operation:

when the trigger pulse is slightly less than $\frac{1}{3} V_{cc}$ the comparator 2 has a high output and reset the flip flop. This cuts off the transistor, allowing the capacitor to ~~discharge~~.

when the capacitor voltage is highly greater $\frac{2}{3} V_{cc}$, the comparator 1 has a high output, which set the flip flop. When Q goes high, it turns on transistor. This quickly discharge the capacitor and remain like this until another pulse is applied.

In fig pin 6 is bypassed to ground through a small capacitor for the to avoid noise filtering and control voltage.

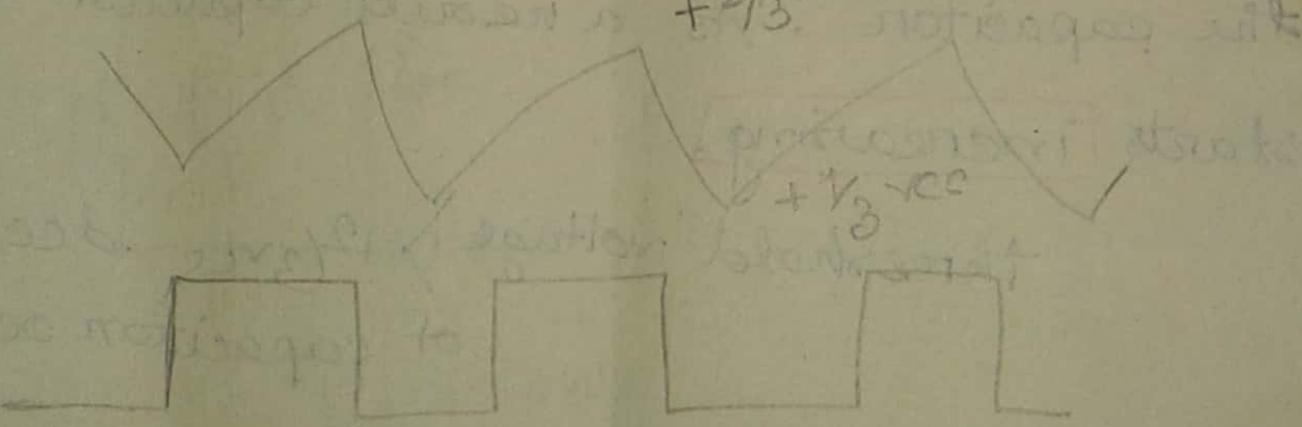
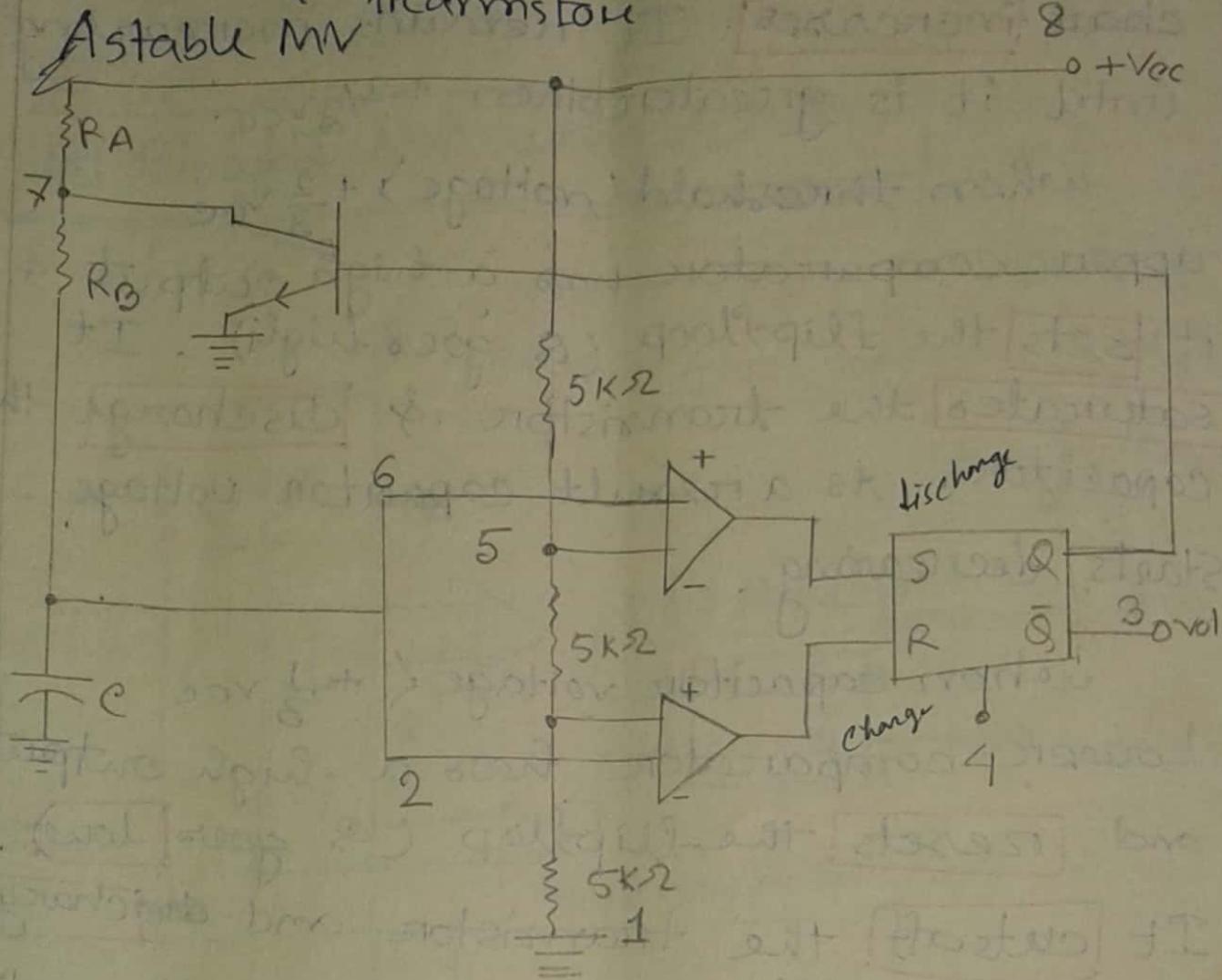
To avoid accidental reset, pin 4 is usually tied to the supply voltage.

Mainly we make astable mv by using

- * 555 IC timer

- * Transistor

Astable MV



Circuit operation:

- when θ is low, transistor is cut off & capacitor is charged.
 - If capacitor charges, threshold voltage increases. It remains increasing until it is greater than $+ \frac{2}{3} V_{cc}$.
- when threshold voltage $> + \frac{2}{3} V_{cc}$

upper comparator has a high output & it sets the flip-flop (θ goes high). It saturates the transistor & discharges the capacitor. As a result capacitor voltage starts decreasing.

when capacitor voltage $< + \frac{1}{3} V_{cc}$

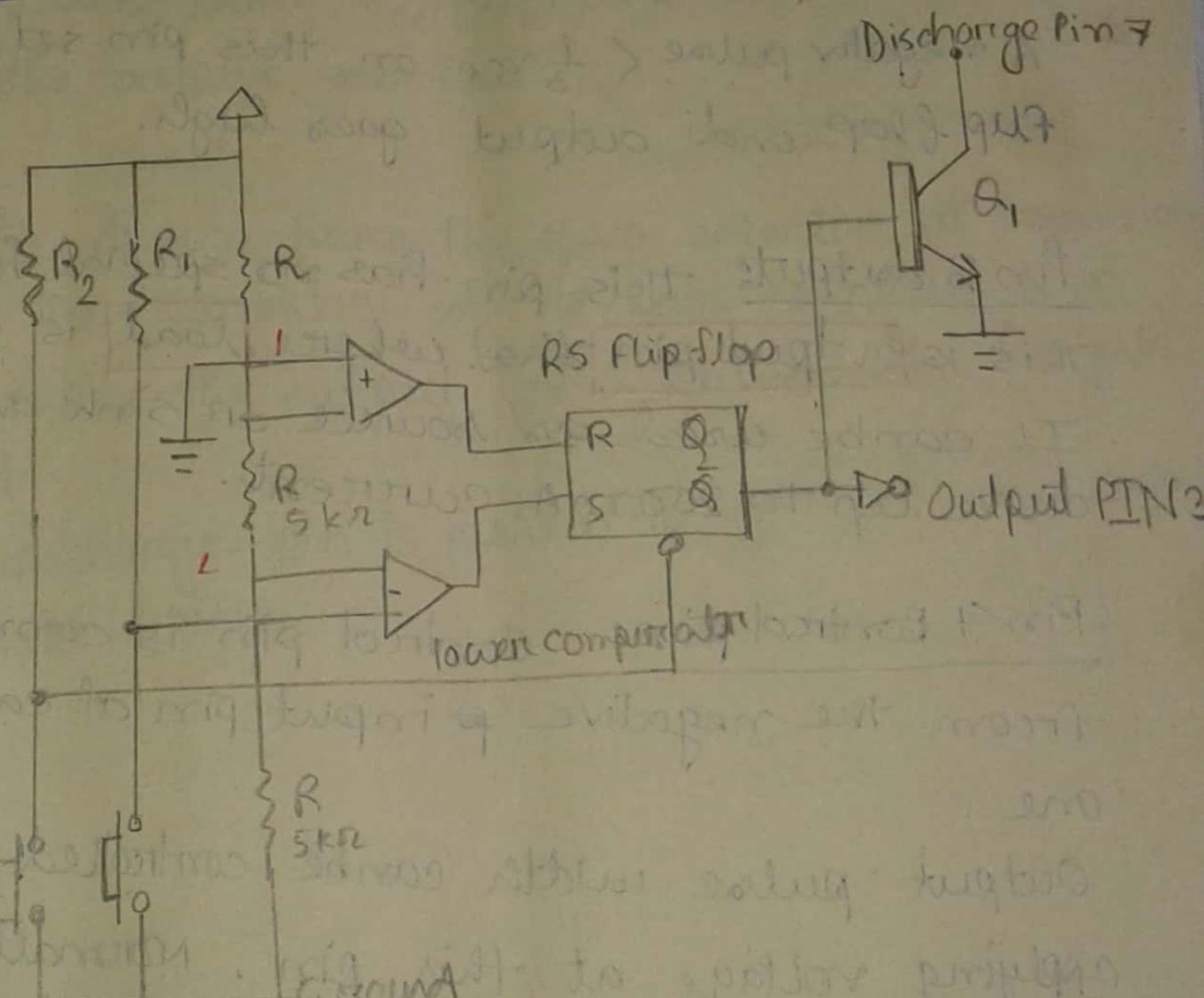
lower comparator has a high output and resets the flip-flop (θ goes low). It cuts off the transistor and ~~discharges~~ the capacitor. As a result capacitor voltage starts increasing.

threshold voltage $> + \frac{2}{3} V_{cc}$. decreasing of capacitor occurs

threshold voltage $> + \frac{1}{3} V_{cc}$ & increasing of capacitor occurs.

thus for once Q goes low & after a interval it goes high. As a result no stable state is found & for this, it is called -Astable multivibrator.

Bistable MV using 555 IC



PIN 1 Ground: This pin is should be connected to ground.

PIN 2 Trigger:

Trigger pin is dragged from the negative input of comparator two.

The lower comparator is connected to Set pin of flip-flop.

A negative pulse $< \frac{1}{3} V_{CC}$ on this pin set the flip flop and output goes high.

Pin 3 outputs: this pin has no special function - this is output pin where load is connected

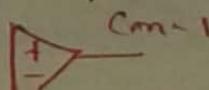
It can be used as source or sink and drive up to 200mA current.

Pin 4 Control pin: Control pin is connected from the negative ~~pin~~ input pin of comparator one.

Output pulse width can be controlled by applying voltage at this pin. Normally this pin is pulled down with capacitor to avoid unwanted noise interference with the working

Pin 6: Threshold: Threshold pin voltage determines when to reset the flip flop in the timer.

The threshold pin is drawn from positive input of upper comparator.



If the control pin is open, then a voltage equal to or greater than $V_{cc} (4_3)$ will reset the flip flop so, the output goes low.

Pin 7: drawn from the open collector of transistor since the transistor got its base connected to \bar{Q} whenever the output goes low or the FF gets reset.

The discharge pin is pulled to ground and capacitor discharges.

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Make a voltage controlled oscillator (VCO) by using 555 IC.

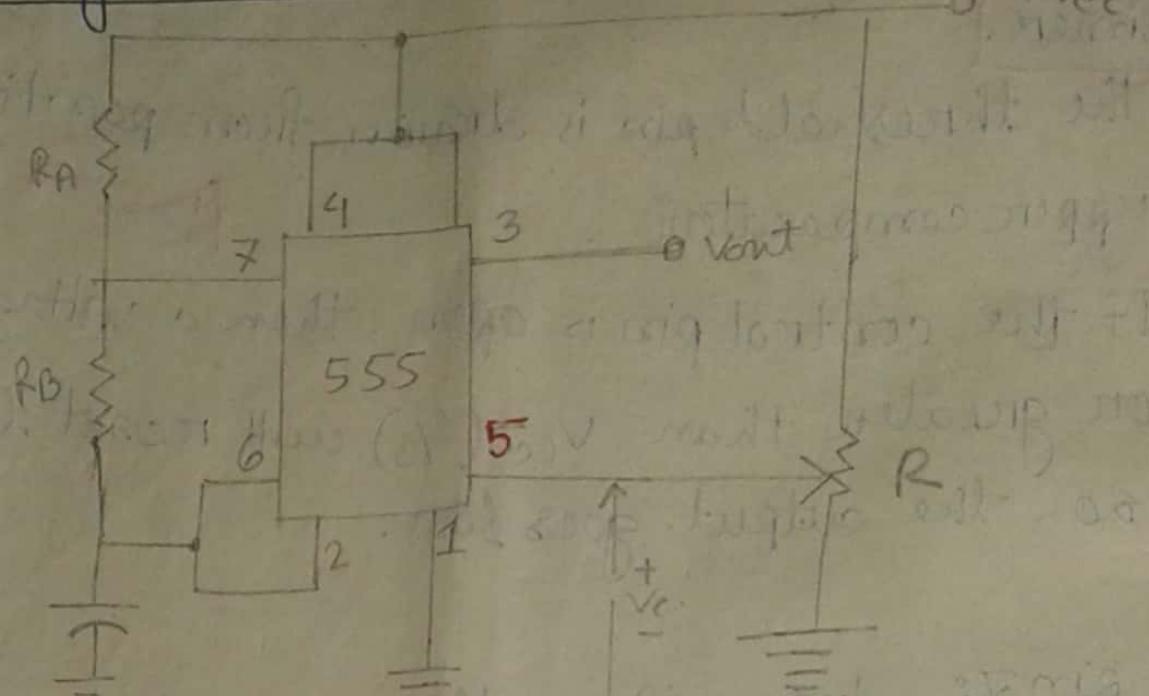


Fig shows a voltage controlled oscillator (VCO) one application for a 555 timer.

This circuit is sometimes called a voltage to frequency converter because an input voltage can change the output frequency.

In a 555 timer, Pin 5 (control) connects to the **inverting** ~~voltage~~ divider input of the **upper** comparator.

Normally, the control voltage is $\frac{2}{3}V_{cc}$ because of the internal voltage dividers.

By applying voltage in control pin, we can override the internal voltage.

In this case, voltage across timing capacitor is varies from $+V_{control}/2$ and $+V_{control}$. If we increase $+V_{control}$, it takes the capacitor longer to charge and discharge, therefore, the frequency decreases. As a result, we can change the frequency of the circuit by varying the control voltage.

By using two npn transistors make an astable my explain it.

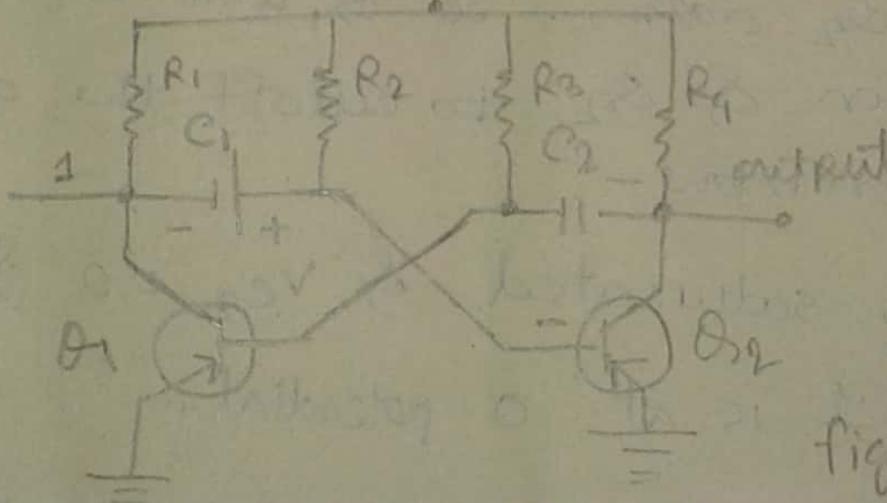


fig: Astable

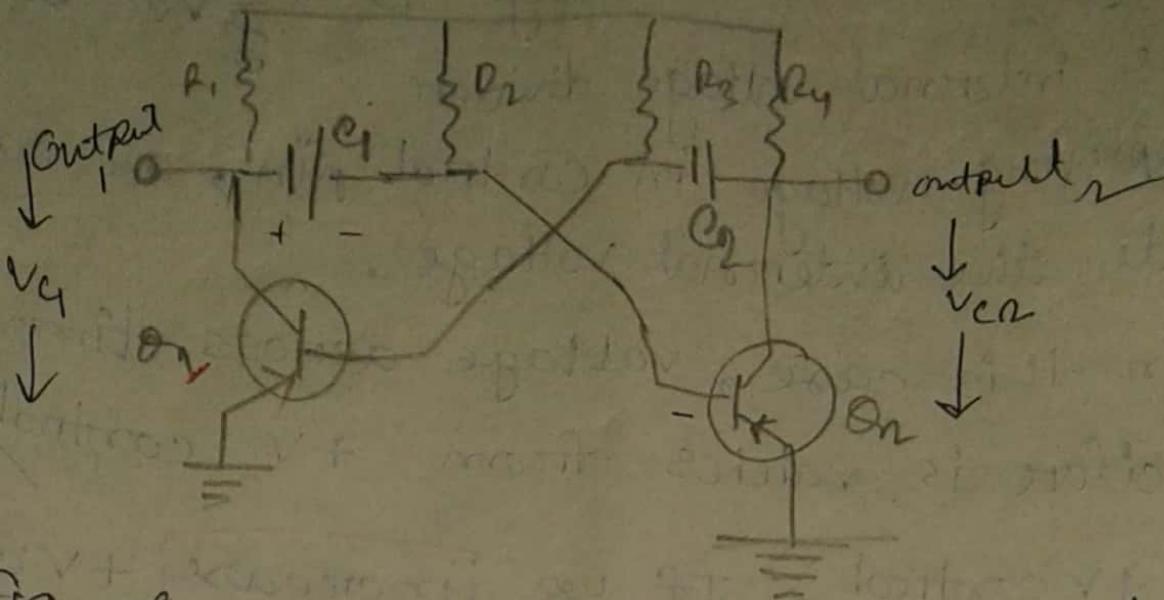


fig shows an astable multivibrator with two npn transistors.

The transistor Q_1 is forward bias by V_{cc} and R_1 and Q_2 is forward bias by V_{cc} & R_2 .

Q_1 and Q_2 are determined by R_1 and R_2

Together with V_{cc} .

when switches on, one of the transistors will start conducting before the other does. suppose that Q_1 starts conducting before Q_2 does. So, Q_1 will driven the saturation & Q_2 to cutoff the operation is given below-

- Q_1 is saturated & $V_{c2} = 0$ & output 1 is at 0 potential.

- Q_1 is cutoff & 2 is at V_{CC}

- C_1 charges towards V_{CC} .

✓ when voltage across $C_1 > 0.7V$, Q_1 is saturated.

Q_1 is saturated

→ when Q_1 is saturated, 2 is at 0 potential.

→ Q_2 is cutoff & 1 is at V_{CC} .

→ C_2 charges towards V_{CC} .

✓ when voltage across $C_2 > 0.7V$, Q_2 is saturated.

In this way, the whole circuit is repeated.

Q# For a 555 Astable timer circuits it is impossible to make the duty cycle 50%. why?

We know,

$$\text{duty cycle} = \frac{\omega}{T} \times 100\%$$

$$= \frac{\text{charging time constant}}{\text{charging & discharging time constant}} \times 100\%$$

To get 50% duty cycle, we need $\frac{\text{charging time constant}}{\text{discharging time constant}} = 1$

$$\left\{ \begin{array}{l} \text{we need } D = \frac{\omega}{T} = \frac{1}{2} \\ \text{or charging time constant} = \text{discharging time constant.} \end{array} \right.$$

But it is impossible, because, in a Astable circuit discharging time constant is less than charging time constant.

$$\text{Again, } D = \frac{R_A + R_B}{R_A + 2R_B} \times 100\%$$

Here, D will be 50% when $R_A = 0$

If $R_A = 0$ then the transistor may be damaged by V_{CC} . So, it is impossible for

astable to cut to make duty cycle 50%.

- Q) # By using two N-P-N transistor, draw a monostable MV.

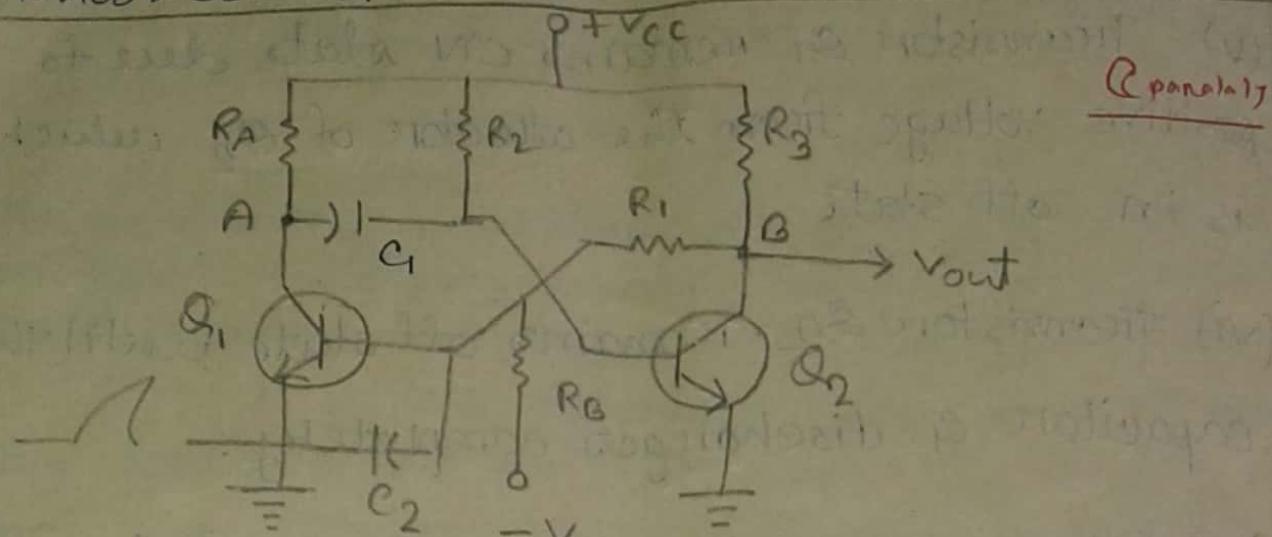


fig: Monostable MV using two N-P-N transistors.

when the circuit is switched on, transistor

- (i) Q_1 will be off and Q_2 will be on.
- (ii) capacitor C_1 gets charged during this state.
- (iii) when a positive trigger is applied to the base to transistor Q_1 , it turns on, which turns off the transistor Q_2 . due to the negative voltage from the

capacitor C_1 .

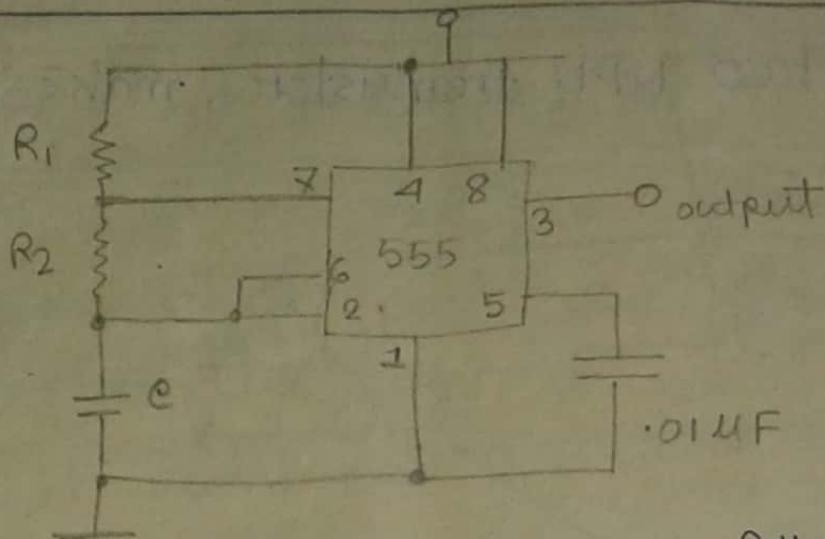
- (IV) Capacitor C_1 starts discharging during the state.
- (V) Transistor α_1 remains ON state due to positive voltage from the collector of α_2 which is in off state
- (VI) Transistor α_2 remains off state until the capacitor C_1 discharges completely.
- (VII) When the capacitor C_1 discharged completely. α_2 turns ON. which turns α_1 off.

Thus a MMVR works.

- Q. # Draw the internal diagram of 555 IC when it is used as an astable MV and explain it

Astable MV is also called a free running MV. It has no stable states and switches between two states without application of any external trigger. The 555 IC can be made to work as a astable mv with the addition of three external components .two resistors (R_1 & R_2) and capacitor C .

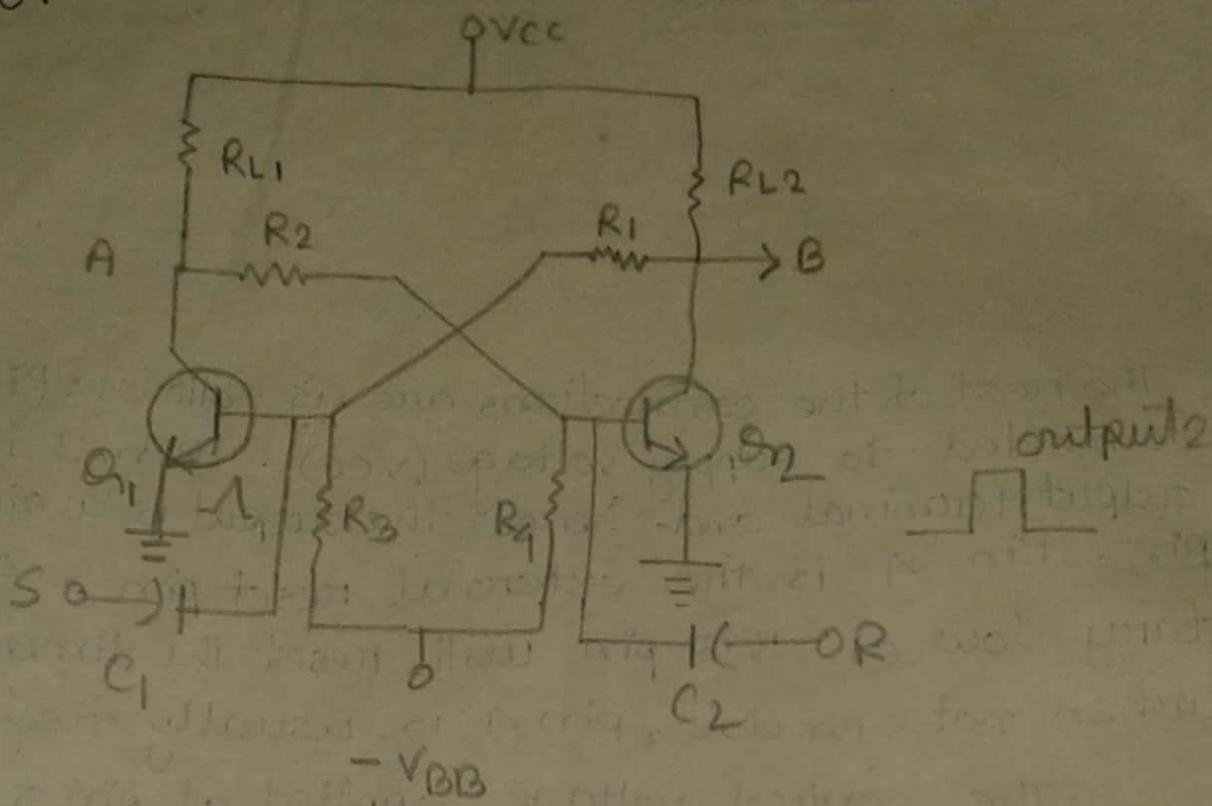
The pins 2 & 6 are connected and hence there is no need of external trigger pulse . It will set trigger and act as a free running mv.



The rest of the connections are as follows: Pin 8 is connected to supply voltage (V_{CC}). Pin 3 is the output terminal and hence the output is available in this pin. Pin 4 is the external reset pin. A momentary low on this pin will reset the timer. Hence when not in use, pin 4 is usually tied to V_{CC} .

The control voltage applied at pin 5 will change the threshold voltage level. Pin 5 is connected to ground via a capacitor ($0.01\mu F$) so the external noise from the terminal is filtered out. Pin 1 is ground terminal. The timing circuit that determines the width of the output pulse is made up of R_1 , R_2 and C .

⑩ # wiring two NPN transistors make a bistable MU.



In Bistable multivibrator the base resistors are joined with a common source $-V_{BB}$. and feedback is coupled through two resistors.

Circuit action:

When Q_1 is conducting,
Point A is at 0 volt
which makes the base of Q_2 negative and holds Q_2 cutoff.

when Q_2 is not conducting or off,

(i) Point B is at nearly V_{CC} which makes the base of Q_1 positive and holds Q_1 on or conducting.

So, it seen that Q_1 holds Q_2 off and Q_2 holds Q_1 on.

when positive pulse is applied to R,

(i) It causes Q_2 to conduct. So, the collector voltage is 0. which cuts off the transistor Q₁

(ii) Consequently the BMV switches over to its other state.

when a positive pulse is applied to S,

It causes the BMV back to its original state.



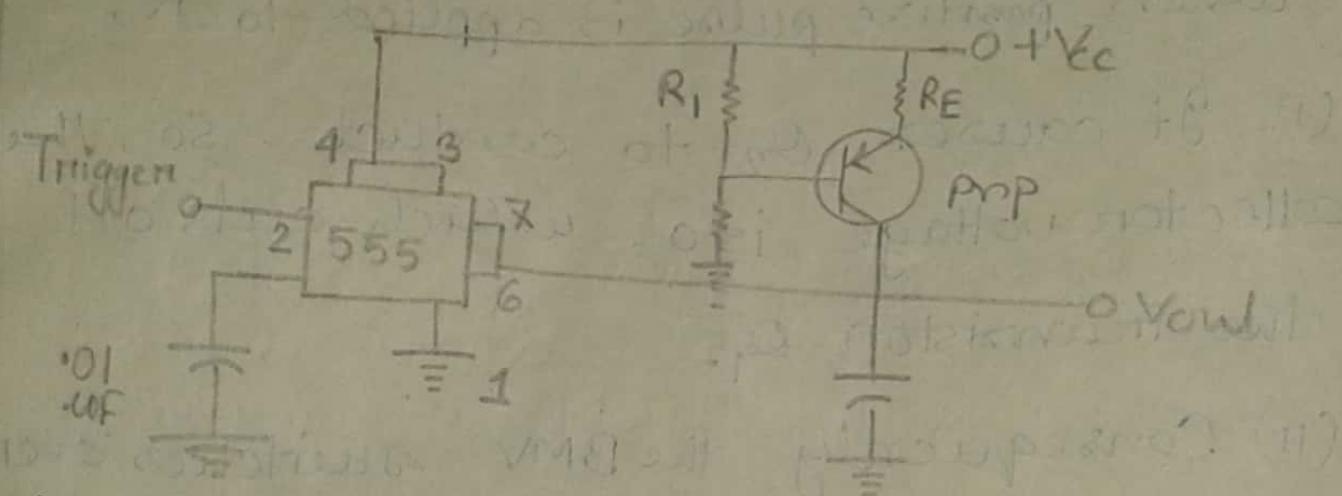
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- (15) # show how to use a 555 timer and a bipolar current source to produce a ramp output

Ramp output:

A ramp is a linearly increasing or decreasing voltage. We get a ramp output waveform if we use a constant current source to charge a capacitor.

Producing Ramp output:



(fig) using a 555 timer and a bipolar current source to produce a ramp output voltage.

In the fig a bipolar constant current source is used to charge a capacitor. Hence here we replace the resistor of 555 timer circuit with open pnp current source that produces a constant charging current of

$$I_C = \frac{V_{CC} - V_E}{R_E}$$

$$\text{Hence, } R_E = \frac{R_2}{R_1 + R_2} V_{CC} + V_{BE}$$

when trigger starts the monostable 555 timer of fig) . the pnp current source forces a constant charging current into the capacitor. therefore the voltage across the capacitor is a ramp as shown in fig(b) . the shape of the ramp is given by $s = I_C/t$

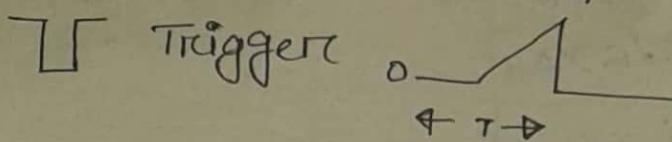


fig b: trigger and ramp waveform

Q # Draw the eqn for calculating output frequency of a stable mv.

prove that output frequency of the MV is

$$f = \frac{1.44}{(R_A + 2R_B)C}$$

In a stable multivibrator waveform, the capacitor upword charges takes time w . The capacitor voltage starts at $\frac{+V_{CC}}{3}$ and ends at $\frac{+2V_{CC}}{3}$ with a ref target voltage of $+V_{CC}$.

$$V = V_i + (V_f - V_i) (1 - e^{-t/R_C})$$

$$\Rightarrow \frac{2V_{CC}}{3} = \frac{V_{CC}}{3} + \left(V_{CC} - \frac{V_{CC}}{3}\right) \left(1 - e^{-t/R_C}\right)$$

$$\Rightarrow V_{end} = start + (target - start) (1 - e^{-t/RC})$$

$$\Rightarrow \frac{2V_{cc}}{3} = \frac{V_{cc}}{3} + \left(\frac{2V_{cc} - V_{cc}}{3} \right) (1 - e^{-t/RC})$$

$$\Rightarrow \frac{2V_{cc}}{3} = \frac{V_{cc}}{3} + \frac{2V_{cc}}{3} (1 - e^{-t/RC})$$

$$\Rightarrow \frac{2V_{cc}}{3} = \frac{2V_{cc}}{3} \left[\frac{1}{2} + (1 - e^{-t/RC}) \right]$$

$$\Rightarrow -(1 - e^{-t/RC}) = \frac{1}{2}$$

$$\Rightarrow 1 - e^{-w/RC} = -0.5$$

$$\Rightarrow -e^{-w/RC} = -1.5$$

$$\Rightarrow -w/RC = -0.693$$

$$\Rightarrow w = 0.693 RC$$

$$w = 0.693(R_A + R_B)C$$

The discharging equation is similar. Except that R_B is used instead of $R_A + R_B$. From a stable waveform the discharge time is $T-w$ which leads to output

$$T-w = 0.693 R_B C$$

$$\text{The period is } T = w + 0.693 R_B C$$

$$\text{Duty cycle } D = \frac{w}{T} = \frac{0.693(R_A + R_B)C}{0.693(R_A + R_B)C + 0.693R_B C}$$

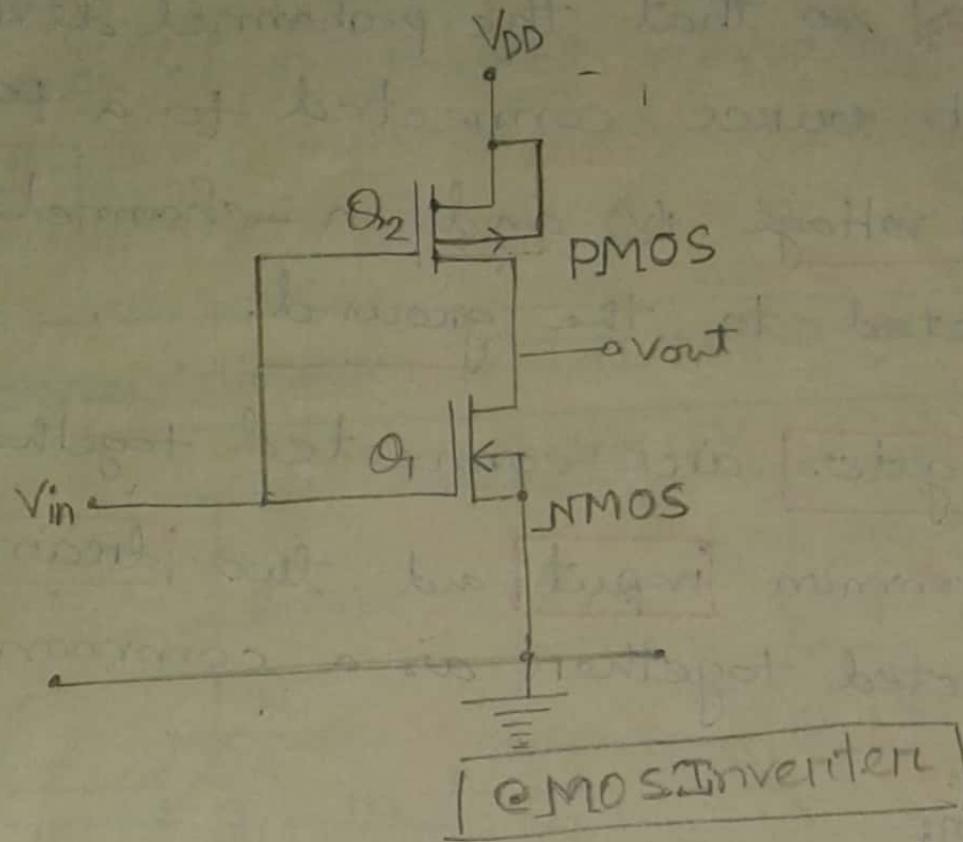
$$= \frac{0.693(R_A + R_B)C}{0.693(R_A + R_B)C + 0.693R_B C} \times 100\%$$

$$= \frac{(R_A + R_B)}{R_A + 2R_B} \times 100\%$$

To get frequency take the reciprocal of the period T

$$f = \frac{1}{T} = \frac{1}{0.693(R_A + R_B)C + 0.693R_B C}$$

Explain the operation of CMOS inverter } or CMOS
not gate



Construction:

- ④ The N channel MOS conducts with its source voltage is positive. when its gate to source voltage is positive.
- ④ The P-channel MOS conducts when its gate to source voltage is negative. when its gate to source voltage is negative.
- ④ Either type of device is turned off when its gate to source voltage is zero.

Now in fig this is a CMOS logic circuit where two MOSFET is connected in series so that the p-channel device has its source connected to a positive supply voltage +V and n-channel is connected to the ground.

Two gates are connected together as a common input and two drains are connected together as a common output

Operations:

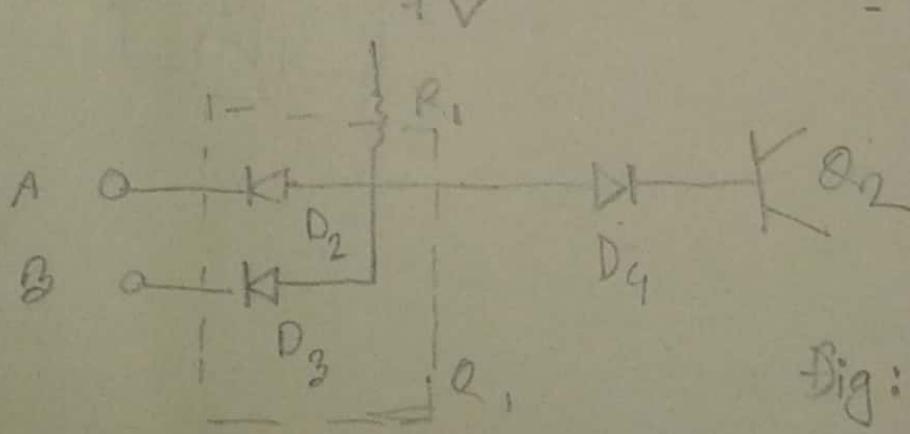
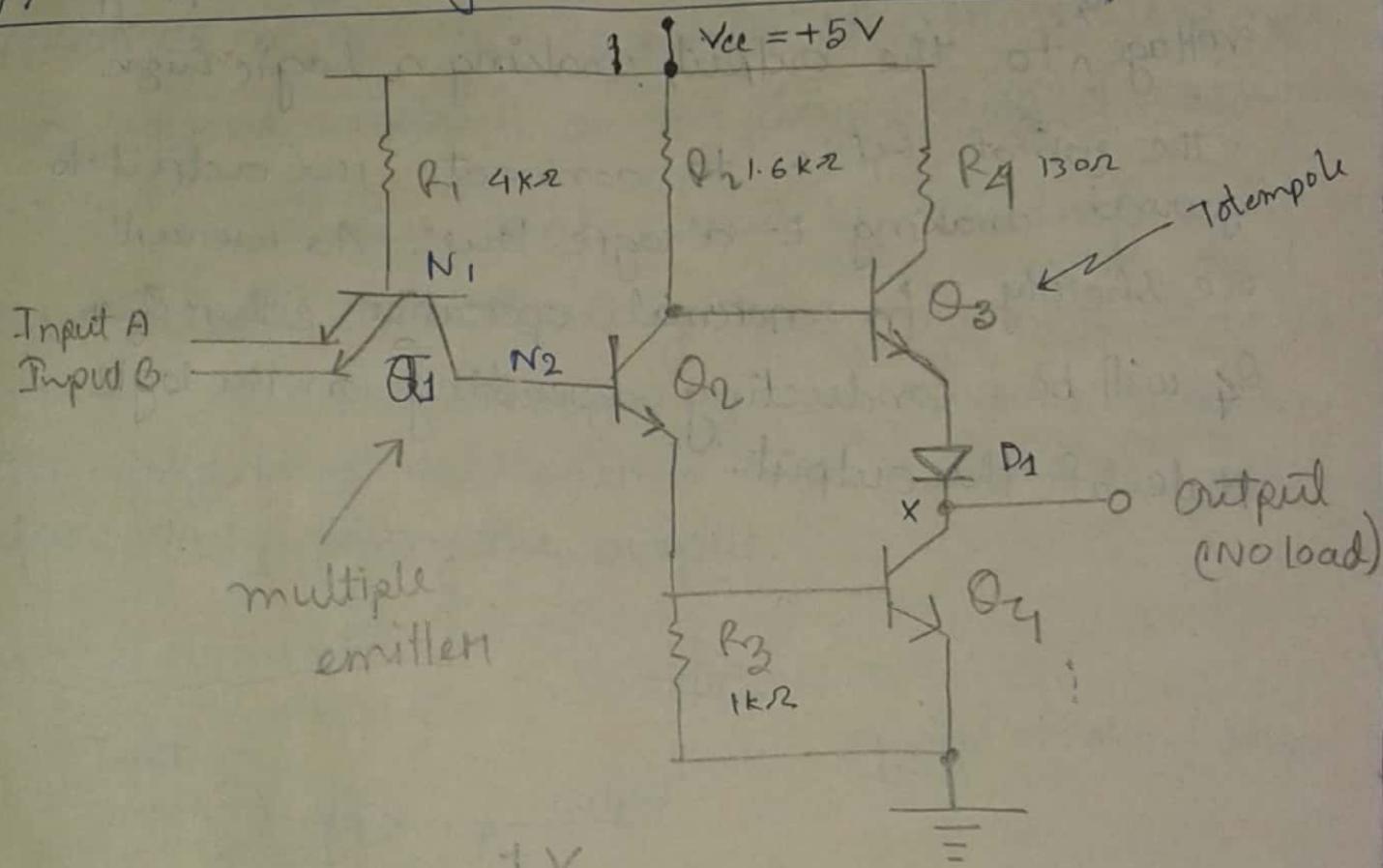
Both Q_1 and Q_2 are enhancement type.

when $V_{in} = 0V$, Q_1 cut off (N-channel MOSFET is off) (P channel mosfet is on). This condition connects the output to supply voltage through the on resistance of P channel, resulting a High output.

when V_{in} is high, n channel is on.

④ P channel MOSFET is off. This condition connects the output to ground through the on channel resistance of n channel resulting a low output.

⑩ # Internal diagram of TTL NAND gate



Big: diode equivalent for Q_1

fig shows TTL NAND gate,

T_1 is a npn transistor with multiple emitters which indicates the inputs.

The output side of the circuit, transistors Q_3 and Q_4 are in a totem pole arrangement

The job of Q_3 is to connect the supply voltage to the output making a logic high

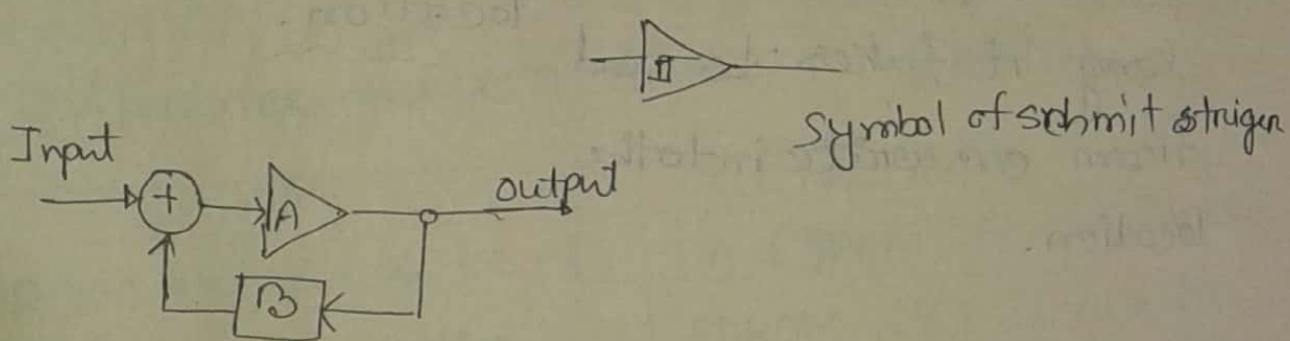
The job of Q_4 is to connect the output to ground making it a logic low. As we will see shortly, in normal operation either Q_3 or Q_4 will be conducting depending on the logic state of the output.

What is hysteresis of a schmitt trigger circuit

Ans: Hysteresis is the time based dependence of a system's output on present and past inputs. The dependence arises because the history affects the value of an internal state.

The hysteresis of a schmitt trigger can be used for a few things with a couple of the applications being the creation of a timer (simple clock signal creation) or the debouncing of a switch.

The timer can be made by adding an RC to the output and feeding that signal back to the input. Simple debouncing can be done by sending the input of the switch to the input of the schmitt trigger and taking the output.



Memory system

Difference between RAM & SAM

RAM	SAM
① Random Access memory	① Sequential access memory
② It works rapidly	② works sequentially
③ The access time is constant	③ access time is not constant
④ It is not time consuming	④ time consuming
⑤ Its working process is frequent	⑤ working process is frequently low.
⑥ Access time is	⑥ Access time is larger than RAM
⑦ smaller than SAM.	⑦ It varies depending on the address location.
⑧ The actual physical location of a memory has no effect how long it takes to read from or write into the location.	

Difference between DRAM & SRAM

	SRAM	DRAM
stands for	Static Random Access memory	dynamic Random access memory
speed	high	low
cost	high	low
Refreshing	Doesn't need	needs periodic refreshing
Data storage device	Transistor	capacitor
used	used for cache memory	used for main memory
External support circuitry	Doesn't require external support circuitry	Requires it.

Difference between EEPROM EPROM

EPROM
EPROM chips can be programmed by the user and it can also be arranged and reprogrammed by a special programming device.

EEPROM

i) EEPROM is similar to EPROM . It is also be erased & reprogrammed.

The contents of EEPROM can be erased by exposing it to ultraviolet light.

It contents of EEPROM chip can be erased by applying electrical pulses to the chip.

Stands for Erasable Programming Read only memory.

Electrically Erasable Programmable Read only memory

Programming & Erasing of it can be done outside of the circuit.

Programming & erasing of it can be done inside of the circuit.

For programming it needs a special PROM programmer unit.

It doesn't need any programmer unit.

It can be programmed by keyboard command.

#	RAM	ROM
	Random access memory volatile memory Data are stored temporarily Data can be written on RAM and read from RAM Data can be written into and read from RAM rapidly.	Read only memory non-volatile. Data are stored permanently. No new data can be written but data can be read from ROM When we turn off power, the data stored in ROM, will not lost.
	RAM is volatile and when we turn off power, data stored in RAM will lost.	ROM is not suitable device to write data on it.
	Speed high	Speed low.
	memory address location easily accessible	It is not easily accessible.

The major drawback of MROM

- Mask ROM is a type of ROM whose contents are programmed by the integrated circuit manufacturer. (physically hard-wired)
- The terminology 'mask' comes from integrated circuit fabrication.
- Region of the chips are marked off during the process of fabrication.
- MROMs typically have tri-state outputs that allow them to be used in a bus system
 - lowest cost per bit of any memory tech
 - highest density of any memory
 - Immune to magnetic field
 - can't be corrupted by software

Major drawback of PROM

- They are blank chips which have nothing recorded on them.
- Once instruction and data are recorded into chip by a special programming device, the PROM chip permanently stores the information like ROM

Programmable read only memory can be written once 33
33

- The programming of PROM chips is generally done by the manufacturers of computer system.
- The major drawback of PROMs is they are primarily used to provide special programs, which can be plugged into the main computer board.
- Often referred as "one time programmable" (OTP) ROMs.

drawback of EPROM

(erased by ultraviolet light)

- EPROM can be programmed as PROM chips. But they can be erased and programmed by a special programming device.
- The contents of EPROM chip can be erased by exposing it to ultraviolet light.
- Main drawback is its inability to erase only selected cells, the UV light erases all

cells at the same time.

#

Here is an EPROM erased

Disadvantages of Mask ROM

- can't (practically) be patched after manufacture
- requires massively costly mask respin
- need fully debugged code beforehand

EPROM

is a type of memory chip that retains its data when its power supply is switched off.

end. Pg

Scanned by CamScanner

Draw & explain the internal structure of
64x4 RAM

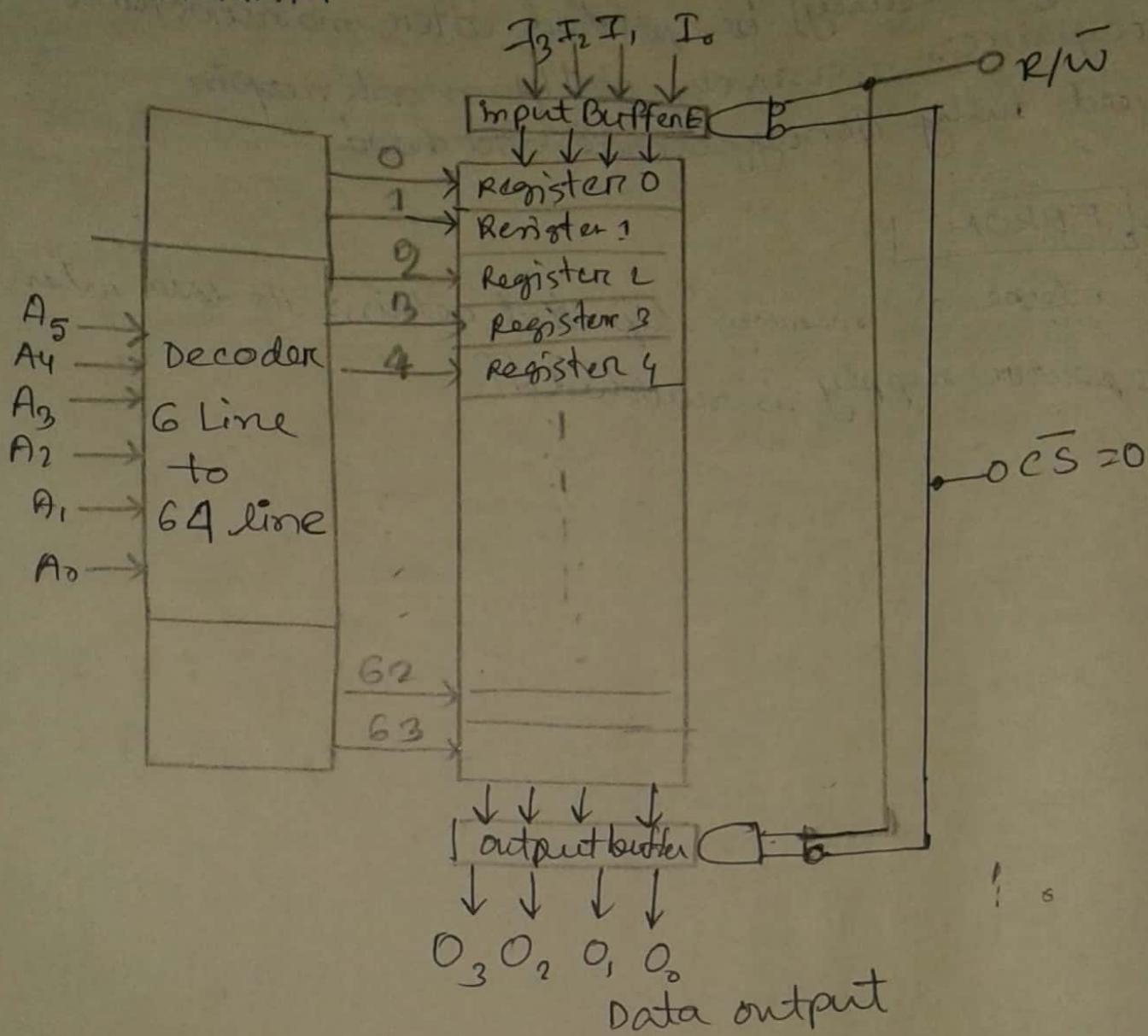


fig: Internal organization of 64×4 RAM

Explains The 64×4 RAM stores 64 words of 4 bits each. These words have address ranging from 0 to 63_{10}

The decoder circuit is used to select one of the 64 address location for reading or writing because $2^6 = 64$. The decoder requires 6 input code.

Read operations

At first chip selector (\overline{CS}) remains zero (0). Let address location is 111110 (62_{10}) & data is 1010 (10). If $R/W = 1$, then input buffer is inactive & output buffer is active.

data input: XXXX

Address Line: 111110

R/W : 1

\overline{CS} : 0 (always)

output data: 1010

Write operation: Let address location is 000111

& data is 1101. When R/W is 0, then input buffer is active & output buffer is inactive

data input: 1101

Address Line: 000111

R/W : 0

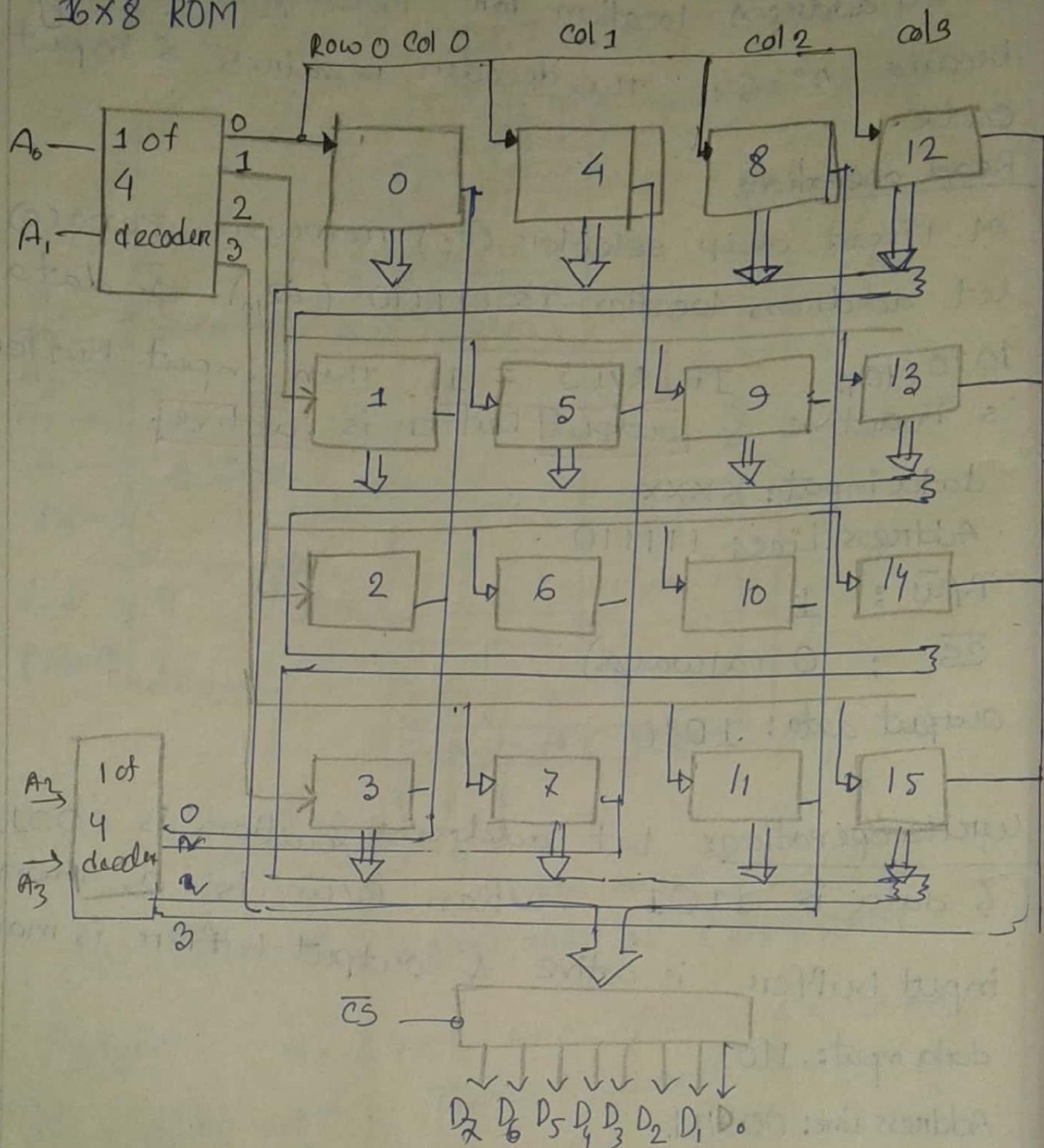
\overline{CS} : 0

data output: XXXX

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Draw & explain the internal structure of

16x8 ROM



39

There are four basic parts of ROM

- ① Register array
- ② row decoder } address decoder
- ③ column decoder
- ④ output buffer

Register array: The register array stores the data that have been programmed into the ROM.

- ⇒ Each register contains a number of memory cell equal to the word size.
- ⇒ Each register stores 8 bit word.
- ⇒ The registers are arranged in a square matrix array.
- ⇒ The ^{data} 8-bit output of each register are connected to the internal data bus.
- ⇒ Each register has two enable input.

Address decoder:

Applied address code $A_3 A_2 A_1 A_0$ determines which register will be enabled.

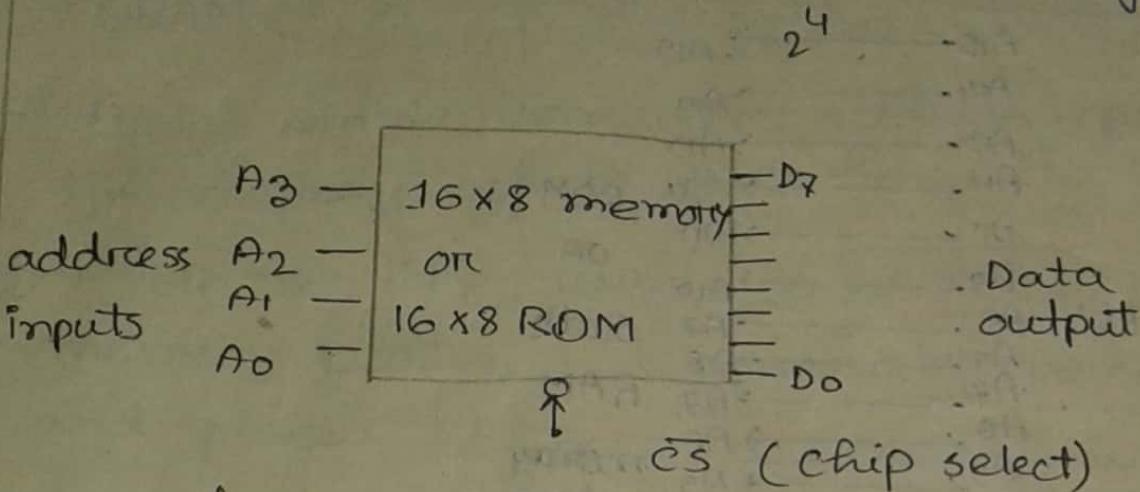
Address bits $A_1 A_0$ determines a 1 of 4 decoder which activates one row select line.

Address bit $A_3 A_2$ determines the second of 4 decoder which actives one column select line.

Only one register will be enabled when both the row & column selected by the address input.

(iii) output buffer: The register that is enabled by the address input will place its data on the data bus. These data feed into the output buffer which will pass data to the external data output provided that $\bar{CS} = 0$. If $\bar{CS} = 1$ the output buffers are in the Hi-Z state and D_7 through D_0 will be floating.

How many address input, data input and output are required for $16K \times 8$ memory?



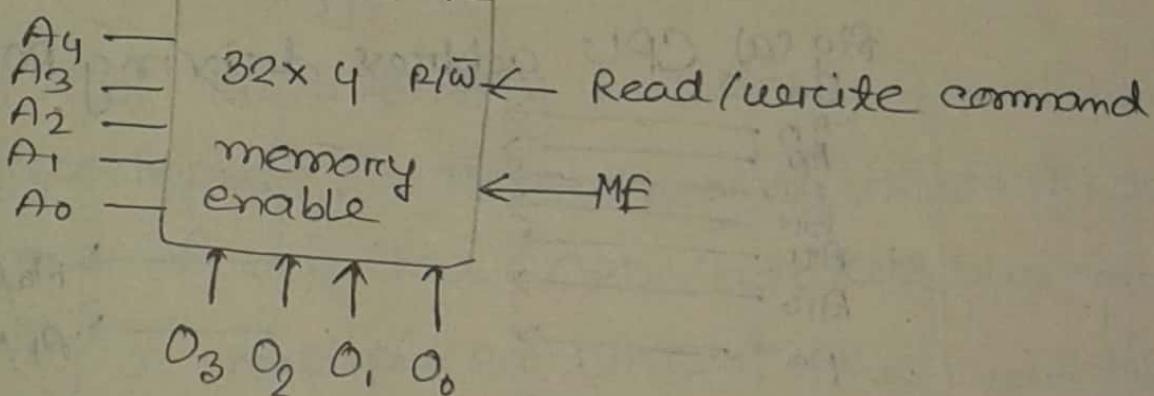
hence, 4 address inputs.

8 Data outputs
There is no data input in 16x8 ROM

32x4 memory Address input, data input, output

2⁵

I₃ I₂ I₁ I₀ Data input



5 address inputs

4 data inputs

4 data output are present in 32x4 memory.

Q2. Benefits of Address Multiplexing

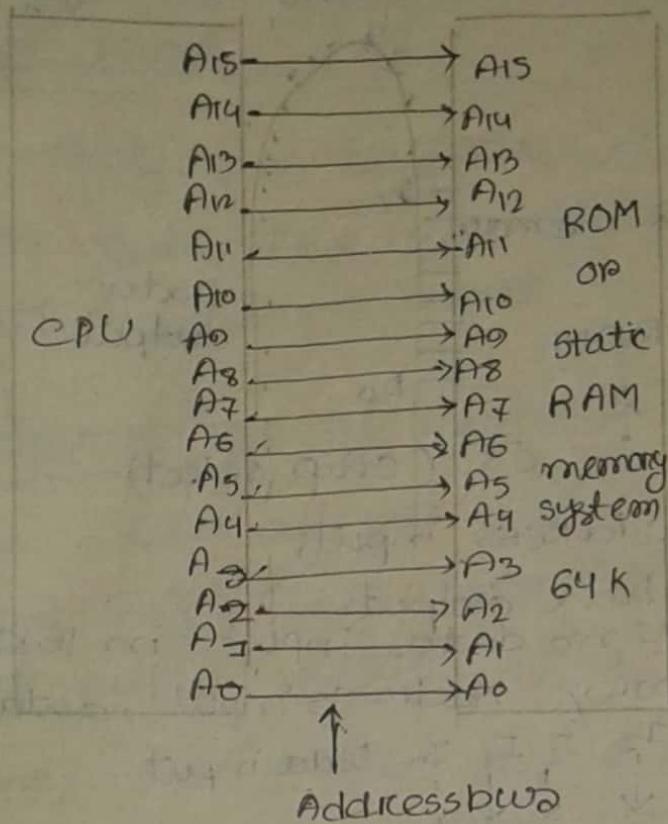


fig (a) CPU address driving ROM

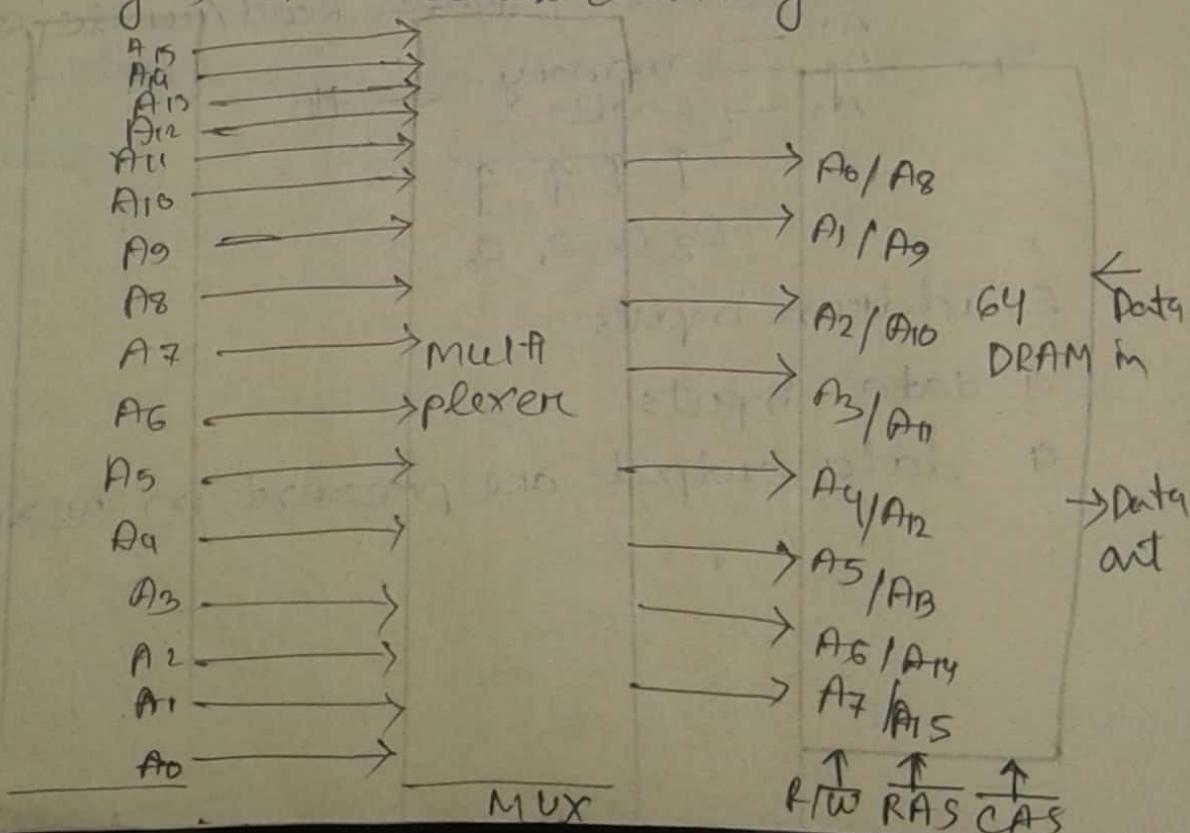


fig: CPU addresses driving a multiplexer that is used to multiplex the CPU address lines to the DRAM.

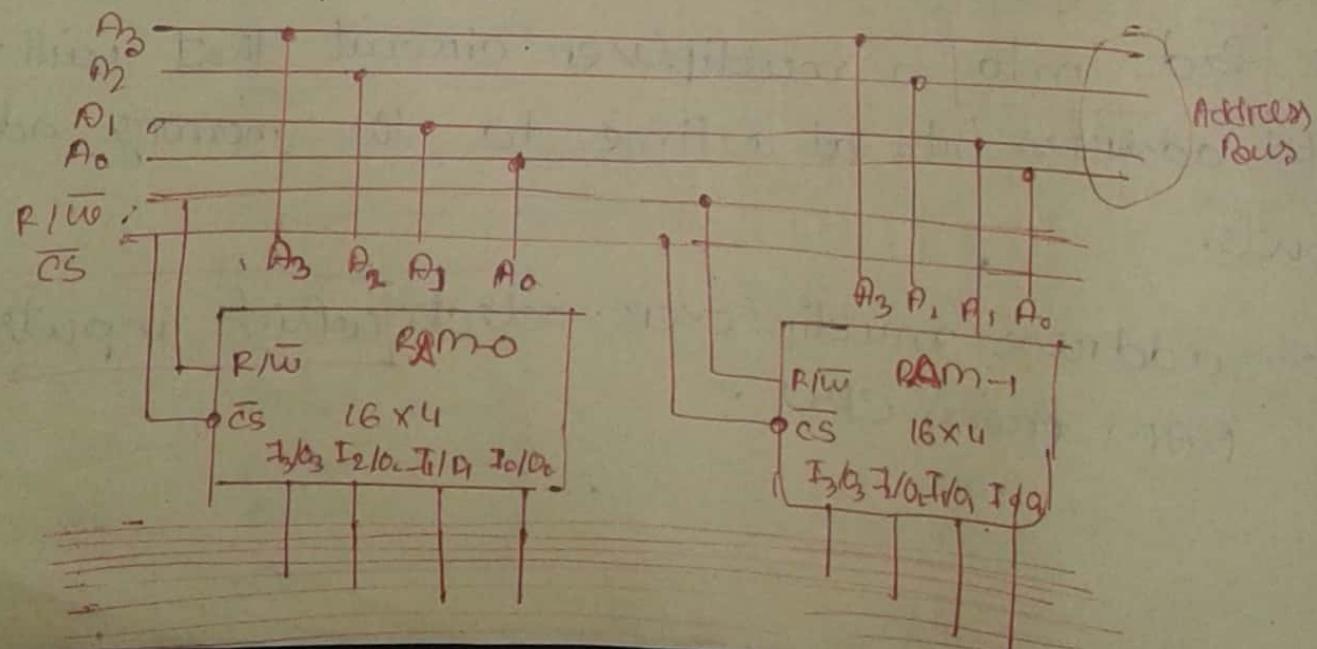
- ⇒ In a simple computer address input comes to the memory system come from the CPU.
- ⇒ when the CPU wants to access a particular memory location, it generates complete address and places it on address lines that make up an address bus. fig (a) shows this
- ⇒ This arrangement works for ROM or static but it must be modified for DRAM that uses multiplexed addressing.
- ⇒ If all 64 K of the memory is DRAM, it will have eight address inputs. This means that the 16 address lines from the CPU address bus must be fed into a multiplexer circuit that will transmit eight address bits at a time to the memory address inputs.
- ⇒ So address multiplexer selects which inputs go to the RAM from CPU.

⇒ The timing of the mux signal must be synchronized with the \overline{RAS} and \overline{CAS} signals so that **clock** the **addressed** into the DRAM.

⇒ Mux must be **low** when **\overline{RAS}** is pulsed low. so that address lines A_8 to A_{15} from CPU will **reach** to the DRAM, address inputs to be **loaded** on the **NAT of \overline{RAS}** .

⇒ Mux must be **high** when **\overline{CAS}** is pulsed low. so that A_0 to A_7 from the CPU will be **present** at the DRAM, inputs to be **loaded** on the **NAT of \overline{CAS}**

29
□ Explain & construct 16×8 RAM by using two 16×4 RAM



Address range 0000 to 1111 (16 word)

The four **higher** order bits of each word are stored in RAM-0

The four **lower** order bits of each word are stored in RAM-1

By using two **16×4** RAM, we can construct **16×8** RAM

⇒ We can store **16 eight bit** words in this RAM.

⇒ Each RAM stores **16 four bit** words.

⇒ RAM-0 stores four higher order bits & RAM-1 stores four lower order bits of each 16 words.

⇒ By using two **16×4** RAM, we can get 8 bit data which is connected to the data bus.

⇒ Address **code** ($A_3 A_2 A_1 A_0$) **connected** to the Address **bus** which is originate at the CPU.

⇒ Each address **bus** is **connected** to the corresponding address **input** of the chip.

⇒ If address is selected, we can read/write operation.

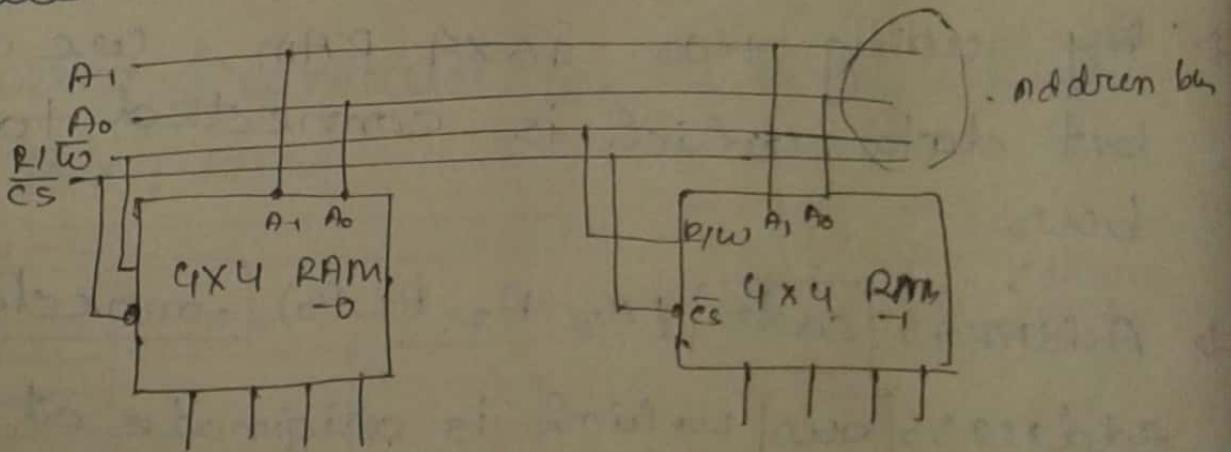
Read operation: If R/W is high (1) & CS is low (0), then the RAM I/O lines act as outputs.

Write operation: If CS is low and R/W is low (0) Then the RAM I/O lines act as inputs.

The higher four bits will be written into the selected location of RAM-0.
the lower 4 bits will be written into RAM-1.

2² ~~not~~

田 A 4×8 module by using two 4×4 RAM module.



000 111

97

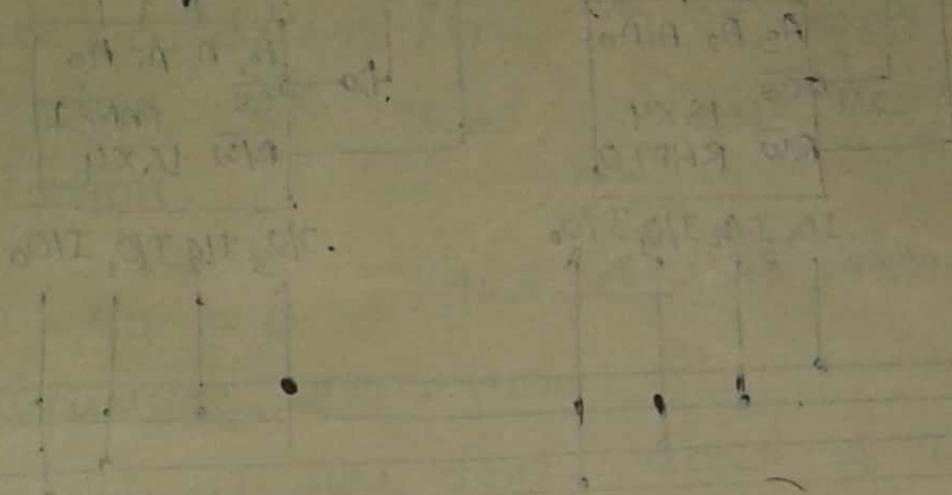
Address range 6000 to 100 (word)

higher order

first 4 bit one

started in RAM-0

the four lower order

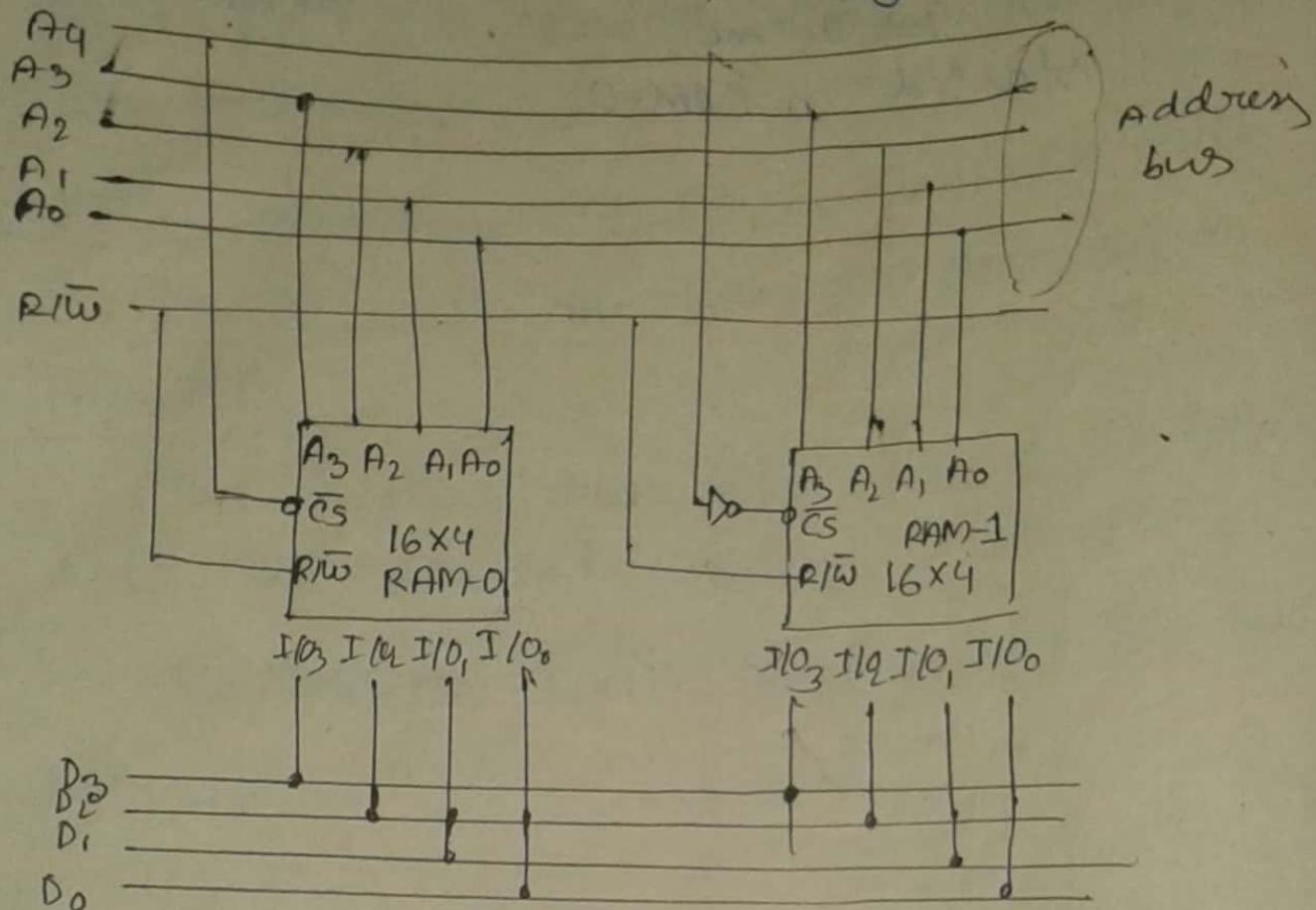


DATA at 6000 200-01 20100

DATA at 6001 000-01

DATA at 6002 0000-01

48
Explain 32×4 RAM by using 16×4 RAM



Address ranges 0000 to 0111 \rightarrow RAM-0
 10000 to 11111 \rightarrow RAM-1

total 00000 to 11111 \rightarrow 32 words

\Rightarrow By using two 16×4 RAM, we can construct 32×4 RAM

\Rightarrow we can store 32 four bit words in this RAM

\Rightarrow each RAM is used to store 16 four bit word.

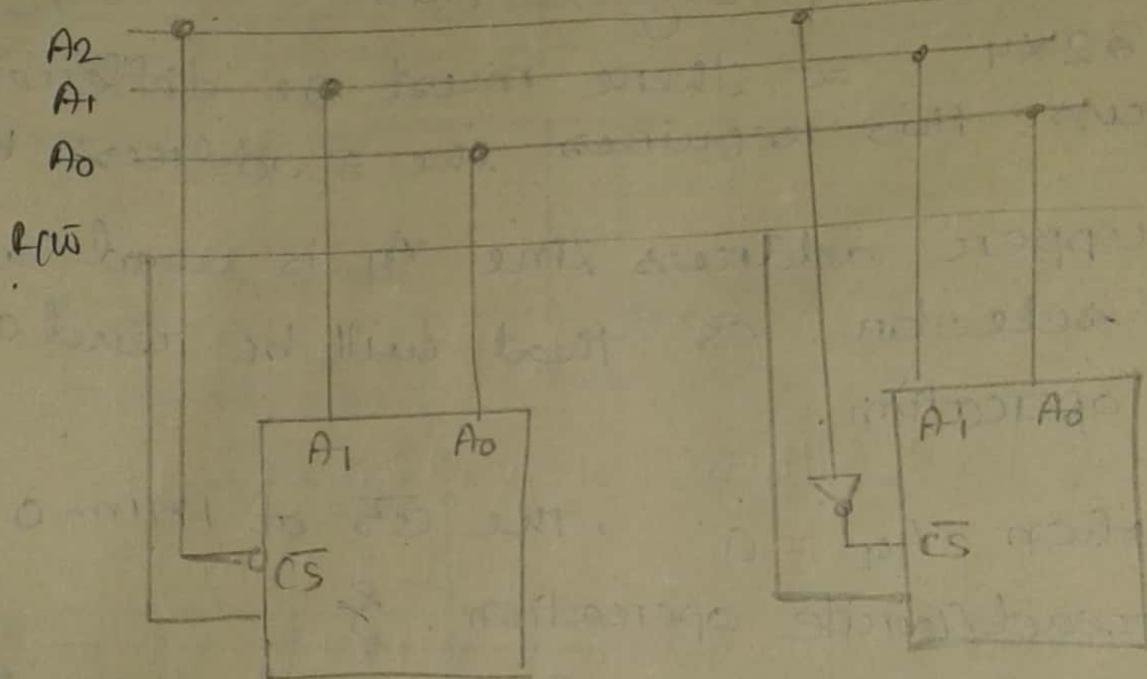
- ⇒ The 4 data I/O pins of each RAM are connected to a common 4 lines data bus.
- ⇒ The total capacity of this memory module is 32×4 so there must 32 different address. This requires the 5 address bus lines.
- ⇒ The upper address line A_4 is used as chip selector. \bar{CS} that will be read or write operation.
- ⇒ When $A_4 = 0$, the \bar{CS} of RAM-0 enables for read/write operation. & RAM-1 is disable for read & write. Therece any address location of RAM-0 can be accessed by A_3 through A_0 . The range of address representing location is RAM-0 is

$$A_4 \ A_3 \ A_2 \ A_1 \ A_0 = 00000 \text{ to } 01111$$

- ⇒ When $A_4 = 1$ ~~\bar{CS}~~ RAM-1 is enabled for read & write operation. & RAM-0 is disable. Therece any address location of RAM-1 can be accessed by A_3 through A_0 . The range of address location in RAM-1 is

$A_3 A_2 A_1 A_0 = 10000$ to 11111

2³ \square 8x4 by using 4x4 RAM



Apu missd the class 😢

Q) What is duty cycle. (show how to calculate duty cycle for a 555 astable timer circuit)

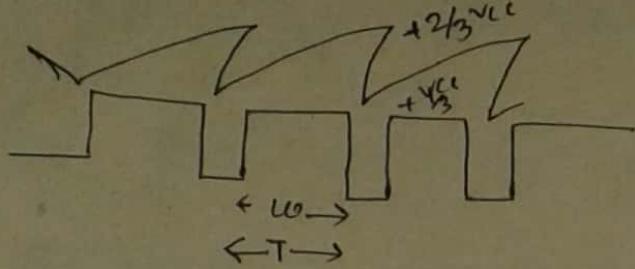


fig: Astable waveform.

Duty cycle is the ratio of charging time constant to charging pulse discharging time constant.

Duty cycle is the width of a pulse divided by the period betⁿ pulses usually multiply by 100% to get the answer as a percentage.

$$\text{Duty cycle} = \frac{w}{T} \times 100\%$$

where

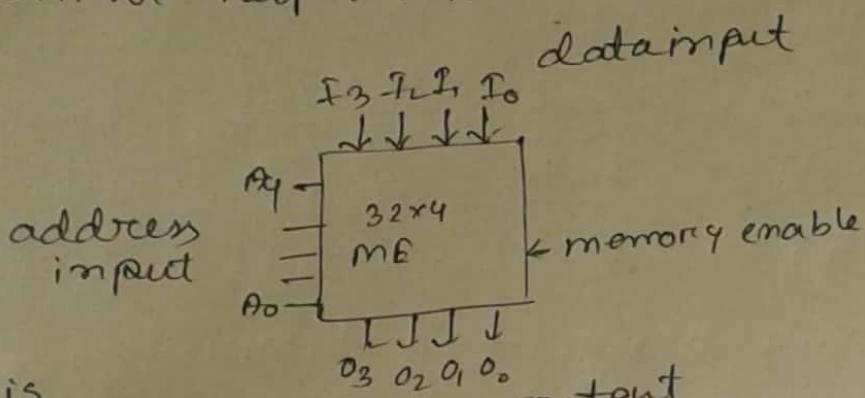
w = charging time constant

T = charging & discharging time constant.



The function of memory enable input :

Ans: Many memory system have some means for completely disable all or part of the memory so that it will not respond to the other inputs.



This is represented in the above figure as the memory enable input.

Although it can be have different names in the various memory system, such as chip enable (CE) chip selector (CS)

Hence it is shown as active high input that enables the memory to operate normally when it is kept high.

A low on this input disables the memory so that it will not respond to the address and data inputs.

This type of input is useful when several memory modules are combined from a larger memory.

Ct Question

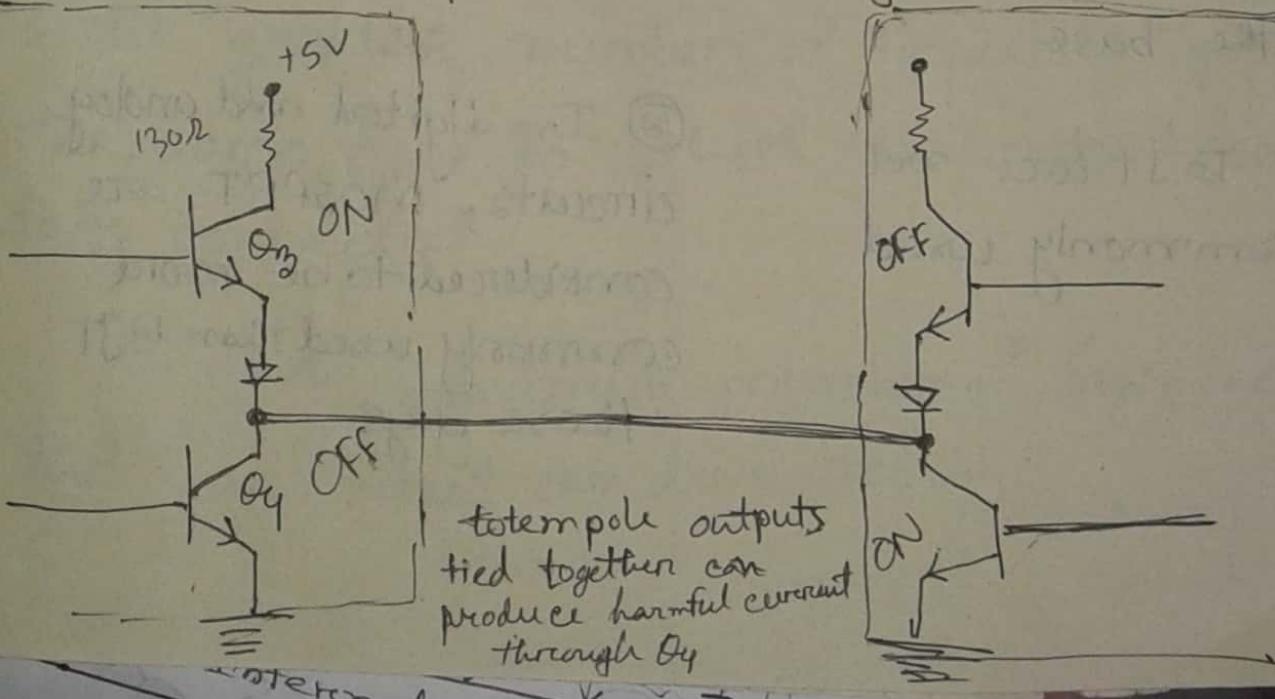
Q5

Q) The totem pole output of a TTL gate cannot be wired together? Why.

Ans: Because the active pull-up or totem pole output of the TTL gate always has one transistor cutoff and the other turned on. we can not connect two outputs together. If one is trying to pull the output high , the other is trying to pull it low . we will have a very low impedance path to ground and very large currents.

For the same reason , the output must not be connected to any voltage source or to ground through a low impedance path.

In one state or the other , there would be a low impedance path and large currents .



Difference between BJT and MOSFET

BJT

MOSFET

- | | |
|---|--|
| <p>① BJT is a Bipolar Junction transistor</p> <p>② A BJT has an emitter, collector and base</p> <p>③ BJT are preferred for low current applications</p> <p>④ the operation of BJT depends on the voltage at the oxide-insulated gate electrode</p> <p>⑤ BJT are not commonly used</p> | <p>① MOSFET is a Metal oxide Semiconductor Field - Effect Transistor</p> <p>② while MOSFET has a gate, source, drain</p> <p>③ MOSFET are preferred for high current function</p> <p>④ the operation of MOSFET depends on the voltage at the oxide insulated gate electrode</p> <p>⑤ In digital and analog circuits, MOSFETs are considered to be more commonly used than BJT these days.</p> |
|---|--|

Q What is meant by "fanout" of TTL devices?

Ans: Fanout is the number of ~~get~~ gate inputs we can connect to a gate output. Example, with a fanout of 8, one TTL gate can drive 8 others.

In most designs, logic gates are connected to form more complex circuits. While no more than one logic gate output is connected to any single input, it is common for one output to be connected for several inputs.

The technology used to implement logic gates usually allows a certain number of gate inputs to be wired together without additional interfacing circuitry. The maximum fan-out of an output measures its load-driving capability. It is the greatest number of inputs of gates of the same type to which the output can be safely connected.

✓ maximum number of logic inputs that an output can drive reliably.

TTL NAND gate (low state output)

Input conditions	Output condition
A and B are both High $> 2V$	Q_3 OFF
Input currents are very low	Q_4 ON so that V_x is low $< 0.4V$

current sink

High state

Input condition	Output condition
A or B or both are Low $< 0.8V$	Q_4 OFF

current source

When the TTL output is the low state, Q_4 acts as a current sink deriving its current from the load. (b) High state, Q_3 acts as a current source, providing current to the load gate.

Difference between TTL & MOS

TTL

① Transistor-transistor logic

MOS

① Metal oxide Semiconductor

② It has unconnected inputs ② It has connected inputs.

③ It has relatively complex and expensive fabricate ③ It has relatively simple & unexpensive fabricate.

④ It is large and consumes very high power ④ It is small and consumes very low power.

⑤ High speed

⑤ Very low speed.

⑥ High fan-out capability

⑥ Relatively low-fanout capability.

⑦ Propagation time per gate
10 ns.

⑦ Cost per bit is very low.

⑧ Tight V_{cc} tolerance

⑧ Requires multiple power source.

Explain working principle of a TTL NOT gate

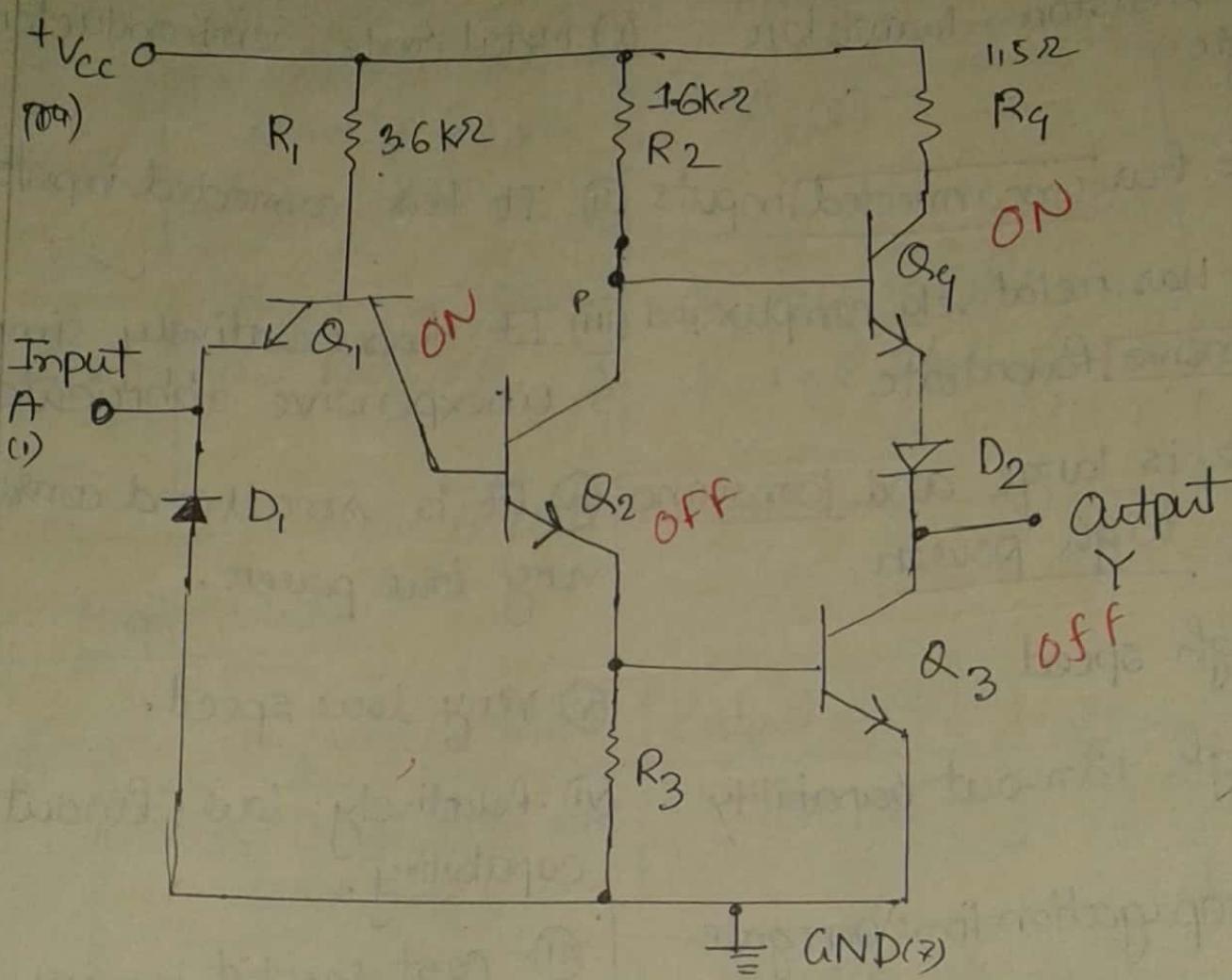


Fig TTL NOT Gate.

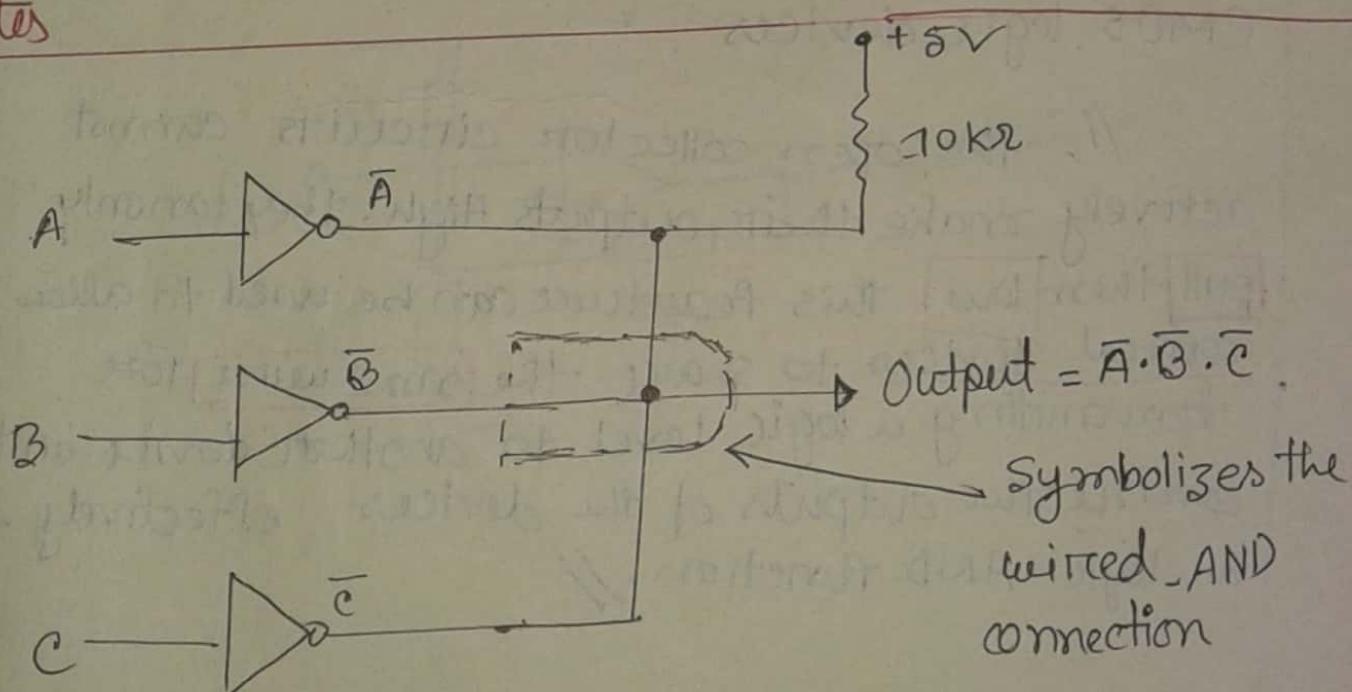
- ⇒ In this NOT gate circuit, point A has 0 V and source 5 V .
- ⇒ Q_1 is the p-n junction that requires 0.7 V and because Q_1 is on.
- ⇒ Q_2 requires less voltage so, Q_2 is off.

⇒ In the point of P, has large voltage than 1.4. So, Q_4 is ~~in~~ saturation state and Q_4 is on.

⇒ Above all these process occurs in forward bias. and so, Q_3 is in off mode.

If point A has input I, then this process occurs in reverse bias. and Q_3 is in on mood.

Explain wired AND operation using open collector gates



74LS05 (open-collector)
or (open-drain)

fig: wired-AND operation using open collector gates

When several open collector or open drain gates share a common connection shown in fig. the common wire is held high by default due to the pull-up-resistor.

When any one of the gate outputs is low, the 5 volts are dropped across R_P and the common connection is in the low state.

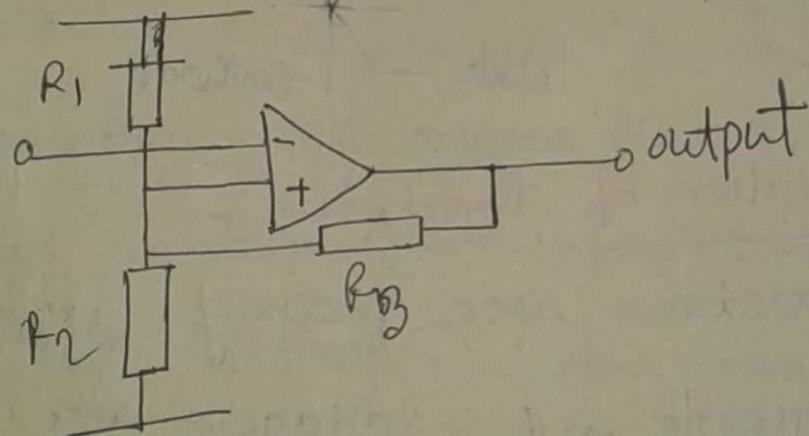
Since the common output is high only when all the outputs are in the High state, connecting the outputs in this way essentially implements the logic AND function. This is called a wired-AND connection.

A wired-AND can be implemented only with open-collector TTL and open-drain CMOS logic devices.

// the open collector circuits cannot actively make their outputs high. They can only pull them low. This feature can be used to allow several devices to share the same wire for transmitting a logic level to another device or to combine the outputs of the devices effectively in a logic AND function. //

Working principle of schmitt trigger

Ans: The schmitt trigger is an electronic comparator that has a slightly different voltage (or current) threshold for turning on than it does for turning off. This means that, once it turns on, it sticks on until the input signal decreases, somewhat below the original turn-on point, and vice versa, once it turns off it sticks off until the input signal increases somewhat above the original turn-off point. This is called hysteresis, and it effectively debounces the input signal and prevents short cycling.



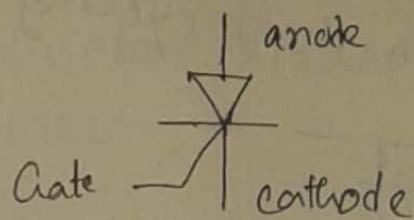
Thyristor

Thyristor is a four layer semiconductor device / rectifier in which the flow of current between two electrodes is triggered by a signal at a third electrode.

consists of alternating P-type and N type materials (PNPN) has three electrode

~~①~~ an anode (control electrode) ② a cathode ③ a gate

most common type of thyristor is SCR (Silicon control Rectifier)



Application of Thyristor -

→ Thyristors are mainly used where high currents and voltages are involved.

used to control alternating currents - referred to as zero & cross operation

→ can be used as control elements for phase angle triggered controllers known as phase fired controllers.

Zero-cross
operation

- used as a sort of enhanced circuit breaker
- is used in conjunction with a zener diode attached to its gate.
- first large scale application of thyristor with associated triggering circ.
- used for decades as lighting dimmers in television, motion pictures and theaters.

✓ → UJT triggered SCR

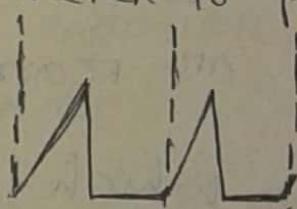
→ Microprocessor controlled SCR

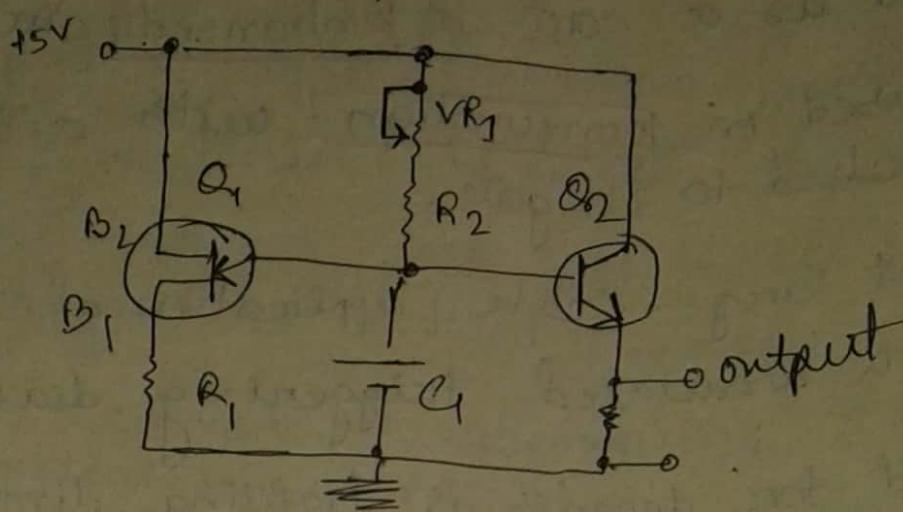
→ full wave control

How to use UJT to produce Sawtooth waveform

A waveform that appears like teeth on a saw

A saw tooth waveform has a slow linear rise time and fast fall time. Also refer to periodic waveform.





- Q_1 is VJT to connect with VR_1 , VR_2 & C_1 .
- They act as a sawtooth wave generator circuit by using C_1 to charge & discharge.
- Then current from $5V$ power supply through VR_1 & R_2 .
- This current that is voltage that increase & reduce, cause Q_1 generate signal which have the sawtooth wave signal or ramp signal to output. which frequency is determined with R & C .

operation

→ Q_2 transistor is derived the signal input to conduct current as the sawtooth signal voltage by at pin E of Q_2 will be connected into the output signal that has voltage ~~for~~ from 0V. Then potentially rises by step up to +vcc of 5V is sawtooth waveform.

→ ^{when} C_1 capacitor discharge voltage that enters to Q_2 will reduce until cause Q_2 stop conduct the voltage ~~at~~ at pin E of Q_2 so make signal out of thus making output signal continuous as well.

→ The capacitor charges toward the vcc but as soon as its voltage exceed stand off voltage and the UJT loses.

→ This discharge the capacitor, until low current dropout across.

→ As soon as UJT opens, the next cycle begins.

→ As a result we get sawtooth wave form.

relaxation oscillator

- built oscillator's
- generates output signal with no external input signal

X
no input
signal
 R

op amp \rightarrow output signal

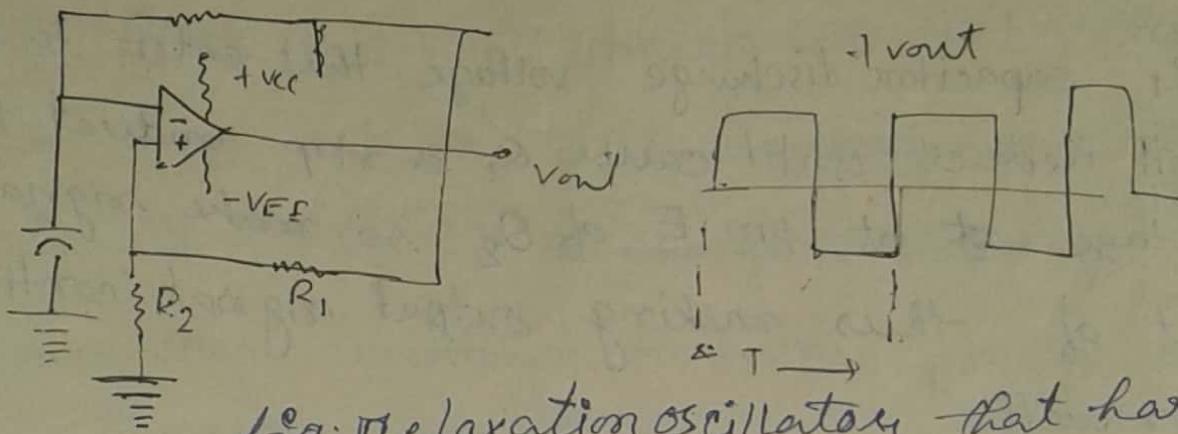
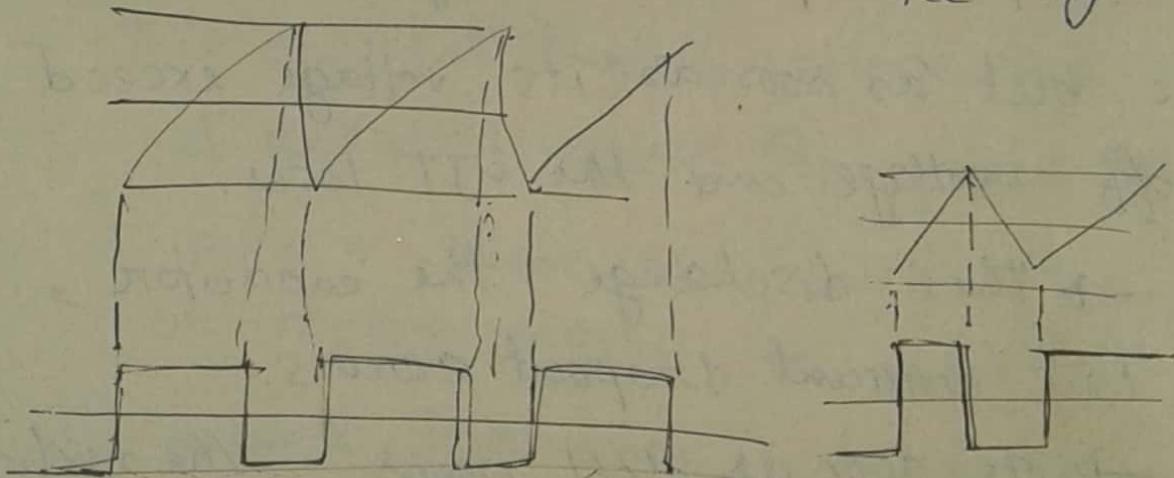


fig: relaxation oscillator that has no input signal but generates an output rectangular wave.



- V_{SAT}

69

→ generates output signal whose frequency depends on changing / discharging of capacitor or inductor (B)

$$\text{Wave } T = 2RC \ln \frac{1+\beta}{1-\beta}$$

output esm
positive saturation, towards V_{sat} at frequency f_{sat}
as its voltage hits the UTP \rightarrow V_{sat}
switches to $-V_{sat}$, capacitor vol decrease.
hits an LTP \rightarrow output switcher back to V_{sat}

$$\boxed{T = 2RC \ln \frac{1+\beta}{1-\beta}}$$

- determine the rate of discharging
- " the period of output signals

$$T = 2RC \ln \frac{1+\beta}{1-\beta}$$

T → Period of output signals

R → feedback resistance

C → Capacitance

$\beta_2 \frac{R_2}{R_1+R_2}$ → feedback fraction

$$V = V_i + (V_f - V_i) (1 - e^{-t/RC})$$

Initial Target charging

70

70

(e)

- B_{VAD} initial value
+ B_{VAT}

