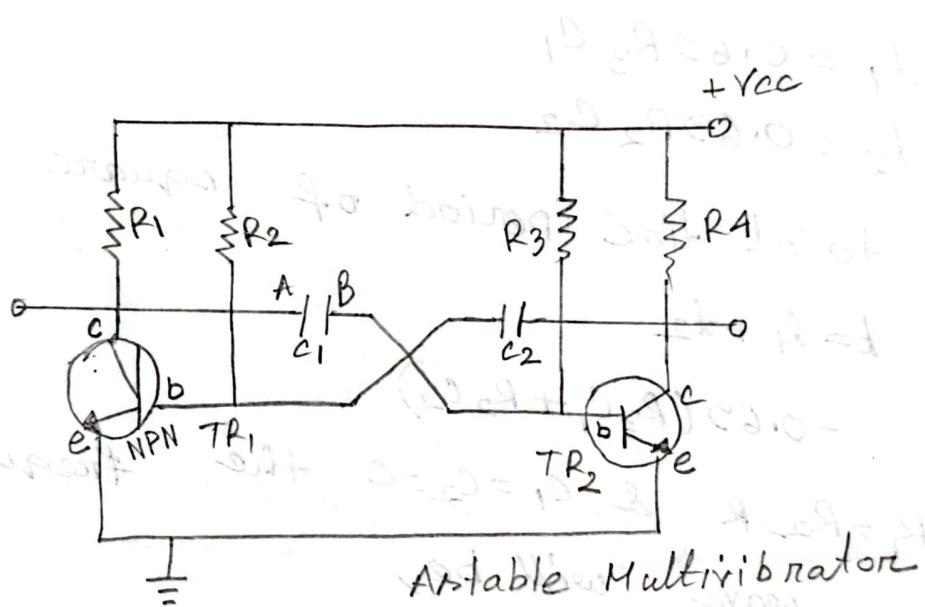


1) Design an Astable multivibrator to oscillate at the frequency of 100kHz.

= The astable multivibrator is another type of cross-coupled transistor switching circuit that has no stable output states as it changes from one state to the other all the time.



Two transistors named TR<sub>1</sub> & TR<sub>2</sub> are connected feed back to one another. The collector of TR<sub>1</sub> is connected to the base of TR<sub>2</sub> through the capacitor C<sub>1</sub> & vice versa. Emitters of the both transistors are connected to the ground. collector. load resistor R<sub>1</sub> and R<sub>A</sub> and the biasing resistors R<sub>2</sub> and R<sub>3</sub> are of the equal values. C<sub>1</sub> and C<sub>2</sub> are of equal values.

Given,

$$\text{Frequency of oscillation} = 100 \text{ kHz}$$

Let,

$$\text{capacitor } C_1 = C_2 = C = 0.1 \mu\text{F}$$

The on time of transistor  $Q_1$  and the off time transistor  $Q_2$  is given by,

$$t_1 = 0.69 R_3 C_1$$

$$t_2 = 0.69 R_2 C_2$$

Hence total time period of square wave,

$$t = t_1 + t_2$$

$$= 0.69(R_3 C_1 + R_2 C_2)$$

As  $R_1 = R_2 = R$  &  $C_1 = C_2 = C$  the frequency of square wave will be,

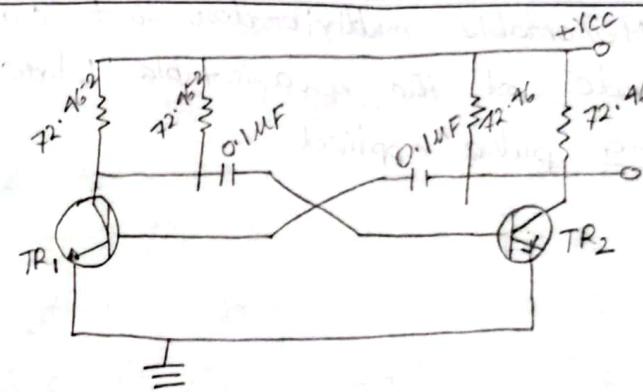
$$f = \frac{1}{t} = \frac{1}{1.38RC}$$

$$\Rightarrow R = \frac{1}{1.38Cf}$$

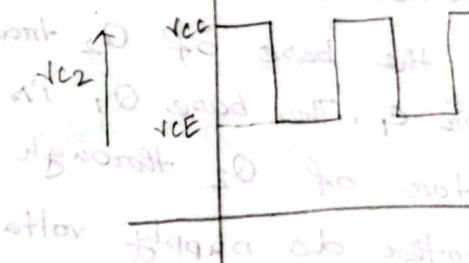
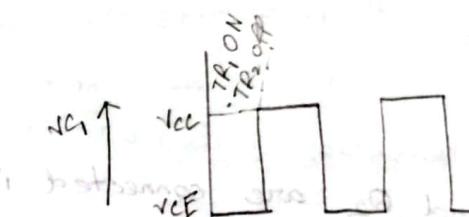
$$= \frac{1}{1.38 \times 0.1 \mu\text{F} \times 100 \text{ kHz}}$$

$$= \frac{1}{1.38 \times 0.1 \times 10^6 \times 100 \times 10^3}$$

$$\Rightarrow 7.246 \Omega$$

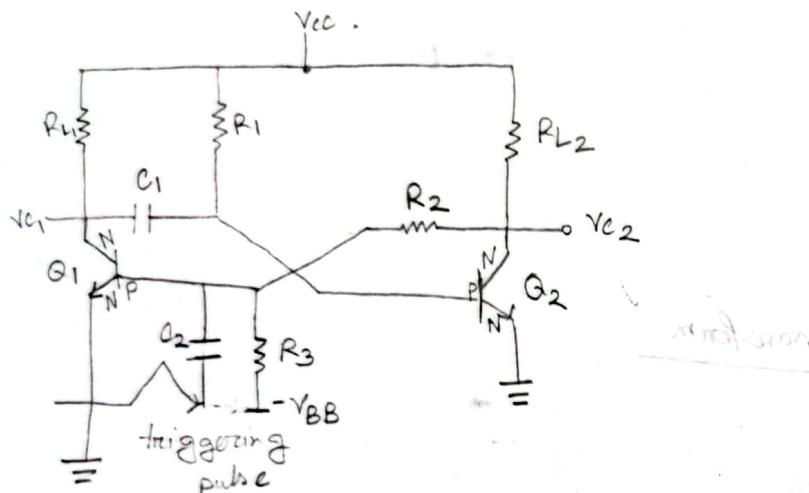


### Waveform



3) Design a Monostable multivibrator that can remain 1 minute at the quasi-stable state after triggering pulse applied.

Ans



Monostable multivibrator.

Two transistors  $Q_1$  and  $Q_2$  are connected in feedback to one another collector of transistor  $Q_1$  is connected to the base of  $Q_2$  transistor through the capacitor  $C_1$ . The base  $Q_1$  is connected to collector of  $Q_2$  through the resistor  $R_2$  and another dc supply voltage  $-V_{BB}$  is given to the base of  $Q_1$  through  $R_3$ . Trigger pulse is given to  $Q_1$  through capacitor  $C_2$ . to change its state.  $RL_1$  and

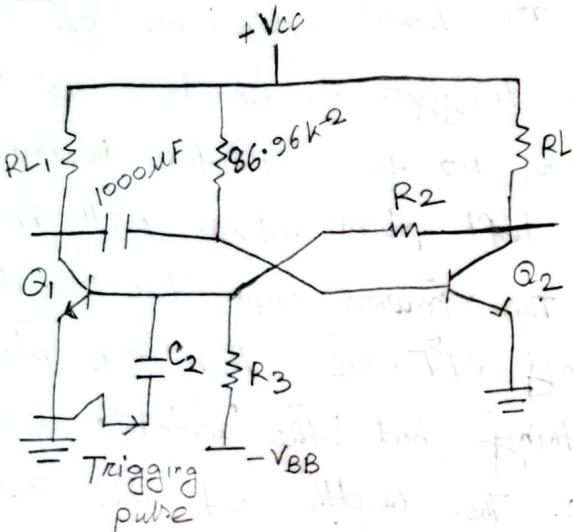
and  $RL_2$  are Load resistors of  $Q_1$  &  $Q_2$ . On Applying trigger to the base of  $Q_1$ , it will turn on, so the collector terminal of  $Q_1$  and the left plate of a will be shorted to ground. This causes capacitor to discharge while turning OFF  $Q_2$ . This off state of  $Q_2$  is nothing but the stable or quasi-stable state. The width of the output pulse depends upon RC time constant. The duration pulse is given by,

$$T = 0.69 R_1 C_1$$

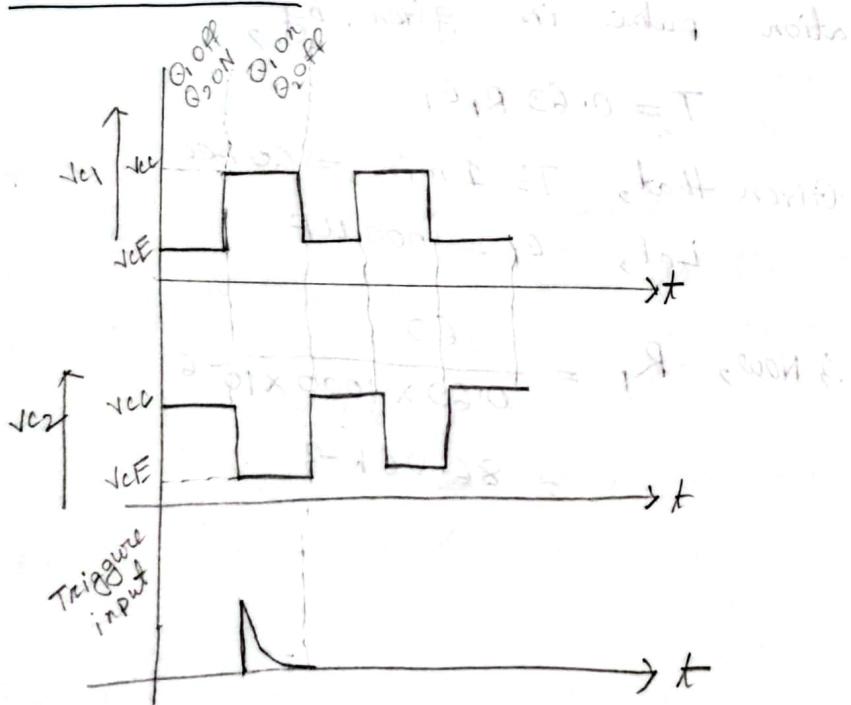
Given that,  $T = 1 \text{ min} = 60 \text{ sec}$

Let,  $C_1 = 1000 \mu\text{F}$

$$\therefore \text{Now, } R_1 = \frac{60}{0.69 \times 1000 \times 10^{-6}} \\ = 86.96 \text{ k}\Omega$$

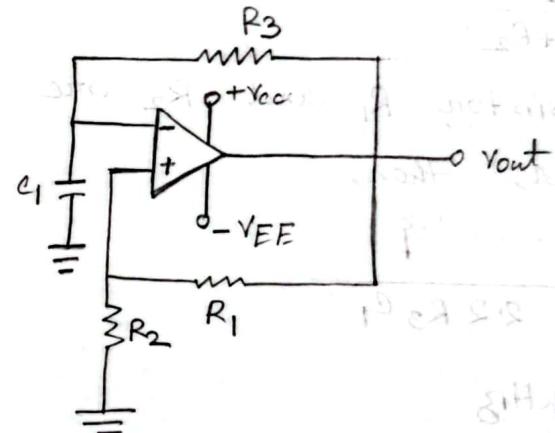


Output wave form



- ③ By using an OPAMP, design a relaxation oscillator to oscillate at the frequency of 10 KHz.

Ans



relaxation oscillator is defined as a non linear electronic oscillator that can generate a non sinusoidal repetitive output signal. To produce a cycle, the capacitor and inductor charge and discharge continuously. The frequency of the cycle of oscillation depends on the time constant of  $C_1$  &  $R_3$ . Here,  $R_1$  &  $R_2$  play a critical role in determining the frequency of the output. So, the relaxation oscillator formula:-

$$f = \frac{1}{2R_3 C_1 \ln\left(\frac{1+k}{1-k}\right)}$$

Here,

$$K = \frac{R_2}{R_1 + R_2}$$

If the resistor  $R_1$  and  $R_2$  are equal to each other, then,

$$f = \frac{1}{2.2 R_3 C_1}$$

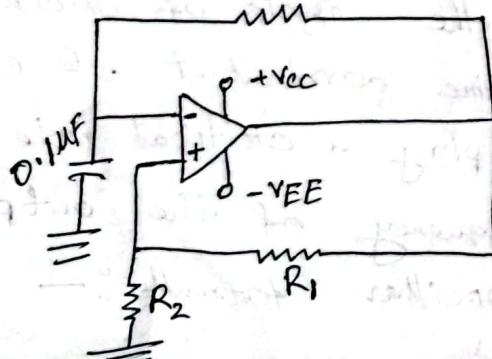
given  $f = 10 \text{ kHz}$

Let,  $C = 0.1 \mu F$

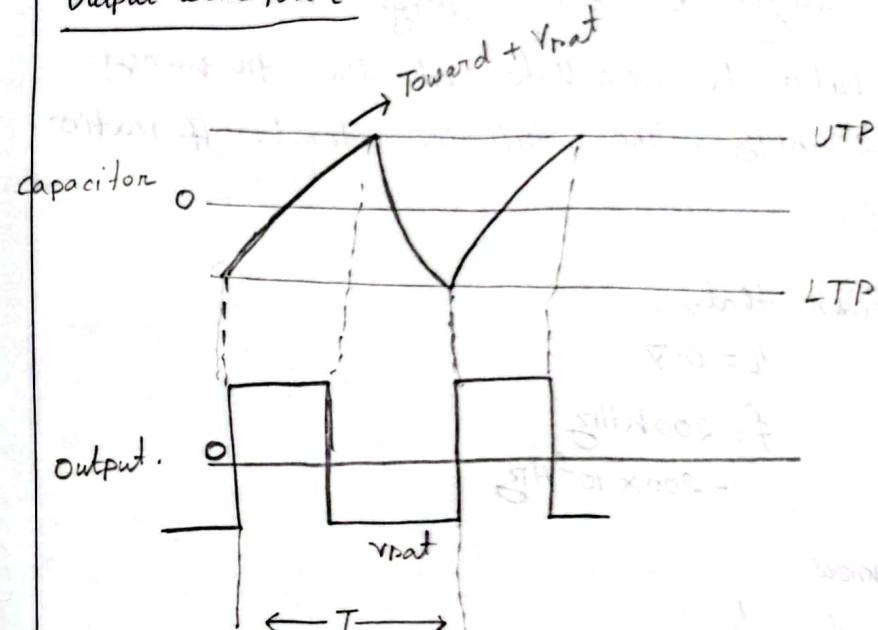
Now, 1 standards will

$$R_3 = \frac{1}{10 \times 10^3 \times 2.2 \times 0.1 \times 10^{-6}}$$

$$= 0.45k - 2$$



### Output waveform



⑤ By using a UJT, design a relaxation oscillator to oscillate at the frequency of 200kHz. The intrinsic stand-off ratio = 0.7.

Ans Given that,

$$n = 0.7$$

$$f = 200 \text{ kHz} \\ = 200 \times 10^3 \text{ Hz}$$

We know,

$$f = \frac{1}{T}$$

$$T = \frac{1}{f} = \frac{1}{200 \times 10^3} = 5 \times 10^{-6} \text{ sec.}$$

We know,

$$T = R_3 C \ln \left( \frac{1}{1-n} \right)$$

$$= R_3 C \ln \left( \frac{1}{1-0.7} \right)$$

$$= R_3 C \ln \left( \frac{10}{3} \right)$$

$$\Rightarrow R_3 = \frac{T}{C \ln \left( \frac{10}{3} \right)}$$

Let,  
 $C = 0.1 \mu F = 0.1 \times 10^{-6} F$

$$\therefore R_3 = \frac{5 \times 10^{-6}}{0.1 \times 10^{-6} \times \ln \left( \frac{10}{3} \right)} \\ = 41.53^{-2}$$

Again,

$$n = \frac{R_1}{R_1 + R_2}$$

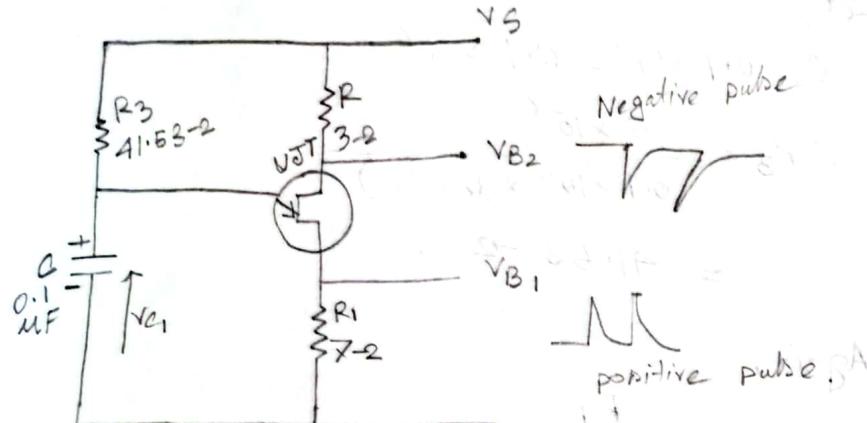
$$\Rightarrow \frac{1}{n} = \frac{R_1 + R_2}{R_1} = 1 + \frac{R_2}{R_1}$$

$$\Rightarrow \frac{1}{0.7} - 1 = \frac{R_2}{R_1}$$

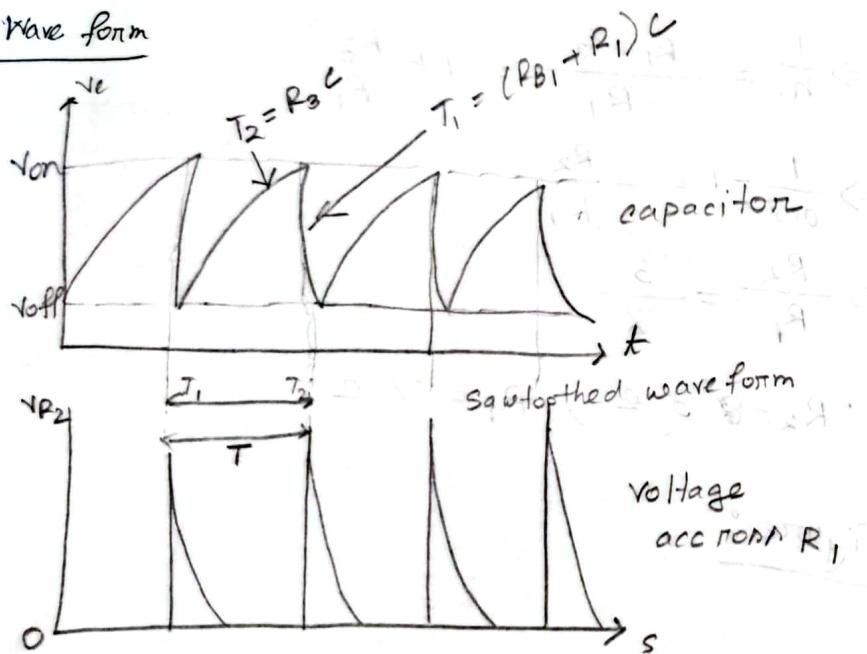
$$\Rightarrow \frac{R_2}{R_1} = \frac{3}{7}$$

$$\therefore R_2 = 3 \Omega ; R_1 = 7 \Omega$$

Figure :



Wave form



- ④ By using a 555 IC, design an Astable multivibrator to oscillate at the frequency of 50 kHz.

Ans

$$f = 50 \text{ kHz} \\ = 50 \times 10^3 \text{ Hz}$$

Let,  
duty cycle,  $50\% = 0.5$

Now,

$$T_{ON} = 0.693 R_A C \quad \dots \textcircled{I}$$

$$T_{OFF} = 0.693 R_B C \quad \dots \textcircled{II}$$

$$D = \frac{T_{ON}}{T_{ON} + T_{OFF}}$$

$$\Rightarrow D = \frac{0.693 R_A C}{0.693 R_A C + 0.693 R_B C}$$

$$\Rightarrow D = \frac{R_A}{R_A + R_B}$$

$$\Rightarrow 0.5 = \frac{R_A}{R_A + R_B} \quad [\text{duty cycle } 50\%]$$

$$\Rightarrow 0.5R_A + 0.5R_B = R_A$$

$$\therefore R_A = R_B \quad \text{--- (ii)}$$

Now,

$$f = \frac{1}{0.693(2R_B)C} \text{ Hz}$$

Let,

$$C = 0.1 \mu F$$

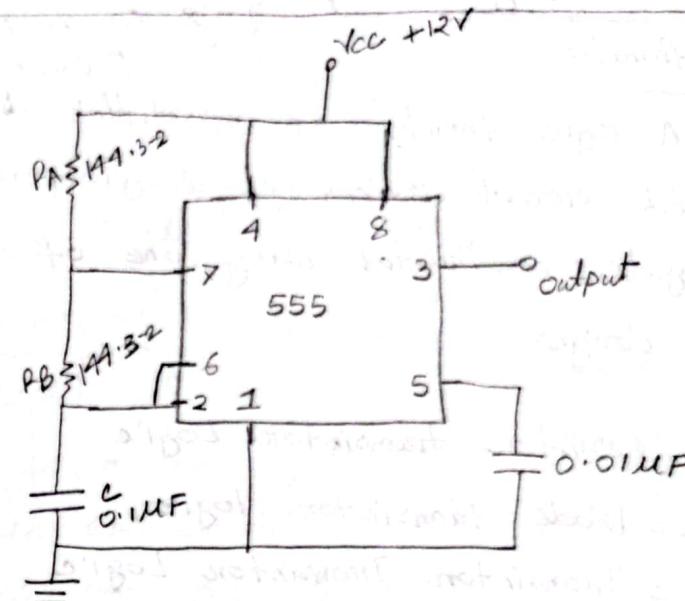
$$f = 50 \times 10^3 \text{ Hz}$$

$$50 \times 10^3 = \frac{1}{0.693(2R_B)0.1 \times 10^{-6}}$$

$$\Rightarrow R_B = 144.3 \Omega$$

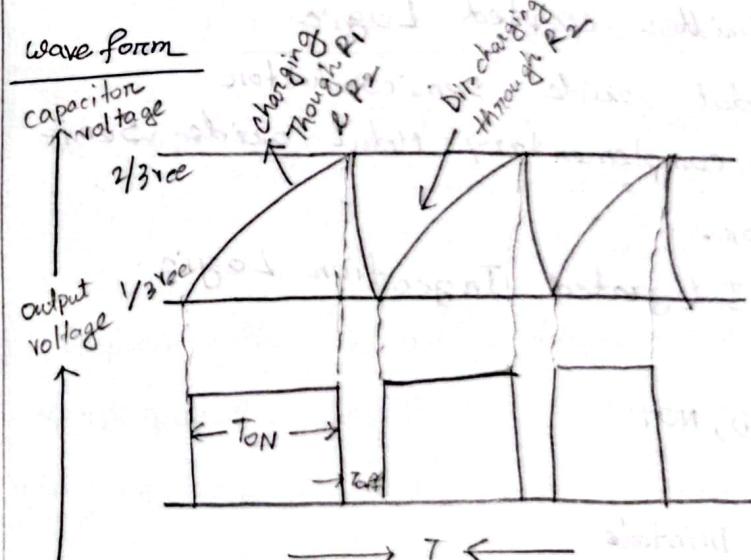
$$\therefore R_A = 144.3 \Omega$$

### Circuit design



Astable multivibrator using 555 IC.

### Waveform



## Logic family

### Logic family

A logic family of monolithic digital logic integrated circuit devices is a group of electronic logic gates constructed using one of several different designs.

- 1) RTL = Resistor Transistor Logic
- 2) DTL = Diode Transistor logic
- 3) TTL = Transistor Transistor Logic
- 4) CCTL = Complementary Transistor Logic
- 5) ECL = Emitter coupled Logic
- 6) MOS = Metal Oxide Semiconductor
- 7) CMOS = complementary Metal Oxide Semiconductor.
- 8) IIL = Integrated Injection Logic.

~~Q~~ ~~TTL~~  $\rightarrow$  NAND, NOT

~~X~~ MOS  $\rightarrow$  NOT

~~X~~ TTL, CMOS  $\rightarrow$  Tristate  
current source, sink.

2) CMOS - NOT / 0  
T, CM = Tristate

### ⑧ Logic family:

Each fundamental approach used to produce different types of digital integrated circuit is called logic family.

### propagation delay : / gate delay :

The length of time which starts when the input to a logic gate becomes stable and valid to change to the time that the output of that logic gate is stable and valid to change. (logique)

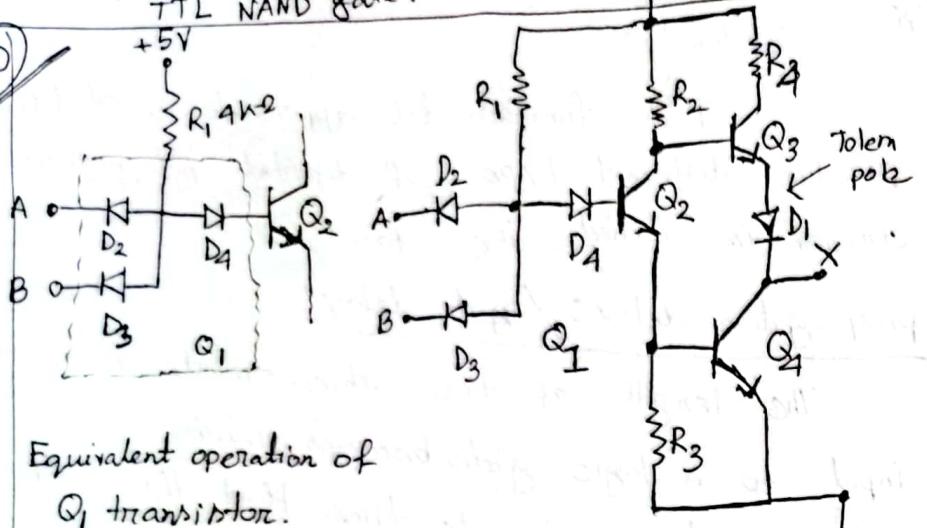
input  $\xrightarrow{\text{propagation delay}}$  output.

It depends on the sub family's property  
It " " construction of logic gate

### ⑨ Explain the internal diagram of a TTL NAND gate ?

Ans: The basic TTL Logic circuit is the NAND gate, shown in figure:

Explain the internal diagram of TTL NAND gate.

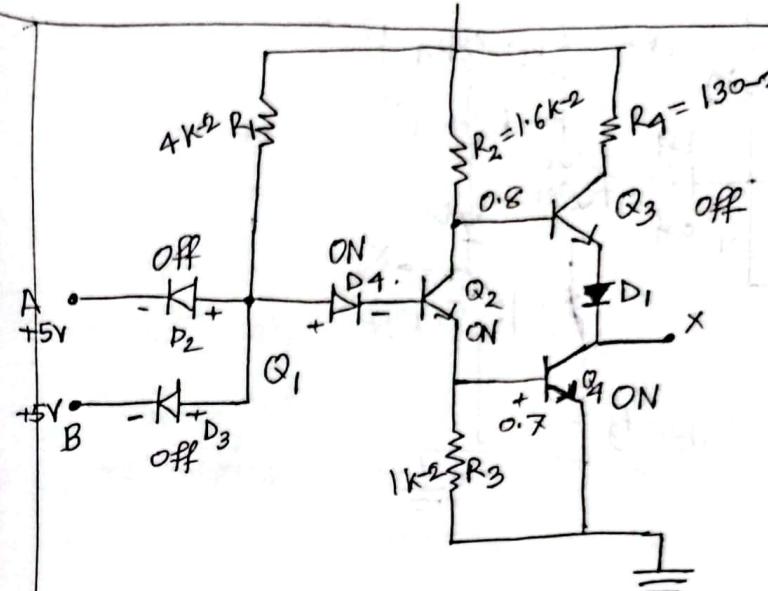


Equivalent operation of  
Q<sub>1</sub> transistor.

TTL NAND gate.  
(Tatem pole output)

Input	Output
A or B or or both are Low < 0.8V	Q <sub>1</sub> off
High > 0.8V	Q <sub>1</sub> on

\* मध्ये २वा इस्तो High  
output Low.



circuit state for low output

Here input A & B both are high, so D<sub>2</sub> & D<sub>3</sub> are reverse bias. and D<sub>4</sub> forward bias. So in R<sub>1</sub> current will flow which on Q<sub>2</sub> transistor. So, current will flow through R<sub>2</sub> and Q<sub>4</sub> will be on and there will be  $0.7V$  and remaining  $0.1V$  ( $0.8 - 0.7$ ) will in Q<sub>2</sub> collector voltage. So in Q<sub>3</sub> we will have  $0.1V$  which is very low which can't on Q<sub>3</sub> and D<sub>1</sub>. So we will get low voltage  $0.4V$ .

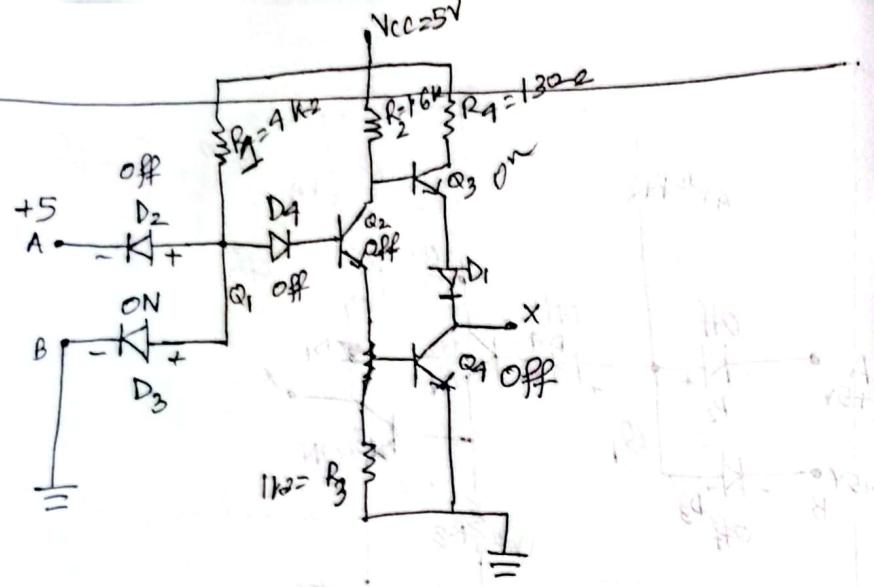


Fig: Circuit state for high output

Here A High and B Low inputs So No current will flow through  $R_1$  and  $D_4$  and  $Q_2$  will off. As  $Q_2$  off, There will be no emitter current, so  $Q_4$  will also off. So all current will flow through  $R_2$  and  $Q_3$ . and  $Q_3$  and  $D_1$  will on with sufficient voltage.  $\therefore$  we will get  $(5 - (0.7 \times 2)) = 3.6V$  will have in X.

\* Draw back of Totem pole Nand gate  
 \* पर्याप्त input होने change होने output change हो। अतः एक transistor on आवश्यक off हो। Totem pole में किसी भी स्थिति में जब वो (Q<sub>3</sub>, D<sub>4</sub>) किसी घटना पर on हो पर्याप्त Power supply होके Large current बहुमात्र वर्धन होता है जिसका Drawback होता है कि इसकी open collector output होने का हो।

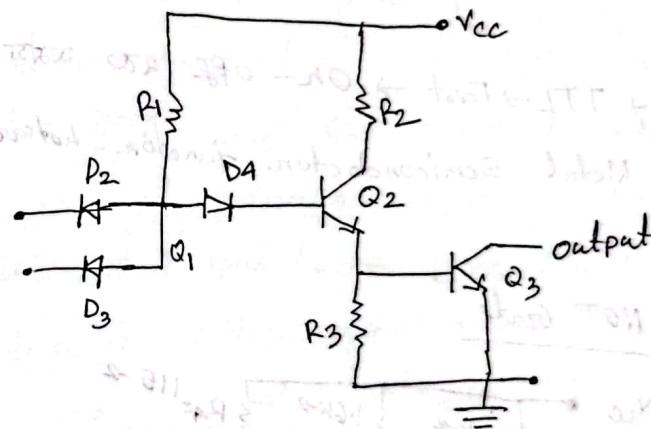


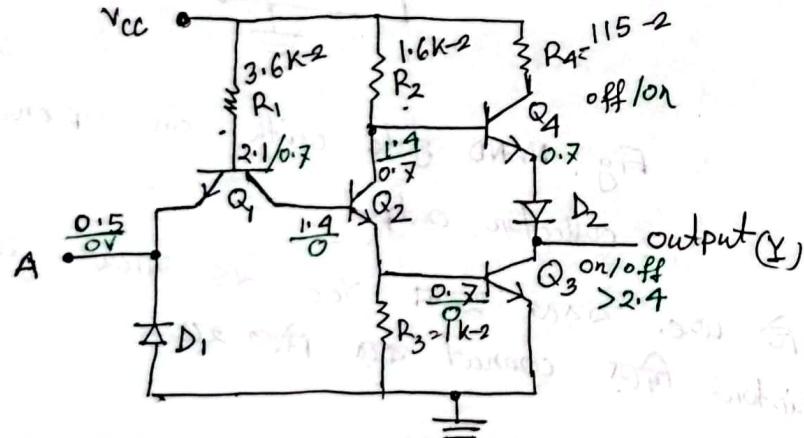
Fig: NAND gate with an open collector output

एक use करते हैं इसे Vcc वाले आवश्यक Resistors द्वारा connect करा दिया हो।

\* ২টা, ৩টা NAND gate এর output যদি প্রস্তাব  
connect করা হয় (wired and) এই operation Totem  
পথ জেলে করা যাবে না। এই PNP এবং NPN একাধিক  
gate এর output একাধিক Tie করে দেয়া হয়।  
তাহলে ৩টা AND gate এর মতো কার্য করে এবং  
হলে Totem-pole এর রেজন ambigious অবস্থার  
মুছি হয় Transistor এ Large current flow  
হলে ৩টা গতি হয়ে নষ্ট হয় যায়।

Schottky TTL  $\rightarrow$  Fast  $\rightarrow$  On-off হত অবস্থা কর  
নাও। Metal Semiconductor junctions - hotcarrier  
junction.

### \* TTL NOT Gate



Here,

if point A has 0V,  $\oplus$  input 0 and source 5V.  $Q_1$  is the plot of PN junction that requires 0.7V and  $Q_2$  requires 0.7V and  $Q_1$  is on,  $Q_2$  requires less voltage, so.  $Q_2$  is off. In this point  $R_2$  have much more voltage than 1.4. So  $Q_4$  become on, we get high output. In this process  $Q_3$  is off mood.

if point A has input 1,  $Q_1$  is off and  $Q_2$  is in saturation and fully on,  $Q_3$  is also on. and  $Q_4$  can't be on because there is not enough voltage (atleast 1.4).

so, we get output Low. ( $Q_2$  on থাকলে  $R_2$  দিয়ে  
resistor এ voltage drop হবে তবে  $Q_4$  on  
করাত কলে enough voltage পাবে না)

$A \rightarrow$  input  $\rightarrow 0 \rightarrow Q_1 = \text{On}, Q_2 = \text{Off}, Q_4 = \text{On}$   
output = high. ,  $Q_3 = \text{off}$ .

$A \rightarrow$  input  $\rightarrow 1 \rightarrow Q_1 = \text{Off}, Q_2 = \text{On}, Q_3 = \text{On},$   
 $Q_4 = \text{Off}$ . output = Low.

## \* CMOS Not Gate / inverter

TTL	CMOS
① Uses bipolar junction transistor.	① Field Effect transistor.
② Lower density than CMOS.	② Greater density than TTL.
③ Consume more power.	③ Less power.
④ Operate at low speed.	④ High speed.
⑤ require more space	⑤ require less space
⑥ Larger than CMOS	⑥ It circuit have better noise immunity

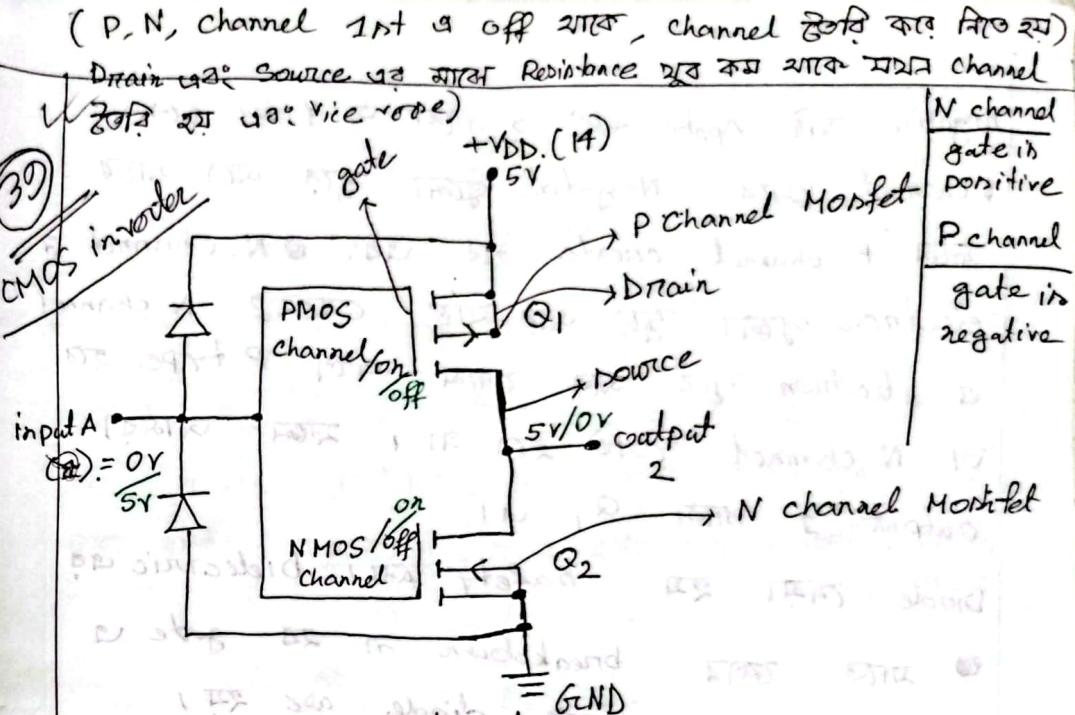


Fig: CMOS Not gate / inverter

Here if we apply 1 in input A (5V), Q1 goes through both side of gate; in Q1 there is P channel mosfet, the channel can't be created, because, there will much resistance but in Q2 there is N channel mosfet, So the channel will be created and the resistance will be low here, so we get our out put in Low voltage means in Q2 will be 0 Again, if we apply 0 voltage in input A, तरीं

negative যদি Apply করি ২ পাশে অ flow হবে +  
 & channel থেকে Negative শুল্ক দ্রুত যাবে মাত্র  
 ফলে P channel create হবে এবং QN channel is  
 electron শুল্ক দ্রুত যাবে যেহেতু N channel  
 এ electron দ্রুত যাবে তাই P type হবে  
 আবার N channel সৈতে হবে না, ফলে অমর্দা  
 output ১ পাশে Q, এব।

Diode সেন্স হয় safety এন্ড Dielectric এবং  
 যাও কেবল breakdown ন হয় gate এ  
 voltage এবং অন্য ডায়ড diode এই,  
 (যাও floating input / unused input থাকে এ  
 & এলেটা পাশে connection রেখায় CMOS টাইপ  
 করে দিত পাই তাই তা Vcc / GND এবং যাও  
 connect করে দিত যাও safety এন্ড এন্ড)

$A = \text{Low}$ ;  $Q_1 = \text{conducting}$ ,  $Q_2 = \text{Non conducting}$   
 $y = \text{output } V_{DD}$ .

$A = \text{high}$ ,  $Q_1 = \text{non conducting}$ ,  $Q_2 = \text{conducting}$

$y = \text{Low}$ .

Buffer এর circuit কোর্ট অবস্থা circuit এ signal pass করি

### Triode buffer

Triode buffer use করে একই Databus এ  
 শুল্ক Device share করে থাকে,

# Read / Write করার জন্য input / output buffer

থাকে Buffer enable করে Read / Write করতে হয়  
 \* Read / write একমাত্র করা যাবে না, কারণ Databus  
 এটা থাকে, Buffer ২ রকম হতে পারে, inverting & non  
 inverting.

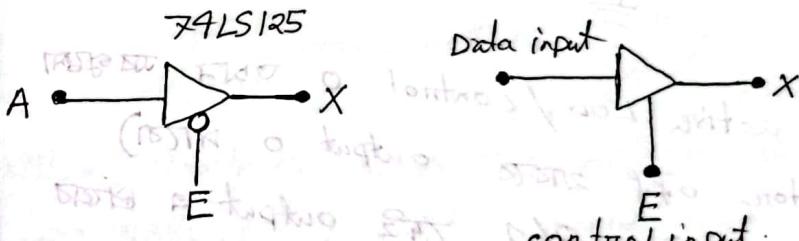


Fig: Triode noninverting buffer.

E	X
0	A
1	HiZ

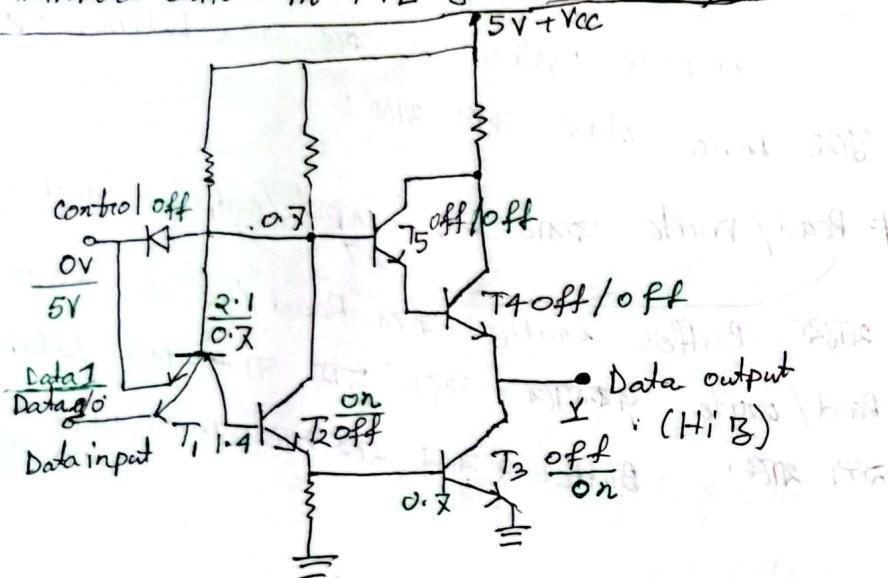
E	X
0	HiZ
1	A

Not symbol আছে E এর থাকে 0

দিলে Enable হবে আব যেহেতু noninverting  
 input এ থা দিব তাই output আব।

1st for Enable  
 হব, input এ থা  
 দিব তাই output.

### Tri-state buffer in TTL gate (inverting)



→ এখন active low/control ০ অধন মাছন  
Transistor off থাকলে output ০ পাবো।

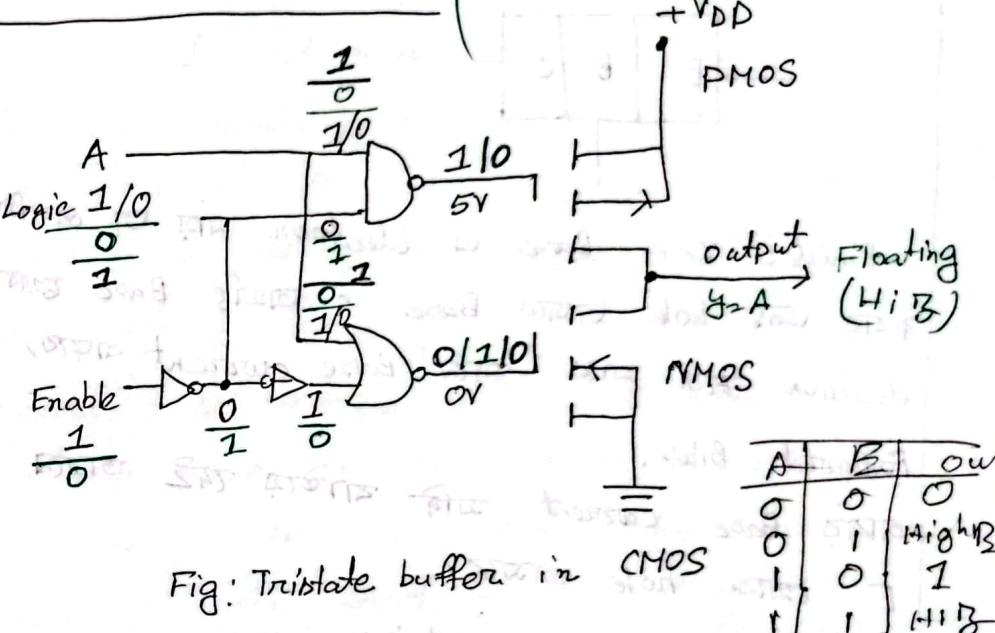
input ০ মতই ০/১ টেক্সে output ০ পেলে  
পদব না।

→ এখন active high/control 1/5V টেক্সে উভ

T<sub>2</sub>, T<sub>3</sub> on রে ; T<sub>5</sub>, T<sub>4</sub> off. Data  
input 1 দিলে output ০ রে।

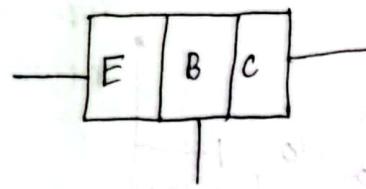
মাত্র data input ০ টেক্সে তবে T<sub>2</sub>, T<sub>3</sub>  
off হবে, রে T<sub>5</sub>, T<sub>4</sub> on হয়ে মাত্র ৩ভ  
output high/1 পাবো।

### Tri-state buffer CMOS (Non inverting)



→ Here enable 1 means NMOS gate ০ ও input 1  
এবং NAND gate ০ ও input 0. Now input A ০ ০/১  
মাত্র দেয়া থাকলে না হলে NMOS ০ ও output 1 এবং  
NOR এর output ০ পাবো। এখন NAND ০ ১/৫V  
means P channel create রে না, N channel  
এর input ০ জুড়ে N channel create  
হবে না। তাই output ০ রে।

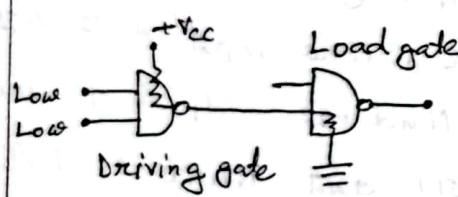
→ Enable ০ টেক্সে, and  $\frac{\text{input}}{\text{Logic 0}}$  দিলে NAND = 1, NOR = 1  
হয়। হলে P channel create হয় না But N channel cre-  
ate হয়। input = 1 দিলে P channel create করে; N create হয় না Y=A হবে।



Emitter  $\rightarrow$  Base  $\rightarrow$  electron যায় এ প্রক্রিয়া  
করার জন্য hole আয়ের Base এ অবস্থির Base হতে  
electron হলু যাবে তাই Base current হওয়ার,  
Forward Bias.

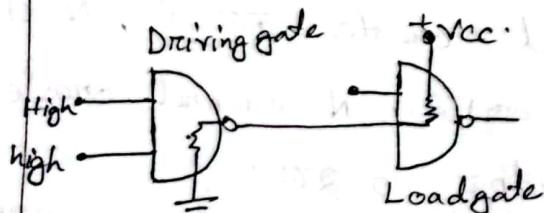
অবস্থি Base current হওয়ার কারণেই তাই তাইলে  
E হতে hole আয়ের,

### current Sourcing & sinking



#### current Sourcing

Driving gate supplies  
(source) current to  
load gate in highstate



#### current sinking

Driving gate  
receives (sink) current  
from load gate in  
Low state.

### 41) Fan out of TTL in

Fan out means Loading Factor. The maximum number of digital inputs that the output of a single logic gate can feed and the gates must be from same logic family.

Example: A logic gate that have fan out of 10 means, it can drive 10 logic inputs. If the number is exceeded, the output logic level voltages can't be guaranteed.

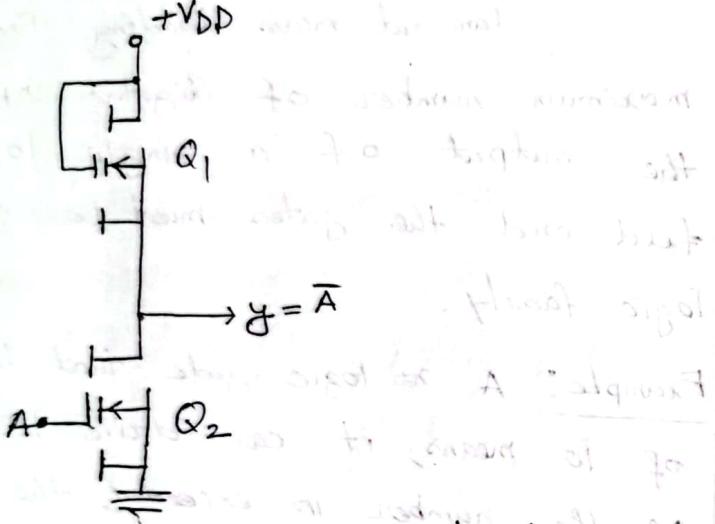
$$\text{Low state fanout(Low)} = \frac{I_{OL}(\text{max})}{I_{IL}(\text{max})}$$

Fan in: High " " (High),  $\frac{I_{OH}(\text{max})}{I_{IH}(\text{max})}$

The number of inputs of a gate that it can handle without its normal operation. Propagation delay increases with number of inputs.

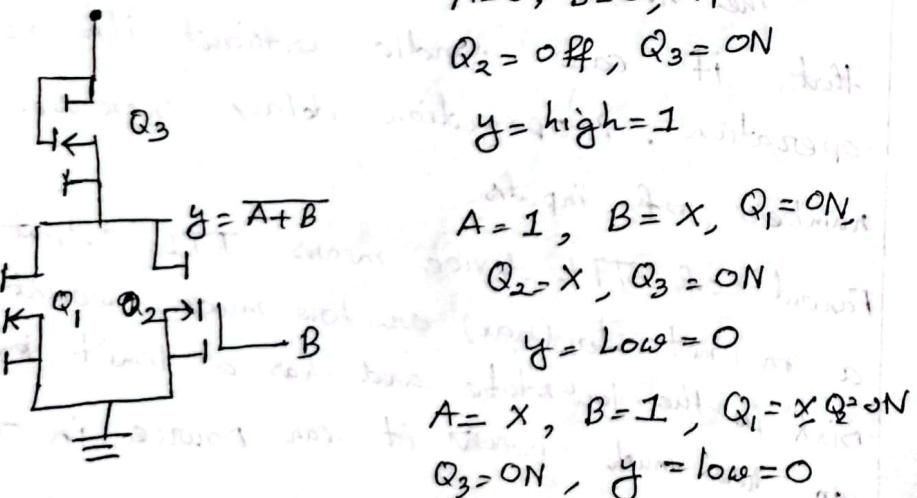
Fanout of TTL device means. TTL output has a limit  $I_{OL}(\text{max})$  on how much current it can sink in the lowstate and has a limit  $I_{OH}(\text{max})$  on how much current it can source in the highstate.

#### ④ N-MOS inverter:



$A=0, Q_2 = \text{off}, Q_1 = \text{on} \quad y = \text{high} = 1$   
 $A=1, Q_2 = \text{on}, Q_1 = \text{off} \quad y = \text{low} = 0$

#### N-MOS NOR



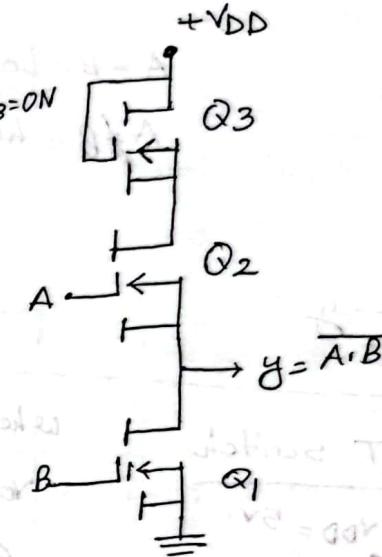
#### N MOS NAND

$A=1, B=1, Q_1=Q_2=Q_3=\text{on}$

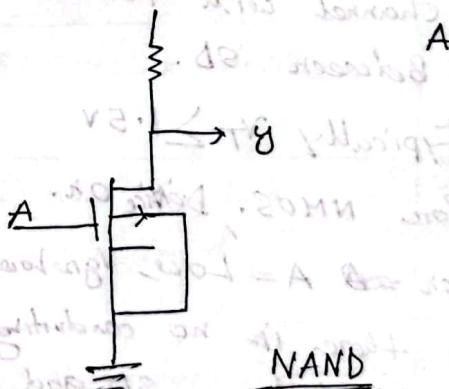
$y=0$

$A=0, B=X$

$B=0, A=X$



#### P MOS NOT inverter



$A=1, \text{PMOS not stop conducting}$

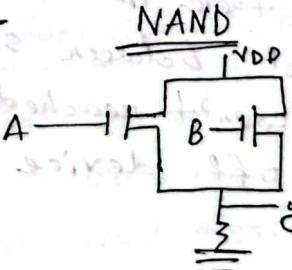
$y = \text{High}$

$A=\text{low}/0 \quad \text{PMOS = conducting}$

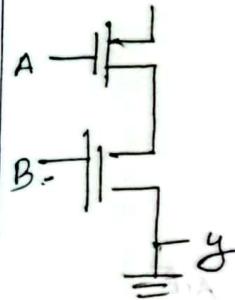
$y = \text{Vdd}$

$A=B=\text{high}, \quad y = \text{Low}$

$A/B=\text{high} \quad y = \text{high}$

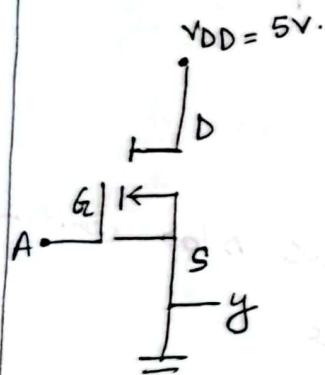


### NOR



$A = B = \text{Low}$ ,  $y = \text{high}$   
 $A \neq B = \text{high}$ ,  $y = \text{low}$

### (43) MOSFET Switch



when  $A = \text{high}$ ,  $V_{Gy}$  / voltage between ground and source is positive  $V_T$  is reached. So, conducting channel will form between SD.

Typically  $V_T \geq 1.5V$

for NMOS, Device On.

when ~~A = Low~~,  $V_{Gy} = \text{Low}$

So there is no conducting channel between SD and  $V_T$  won't be reached so  $y = \text{off}$  device off.

(45)

high fan out capability

TTL

low fan out capability

MOS

1) Transistor Transistor Logic.

2) current operator device

3) requires much space.

4) much power consuming

5) complex device

6) used in Lab

experiment.

1) Metal Oxide Semiconductor logic

2) voltage operator device

3) less space

4) less power consuming

5) small device, simple

6) dominants in SSI and MSI market

### Characteristics of ECL

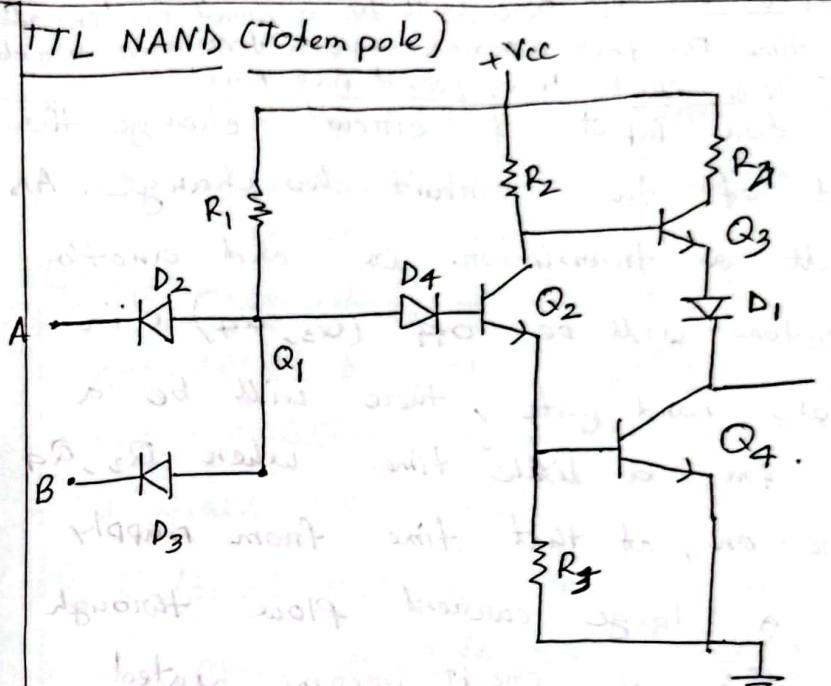
① Faster available logic family

② The transistors never saturated, so switching speed very high.

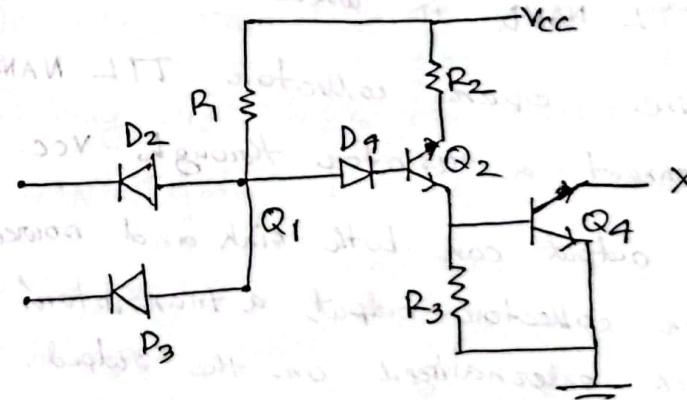
- ③ propagation delay time is 360 ps.  
 ④ The logic levels are nominally  $-0.8V$  and  $-1.2V$  for logic 1 and 0 respectively  
 ⑤ ECL logic block usually produces an output and its complement.  
 ⑥ Eliminate the need of inverter  
 ⑦ Fanout around 25  
 ⑧ power dissipation in 25 mW.

### 14 batch

- ② a) TTL not gate  
 b) CMOS Not gate  
 c) TTL NAND gate.  
 ⑤ d) compare the properties of open collector TTL NAND and Totempole TTL NAND:



TTL NAND (open collector)



~~the on action of  $Q_3$ . For this there will be a small fraction of Properties time. For few nano second both transistors are conductive. There will be heavy current from supply.~~

1) When for input of circuit change the output of the circuit also change. As a result one transistor on and another transistor will be off ( $Q_3, Q_4$ ). In totem pole NAND gate, there will be a situation for a little time when  $Q_3, Q_4$  both are on, at that time from supply power, a large current flow through it, for this, the circuit become heated and it damages. To solve this problem open collector TTL NAND is used.

2) To use open collector TTL NAND gate connect a resistor through Vcc.

3) Totem pole output can both sink and source. For open collector output, a transistor's collector is externalized on the output. Open collector output only sinks.

4) Totem pole offers low output impedance

in both the high and low output states.

Open collector TTL gate, output stage doesn't have  $Q_3$ , output is taken of transistor  $Q_4$ .

① in totem pole: output of the two end gate can't be tied together

open collector: can be tied together using a wired AND method.

⑤ External pull up resistor is not required in case of totem pole

open collector: External pull up resistor is required

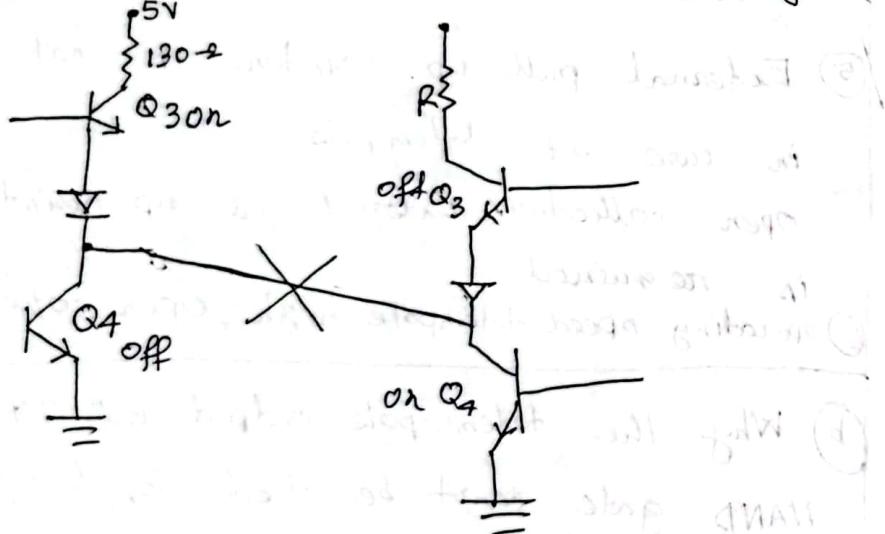
⑥ operating speed totem pole high, open collector low

b) Why the totem-pole output of TTL NAND gate can't be tied together?

~~Ans~~ Transistor  $Q_3$  and  $Q_4$  in TTL constitute totem pole output. In such an arrangement either  $Q_3$  or  $Q_4$  conducts at a time.

Because totem pole output of the TTL gate always

has one transistor cut off and the other turned on, we can't connect two output together. If one is trying to pull the output high the other is trying to pull it Low. we will have a very low impedance path to ground and a large current from supply  $+V_{CC}$  will flow which we'll damage the output transistor totem pole TTL arrangement.



if produce harmful current through  $Q_4$ .

13 batch

④ a

	ECL	TTL	CMOS	IIL
①	Emitter Coupled Logic	Transistor Transistor Logic	complementary Metal oxide Semiconductor	Integrated Injection Logic.
②	BJT	BJT	BFET	BJT
③	consume more power than CMOS	high power consumption	Low power	Low power
④	used in making ASLT circuit.	used in Lab experiment	in all micro-computer chips.	used in VLSI integrated circuit.
⑤	good	very good	noise immunity	It has high noise immunity
⑥	Noise margin lower	average	highest	highest
⑦	Fan in $> 10$	12 - 14	$> 10$	
⑧	Fan out 25	10	25	56

### Duality character for CMOS

CMOS is made with PMOS and NMOS. An important characteristic of a CMOS circuit exists between its PMOS and NMOS transistors. A CMOS circuit is created to allow a path always to exist from the output to either the power source or ground.

A CMOS consist of PMOS and NMOS. It has the characteristics of both P & NMOS. This is the duality.

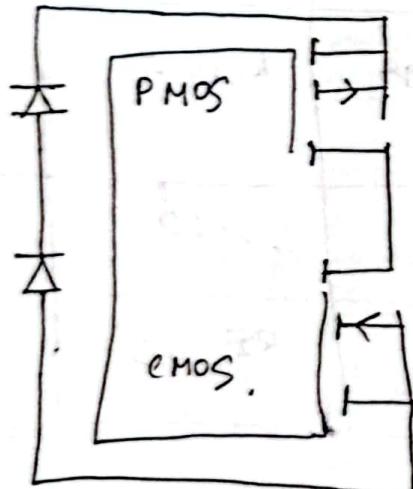


Fig: CMOS inverter

④  $V_{DD}$  = It stands for voltage at drain.

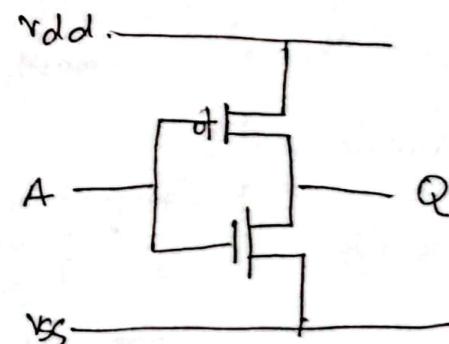
In some PMOS it is negative but pure PMOS chips found rarely.

$V_{SS} = V_{DD}$  stands for voltage at source.

PMOS devices might be positive, but PMOS is relic, so it must be the most negative on the chip won't work.

$V_{CC}$   $\Rightarrow$  Voltage at collector and it is primarily used for bipolar device.

$V_{EE}$  = Voltage at emitter and it is usually most negative.



#### 44 MOS Logic gate characteristics:

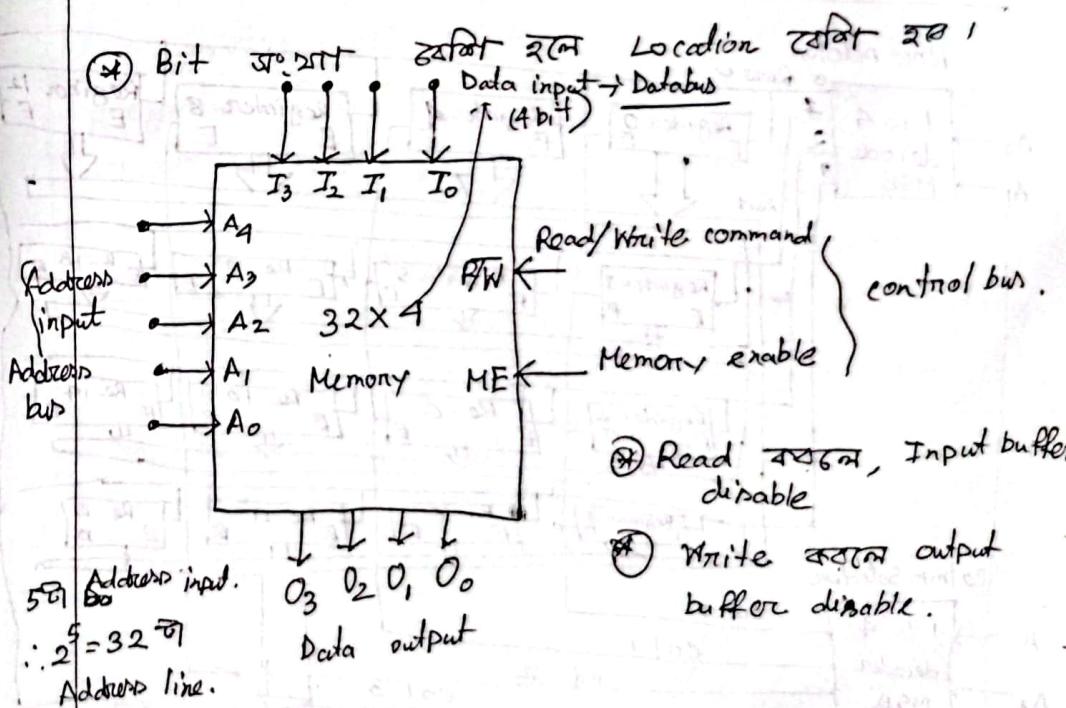
- ① MOS is high speed device than TTL.
- ② power consuming is less.
- ③ small, simple device so take less space than TTL.
- ④ The increased packing density of MOS transistor over bipolar has resulted in PROMs.
- ⑤ In high speed MOS, there is high packing density.

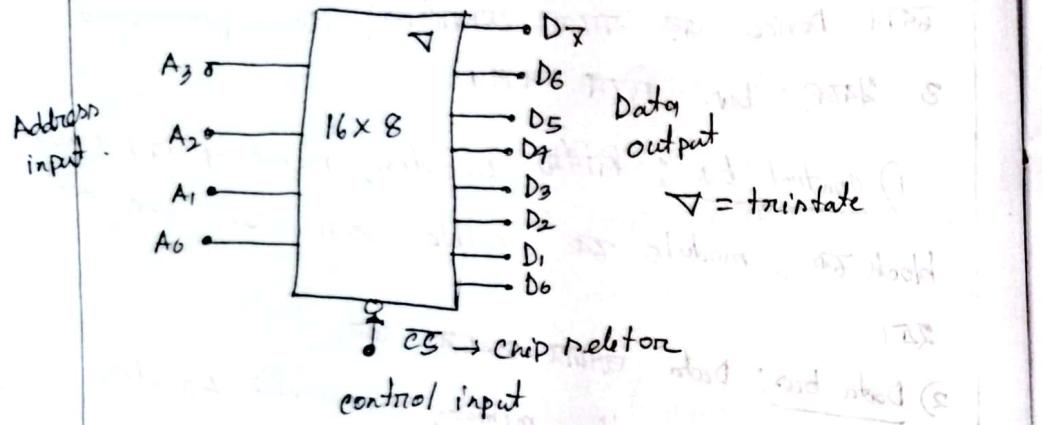
#### Memory

କୋଡ଼ା ଦେବି ଏବଂ ଏକ୍ସର୍-ମେମୋର୍ ମିକ୍ରୋ ପ୍ରାକ୍ଷ୍ସର୍

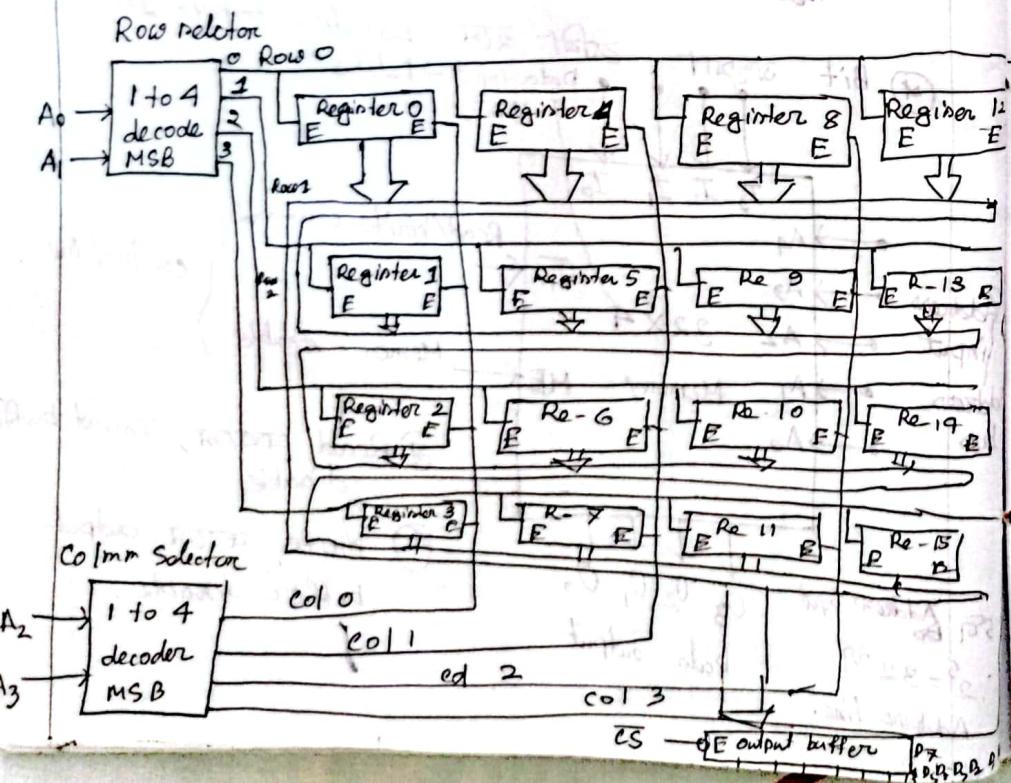
୩ ବ୍ୟବସ୍ଥା ବୁନ୍ଦିଲେ, କବା।

- 1) control bus: Address Location, memory as whole block କାହାରେ, module କାହାରେ enable କରାଯାଇବା କାହାରେ
- 2) Data bus: Data କରାଯାଇବା କାହାରେ
- 3) Address bus: exactly memory କାହାରେ location select କରାଯାଇବା





internal structure of 16x8 ROM



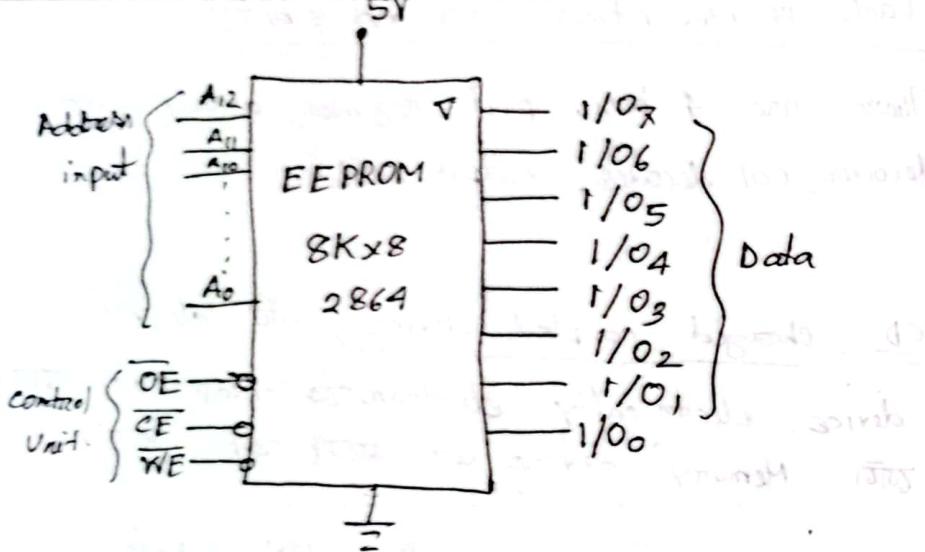
Each register stores one bit. 8 bit

There are 4 basic part: register, array, row decoder, col decoder, output buffers.

CCD: charged coupled device, an electronic device. electrically erasable & trap करने सकता है।  
Memory device, यह मात्र करने का है।

\* EPROM: word window for UV erasing.  
एप्रोम एटि window बाके UV erasing करने के programming ए फूल हल्ले जा मुद्दे ठम्हा। अरे अपना हल्ले बड़ो फूल हल्ले उपरे मुद्दे सक्ता है।

EEPROM: Electrically Erasable programmable memory. एप्रोम को एटि memory location program करने फूल हल्ले के specific एवं वह location के मुद्दे नियम करने program करा सकता है।

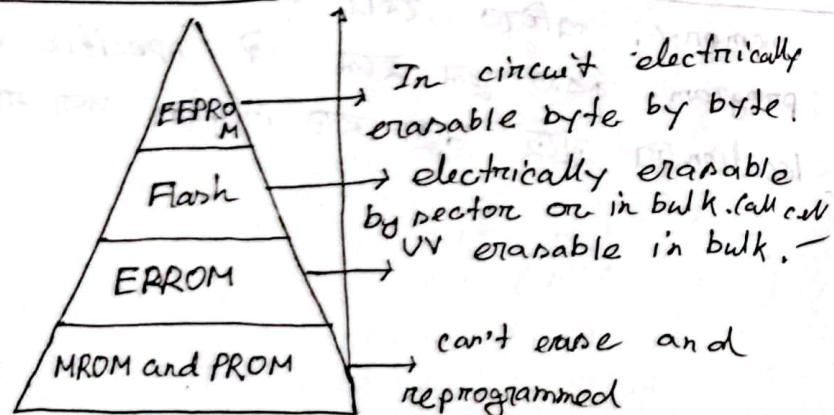


এটি এমন চেম্পি সংস্করণ করা হয়। এই মোড়ে

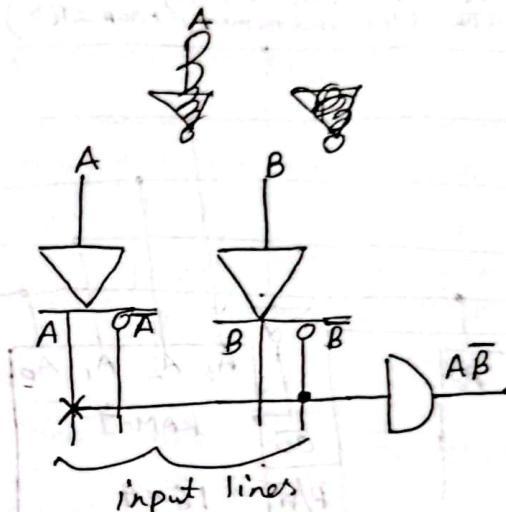
$8K \times 8 \rightarrow$  একটি location = no of bit / 8 bit

↓  
no of memory location  $8K = 2^{13}$

Device complexity and cost

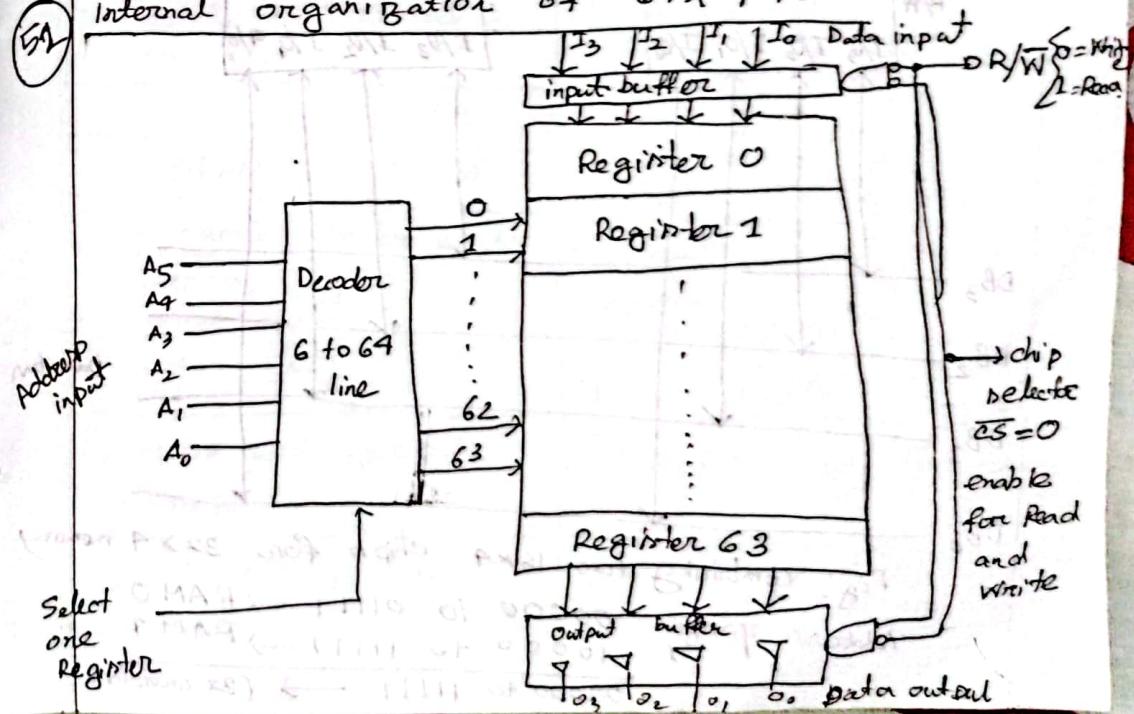


## Programmable logic device PLD:



X → in fact fuse  
• → hard wired

internal organization of 64x4 RAM:



④ increase Location increase but bit remain same.  
 (at a time Data Read / write हो ना) (word name)  
 (1st memory का तरह 2nd memory तक नहीं चले)

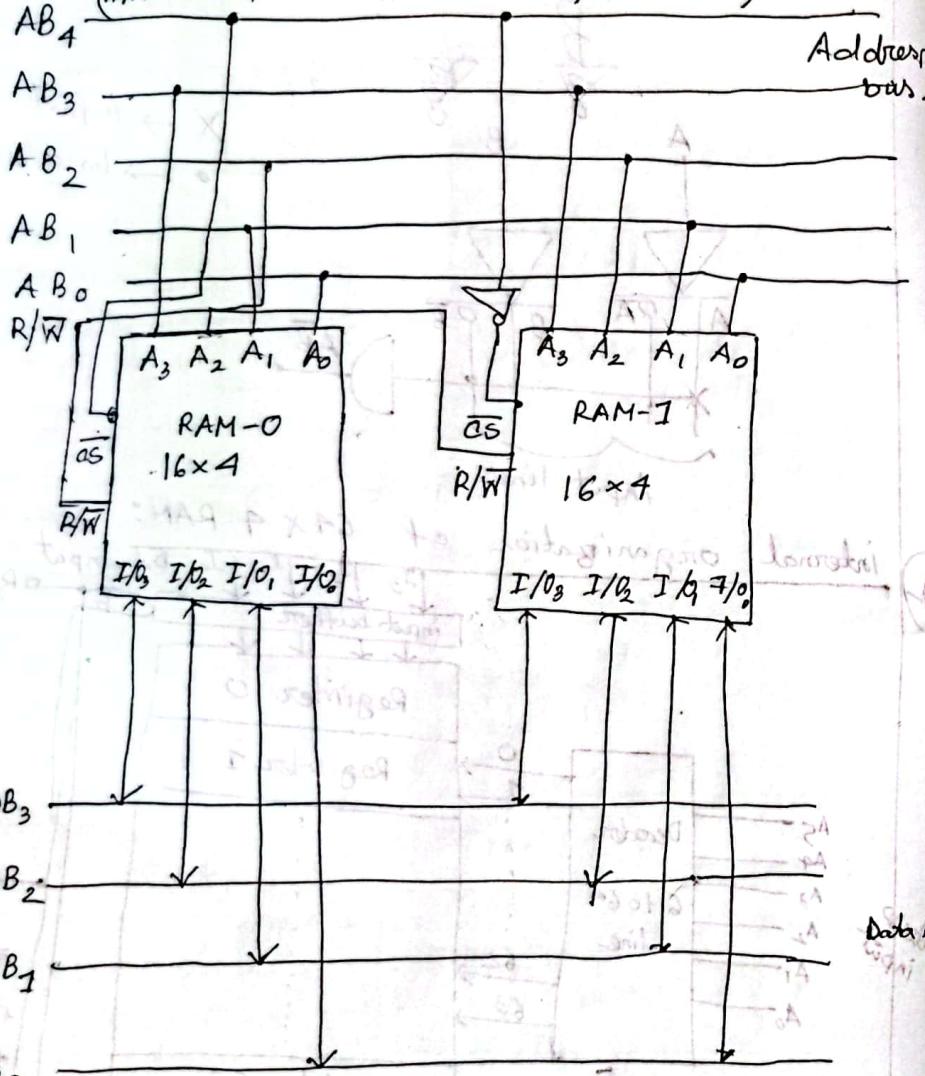


Fig: combining two  $16 \times 4$  chips for  $32 \times 4$  memory

Address range      00000 to 01111  $\rightarrow$  RAM 0

10000 to 11111  $\rightarrow$  RAM 1

00000 to 11111  $\rightarrow$  (32 words)

### Question bank

④

RAM

SAM

1) Random Access Memory

1) Sequential Access Memory

2) Data can be accessed in any order.

2) Data can be accessed in a sequential way

3) Access time is constant.

3) Access time is not constant

4) Not time consuming

4) time consuming

5) Access time is smaller than SAM.

5) larger than RAM

DRAM

SAM

1) Dynamic Random access memory

1) Static Random Access memory

2) Speed Low

2) Speed high

3) Doesn't need periodic refreshing

3) Doesn't need refreshing

4) Data storage device capacitor.

4) Data storage device Transistor.

5) used for main memory	5) used for cache memory
RAM	ROM
1) Random access memory	1) Read only memory
2) Data is present till power present.	2) Data is permanent present without power
3) Data are stored temporary	3) Data is permanent
4) Data can be read, write, modify, erased	4) Data is only read
5) Speed high	5) Speed Low
6) Expensive	6) cheaper.

EPROM	EEPROM
① Erasable and programmable ROM.	2) Electrically Erasable and programmable ROM
② UV rays are used to erase contents.	② Electric signal is used to erase content
③ erase entire content.	③ Erase byte by byte
④ Erasable programming Read only memory	4) Electrically programmable Read only memory
⑤ Erasing operation takes 15-20 min	5) 5 ms
⑥ For programming it needs a special PROM programmer unit.	6) doesn't need any programmer unit
⑦ Major Drawback of MROM, PROM and EPROM, = MROM; (Mask ROM)	
1) Design bugs are costly	
2) if bug is detected the MROM is useless and	

must be replaced in order to change.

- 3) Mask is very expensive
- 4) Life time is short.

PROM: Programmable Read only memory.

- 1) If any error occurs, data can't be modified/rewritten.
- 2) They are blank chips which have nothing recorded on them.
- 3) Impossible to erase a particular byte, must erase entire content.
- 4) consume high static power.

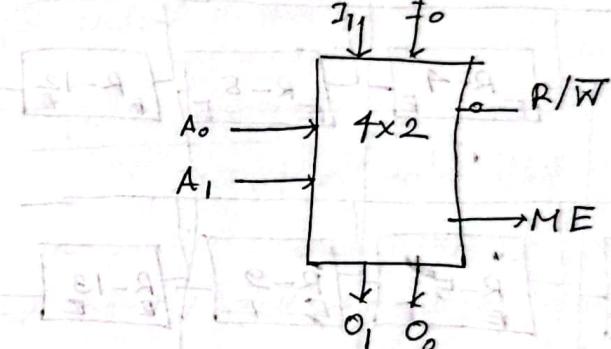
How EPROM is erased?

It has no electrical connection.

It is Erasable programmable read only memory. Here impossible to erase a particular byte. If a program error is detected entire content is erased by UV rays. (Ultraviolet light).

(49) Function of memory enable input?

Ans Memory enable / chip enable / chip select input can completely disable all other part of memory to activate a particular part.



Here it is shown an active high input that enables a memory to operate normally when it is kept high. Input Low disable memory.

(50) Drawback of SRAM:

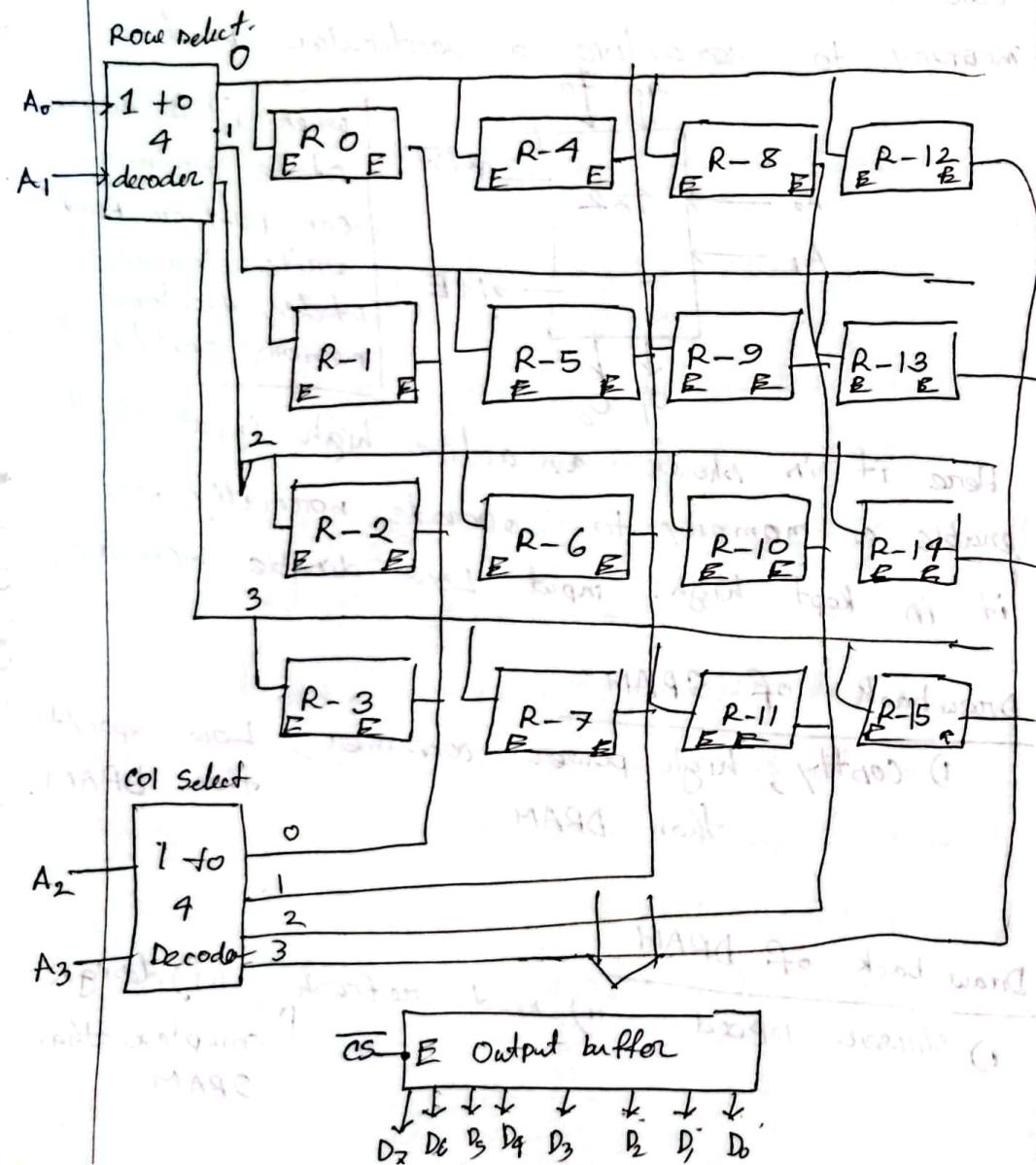
- I costly, high power consumer, Low capacity than DRAM.

Draw back of DRAM

- I slower speed
- II need refresh
- III design complex than SRAM.

## 5) Internal structure of $16 \times 8$ ROM.

Draw:



There are 4 basic part of ROM.

① Register array

② Row decoder

③ Col " "

④ Output buffer.

Address decoder.

① Register array:

It stores data that have been programmed into ROM. Each register contains a number of memory cell equal to the word size. Each register has two enable input.

② Address decoder

Applied address code A<sub>1</sub>, A<sub>2</sub>, A<sub>3</sub> ..

determines register will be enable.

Address bits A<sub>1</sub>, A<sub>0</sub> determines 1 to 4 decoder which active one row select line.

Address bit A<sub>3</sub> A<sub>2</sub> determines second 1-4 decoder which active one col select line.

only one register will be enabled when both the row and col selected by the address input.

### Output buffer

The register that is enabled by the address input will place its data on the data bus. These data feed into the output buffer which will pass data to the external data output if  $\overline{CS} = 0$ . If  $\overline{CS} = 1$  the output buffer are in the High state.

(52)

Explain: The  $64 \times 8$  RAM stores 64 words of 8 bits each. These words have address line 0 to  $63_{10}$ . The de coder requires input code or  $2^6 = 64$ .

Read operation: At first chip selector  $\overline{CS} = 0$ . Let address location is  $111110(62)_{10}$  data is  $(1010)_{10}$  if  $R/\overline{W} = 1$  then it disable input buffer, active output buffer so that the input don't affect the memory.

### Write operation

$R/\overline{W} = 0$ ;  $\overline{CS} = 0$  enables write operation. It enable input buff so that 8 bit word applied to the data, disable the output buffer so that outputs are on High 8 bits.

### Chip selector

$\overline{CS} = 0$  always. Then write/read operation can be happen. If  $\overline{CS} = 1$ , disable any w/r operation.

(53)

$16K \times 8$  memory means

$$\text{MA8} + \text{X} \cdot 2^1 \quad \text{Total } 16K \\ \downarrow \quad \downarrow \\ 2^4 \cdot 2^{10} = 2^{14}$$

The memory stores  $2^{14}$  words. 14 bit address code to specify 1 of  $2^{14}$  address  
address input = 14

word size = 8

data input = 8

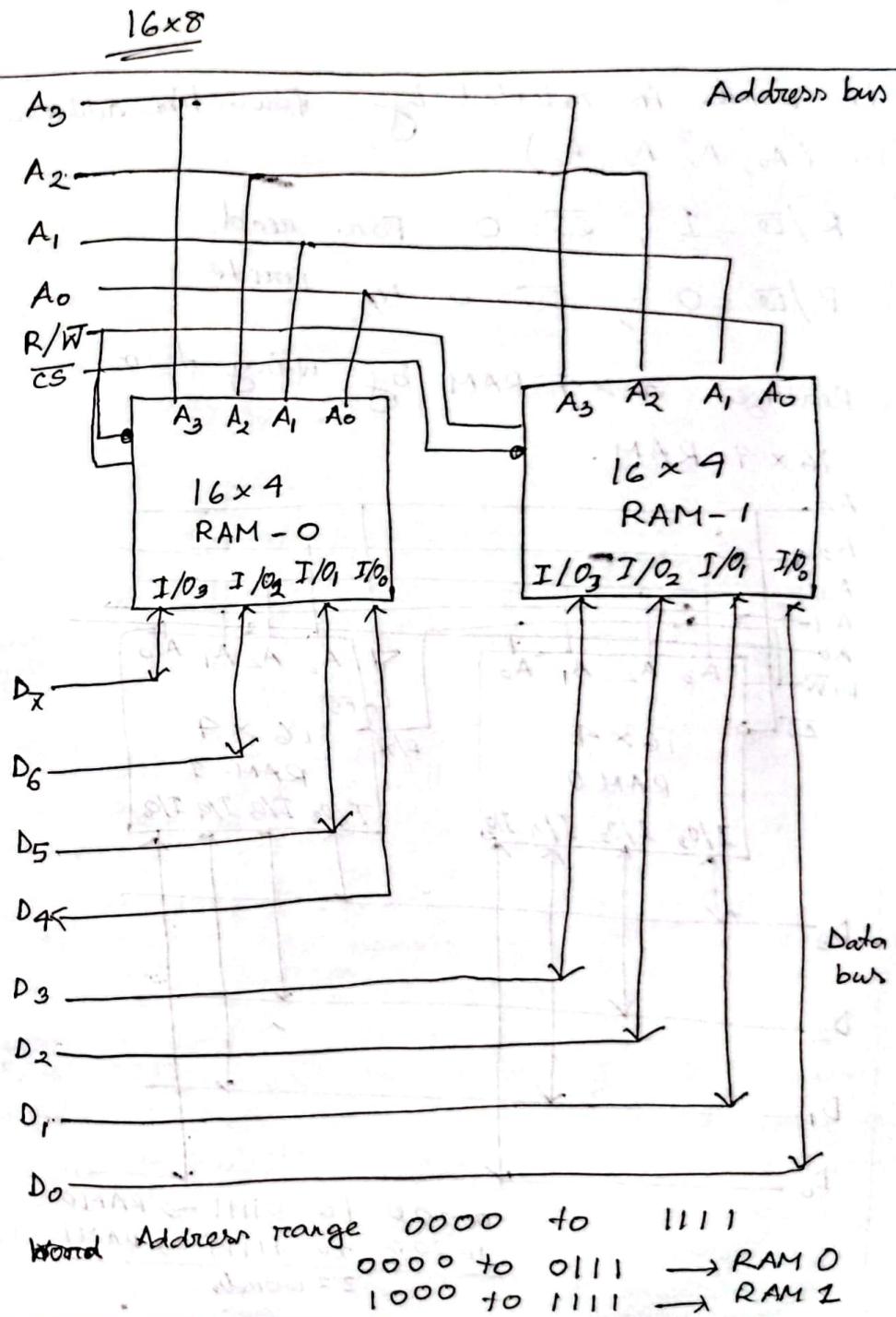
5A What is the benefit of address multiplexing?

Ans The  $16k \times 1$  DRAM array would have 14 address inputs.

- " 64Kx1 " " " " 16 " "  
 " 1Mx4 " " " " 20 " "  
 " 4Mx1 " " " " 22 " "

High capacity memory chips such these would require many pin. In order to reduce the number of pins on this DRAM chip multiplexing is needed. In multiplexing address input pin can accomodate two different address bit.

(55) 16x8 RAM module using 16x4 RAM module; by using two 16x4 RAM.

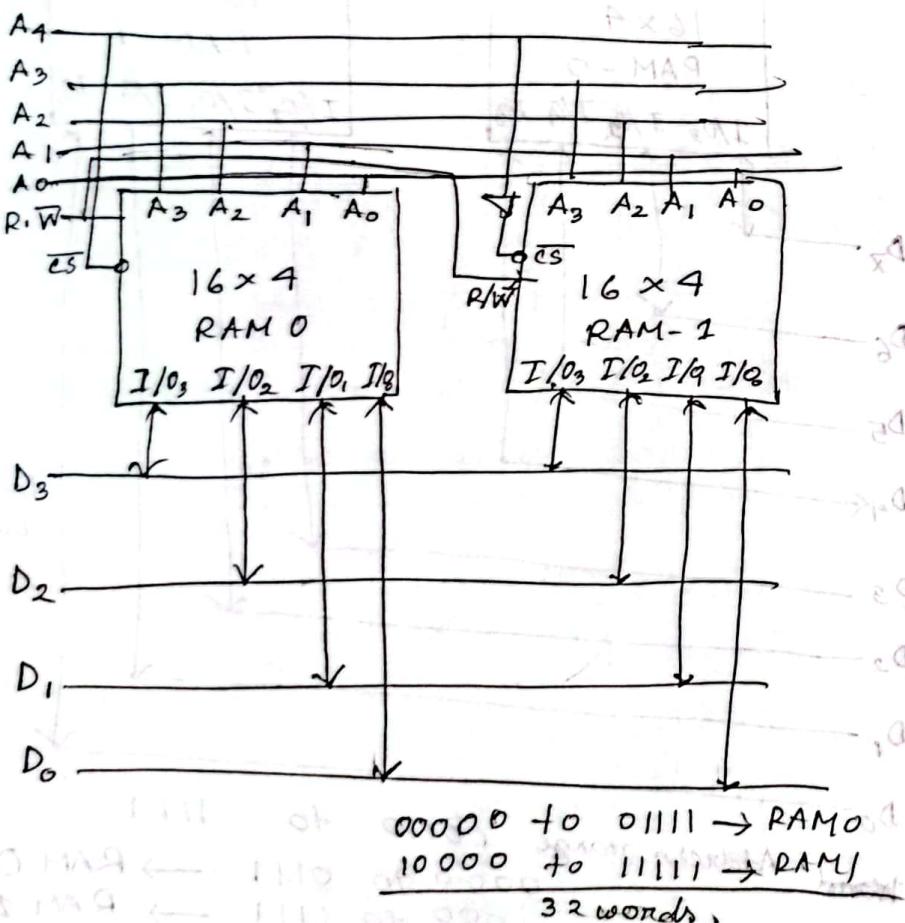


16 words is selected by four line address bus ( $A_0, A_1, A_2, A_3$ )

$R/W = 1, \overline{CS} = 0$  For read

$R/W = 0, \overline{CS} = 0$  For write.

Realize  $32 \times 4$  RAM by using two  $16 \times 4$  RAM.



### 57 Application of ROM

1) used to store data and information that are not to change during normal operation.

2) store permanent data.

3) storage of program in microcomputer.

19 batch

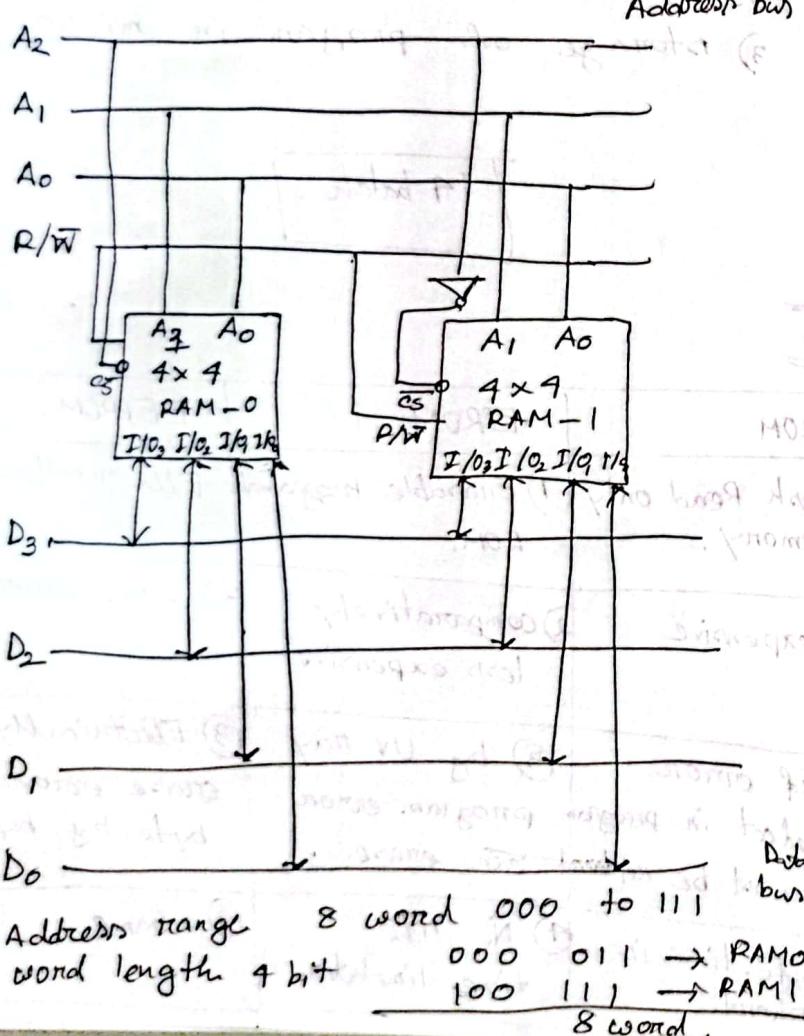
④ a

MROM	EPROM	EEPROM
1) Mask Read only memory.	1) Erasable Programmable Electrically ROM.	
2) expensive	2) comparatively less expensive	2) Less expensive
3) if error detect in program it must be replaced	3) by UV ray	3) Electrically erase error by byte by byte
4) Life time is short.	4) No life time limitation	4) Same

13 batch

⑨ @ Q bank  $48^{\circ}$

⑩ ⑪  $8 \times 4$



## ✓ Clipper and clammer circuit

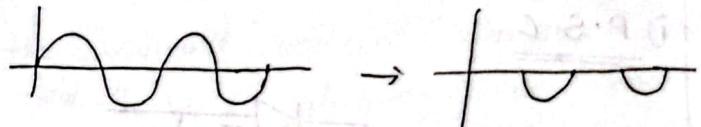
clipper: clipper circuits are the circuit that clip off or remove a portion of an input signal without causing any distortion to the remaining part of the wave. Slicers / limiters.

② It control the shape of an output waveform.

### positive clipper circuit

AC signal w/ positive half cycle

cut  $\rightarrow$

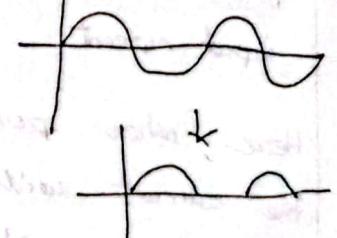


- 1) positive series clipper
- 2) " shunt "

### Negative clipper circuit - (Negative half cycle cut)

1) positive series clipper

2) " shunt "



60) Draw and explain a clipper circuit with the positive half cycle.

Positive clipper circuit:

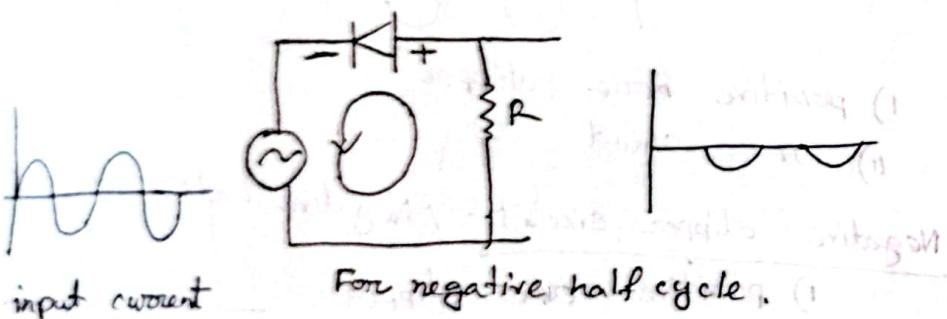
1) positive series clipper:

It is used for clip the current wave form.

2) positive shunt clipper:

It is used for clip the voltage wave form.

i) P.S.C



Here, when positive half cycle arrives then the circuit will be in reverse bias, so, it blocks positive half cycle. But when negative half cycle arrives, then the circuit will be in forward bias, so, it allows to

pass negative half cycle.

positive shunt clipper:

17 batch

6-(a)  $\rightarrow$  59%;

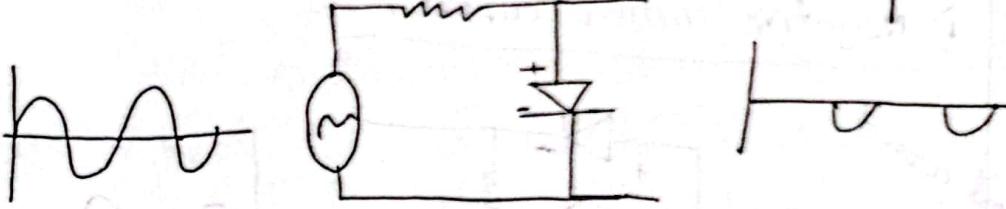
(b)  $\rightarrow$  60%;

18 batch

③ (a)  $\rightarrow$  60

(b)  $\rightarrow$  61

1(a) 5%



when in this circuit positive half cycle arrives, the circuit is in forward bias, if we take resistance negligible, we can replace the diode with short circuit, so it blocks the positive half cycle as the voltage of the circuit is 0.

Again when the negative half cycle arrives, the diode is in reverse bias and we replace it with open circuit and it allows to pass negative half cycle.

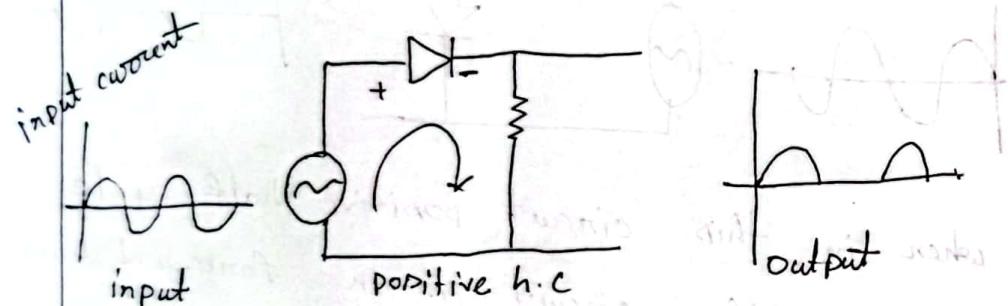
(61) Draw and explain w.r.t negative half cycle

### Negative clipper circuit:

current/voltage vs negative half cycle

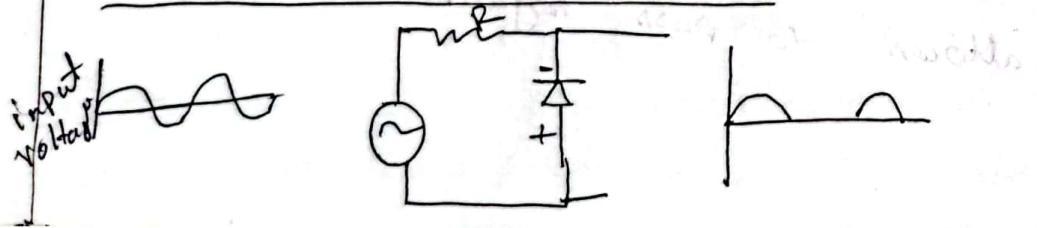
clip ॥

#### i) Negative series clipper:



when positive half cycle arrives forward bias in the diode happens and it pass the positive half cycle, But when negative half cycle arrives, ~~as~~ now the diode is in reverse bias and it block the negative half cycle.

#### ii) Negative shunt clipper circuit:



When positive half cycle arrives in the circuit the diode is in reverse bias, it means it can replace with open circuit and the positive half cycle will pass.

When the negative half cycle arrives in the circuit the diode is in forward bias, it means it can replace with short circuit, no negative half cycle can't be passed as the voltage of two terminals will be 0.

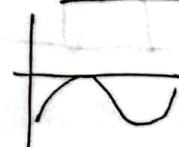
### Clampers:

clampers are the electronic circuits that shift the DC level of the AC signal. It is also known as DC voltage restorers or level shifter

#### i) Positive clapper



#### ii) Negative

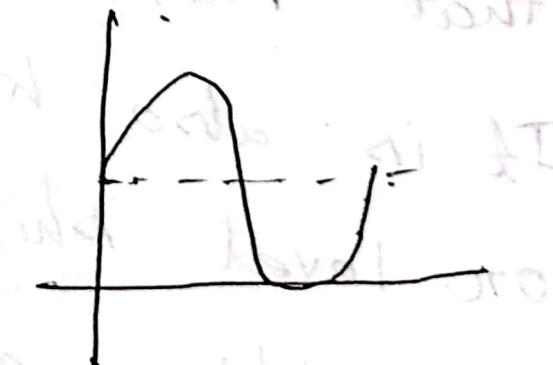
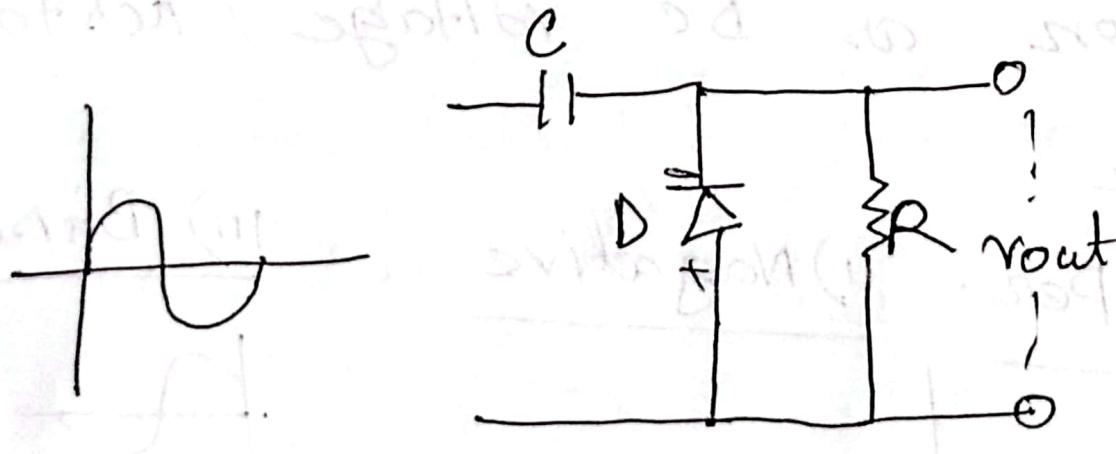


#### iii) Biased



the time period. conversely , a small value of the capacitor is chosen so that it will charge rapidly at the time of conduction of the diode.

### positive clampler



Q) Why should the RC time constant be larger in a clamp circuit.

Clamping is the process of introducing a dc level into an signal. It is also known as dc restorers. The circuit contains a capacitor, a diode, and resistive element, but it can also have independent DC supply source. The magnitude R and C to be used in the clamp circuit must be chosen such that the time constant  $\tau = RC$  is larger enough to ensure that the voltage across the capacitor does not discharge significantly during the interval the diode is non conducting. In a good clamp circuit, the circuit time constant  $t = RC$  should be at least ten times the time period of the input signal voltage. So it is clear that in order to maintain the time period of the waveform, the time constant must be greater than half of

58) Show the effect of RC time constant in a clamping circuit.

Ans A clamping circuit is a circuit that adds a DC level to an AC signal. Actually the positive and negative peaks of the signal signals can be placed at desired levels using clamping circuit. It consists of capacitor, resistor, diode, dc battery.

In order to maintain the time period of the wave form, the time must be greater than half the time period.

$$T = RC$$

where,

$R$  = the resistance of the resistor employed.

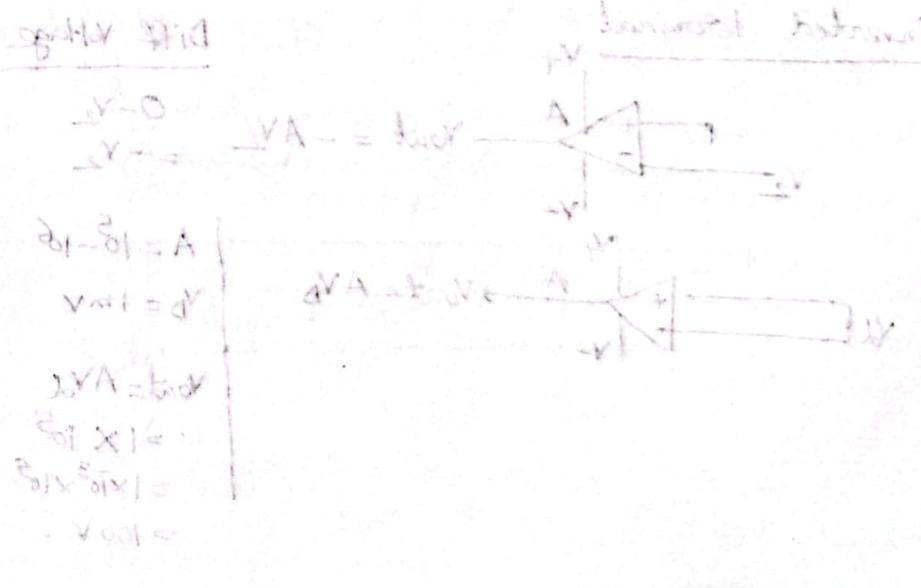
$C$  = capacitance of the capacitor used.

The time constant of charge and discharge of the capacitor determines the output of a clamping circuit.

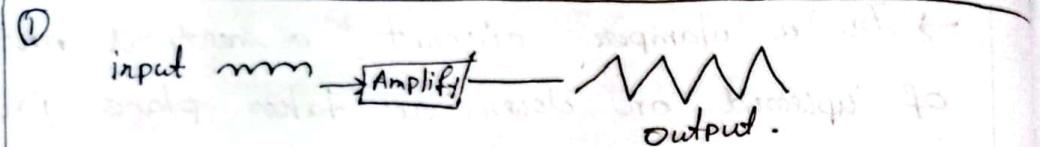
→ In a clamping circuit, a vertical shift of upward or downward takes place in the output waveform with respect to the input signal.

→ The Load resistor and capacitor affect the waveform. So, the discharging time of the capacitor should be large enough.

The DC component present in the input is rejected when a capacitor coupled network is used. Hence when DC needs to be restored, clamping circuit is used.

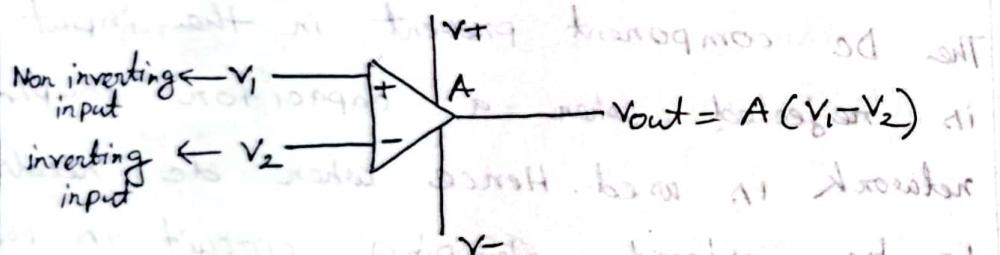


## OP-Amp (operational Amplifier)



Opamp: 2 input, 1 output  
2 power supply.

An opamp is an ~~integrated~~ circuit that can amplify weak electric signals.



Diff Voltage

$$0 - V_2 \\ = -V_2$$

$$A = 10^5 - 10^6$$

$$V_D = 1 \text{ mV}$$

$$\begin{aligned} V_{out} &= AV_d \\ &= 1 \times 10^5 \\ &= 1 \times 10^3 \times 10^5 \\ &= 100 \text{ V} \end{aligned}$$

## characteristics of ideal op-amp

$$R_i = \infty \quad \text{Bandwidth} = \infty$$

$$R_o = 0 \quad \text{gain } A = \infty$$

$$\text{Settling time} = 0$$

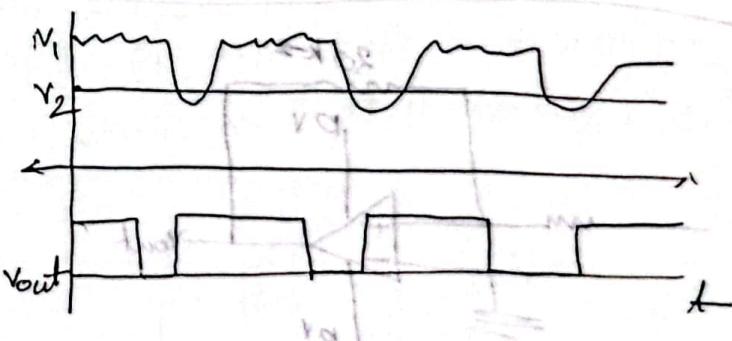
CMRR  $\rightarrow$  Common Mode Rejection Ratio

If  $V_1 = V_2$  then  $V_{out} = 0$

$$\frac{A_d}{A_c} = \frac{\text{differential gain}}{\text{common mode gain}} = \infty$$

## Schmitt Trigger Explained

If input signal is noisy then output will be affected. This kind of noise problem can be avoided by using schmitt trigger.



Hysteresis: trip point is called

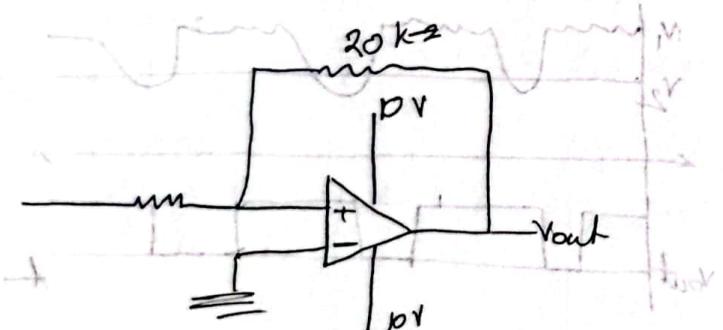
Schmitt trigger is a comparator with the hysteresis, so, it has 2 threshold voltage

$$\text{Hysteresis voltage} = V_{UT} - V_{LT}$$

④ Comparator circuit with positive feedback are called Schmitt trigger.

# Comparator: In electronics, a comparator is a device that compares 2 voltage or currents and outputs a digital signal indicating which is larger.

$$\text{Duty cycle} = \frac{\text{On time pulse}}{\text{Total time}} = \frac{T_{on}}{T_{total}}$$



Non inverting schmitt trigger.

Given,  $R_2 = 20\text{ k}\Omega$ ,  $V_H = 10\text{V}$ ,  $V_L = -10\text{V}$ ,  $V_{DD} = 10\text{V}$

$$V_{UT} = -\frac{R_1}{R_2} V_L$$

$$= -\frac{R_1}{20\text{ k}\Omega} 10$$

$$V_{LT} = -\frac{R_1}{R_2} V_H$$

$$= -\frac{R_1}{20\text{ k}\Omega} 10$$

Hysteresis width.

$$V_{UT} - V_{LT}$$

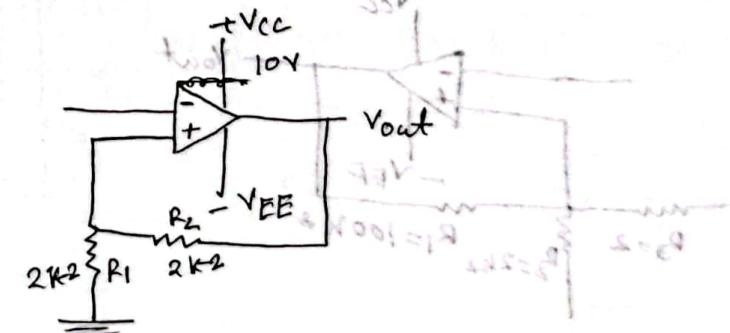
$$\Rightarrow -\frac{R_1}{R_2} 10 + 10 \frac{R_1}{R_2} = 20 \frac{R_1}{R_2}$$

$$\text{Given } 20 \frac{R_1}{R_2} = 1\text{V}$$

$$\Rightarrow R_1 = \frac{1 \times R_2}{20} = \frac{1 \times 20}{20} = 1\text{ k}\Omega$$

Q1 By using Op-amp draw and explain schmitt trigger which is 0 volt centered hysteresis.

Ans



$$V_{CC} = 10V; R_1 = R_2 = 2k\Omega, V_{cen} = 0V.$$

$$\therefore B = \frac{R_1}{R_1 + R_2} = \frac{2}{4} = \frac{1}{2}$$

$$UTP = V_{cen} + B V_{sat}$$

$$= 0 + \frac{1}{2} \times 8$$

$$= 4$$

$$LTP = V_{cen} - B V_{sat}$$

$$= 0 - \frac{1}{2} \times 8 = -4V.$$

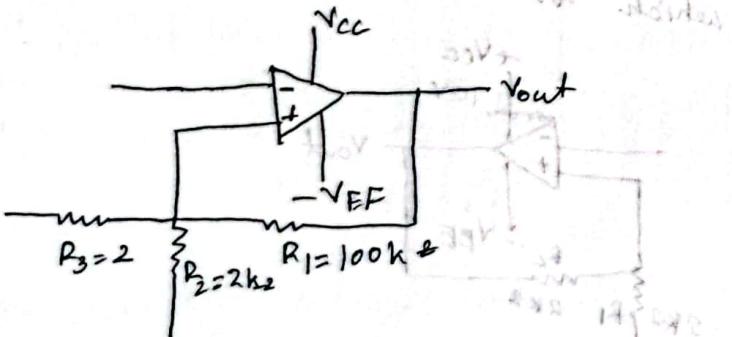
Explain: For the positive saturated output,

Non inverting input = UTP

For negative " " " " = LTP.

② Using OP-Amp draw and explain Schmitt trigger that has 5V centered hyst.

Ans: 5V centered hyst.



$$V_{cen} = \frac{R_2}{R_2 + R_3} V_{CC}$$

$$\Rightarrow 5 = \frac{2}{2+2} \cdot 10V$$

$$\therefore V_{CC} = 10V.$$

$$B = \frac{R_2 || R_3}{R_1 + R_2 || R_3}$$

$$= \frac{2||2}{100 + 2||2} = \frac{\frac{2 \cdot 2}{2+2}}{100 + \frac{2 \cdot 2}{2+2}} = \frac{1}{101} = 0.0$$

$$UTP = V_{cen} + B V_{sat}$$

$$= 5 + 0.01 \times 10 = 5.1$$

$$LTP = V_{cen} - B V_{sat} = 5 - 0.01 \times 10 = 4.9V$$

③ produce rectangular wave:

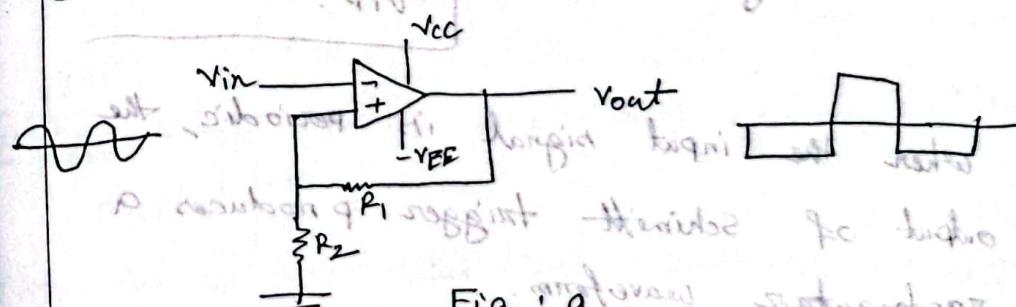


Fig: a

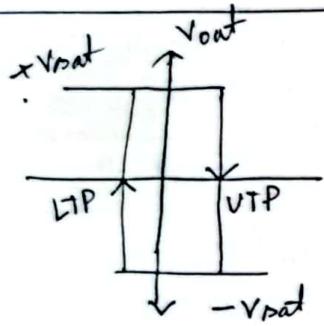


Fig b

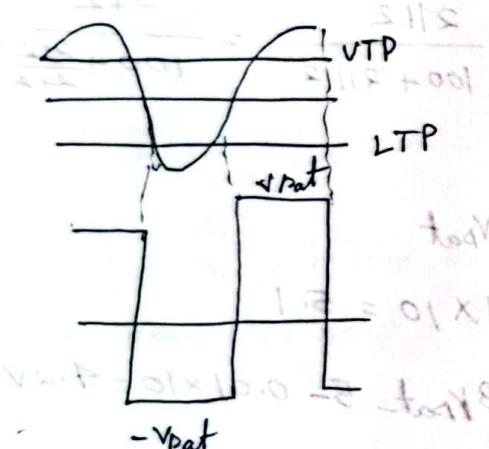


Fig c

when the input signal is periodic, the output of Schmitt trigger produces a rectangular waveform.

Fig a: Schmitt trigger  
Fig b: Transfer character

Fig c: Output voltage vs input

→ The input signal less than VTP the output remain high.

→ Input cross LTP the output Low and remain Low until cross LTP

→ Cross LTP the out become high and remain High until cross VTP.

produce triangular wave from rectangle

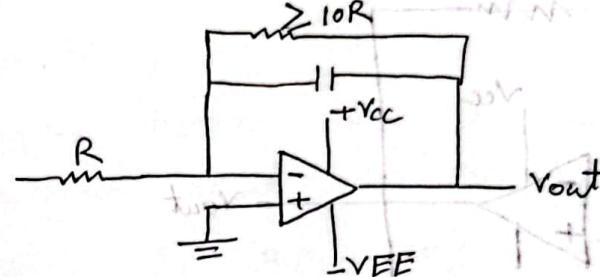


Fig a.

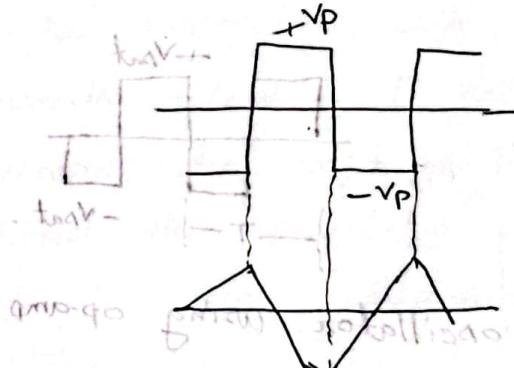


Fig b.

By using OPamp draw and explain relaxation oscillator.

An op-amp relaxation oscillator is also known as an astable multivibrator. It is used to generate square waves.

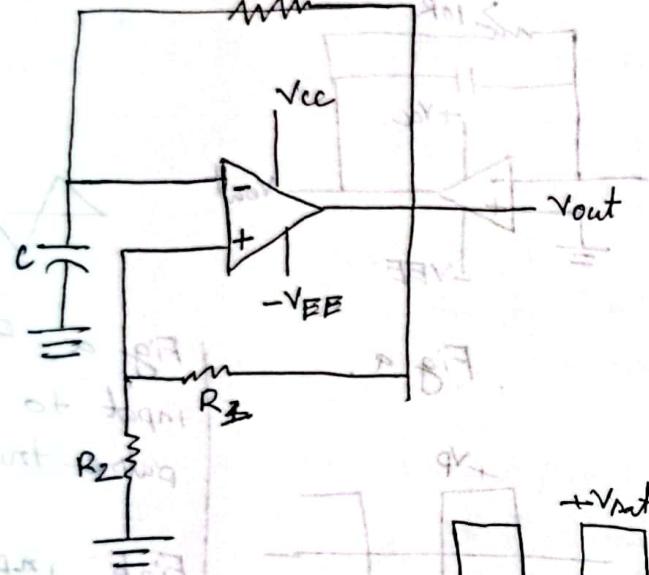
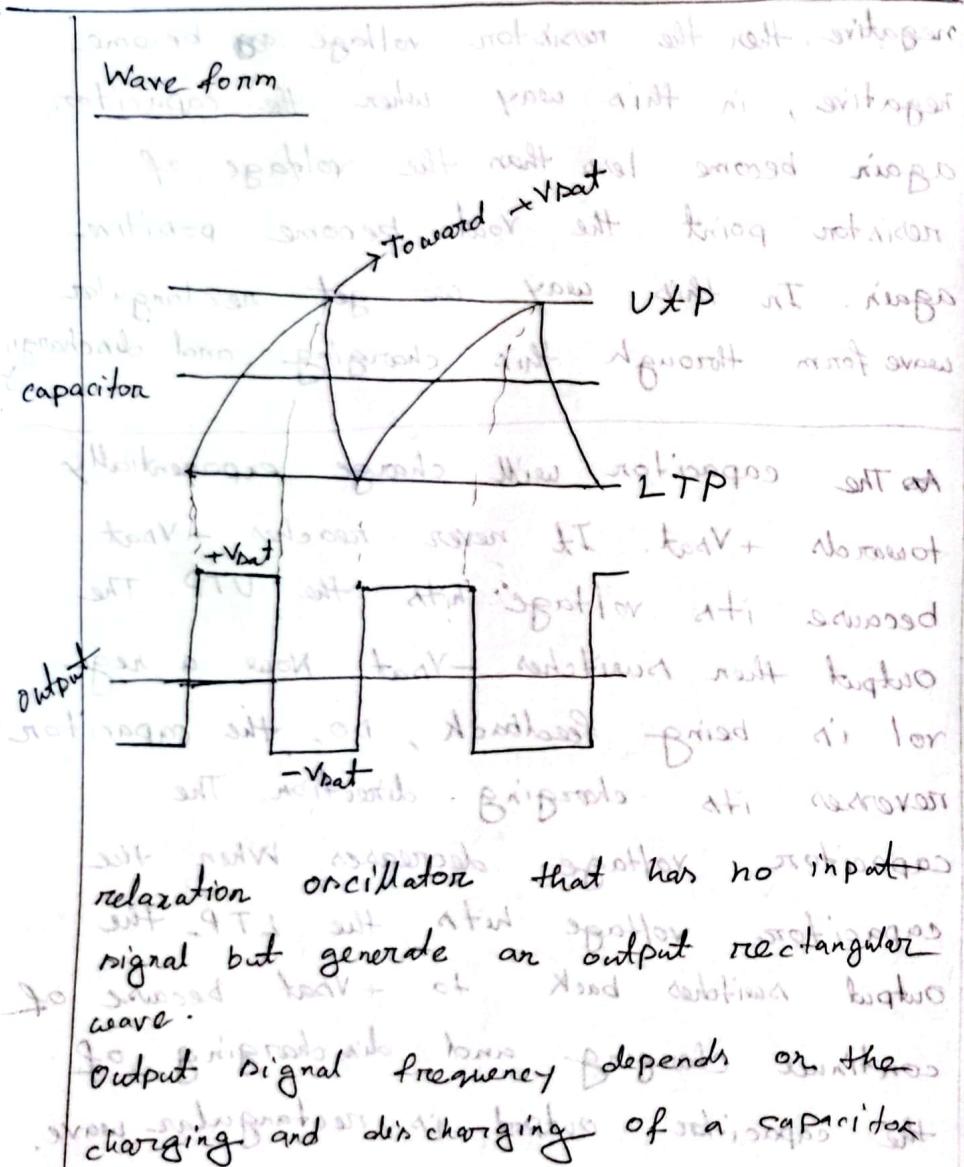


Fig: Relaxation oscillator using opamp

Assume that the output ~~is~~<sup>is</sup> in positive saturation. if  $V_{CC} = +10V$  and  $-V_{EE} = -10V$  and the value of capacitor is less than those voltage we will get positive vol in  $V_{out}$  and a part of this vol go through the resistors. When a capacitor want to cross the voltage of resistors  $V_{out}$  become

negative. then the resistor voltage ~~will~~ become negative, in this way when the capacitor again become less than the voltage of resistor point the  $V_{out}$  become positive again. In this way we get rectangular wave form through this charging and discharging.

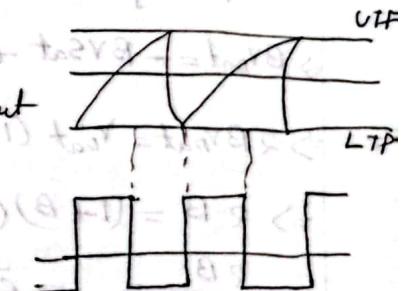
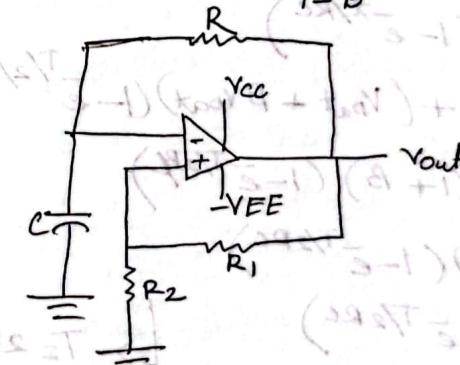
As the capacitor will charge exponentially towards  $+V_{sat}$ . It never reaches  $+V_{sat}$  because its voltage hits the UTP. The output then switches  $-V_{sat}$ . Now a reg vol is being feedback, so the capacitor reverses its charging direction. The capacitor voltage decreases. When the capacitor voltage hits the LTP, the output switches back to  $+V_{sat}$ . because of continue charging and discharging of the capacitor, output is rectangular wave.



When the output is in  $+V_{sat}$ , the capacitor started charging toward  $+V_{sat}$  & never reaches  $+V_{sat}$ .

When the output switches to  $-V_{sat}$  then the capacitor started discharging towards  $-V_{sat}$ . It also never reaches  $-V_{sat}$ .

Prove  $T = 2RC \ln \frac{1+B}{1-B}$   $B = \text{feedback fraction}$



Relaxation oscillator.

We get,

$$v = v_i + (v_f - v_i) (1 - e^{-t/RC}) \quad (1)$$

where  $v$  = capacitor voltage.

$t$  = charging time

$v_i$  = initial capacitor voltage

$V_f$  = target capacitor voltage  
here,  $v_i = -BV_{sat}$

$$v_i = -BV_{sat}$$

$$V_f = +V_{sat}$$

$$t = \frac{T}{2}$$

$$V = BV_{sat}$$

So, (1)  $\Rightarrow$

$$V = V_i + (V_f - V_i)(1 - e^{-t/RC})$$

$$\Rightarrow BV_{sat} = -BV_{sat} + (V_{sat} + BV_{sat})(1 - e^{T/2RC})$$

$$\Rightarrow 2BV_{sat} = V_{sat}(1+B)(1 - e^{T/2RC})$$

$$\Rightarrow 2B = (1+B)(1 - e^{T/2RC})$$

$$\Rightarrow \frac{2B}{1+B} = 1 - e^{T/2RC}$$

$$\Rightarrow e^{T/2RC} = 1 - \frac{2B}{1+B}$$

$$\Rightarrow e^{-T/2RC} = \frac{1+B-2B}{1+B} = \frac{1-B}{1+B}$$

$$\Rightarrow -T/2RC = \ln\left(\frac{1-B}{1+B}\right)$$

$$\Rightarrow T = 2RC \ln\left(\frac{1-B}{1+B}\right)$$

$$\Rightarrow -T = 2RC \ln\left(\frac{1+B}{1-B}\right)$$

$$\Rightarrow T = 2RC \ln\left(\frac{1+B}{1-B}\right)$$

[Proven]

⑧ feedback fraction  $B=0.9$ , feedback resistor  $R=4.7 \text{ ohm}$ ,  $C=0.022 \mu F$ , what is the frequency of the output rectangular wave.

Ans

We know,

$$T = 2RC \ln\left(\frac{1+B}{1-B}\right)$$

$$\Rightarrow T = 2 \times 4.7 \times 0.022 \times \ln\left(\frac{1+0.9}{1-0.9}\right)$$

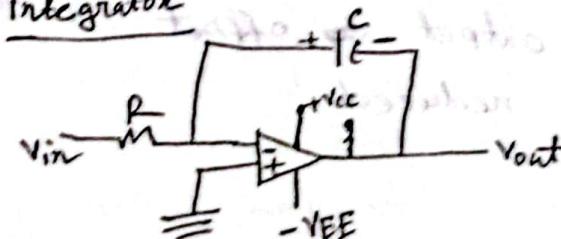
$$= 0.2068 \times \ln\left(\frac{1.9}{0.1}\right)$$

$$= 0.6089 \text{ sec.}$$

$$\therefore f = \frac{1}{T} = \frac{1}{0.6089} = 1.6423 \text{ Hz.}$$

⑨ Draw and explain a practical op-amp integrator. Explain the necessity of larger resistor across the capacitor.

Ans integrator



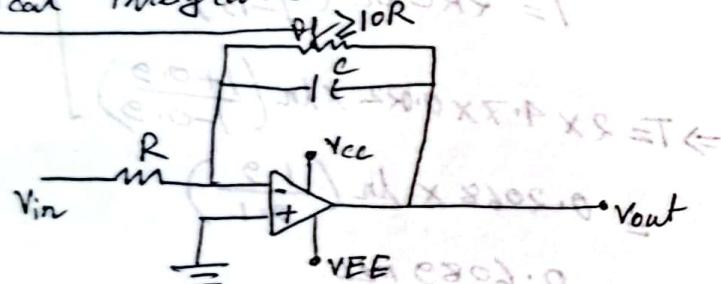
$V_{in}$  represents constant voltage during pulse time  $T$ .

$$I_{in} = \frac{V_{in}}{R}$$

$$C = \frac{Q}{V} \Rightarrow V = \frac{IT}{C}$$

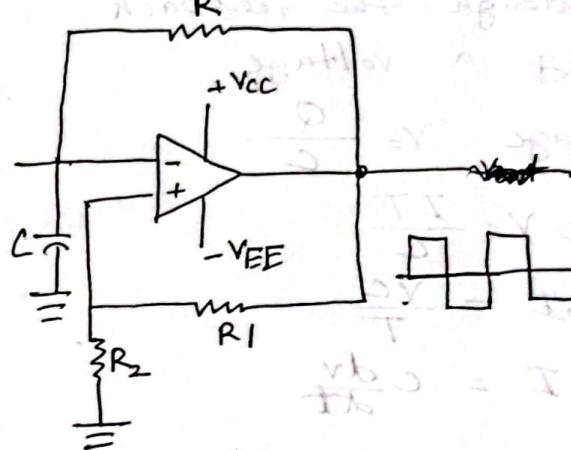
$V$  = capacitor Vol.  
 $I$  = charging curr.  
 $C$  = capacitance  
 $T$  = charging time

### (g) Practical integrator

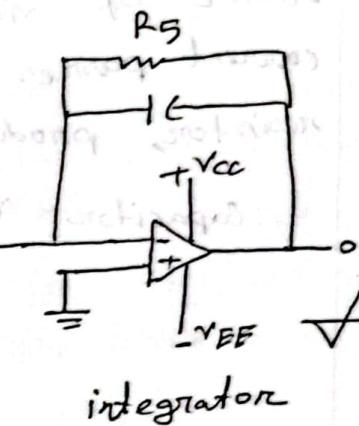


limitation of an ideal integrator can be minimize in the practical circuit by adding resistor  $R_f$  in parallel with capacitor  $C$ . This  $R_f$  avoids op amp going into open loop configuration at low frequencies. The resistor should be at least 10 times larger than the input resistor. The output offset voltage is greatly reduced.

### (f) Rectangular to triangular.

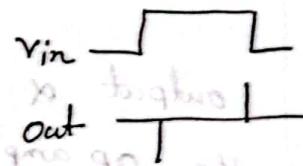
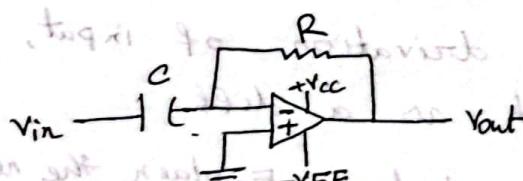


Relaxation oscillator



integrator

### OP Amp differentiator



An op-amp diff. is a circuit configuration that produces output voltage amplitude which is proportional to the rate of change in input voltage means that change in input voltage will immediately change output voltage.

Because of virtual ground, the capacitor current passes through the feedback resistor, producing a voltage.

$$\text{capacitor voltage } V = \frac{Q}{C}$$

$$\Rightarrow V = \frac{IT}{C}$$

$$\Rightarrow I = \frac{VC}{T}$$

$$I = C \frac{dV}{dt}$$

$$\Rightarrow -\frac{V_{out}}{R} = C \times \frac{dV_{in}}{dt}$$

$$\Rightarrow V_{out} = -RC \frac{dV_{in}}{dt} = -IR$$

output  $\propto$  time derivation of input, so, the op amp act as a diff.

⑩ practical differentiator, Explain the necessity

of a small resistor in series with cap.

The opamp differentiator has a tendency to oscillate an undesirable condition.

To avoid this, a practical diff usually includes some added resistance in series with

capacitor. The effect is limit closed loop voltage gain at higher frequencies, where oscillation problem arises and it makes the circuit unstable and noisy.

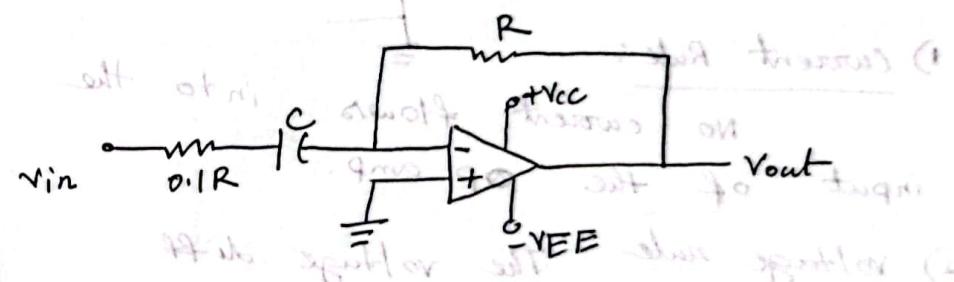
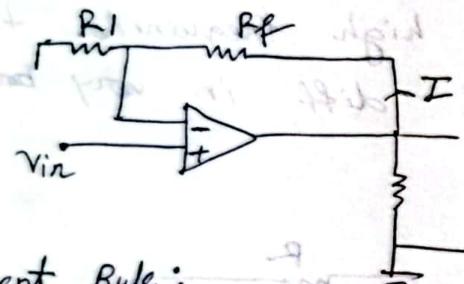


Fig: Practical opamp diff

$$\frac{V_{out}}{V_{in}} = \frac{-RC}{0.1R} = -10RC$$

IR batch 13:00 - w/ notings

- ① @ Working principle of non inverting amplifier with op-amp.



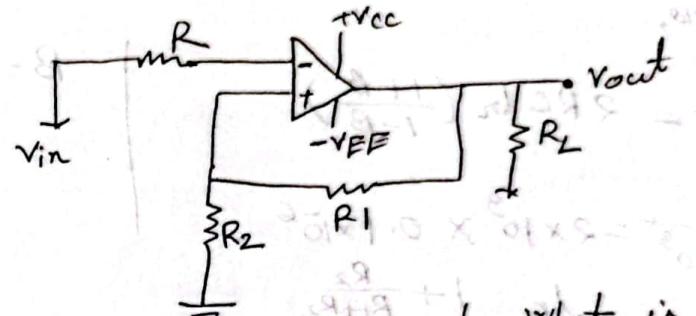
- 1) current Rule:

No current flows into the input of the op amp.

- ② voltage rule The voltage diff between two input is 180°

$$gain = \frac{V_{out}}{V_{in}} = 1 + \frac{R_2}{R_1}$$

- ⑥ Schmitt trigger is basically an inverting comparator circuit with a positive feedback. The purpose of Schmitt trigger is to convert any regular or irregular shape input waveform into a square shape.



What is OP-amp  
comparator?

- ② a Q.B - 67%

- ## b) Assignment 1

$$\boxed{22 = 18 + 4}$$

$$\textcircled{2} - a \rightarrow 0.B\overline{679}$$

b) → „-↗↖“

14

⑦-⑧ → UTP, LTP

Given,

$$f = 1.7 \times 10^3 \text{ Hz}$$

$$C = 0.1 \mu F, \quad R = 1 k\Omega = 10^6 \Omega$$

$$= 0.1 \times 10^{-6} F \quad = 1000 \Omega$$

We know,

$$\frac{1}{f} = 2RC \ln \left( \frac{1+B}{1-B} \right)$$

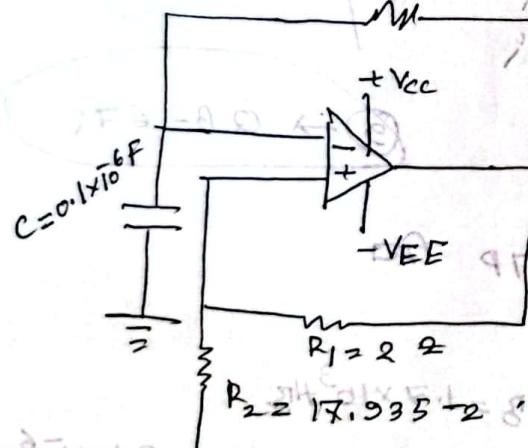
$$\Rightarrow \frac{1}{1.7 \times 10^3} = 2 \times 10^3 \times 0.1 \times 10^{-6}$$

$$B = \frac{R_2}{R_1 + R_2}$$

$$\ln \frac{1 + \frac{R_2}{R_1 + R_2}}{1 - \frac{R_2}{R_1 + R_2}}$$

$$\Rightarrow 2.941 = \ln \frac{1 + \frac{R_2}{2+R_2}}{1 - \frac{R_2}{2+R_2}}$$

$$\Rightarrow R_2 = 17.935 \Omega$$



$$2 \times 1 = 8 \quad 7 \times 1.0 = 7$$

$$8 - 0.001 = 7.999 \times 10^{-6}$$

### 26 Quantization error

It is the difference

difference between the analog signal and the closest digital value at each sampling instance from A/D converter. It is the inherent uncertainty in digitizing analog value. The higher the resolution of the ADC, the lower quantization error.

Example: error in rounding & truncation.

### Step size (resolution):

The amount of change in  $V_{out}$ , when the digital input value is changed from one step to the next.

A D/A converter with  $n$  bits, divides a range of analog value into  $2^n - 1$  pieces.

The size or magnitude of the least significant bit each piece is the analog equivalent weight of the least significant bit. It is step size.

Resolution of ADC and DACR of ADC

Resolution of an ADC is the number of bits which are used to digitize the input sample. It determine how many output code ( $2^n$ ) the converter can produce.

R of DAC

It is given by the number of bits,  $N$ . The resolution is the smallest increment of output that the DAC can produce. An 8 bit DAC resolution is 1/256 of a volt.

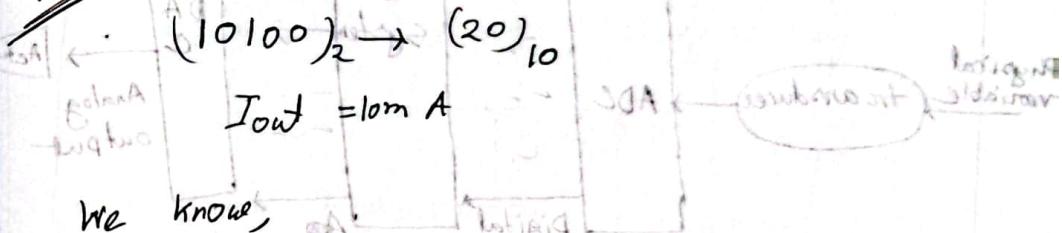
percentage of resolution =  $\frac{\text{Step size}}{\text{Full scale (F.S)}}$  × 100%

$$\% \text{ resolution} = \frac{\text{Step size}}{\text{Full scale (F.S)}} \times 100\%$$

A digital 1-8 bit is either broken up into 2-bit segments or 4-bit segments. A 4-bit segment is 1/16 of a volt. A 2-bit segment is 1/4 of a volt. A 1-bit segment is 1/2 of a volt.

- 27) A 5 bit DAC has a current output digital input of 10100, an output current of 10 mA is produced. What will  $I_{out}$  be for digital input of 11101?

Ans



We know,

$$\text{analog output} = K \times \text{digital input}$$

$$\Rightarrow K = \frac{A \cdot O}{D \cdot I}$$

$$K = \frac{10}{20} = 0.5 \text{ mA}$$

↓  
proportionality  
factor

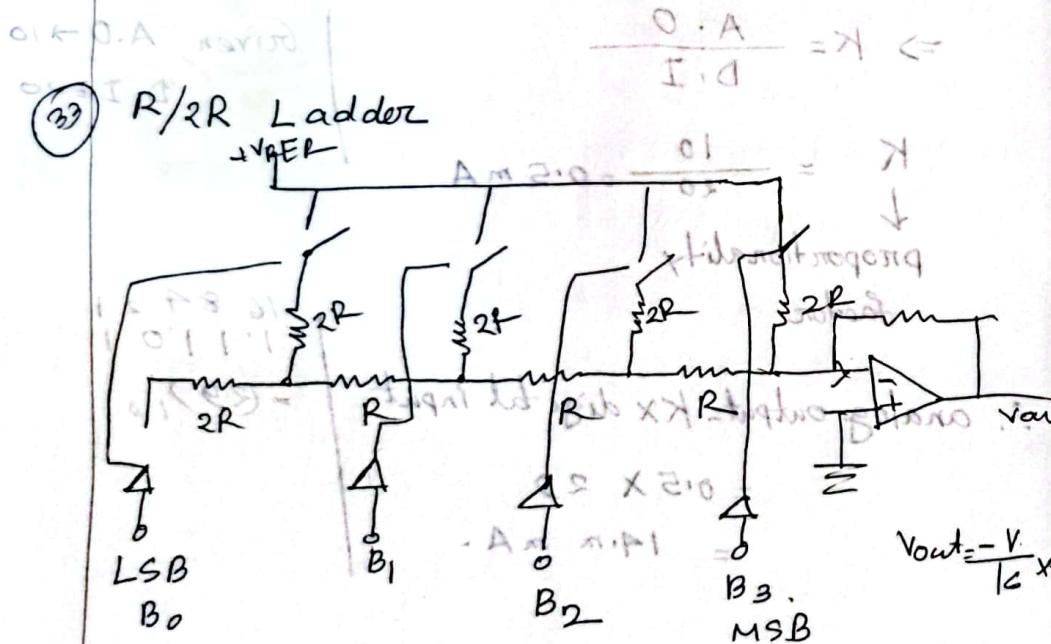
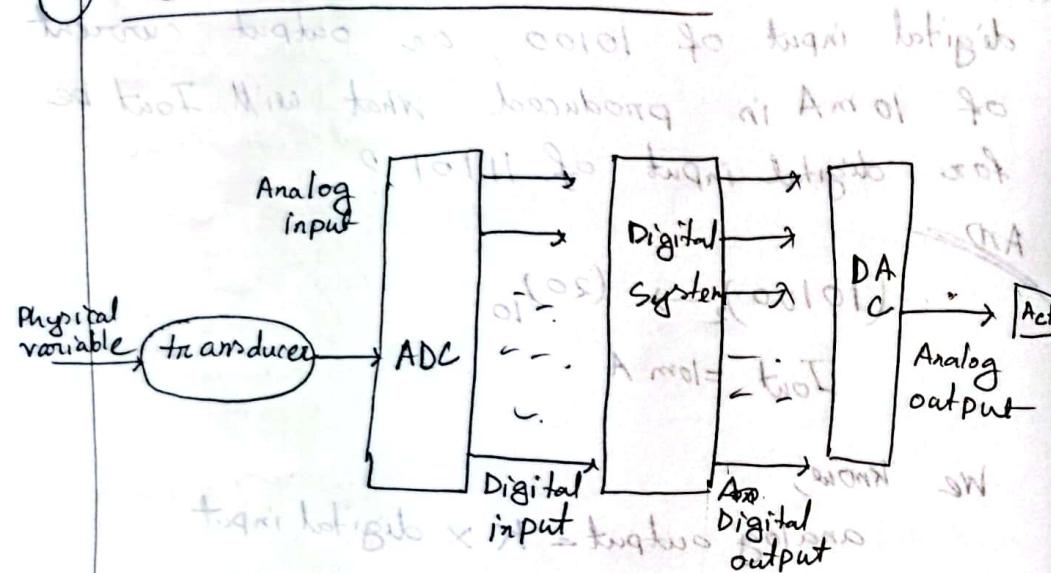
$$\therefore \text{analog output} = K \times \text{digital input}$$

$$= 0.5 \times 29$$

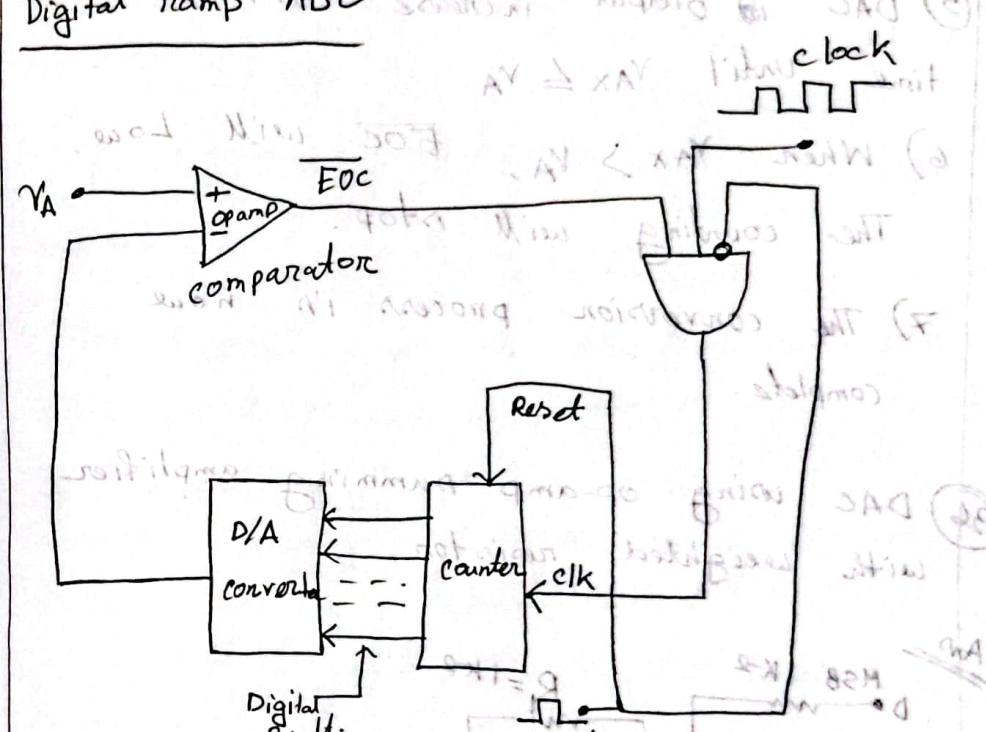
$$= 14.5 \text{ mA}$$

$$16 \cdot 8 \cdot 4 \cdot 2 \cdot 1 \\ 1 \cdot 1 \cdot 1 \cdot 0 \cdot 1 \\ = (29)_{10}$$

### 30) ADC and DAC interfacing



### Digital ramp ADC



- ① Start pulse resets the counter to 0. It also inhibits clock pulses.
- ② With 0 in all output  $V_{AX} = 0V$ .
- ③ As  $V_A > V_{AX}$ , EOC will go high.
- ④ When start returns to zero, AND gate enables and clock pulses get through counter.

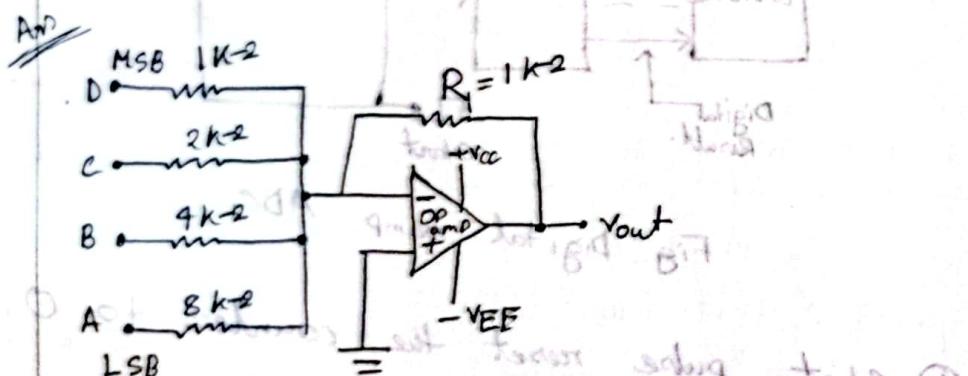
⑤ DAC output increase one step at a time until  $V_{AX} \leq V_A$ .

⑥ When  $V_{AX} > V_A$ ,  $\overline{E_{OC}}$  will low.

The counting will stop.

⑦ The conversion process is now complete.

⑥ DAC using op-amp summing amplifier with weighted resistor.



Digital input of 5V. Adds address code to

The op-amp is employed as a summing amplifier which produces weighted sum of the input voltage. The summing amplifier

multiplies each input voltage by ratio of the feedback resistor  $R_f$ . Output of this is

The output for DAC;

$$V_{out} = -(V_D + \frac{1}{2}V_C + \frac{1}{4}V_B + \frac{1}{8}V_A)$$

The negative sign is present because the summing amplifier is polarity inverting amp.

The summing amplifier output is an analog voltage that represent a weighted sum of the digital input.

D	C	B	A	$V_{out}$
0	0	0	0	0
0	0	0	1	$-\frac{1}{8} \times 5 = -0.625$
0	0	1	0	-1.25
0	0	1	1	-1.875
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

## Multivibrator

Multivibrator is the electronic circuit which is used to implement two state devices like oscillator, linear and flip flop.

Two state means High & Low voltage.  
 $(AV_s + AV_p + V_{CE} + dV) = 2V$

3 type according to the number of stable states

- 1) Astable both are unstable
  - 2) Monostable one stable  
one unstable
  - 3) Bistable both stable
- 1) Astable: used in Relaxation oscillator

Q) By using two npn transistors draw astable

\* Base Emitter junction  $\downarrow 0.7 \text{ V}$  at point A

- 1) Forward bias, transistors short circuit
- 2) Transistor saturation mode
- 3)  $V_{CE} = 0 \text{ V}$ .

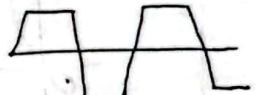
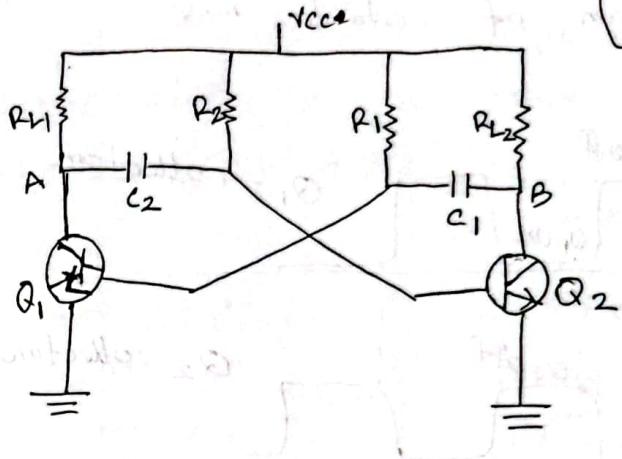
\* B-E junction  $\downarrow 0.7 \text{ V}$  at point C का रखा

- 1) Reverse bias, open circuit
- 2) Cut off condition.

$$R = \infty, I = 0, V_{CE} = V_{CC}$$

PNP  $= V_{CC}$

NPN  $= V_{CC}$

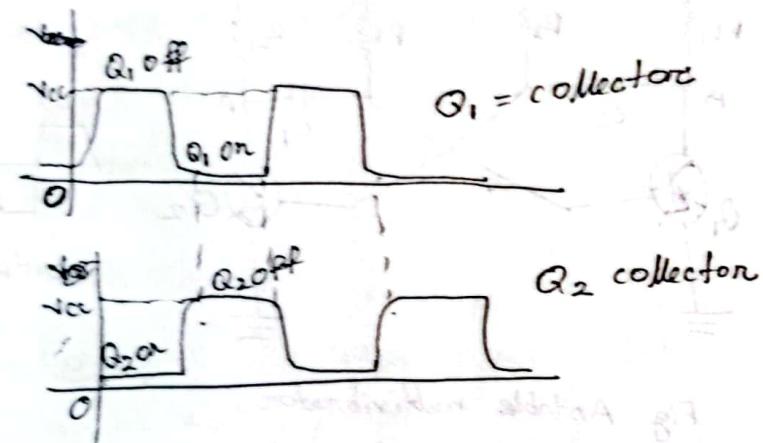


Output wave.

Fig Astable multivibrator using npn transistor

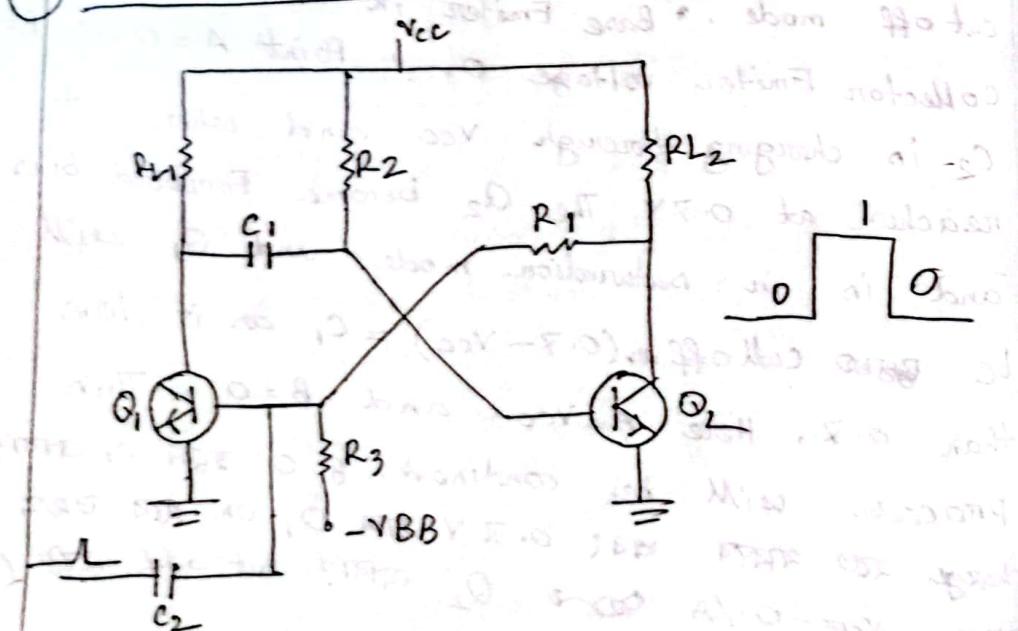
Here,  $Q_1$  is in saturation mode and  $Q_2$  is in cut off mode.  $\therefore$  Base Emitter in  $Q_1 = 0.7 \text{ V}$ . So Collector Emitter voltage  $0 \therefore$  Point  $A = 0$ ,  $B = V_{CC}$ .  $C_2$  is charging through  $V_{CC}$  and when it reaches at  $0.7 \text{ V}$ , the  $Q_2$  become forward bias and is in saturation mode. and  $Q_1$  will be cut off as  $(0.7 - V_{CC}) = C_1$  as it less than  $0.7$ . Here  $A = V_{CC}$  and  $B = 0$ . This process will be continuous.  $\therefore$   $C_1$  लगाए चाहे  $0.7 \text{ V}$  हल  $Q_1$  तो यह उड़ाना आवाहन  $V_{CE} = 0 / A$   $\Rightarrow$   $Q_2$  आवाहन cut off हो।

20 Wave form of bistable m.v.



বয়া দ্বারা  $0, V_{cc}$  দ্বারা Toggle করা একই bistable.

21 two npn transistor monostable multib.

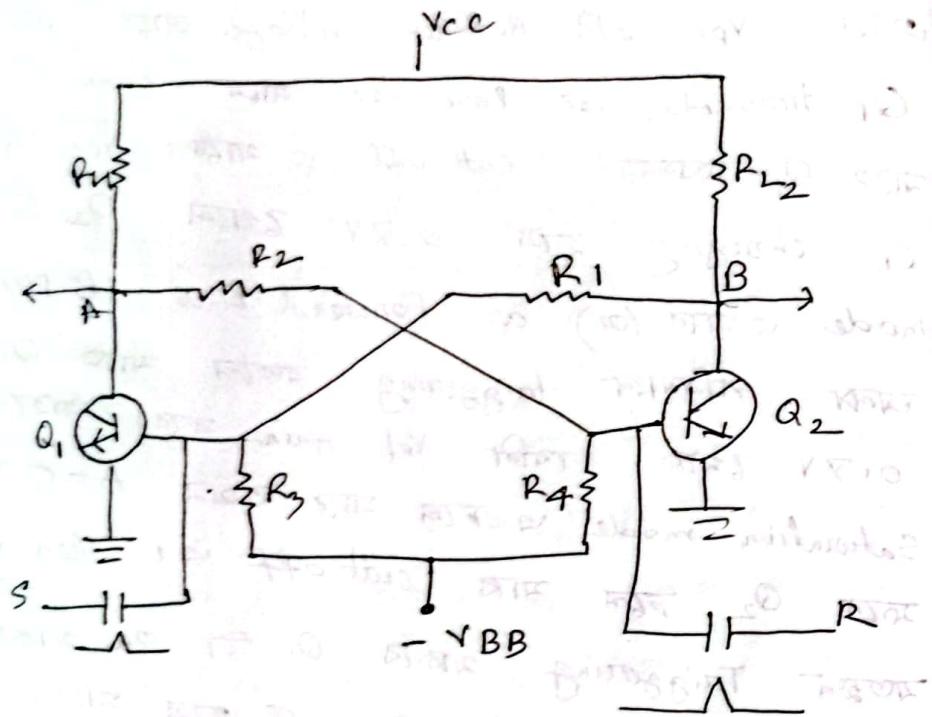


এখানে  $-V_{BB} > R_2$  Reference voltage আছে তামনি  
 Q<sub>1</sub> transistor এর Base এর সাথে connect করা  
 হাতে Q<sub>1</sub> অবস্থায় cut off এ থাকে,  $V_{cc}$  দ্বারা  
 C<sub>1</sub> charging হয়ে 0.7V পর্যন্ত Q<sub>2</sub> Saturation  
 mode হাতে (on) এর Forward Bias. B point=0V  
 অল্প পরিমাণ triggering করলে সাতে Q<sub>1</sub> এ  
 0.7V দ্বারা কৈবল্য যোগ দেয়। আহলে Q<sub>1</sub>  
 Saturation mode এ চলে যাব তখন A=0V.  
 ফলে Q<sub>2</sub> এখন সাতে cut off এ। Then B point  
 =  $V_{cc}$ .  
 অত্যন্ত Triggering থাকবে Q<sub>1</sub> টি on থাকত,  
 Trigger দ্বারা দিলে Q<sub>1</sub> off হয়ে যাব;  
 Trigger করলে কৈবল্য ঘটে, State ও যাব।

22 By using two npn transistor bistable

এটি Stable state থাকত, 0 এর মিল

0 এ থাকব, 1 এ দিলে 1 এ থাকব।



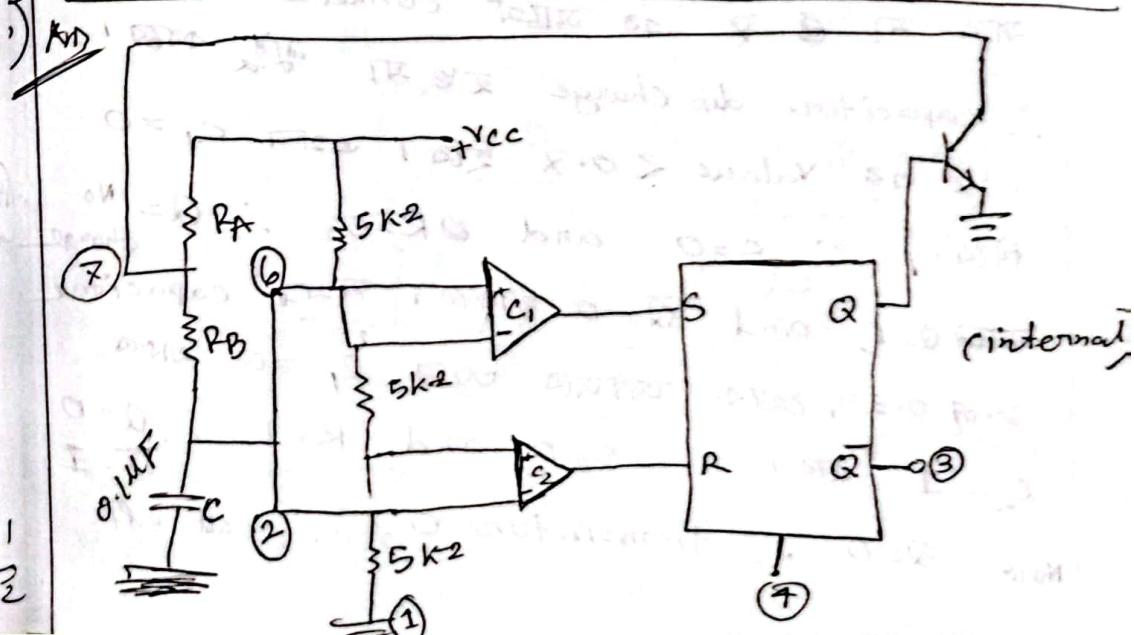
$-V_{BB}$  reference voltage  $R_3$  দিয়ে এবং  $R_4$  দিয়ে  $Q_2$  connect করা।

Initially  $Q_1$  saturation and  $Q_2$  cut off  
 $A = +V_{CC}$  and Forward bias  $B = 0$ ; reverse  
 bias. It is now unstable node.

$R$  এ স্থানে পরিণাম Trigger করতে  $Q_2$  এর  
 base pin পাশে অবস্থানে  $Q_2$  Sat  $\approx 0$   
 অবস্থান  $B = 0$  and অবস্থান  $Q_1$  এর Base 0 হয়।  
 $\therefore Q_1$  cut off হয়ে যাবে; অবস্থান  $Q_2$  cut off?

শর্কর  $Q_2$  হয় Sat.  $\therefore A = +V_{CC} V$ .  
 সম্ভব S এ Trigger করতে  $Q_1$  এর base pin  
 হবে ০.৩V অথবা কমে কমে করতে হবে,  
 $\therefore Q_1$  Sat  $\approx 0$ .  $\therefore A$  point = ০ V  
 $Q_2 = 0$  হয়ে যাবে;  $\therefore$  cut off হয়ে যাবে,  
 $\therefore B$  point =  $V_{CC}$  V.  $\therefore$  ০.৩V state  $\Rightarrow$  stable  
 state।  
 এ অবস্থার স্থানে কি Trigger করতে  
 Trigger করা মাধ্যমে State change করা যাবে।

II) Draw and explain astable using 555 IC.



V<sub>CC</sub> Apply कराए पर R<sub>A</sub> and

R<sub>B</sub> एवं Through C द्वाये तेजले group capacitor charge होगा जूँके trigger

इन 1 charge होते होते

एवं V<sub>1</sub> 0.33V होते

तेजले C<sub>1</sub> and C<sub>2</sub> Reset

हो मात्र 50% C<sub>1</sub>=C<sub>2</sub>

एवं output 1,0 हो मात्र, (V<sub>1</sub>>V<sub>2</sub>) O/P (high)

एवं S=1 and R=0 तेजले Q=1  $\bar{Q}=0$

इन output 3 होते निम्न 3 तो 0.

Q एवं 1 Transistor ए तेजले 01 Sat हो

याहे मा X एवं मात्र connected

∴ capacitor dis charge होगा जूँके करते

∴ C एवं Value < 0.3 होते। एवं C<sub>1</sub>=0

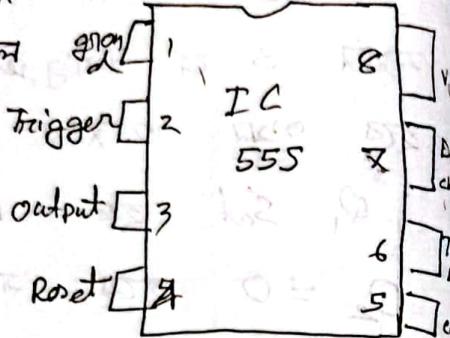
द्विया ∴ S=0 and R=0. ∴ Q=No change

मात्र Q=1, and  $\bar{Q}=0$  होता। यसके capacitor

ठाण 0.33V होते आणि ठाण C<sub>1</sub>=0 होता

C<sub>2</sub>=1 होता. ∴ S=0 and R=1. ∴ Q=0  $\bar{Q}=1$

Now Q=0 से transistor O. ∴ cut off.



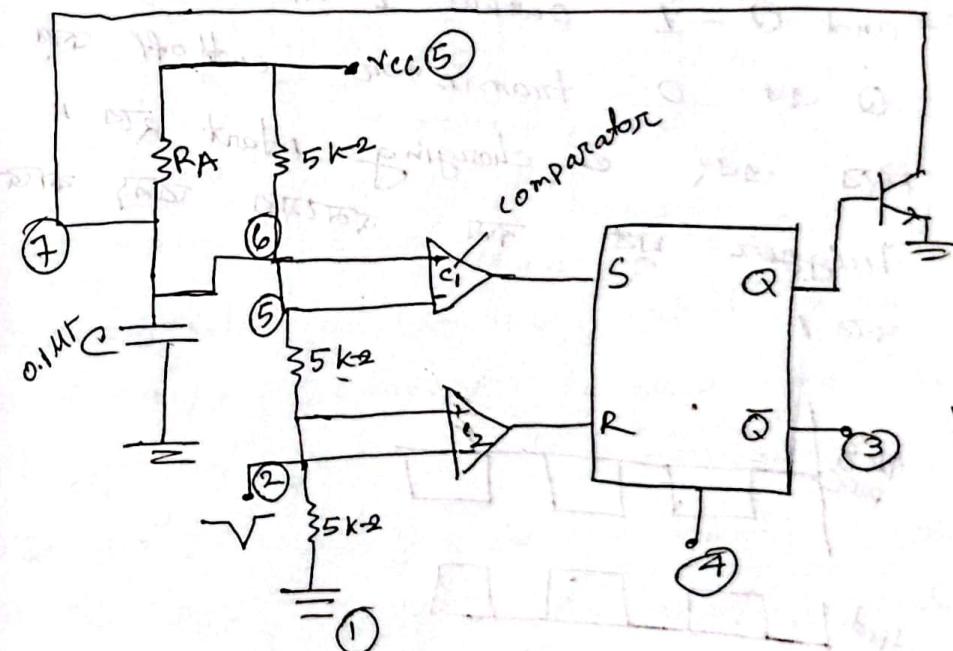
① discharging off हो यावे 50%

capacitor आवे charging हो, 50%

process तेजले घटता

Monostable:

S	R	Q
0	0	unchanged
0	1	0
1	0	1
1	1	ambiguity

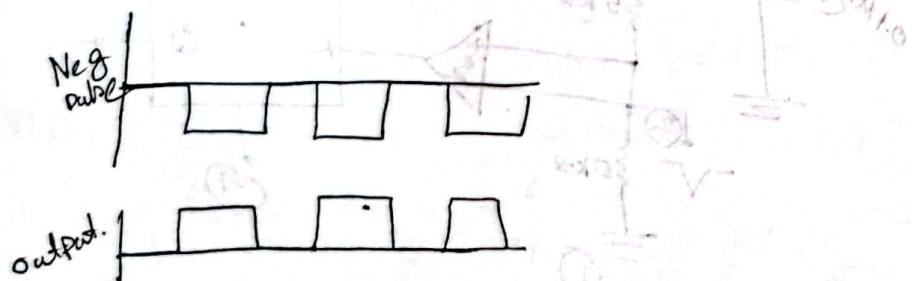


V<sub>CC</sub> एवं Through C charge होगा जूँके हो

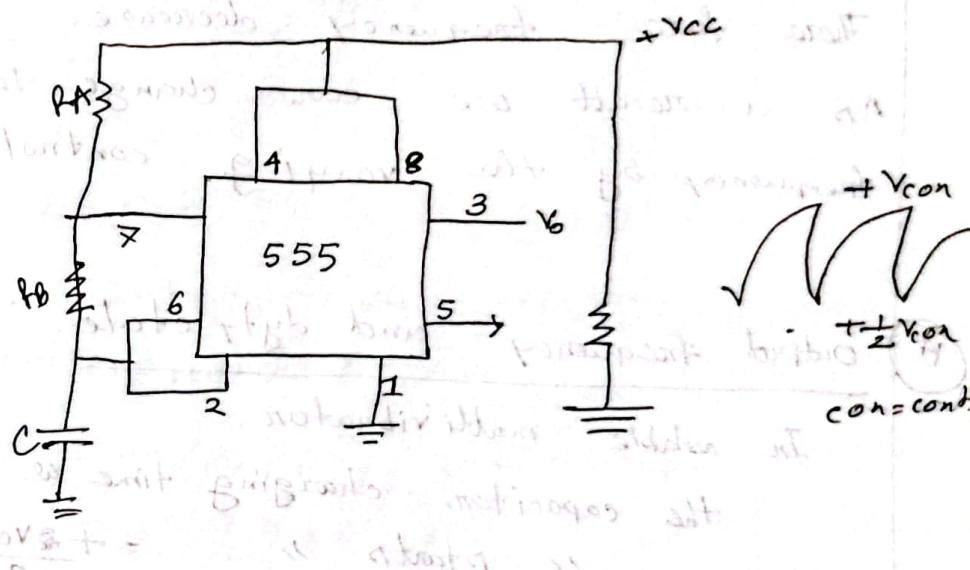
0.7 होते तेजले C<sub>1</sub> on हो मात्र output

1 हो। ∴ C<sub>2</sub> off. ∴ output 0.

⑩  $S=1, R=0 \therefore Q=1, \bar{Q}=0$   
 1 transistor is ON on  $\bar{Q} \cdot C$   
 discharge  $\bar{Q} \cdot 1$  2nd pin is trigger apply  
 Then we will get 1 output in  
 $C_2$  and  $C_1$  become 0  $S=0$  and  
 $R=0$  so output will be  $Q=0$   
 and  $\bar{Q}=1$  output 1 after 93%  
 $Q$  is 0 transistor cut off  
 For 93%  $C$  charging starts  
 Trigger is का एमान्य दृग्य का  
 फॉर्म



⑪ Voltage control Oscillator (VCO) using 555.



- 1) The circuit is sometimes called a voltage to frequency converter because an input voltage can change output frequency.
- 2) The pin 5 connects to the inverting input of the upper comparator. By applying voltage in control pin from an external potentiometer can override the internal voltage. Voltage across timing capacitor varies between  $+V_{con}/2$  to  $+V_{con}$ .

if we increase +V control it takes the capacitor longer to charge and discharge. Therefore frequency decrease.

As a result we can change the frequency by the varying control voltage.

#### A) Output frequency and duty cycle.

In astable multivibrator,

the capacitor charging time is

$$\text{starts} \quad = +\frac{V_{CC}}{3}$$

$$\text{ends} \quad = -\frac{2}{3}V_{CC}$$

$$\text{target} \quad = V_{CC}$$

$$\text{so, } \frac{2}{3}V_{CC} = \frac{1}{3}V_{CC} + \left(V_{CC} - \frac{1}{3}V_{CC}\right)(1 - e^{-t/RC})$$

$$\Rightarrow \frac{2}{3}V_{CC} = \frac{1}{3}V_{CC} + \left(\frac{2V_{CC}}{3} - \frac{V_{CC}}{3}\right)(1 - e^{-t/RC})$$

$$\Rightarrow \frac{2}{3}V_{CC} = \frac{1}{3}V_{CC} + \frac{2V_{CC}}{3}(1 - e^{-t/RC})$$

$$\Rightarrow \frac{2}{3}V_{CC} = \frac{3}{3}V_{CC} \left(\frac{1}{2} + (1 - e^{-t/RC})\right)$$

$$\Rightarrow 0 = \frac{1}{2} + (1 - e^{-t/RC})$$

$$\Rightarrow \frac{1}{2} = 1 - e^{-t/RC}$$

$$\Rightarrow -\frac{1}{2} = (1 - e^{-t/RC})$$

$$\Rightarrow -1.5 = -e^{-t/RC}$$

$$\Rightarrow t = 0.693RC$$

$$w = 0.693(R_A + R_B)C \text{ (charging)}$$

$$\text{discharging} = 0.693R_B C$$

$$T = 0.693(R_A + R_B)C + 0.693R_B C \\ = 0.693(R_A + 2R_B)C$$

$$\text{Duty cycle} = \frac{w}{T} \times 100\%$$

$$= \frac{0.693(R_A + R_B)C}{0.693(R_A + 2R_B)C} \times 100\%$$

$$= \frac{R_A + R_B}{R_A + 2R_B} \times 100\%$$

$$\text{frequency : } f = \frac{1}{T} = \frac{1}{0.693(R_A + 2R_B)C}$$

## Duty cycle

Duty cycle is the ratio of charging time constant to charging plus discharging time constant.

$$\text{Dytrycycle} = \frac{\omega}{T} \times 100\%$$

$w = \text{charging time constant}$

$T$  = charging & discharging time constant

$$\text{Duty cycle} = \frac{R_A + R_B}{R_A + 2R_B} \times 100\% = T$$

if  $R_A$  is much much smaller than  $R_B$

$$\text{then } R_B \gg R_A \therefore \frac{O+R_B}{O+2R_B} \times 100 \\ = 50\%$$

For 555 astable timer circuit

impossible to duty cycle 50% why

To get 50% duty cycle,  $D = \frac{t_0}{T} = \frac{1}{2}$

$$\Rightarrow T = 2\omega.$$

OR, in a Astable circuit discharging time constant is less than charging time constant.

$$D = \frac{R_A + R_B}{R_A + 2R_B} \times 100$$

$$D = 50\pi \text{ when } R_A = 0$$

But if  $R_A = 0$  the transistor can get damaged by  $V_{ce}$   
so, it is impossible.

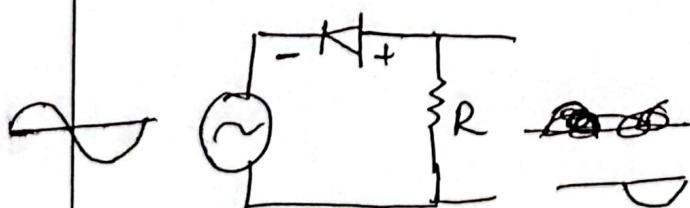
## clipper

- ① Clipper is a circuit which clip a portion of a input signal without distortion of remaining part.

i) It control the output wave form.

ii) Another name dicer, limiter.

iv) made with diode, resistor.



positive clipper

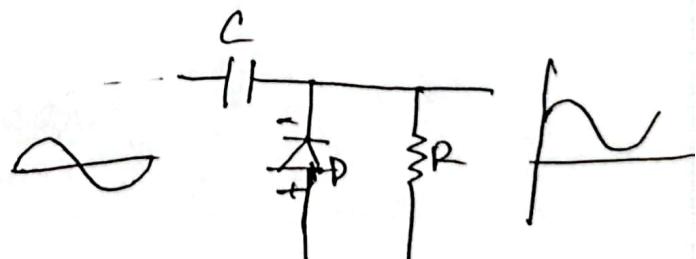
## clamper

- ② A clamper is a signal which shift DC level of AC signal.

ii) It doesn't change the shape of wave form

iii) Another name D level shifter

iv) diode, resistor and capacitor.



positive clamper

## Quantization error:

It is the difference between analog signal and closest digital value at each sampling instance from A/D converter.

It is an inherent uncertainty of digitizing analog value.

Example:

In rounding and truncation  
The higher the resolution of the ADC  
The lower quantization error.

We know The resolution of ADC is  
the number of bit which are used to  
digitilize analog value. It determines  
how many output code ( $2^n$ ) a converter  
can produce.

Increasing the divisor, increasing the  
counter timerbase rate or lowering the  
input signal frequency can reduce  
quantization error.