

No linear

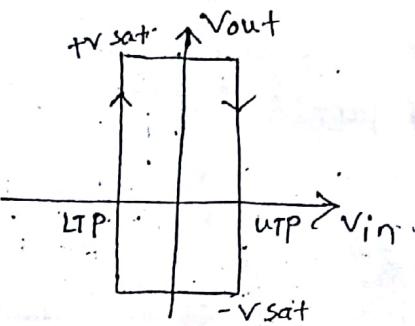
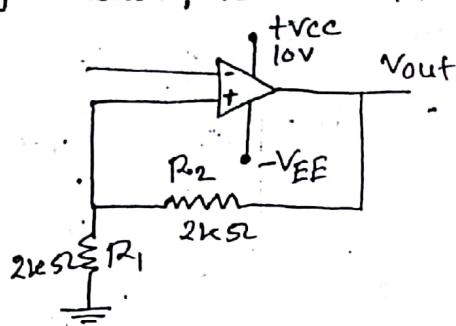
DEPT (Code: 2203)

①

Application of op-amp

Q1 By using op-amp draw & explain a schmitt trigger circuit that has zero volt centered hysteresis.

Ans Fig shows the schmitt trigger.



Because of the voltage divider, we have positive voltage feedback.

Here, $V_{CC} = 10V$, $R_1 = R_2 = 2k\Omega$ & $V_{cen} = 0V$.

Feedback fraction is, $B = \frac{R_1}{R_1 + R_2} = \frac{2}{2+2} = \frac{1}{2}$

Assume, V_{sat} is 8V

The schmitt trigger has zero volt centered hysteresis

The trip point are

$$UTP = V_{cen} + B V_{sat} = 0 + \frac{1}{2} \times 8 = 4V$$

$$LTP = V_{cen} - B V_{sat} = 0 - \frac{1}{2} \times 8 = -4V$$

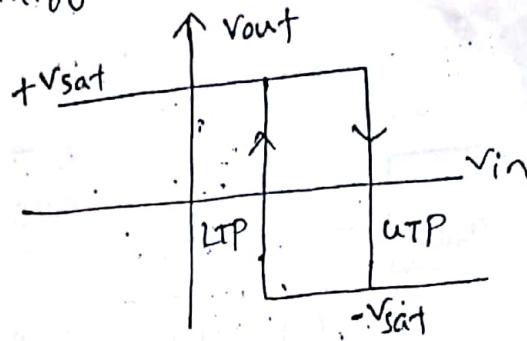
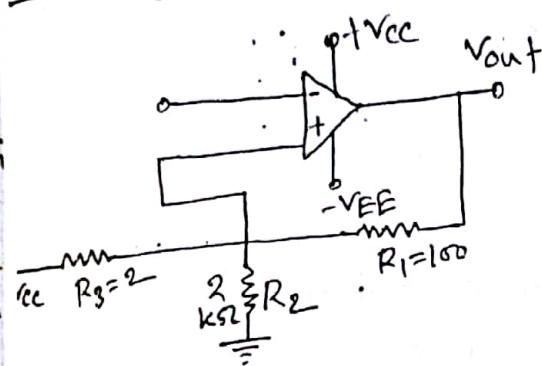
So for the positively saturated output, the difference voltage applied to the non-inverting input is equal to the UTP & for negative saturated voltage, is equal to the LTP

Schmitt trigger: schmitt trigger is a comparator with positive feedback which is used to avoid noise triggering.

(ii) By using op-Amp draw & explain a schmitt trigger circuit that has +5V centered hysteresis.

Ans: Fig shows a schmitt trigger circuit.

Ans:



An additional resistor R_3 is connected between the non-inverting input & $+V_{CC}$. The centre of the hysteresis loop is

$$V_{cen} = \frac{R_2}{R_2 + R_3} V_{CC}$$

$$\Rightarrow S = \frac{2}{2+2} V_C \Rightarrow V_{CC} = 10V$$

The positive feedback spread the trip point on each side of the center voltage

$$\text{The feedback fraction is, } B = \frac{R_2 || R_3}{R_1 + R_2 || R_3} = \frac{2 || 2}{100 + 2 || 2} = \frac{1}{100+1} \frac{1}{101} \approx 0.01$$

The trip points are

$$UTP = V_{cen} + B V_{sat} = 5 + 0.01 \times 10 = 5.1V$$

$$\& LTP = V_{cen} - B V_{sat} = 5 - 0.01 \times 10 = 4.9V$$

Hysteresis in schmitt trigger: In a schmitt trigger, the difference b/w two trip points is called hysteresis

fig @
output

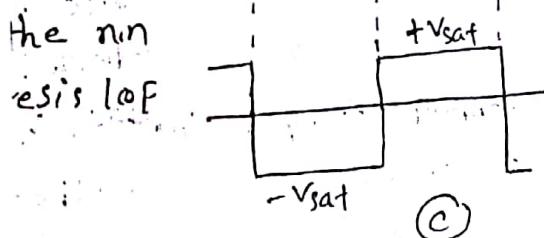
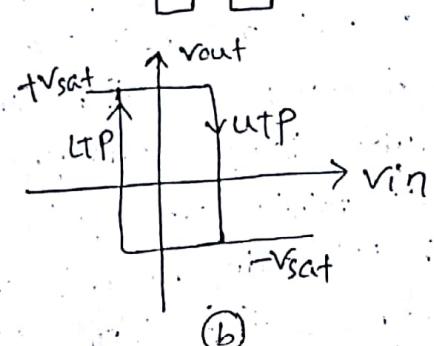
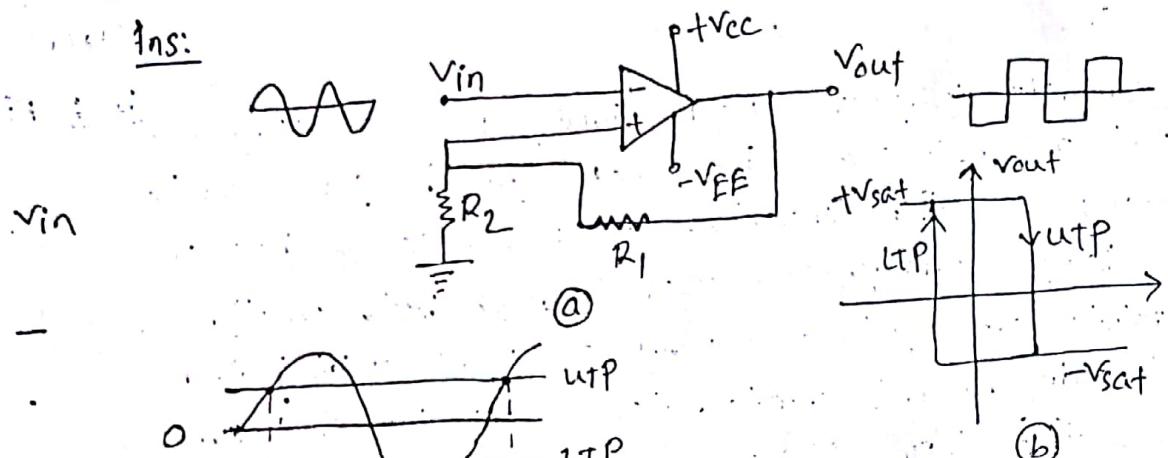
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Q2) By using op-amp draw & explain a schmitt trigger circuit to produce rectangular wave from sine wave.

Ans:



The graph showing (a) schmitt trigger (b) transfer characteristic (c) graph showing each output voltage versus input voltage

figure shown the graph of output voltage versus input voltage and shown the transfer characteristics & a schmitt trigger.

When the input signal is periodic, the output of schmitt trigger produces a rectangular waveform.

Let assumes that the input signal is large enough to pass through both trip points in Fig c.

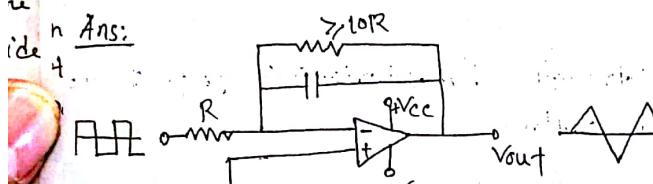
When the input voltage exceeds the UTP on the upper

(c) By using op-amp draw a circuit. During the positive half cycle, the output voltage switches to $-V_{sat}$. Half a cycle later, the input voltage decreases & the output switches back to $+V_{sat}$.

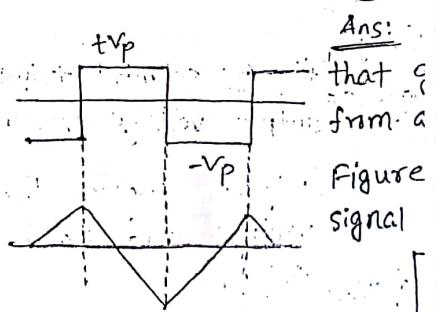
A schmitt trigger always produces a rectangular wave output regardless of the shape of the input voltage signal. As long as the waveform is periodic & has an amplitude large enough to pass through between the two trip points, we get a rectangular wave output from the schmitt trigger. This rectangular wave has the same frequency as the input signal.

(d) By using op-amp draw & explain a schmitt trigger circuit to produce triangular wave form rectangular wave.

Ans:



(a) Rectangular input to integrator produces triangular output



(b) Input & output wave form

Fig (a) a rectangular wave to an integrator. Since the input signal has a dc or average value of zero, the dc & average value of the output is also zero.

As shown in Fig (b), the ramp is decreasing during the

Ans:

that from a figure signal

Astable
 multivibrators using
 Diving
 pulse

①

Oscillator: It's an electronic circuit that produces a periodic, oscillating electronic signal often a sine or square wave. convert DC to AC.
 types - ① Harmonic oscillator: sinusoidal output.
 ② Relaxation oscillator: produce non-sinusoidal output

Q. A positive half cycle of the input signal & increasing during the negative half cycle of the input signal. therefore, the output waveform has the same frequency as the input voltage.

Ans: The ramp waveform is periodic and has a peak-to-peak output.

$$V_{out}(P-P) = \frac{V_{in}(P-P)}{4fRC}$$

where, $V_{out}(P-P)$ = peak-to-peak output voltage, triangular

$V_{in}(P-P)$ = " " " input, " " rectangular

f = input frequency, R = Resistance of integrator,
 C = capacitance of integrator.

B1 No. 8(a)

Q. By using op-amp draw and explain a relaxation oscillator.

Ans: with positive feedback, it is possible to build oscillators that generate an output signal with no external input signal from an operational amplifier.

Figure shows a relaxation oscillator, that has no input signal but generates an output rectangular wave.

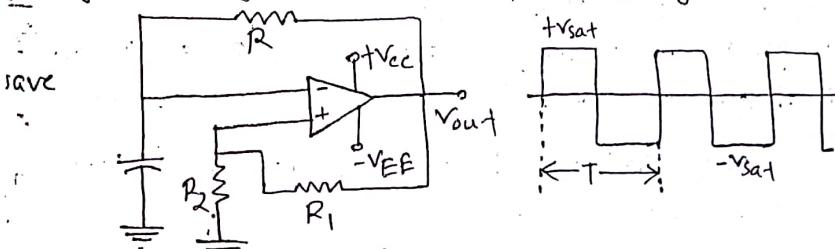


Fig: a relaxation oscillator

Q) By using OP-AMP

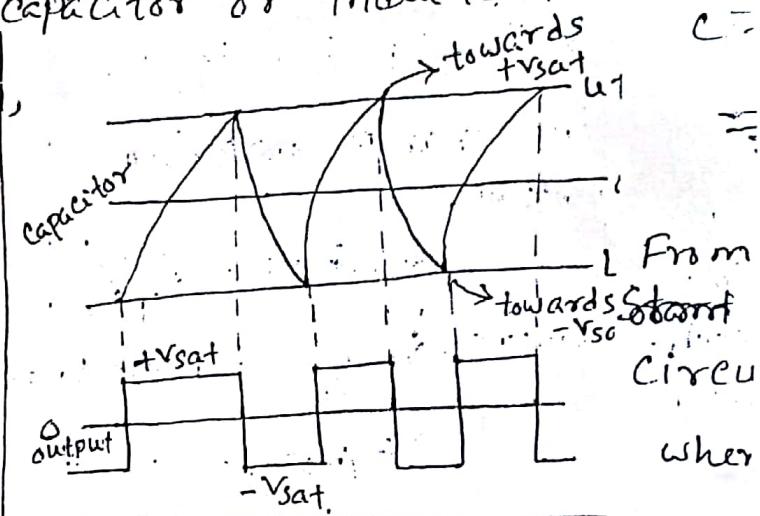
In other words, a relaxation oscillator is a circuit that generates an output signal whose frequency depends on the charging or discharging of a capacitor or inductor.

If the output is in positive saturation, the capacitor will charge exponentially towards $+V_{sat}$. It never reaches $+V_{sat}$ because its voltage hits the UTP [fig (b)]

Then the output switches to $-V_{sat}$.

Now a negative voltage is being

feedback. So the capacitor reverse fig (b) continuous charging & its charging direction. The capacitor discharging of capacitor makes voltage decreases as shown.



C
=
From
to
Output
+Vsat
-Vsat
Circu
wher

When the capacitor voltage hits the LTP the output switches back to $+V_{sat}$. Because of the capacitor continuous charging initial & discharging of the capacitor, the output is as rectangular wave. This is how a relaxation oscillator works.

~~So prove that, $T = 2RC \ln \frac{1+B}{1-B}$~~ is the period of the output rectangular wave of an op-amp relaxation oscillator where B = feedback fraction.

Ans: Figure shows that UTP has a value of $+B.V_{sat}$ & LTP has a value of $-B.V_{sat}$

Difference bet. two t.o.

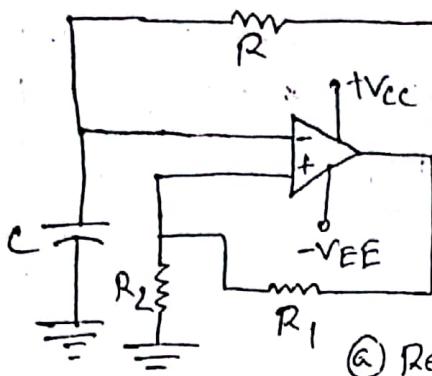
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+1

vi

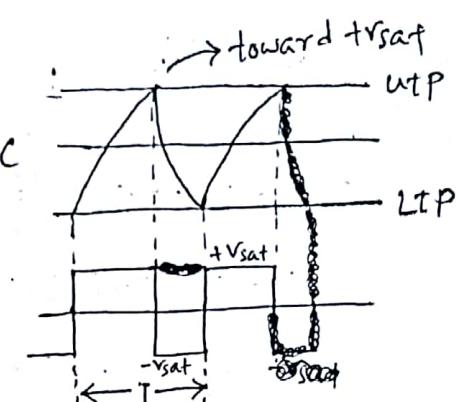
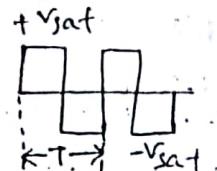
ls

-1



(a) Relaxation oscillator.

②



(b) Capacitor & output voltage

From

and from with the basic switching equation applies to any RC circuit, $V = V_i + (V_f - V_i)(1 - e^{-t/RC}) \quad \text{--- (1)}$

where, V = instantaneous capacitor voltage

V_i = initial capacitor voltage.

V_f = Target capacitor voltage

t = charging time

Figure shows that, the capacitor charge starts with an initial value of $-BVs_{sat}$ & ends with a voltage of $+BV_{sat}$.

The target voltage is $+V_{sat}$ & the capacitor charging time is half of the period, T_0 .

So from the equation (1)

$$V = V_i + (V_f - V_i)(1 - e^{-t/RC})$$

$$\Rightarrow BV_{sat} = -BV_{sat} + (V_{sat} + BV_{sat})(1 - e^{-T_0/RC})$$

$$\Rightarrow BV_{sat} + BV_{sat} = V_{sat}(1+B)(1 - e^{-T_0/2RC})$$

$$\Rightarrow 2BV_{sat} = V_{sat}(1+B)(1 - e^{-T_0/2RC})$$

$$\Rightarrow 2B = (1+B)(1 - e^{-T_0/2RC}) \Rightarrow \frac{2B}{1+B} = 1 - e^{-T_0/2RC}$$

(7) By using op-amp

$$\Rightarrow e^{-T/2RC} = 1 - \frac{2B}{1+B} \Rightarrow e^{-T/2RC} = \frac{1+2B-2B}{1+B} = \frac{1-B}{1+B}$$

$$\Rightarrow -T/2RC = \ln\left(\frac{1-B}{1+B}\right)$$

$$\Rightarrow -T = 2RC \times \left[-\ln\left(\frac{1-B}{1+B}\right)\right]$$

$$\Rightarrow T = 2RC \ln \frac{1+B}{1-B}$$

(8) An op-amp relaxation oscillator has feedback fraction $B=0.9$, feedback resistor $R=4.7$ ohms & charging-discharging capacitor $C=0.022\text{MF}$: what is the frequency of the output rectangular wave?

Ans: we know, $T = 2RC \ln \frac{1+B}{1-B}$

$$\Rightarrow T = 2 \times 4.7 \times 0.022 \times \ln \frac{1+0.9}{1-0.9}$$

$$= 0.2068 \times \ln 19 = 0.6089 \text{ S}$$

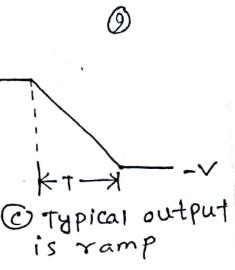
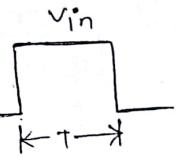
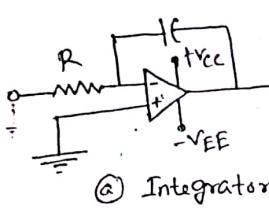
$$\therefore \text{Frequency, } f = \frac{1}{T} = \frac{1}{0.6089} = 1.6423 \text{ Hz}$$

(9) Draw & Explain a practical op-amp integrator. Explain the necessity of large resistor across the capacitor.

Ans: An integrator is a circuit that performs the mathematical operation of integration because it produces an output voltage that is proportional to the integration of the input.

A common application is to use a constant input voltage to produce a ramp of output voltage.

$\frac{-B}{+B}$



The typical input to an integrator is a rectangular pulse. Because of the virtual ground, the input current is constant & equals: $I_{in} \approx \frac{V_{in}}{R}$

Approximately all the current goes to the capacitor.

$$C = \frac{Q}{V} \therefore V = Q/C \quad \text{--- (1)}$$

Since a constant current is flowing into the capacitor, charge Q increases linearly.

Because of the phase reversal of the op-amp, the output voltage is a negative ramp.

By dividing the equation (1) by T :

$$\frac{V}{T} = \frac{Q/C}{T} \Rightarrow \frac{V}{T} = \frac{Q}{C} \times \frac{1}{T} \Rightarrow \frac{V}{T} = \frac{Q}{T} \times \frac{1}{C}$$

$$\Rightarrow \frac{V}{T} = I \times \frac{1}{C} \Rightarrow V = \frac{IT}{C}$$

where, V = Capacitor voltage
 I = charging current $= \frac{V_{in}}{R}$

T = charging time

C = capacitance

Necessity of large resistor across the capacitor:

Ans: Circuit that has +5V op-amp draw of current.
Fig. 1x swing of the pot.:
 $\Rightarrow e^{-T/2RC} = 1 - \frac{2B}{e}$. (19)

An: Ans sheet

Ans:
1) v_c
2) v_i
3) v_o

v_{in}

Solvin

Q) Draw and explain a practical op-amp differentiator. Explain where the necessity of a small resistor in series with the capacitor.

Ans: Fig. (a) shows an op-amp differentiator. When the input voltage varies, the capacitor charges or discharges. Because of the virtual ground, the capacitor current passes through the feedback resistor, producing a voltage. This voltage is proportional to the slope of the input voltage.

Ans: An input often used with op-amp differentiators is ramp like the top waveform of fig. (b). Because of the virtual ground, all the input voltage appears across the capacitor. The ramp of voltage implies that the capacitor current is constant. Since all this constant current flows through the feedback resistor, we get an inverted pulse at the output, as shown in Fig. (b).

At the end of the ramp, the capacitor voltage is

$$V = Q/C$$

①

Dividing both sides by the ramp time gives

$$\frac{V}{T} = \frac{Q/T}{C} \Rightarrow V_T = \frac{I}{C}$$

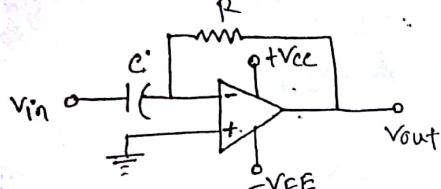


Fig: (a)

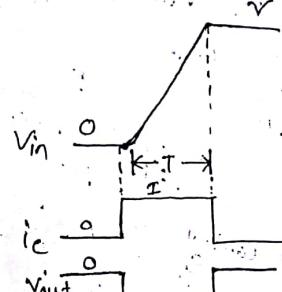


Fig: (b)

Solving for Current, we get

$$I = \frac{CV}{T}$$

Plz
where
I = Capacitor current
C = Capacitance

V = voltage at end of ramp

T = time between start & end of ramp

The necessity of small resistor in series with capacitor:

Writ Sheet

ramp
virtual

08

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✓ Multivibrator (15)

Draw & explain the following multivibrators by using 555 IC.

① Monostable ② Astable

① monostable:

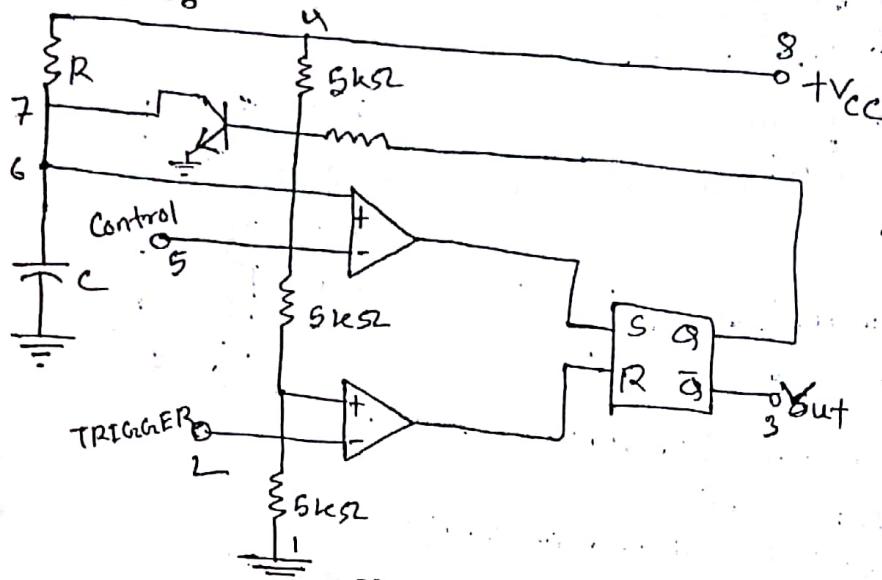
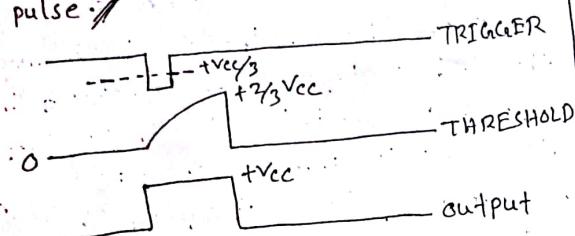


Fig: 1(a)

[Figure 1(a) shows the operation of the 555 timer for monostable. The circuit works as follows: When the trigger input is slightly less than $+V_{CC}/3$, the lower comparator has a high output and resets the flip-flop. This cuts off the transistor, allowing the capacitor to charge. When the capacitor voltage is slightly greater than $+2/3(V_{CC})$, the upper comparator has a high output, which sets the flip-flop. As soon as Q goes high, it turns on the transistor, & quickly the capacitor discharges.] Fig 1(b) shows typical waveforms. The trigger input is a narrow pulse with a quiescent value of $+V_{CC}$. The pulse must drop below $+V_{CC}/3$ to reset the flip-flop & allow the capacitor to charge again.

when the threshold voltage slightly exceeds $+2V_{cc}/3$, the flip-flop sets, this saturates the transistor & discharge the capacitor. As a result we get one rectangular output pulse.



In figure 1②, pin 5 is bypassed to ground through a small capacitor typically $0.1\mu F$. This provides noise filtering for the control voltage. To avoid accidental reset, pin 4 is usually tied to the supply voltage.

In summary, the monostable 555 timer produces a single pulse whose width is determined by the external R and C used in Fig 1②.

Schematic diagram for the monostable circuit

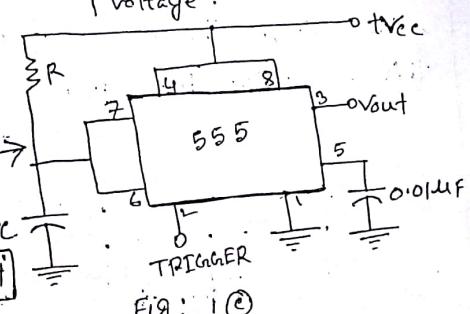
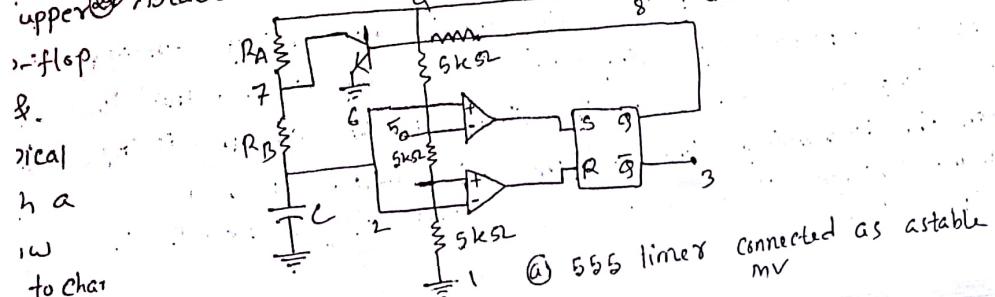


Fig: 1②

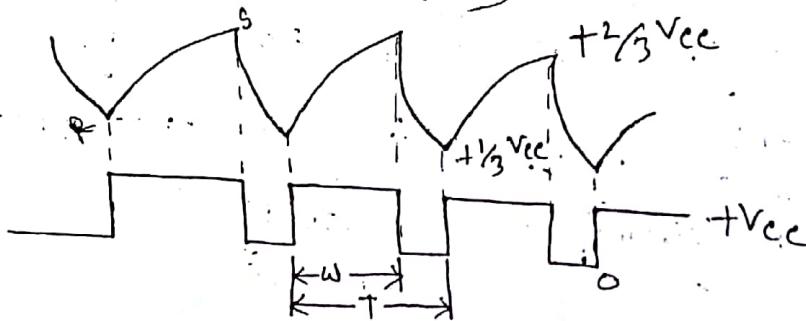
Astable multivibrator using 555 timer IC:



④ 555 timer connected as astable mv

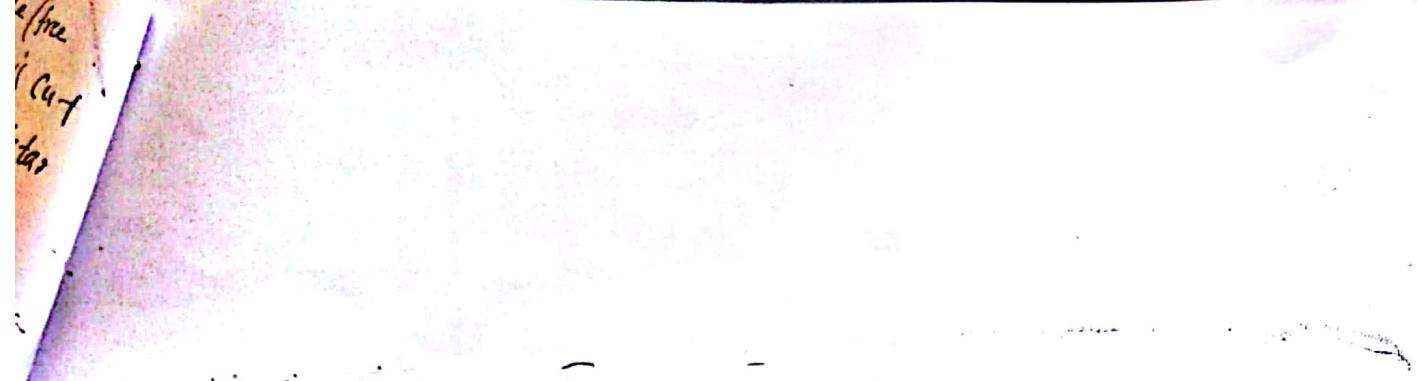
(14)

Figure shows the 555 timer connected for astable (free running) operation. When Q is low, the transistor is cut off and the capacitor is charging through a total resistance of $R_A + R_B$. Because of this, the charging time constant is $(R_A + R_B)C$. As the capacitor charges, the threshold voltage increases. Eventually, the threshold voltage exceeds $+2V_{CC}/3$ the upper comparator has a high output & this sets the flip-flop with Q high, the transistor saturates. Now the capacitor discharges through R_B . Therefore, the discharging time constant is $R_B C$. When the capacitor voltage drops slightly below $+V_{CC}/3$, the lower comparator has a high input & this resets the flip-flop.



⑥ Capacitor and output waveform

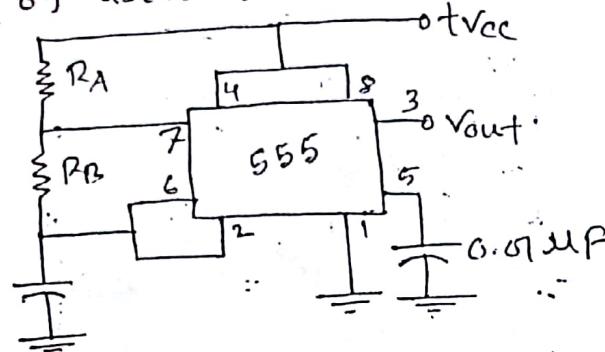
This figure illustrates the waveforms. The timing capacitor has an exponentially rising & falling voltage. The output is a rectangular wave. Since the charging time constant is larger than the discharging time constant, the output is not symmetrical. The high output state lasts longer than the low output state.



Internal diagram of astable

MV

(15)



Ques 2) ~~VCO. By using 555 IC timer~~

Ans: Fig ① shows a voltage controlled oscillator (vco), one application for a 555 timer. This circuit is sometimes called a voltage to frequency converter because an input voltage can change the output frequency. In an 555 timer IC, pin-5 (control) connects to the inverting input of the upper comparator. Normally, the control voltage is $+2V_{CC}/3$ because of the internal voltage divider. In fig, by applying a voltage in control pin, we can override the internal voltage.

In this case, voltage across timing capacitor varies betn $t_{Vcontrol}/2$ and $t_{Vcontrol}$. If we increase $t_{Vcontrol}$, it takes the capacitor longer to charge & discharge, therefore the frequency decrease. As a result, we can change the frequency of the circuit by varying the control voltage.]

(10)

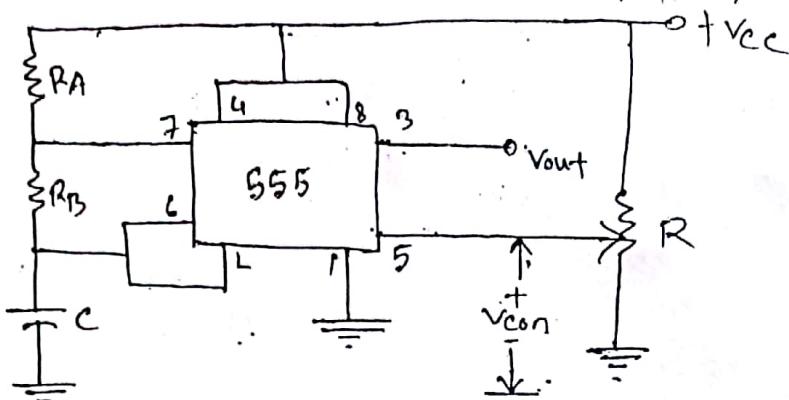


fig (b) illustrates the voltage across the timing capacitor. Notice that, it varies between $+V_{Control}$ and $-V_{Control}$. If we increase $V_{Control}$ it takes the capacitor longer to charge & discharge, therefore the frequency decreases. As a result, we can change the frequency of the circuit by varying the control voltage. Incidentally, the control voltage may come from a potentiometer or it may be the output of a transistor circuit, op-amp or some other device. One of the more interesting applications for a VCO is the phase-lock loop (PLL).

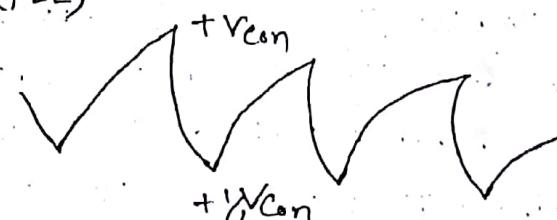


fig (b)

16) Show how to use a 555 timer and a bipolar current source to produce ramp output. (V.V.Q)

(17)

Ans: Ramp output: A ramp is a linearly increasing or decreasing voltage. We get a ramp output waveform if we use a constant current source to charge a capacitor producing ramp output.

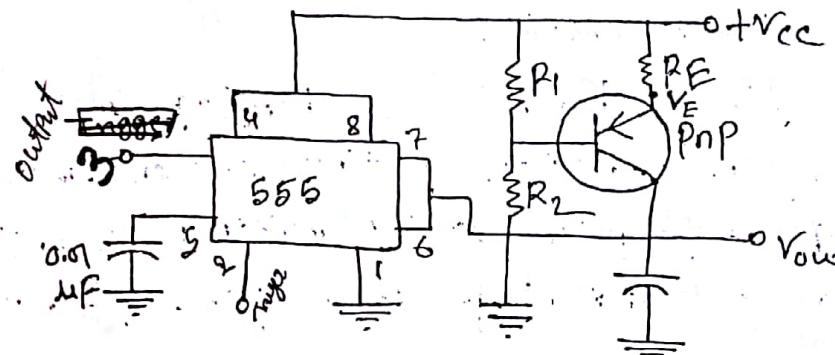


Fig.(a): using a 555 timer and a Bipolar Current source to produce of ramp out put voltage

In the figure, a bipolar constant current source is used to charge a capacitor.

Here we replace the resistor of 555 timer circuit with a PNP current source that produces a constant charging current of $I_C = \frac{V_{CC} - V_E}{R_E}$

Here,

$$V_E = \frac{R_2}{R_1 + R_2} V_{CC} + V_{BE}$$

when trigger starts the monostable 555 timer of fig.(a), the PNP current source forces a constant ^{charging} current into the capacitor. Therefore, the voltage across the capacitor is a ramp as shown in figure (b). The slope of the ramp is given by $s = I_C/C$

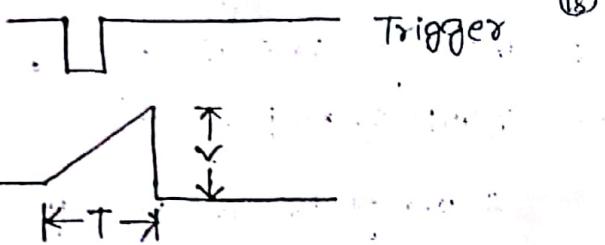


Fig ⑥: Trigger and ramp waveform

But

- ⑯ what is duty cycle? show how to calculate duty cycle is for a 555 astable timer circuit.

Duty cycle: Duty cycle is the ratio of charging time constant to charging plus discharging time constant. Duty cycle is the width of a pulse usually, multiply by 100% to get the answer as a percentage duty cycle = $\frac{W}{T} \times 100\%$, where, W = charging time constant and T = charging & discharging time constant.

⑯ v

vib

Ans:

tra

& R

Capacitor charges through $(R_A + R_B)$. So charging time constant is $(R_A + R_B)C$. Capacitor discharges through R_B . So discharging time constant is $R_B C$.

$$\text{Duty Cycle} = \frac{R_A + R_B}{R_A + 2R_B} \times 100\%$$

Q

if R_A is much smaller than R_B then the duty cycle approaches 50%

For a 555 astable timer circuit it is impossible to make the duty cycle 50%. why?

Ans: we know that, Duty Cycle = $\frac{W}{T} \times 100\%$

$$\textcircled{19} \quad = \frac{\text{charging time constant}}{\text{charging + Discharging time constant}} \times 100\%$$

To get 50% duty cycle, we need $D = \frac{w}{T} = \frac{1}{2}$

or charging time constant = discharging time constant

But it is impossible because discharging time constant is less than charging time constant.

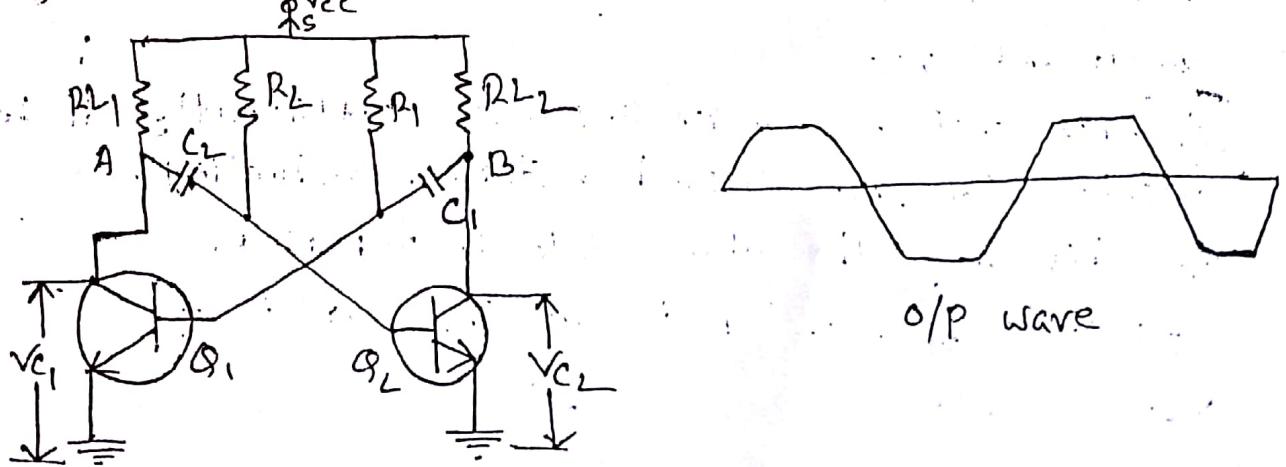
$$\text{Again, } D = \frac{R_A + R_B}{R_A + 2R_B} \times 100\% \text{ for a astable circuit}$$

D will 50% when $R_A = 0$. If $R_A = 0$, the transistor may be damaged by V_{cc} . So it is impossible for astable circuit to make duty cycle 50%.

~~(19)~~ \checkmark By using two npn transistors draw an astable multivibrator. Explain it.

Ans: Fig shows an astable multivibrator with two npn transistors. The transistor \textcircled{Q}_1 is forward biased by V_{cc} & R_1 & the transistor \textcircled{Q}_2 is forward biased by V_{cc} & R_2 .

\textcircled{Q}_1 & \textcircled{Q}_2 are determined by R_{L1} & R_{L2} together with V_{cc}



- (2)
- when switches on by closing S, one of the transistors will start conducting before the other does. Suppose that, Q_1 starts conducting before Q_L does. The operations are:
- ① since Q_1 is in saturation, whole of V_{CC} will drop into R_{L1} . Hence $V_{C1} = 0$ & point A is at zero or ground potential.
 - ② since Q_2 is in cut-off, no voltage drop across R_{L2} so B_{MV} is equal to V_{CC} .
 - ③ since A is at 0V, C_L starts charging through R_2 towards Q_2 & is soon moved to saturation. So that it starts conducting & V_{C2} decreases and become almost 0 when Q_L get saturated. The potential of point B decreases from V_{CC} to almost 0V. So, Q_1 is pulled out of saturation & is soon driven to cut-off.
 - ④ since now point B is at 0V, C_1 starts conducting the current collected in the circuit.
 - ⑤ V_{C2} becomes forward of C_1 increases sufficiently. Q_1 becomes biased & starts conducting. In this way, the whole cycle is repeated.
 - ⑥ It is seen when Q_1 is on then Q_L is off.
 - ⑦ When voltage across C_1 becomes forward, C_1 starts conducting the current collected in the circuit.

(21)

Q21) By using two npn transistors draw a monostable multivibrator. Explain it.

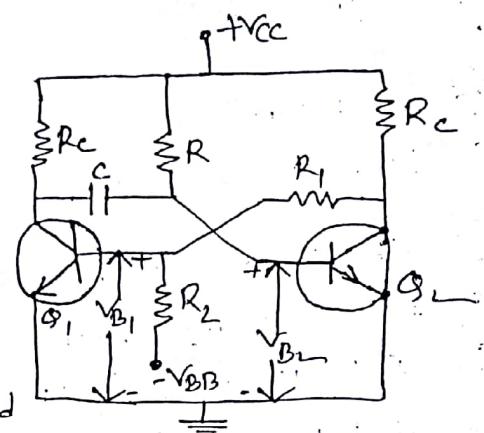
e: Ans: Fig shows the circuit of an monostable multivibrator with two npn transistor.

Assume that the circuit parameters have been adjusted properly so that B MV finds itself in its stable state with transistor \varnothing_1 OFF & \varnothing_2 ON i.e.

\varnothing_2 is in the saturation region of the transistor.

assume that a single trigger is applied to base B_2 and that a regenerative action takes place & driving transistor \varnothing_2 completely below cut-off. The voltage at collector C_2 now rises to approximately V_{CC} & because of the cross-coupling between collector C_2 and base B_1 , the first transistor \varnothing_1 comes into conduction. This transistor may be driven into saturation. A current I_1 now exists in the output-circuit resistor R_C of transistor \varnothing_1 & the voltage at collector C_1 drops abruptly by an amount $I_1 R_C$. The voltage at base B_2 drops by the same amount because the voltage across C cannot change instantaneously. The MV is now in its quasi-stable state.

The circuit will remain in this quasi-stable state for only a finite time T because B_2 is connected to V_{CC} through R . Therefore B_2 will rise in voltage & when it passes the cut-in-voltage V_B of \varnothing_2 , a regenerative action will take place, turning \varnothing_1 off and eventually returning the MV



to its initial stable state.

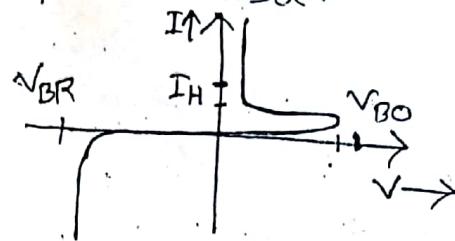
(22)

In this way, the whole cycle is repeated. It is seen when φ_1 is on then φ_L is off & vice-versa.

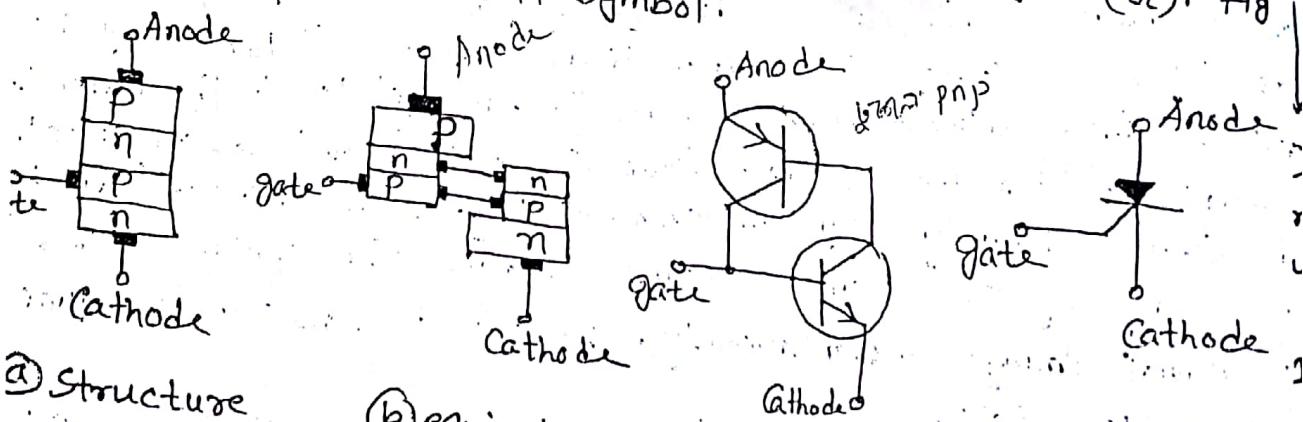
Thyristors

(22) Explain the characteristics of thyristors. e.g SCR, DIAC, TRIAC, UJT

Ans:



- ① SCR (Silicon Controlled Rectifier): The SCR consists of four layers of semiconductor material. Because of its construction, the SCR is sometimes referred to as a four layer diode or a pnpn device. There are three junctions: J_1 , J_2 , & J_3 and three terminals: anode (A), cathode (K) & gate (G).
- ② Shows the SCR circuit symbol:



③ Structure

SCR are not intended for break over operation. They are intended for break over voltage range from 50 to more than 2500V, depending on the SCR type number. Most people think,

(b) equivalent structure

(c) Equivalent circuit

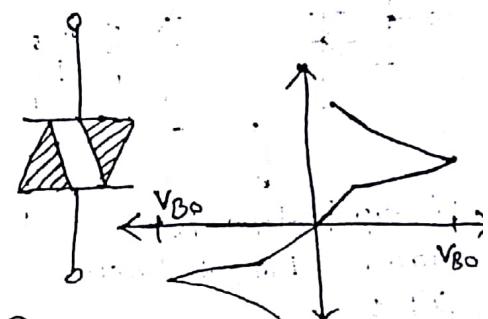
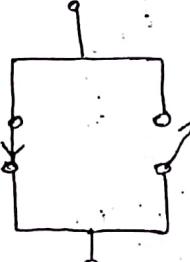
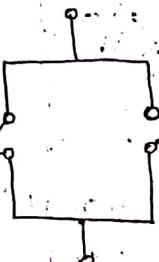
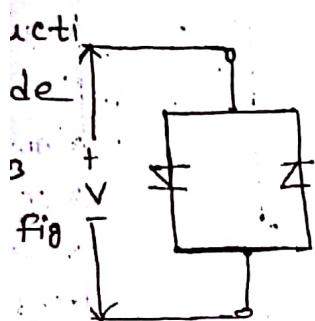
(d) schematic symbol

②³) SCR is a device that blocks voltage until the trigger loses it. For this the breakdown voltage is called the forward blocking voltage.

The 2N4441 has a forward blocking voltage of 50V. As long as the supply voltage is less than 50V, the SCR can not break over. The only way to close it is with a gate trigger. The only way to open SCR is with low current dropout.

IAE

① DIAC: DIAC is a bidirectional bidirectional devices in which four the latch current can flow in either direction.



② Equivalent to ③ equivalent ④ left ⑤ schematic symbol

parallel back to back circuit. latch circuit

pair of

IAE is a four layer diodes in parallel shown in fig ⑤,

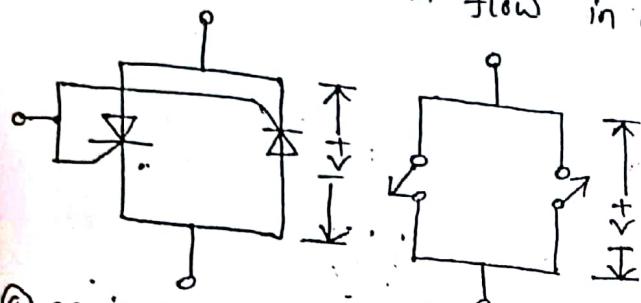
left equivalent circuit of DIAC shown in fig ③: V has the polarity indicated in fig ⑤. The left diode conducts when V tries to exceeds the break over voltage. In this case, left latch closes as shown in fig ④ & other is open. On the other hand, if the polarity of V is opposite th

(24)

right latch is closed when V tries to exceed the break over voltage.

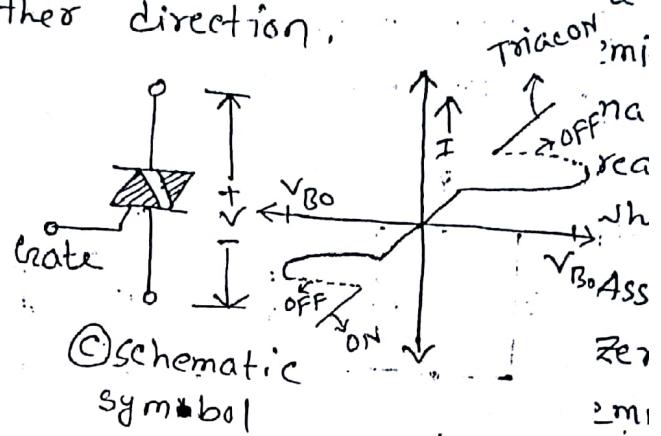
once the DIAC is conducting, the only way to open it, is below the rated dropout. This means reducing the current holding current of the device.

③ TRIAC: TRIAC is a bidirectional device in which the current can flow in either direction.



④ equivalent to parallel back-to-back SCR's

⑤ equivalent circuit

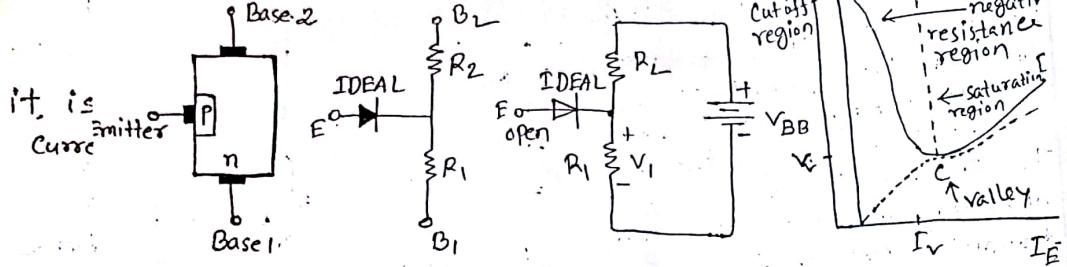


[TRIAC is a pair of two SCRs in parallel shown in fig (a). The break over voltage is usually high in TRIAC. So the normal way to turn on a TRIAC is by applying forward bias trigger.

If V has the polarity, we have to apply positive trigger to close the left latch. When V has opposite polarity, a negative trigger is needed to close the right latch.]

Once the TRIAC is conducting, the only way to open it is by low Current dropout.

29
break
② UJT (unijunction transistor):



The UJT has two doped regions with three leads. It has one emitter and two bases. The emitter is heavily doped, having many holes. The n region is lightly doped. For this reason, the resistance between the bases is relatively high, when the emitter is open.

Assume that the emitter supply voltage is turned down to zero. Then the intrinsic standoff voltage reverse-biases the emitter diode. When we increase the emitter supply voltage, V_E increases until it is slightly greater than V_I . This turns on the emitter diode. Since the p region is heavily doped (composed with n region; holes are injected into the lower half of the UJT). These holes create a conducting path between the emitter and lower base.

③ Write down some applications of thyristors

- a) Ans:
- | | |
|------------------------------|---------------------------------|
| ⇒ DIAC triggered SCR | ⇒ OP to couple control |
| ⇒ UJT triggered SCR | ⇒ Automobile ignition |
| ⇒ UJT relaxation oscillation | ⇒ Microprocessor controlled SCR |
| ⇒ Full wave control | |

Q4) Show how to use UJT to produce sawtooth waveform.

Ans: Fig shows a sawtooth generator. The capacitor charges towards the V_{CC} but as soon as its voltage exceed the stand off voltage & the UJT closes. This discharge the capacitor, until low current dropout across. As soon as UJT opens & the next cycle begins. As result we get sawtooth output.

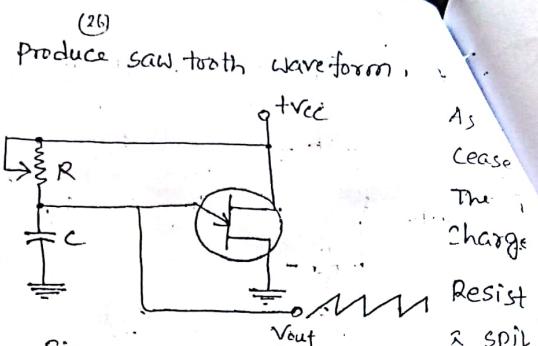


Fig: sawtooth generator

As
cease
the
charge
Resist
& spill
surge
voltage
included
going

Q5) Draw & explain a relaxation oscillator circuit by using UJT.

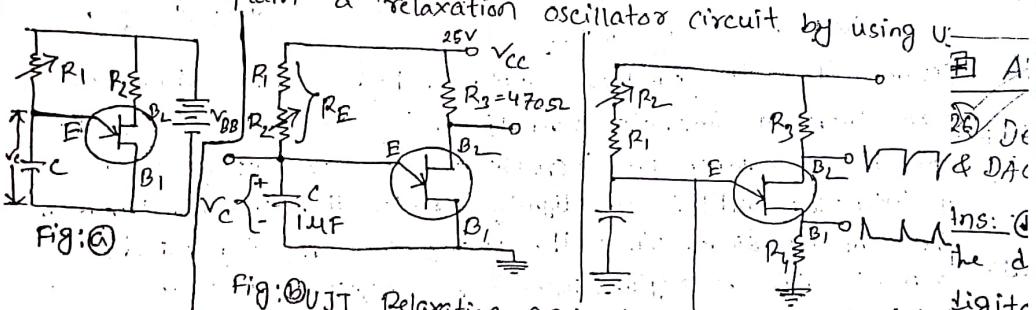


Fig: Q5 UJT Relaxation oscillator

Fig shows UJT relaxation oscillator where the discharging of a capacitor through UJT can develop a saw-tooth output called when battery V_{BB} is turned on, the capacitor C charges increasing through resistor R_1 . During the charging period, the voltage across the capacitor rises in an exponential manner until it reaches the pick-point voltage.

At this instance of time, the UJT switches to its low resistance conducting mode & the capacitor is discharged.

Ans: Q5
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digit

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magn

(27)

ii. between E & B_1 .

As the capacitor voltage fly's back to zero, the emitter ceases (અમાળ) to conduct & UJT is switched off.

The next cycle then begins, allowing the capacitor C to charge again.

iii. Resistor R_3 in the circuit in fig (b) is included to produce a spike wave form output. When the UJT fires, the current surge through terminal B_2 produces the negative-going voltage spike wave form. A resistor can also be included in series with terminal B_1 to produce positive going spike.

ing UJ

ADC & DAC

Q Define: Quantization error, step size, resolution of ADC & DAC, percentage of resolution.

Ans: ① Quantization error: In analog to digital conversion, the difference between the actual analog value and quantized digital value is called quantization error. The error is either due to rounding or truncation. The error signal is sometimes considered as an additional random signal called 'quantization noise'. The error can be reduced by increasing the number of bits in the counter.

② Step size: A D/A converter with n bits, divides a range of analog values into 2^n pieces. The size or magnitude of each pieces is the analog equivalent weight of the least significant bit. This is called step size.

(*) Resolution of ADC & DAC: Resolution of a D/A converter is defined as the smallest change that can occur in analog output as a result of a change of the digital input. The resolution is always equal to the weight of the LSB & is also referred to as the step size.

$$\text{resolution, } k = \frac{A_{fs}}{(2^n - 1)} \quad (\text{full scale output})$$

(*) Percentage Resolution: Although resolution can be expressed as the amount of voltage or current per step of the full-scale output, it is also useful to express it as a percentage.

$$\% \text{ resolution} = \frac{\text{step size}}{\text{full scale(FS)}} \times 100\%$$

(27) A five bit DAC has a current output. For a digital input of 10100, an output current of 10mA is produced. What will I_{out} be for a digital input of 11101?

Ans: The digital input 10100 is equal to decimal 20. Because $I_{out} = 10\text{mA}$ for this case, the proportionality factor must be 0.5mA. Thus, we can find I_{out} for any digital input such as $11101_2 = 29_{10}$ as follows:

$$I_{out} = (0.5\text{mA}) \times 29$$

$$= 14.5\text{mA}$$

* proportionality factor

$$= \frac{I_{out}}{\text{decimal value of input}}$$

(29)

Q. 28) What are the merits & demerits of flash ADC?

Ans: Merits of flash ADC:

i) The flash ADC are high speed and faster converters because the only delays involved are propagation delays. For example: Analog devices 409020 is a 10 bit flash converter with conversion time under 17 ms.

ii) The flash converters uses no clock signal.

iii) The conversion takes place continuously.

iv) When the value of analog input changes, the comparator output will change, thereby causing the encoder outputs to change.

Demerits: ① The flash converter requires much more circuit than other type. For example, a six-bit flash ADC requires 6 digital-analog comparators.

② The large number of comparators has limited the size of flash converters.

Q. 29) What are the advantages of successive Approximation ADC.

Ans: Advantages:

① The successive approximation converters is one of the most widely used type of ADC.

② It takes a much shorter conversion time.

③ Successive approximation converter (SAC) have a fixed value of conversion time that is not dependent on the value of the analog input.

(*) Resolution of ADC & DAC: Resolution is defined as the smallest change in analog output as a result of a change in input. The resolution is always equal to the LSB & is also referred to as resolution, $k = \frac{A_{fs}}{(2^n)^{\text{ADC}}}$

(**) Percentage Resolution: expressed as the ratio of the full scale signal.

(*) A input wires 63
the circuitry

(1) Transducer: Transducer is a device that converts the physical variable to electrical variable. The electrical output of the transducer is an analog current or voltage that is proportional to the physical variable.

(2) ADC: the transducer's electrical analog output serves as the analog input to the ADC. The ADC converts this analog input to a digital output.

merits & demerits of flash ADC?

(*) Analog data

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thus output digits

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(31)

heir. (3) Computer: The digital representation of the process variable are transmitted from the ADC to the digital computer which shows the digital values & process it.

(4) DAC: The digital output of the Computer is connected to DAC which converts it to a proportional analog value.

(5) Actuators: The analog signal from the DAC is often connected to some device or circuit that serves as an actuator to control the physical variable.

Thus ADCs & DACs work as interfaces between a completely digital system such as a Computer & the analog world.

(32)

To Contd. (1) Write down some applications of ADC and DAC / why are ADC & DAC used?

Ans: Application of ADC:

- (1) up/down tracking
- (2) Sigma/delta conversion
- (3) music recording
- (4) Digital signal processing
- (5) Digital voltmeter
- (6) Multiplexing
- (7) Voltage to frequency conversion
- (8) Integrating
- (9) Sample & hold circuit

application of DAC:

- (1) Control
- (2) automatic testing
- (3) Signal reconstruction
- (4) Digital amplitude control
- (5) A/D conversion
- (6) Serial DAC's

- (33) Draw the diagram of the following circuits & explain their working principle: (1) R/2R ladder; (2) Digital ramp ADC; (3) successive approximation ADC; (4) Flash ADC

Ans:

① R/2R ladder: For the case of large difference resistor values, there are some limitations in weight ramp resistor D/A converters. For this reason, it is preferable to have a circuit that uses resistance that are fairly close in value. R/2R ladder network satisfy this requirement, where the resistance values span a range of values only 2 to 1.

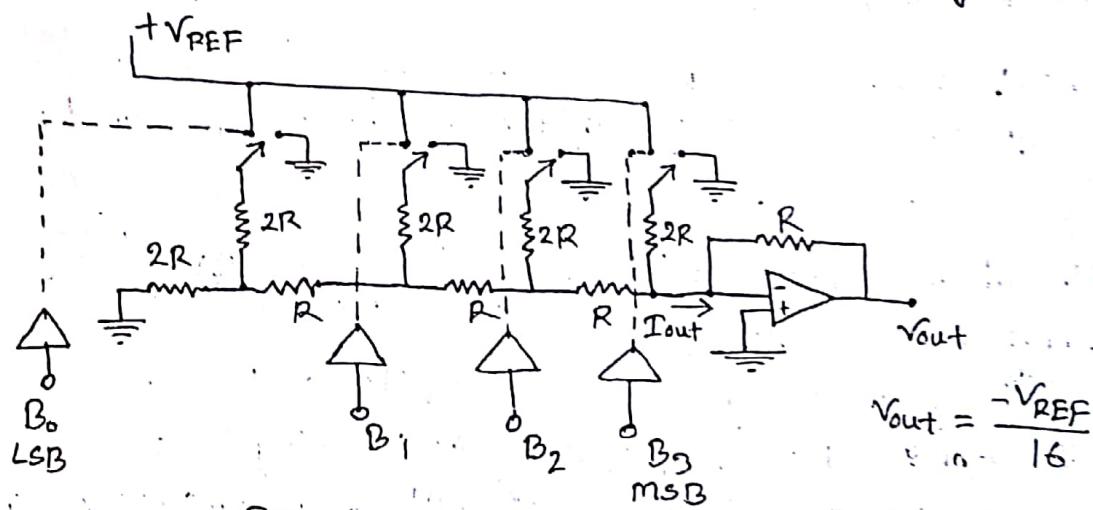


Fig: R/2R ladder

Here only two difference resistor is used, they are R & $2R$. The current I_{out} depends on the position of the 4 switches. The Binary input $B_3 B_2 B_1 B_0$ Controls the state of the switches. The current is allowed to flow through a follower op-amp current to voltage converter to develop V_{out} . V_{out} can be expressed likely, $V_{out} = \frac{-V_{REF}}{16} \times B$, where B is the value of the Binary input which can range from 0000 to 1111.

Fig 6

(2)

Expl@ Digital-Ramp ADC: one of the simplest versions of the ramp ADC general ADC is digital-Ramp ADC which uses a binary count as the register & allows the clock to increment the counter one step at a time until $V_{AX} \geq V_A$. It is called a digital reference ramp ADC because the waveform at V_{AX} is a step by step weight ramp like the fig (2). It is also referred to as a counter-timerable-ADC.

fairly
require
values

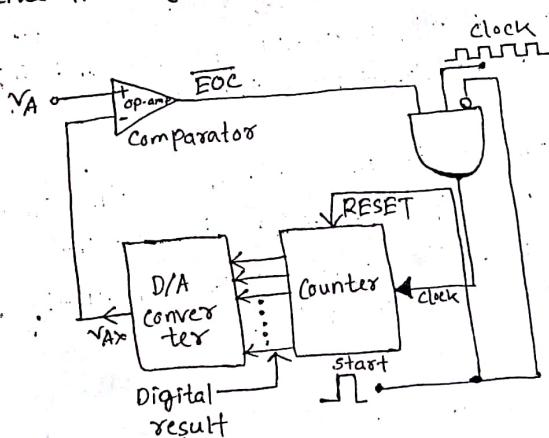


Fig: (1)

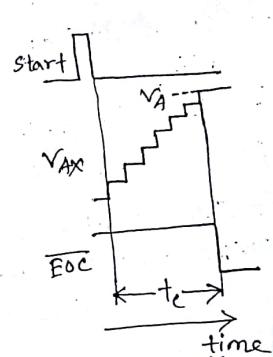


Fig: (2)

Fig (1) shows the diagram for a digital-ramp ADC. It contains a counter, a DAC, an analog comparator & a control AND gate. The comparator output serves as the active-low end of one of the version (EOC) signal. If we assume that V_A (the analog input voltage) to be converted, the operation proceeds as follows:

1. A START pulse is applied to reset the counter to 0. The HIGH at START also inhibits clock pulses from passing through the AND gate into the counter.

- (3) with all 0s at its input, the DAC's output will be $V_{Ax} = 0$
- (4) Because $V_A \geq V_{Ax}$, the comparator output, EOC will be HIGH.
- (5) When start returns LOW, the AND gate is enabled & clock pulses get through the counter.
- (6) As the counter advances, the DAC output V_{Ax} increases one step at a time, shown in fig ②.
- (7) This process continues until V_{Ax} reaches a step that exceeds V_A . At this point, EOC will go low and inhibit flow of pulses into the counter & the counter will stop counting.
- (8) The conversion process is now complete & the contents of the counter are the digital representation of V_A .
- (9) The counter will hold the digital value until the next START pulse initiates a new conversion.

(3) successive approximation ADC: The successive approximation converter is one of the most widely used types of ADC. It has more complex circuitry than the digital ramp ADC but a much shorter conversion time.

The SAC does not use a counter to provide the input to the DAC block but uses a register instead.

The fig shows the block diagram of successive approximation ADC. The control logic modifies the contents of a register bit by bit until the register data are the digital equivalent of the analog input V_A within the resolution range of the converter.

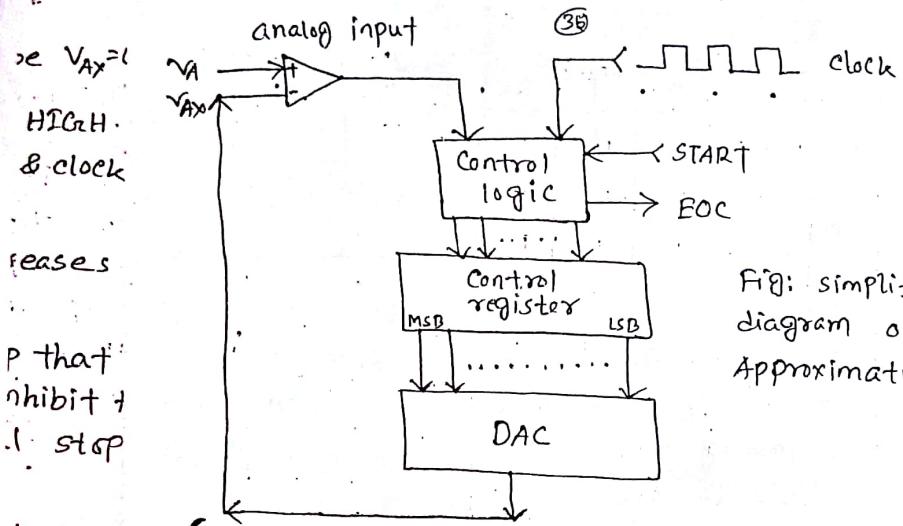


Fig: simplified block diagram of successive Approximation ADC

p that inhibit + stop

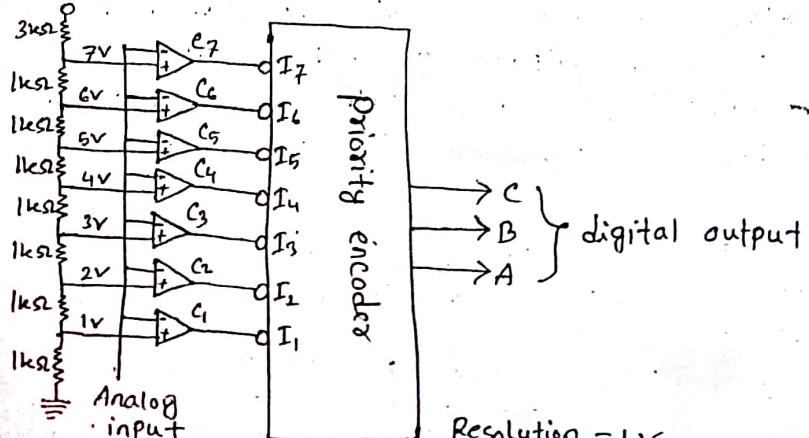
starts o.

④ Flash ADC: The flash converter is the highest-speed ADC. Next but it requires much more circuitry than the other types. For example, a six bit flash ADC requires 63 analog comparators, while an eight bit unit requires 255 comparators. The large number of comparators has limited the size of flash converters.

ADC

input to

proximity
of a
digital
resolution



(36)

V_A	Comparator output							Digital output		
	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C	B	A
0-1 V	1	1	1	1	1	1	1	0	0	0
1-2 V	0	1	1	1	1	1	1	0	0	1
2-3 V	0	0	1	1	1	1	1	0	1	0
3-4 V	0	0	0	1	1	1	1	0	1	1
4-5 V	0	0	0	0	1	1	1	1	0	0
5-6 V	0	0	0	0	0	1	1	1	0	1
6-7 V	0	0	0	0	0	0	1	1	1	0
>7 V	0	0	0	0	0	0	0	1	1	1

Fig shows a Flash ADC which has a three bit resolution & a step size of 1V. The voltage divider sets up comparators so that there are

- ⑤) C
- 4ns:
- are
- D RA
- ine
- D RAN
- uses
- ③) Ra
- ④) Rc
- ⑤) R
- SAC
- depends on

(37)

• 3) Flash ADC require much more circuitry than the SAC ADC

• 4) Compare Digital ramp ADC to SAC ADC.

Ans: The comparisons between digital ramp ADC & SAC ADC are given below:

1) RAMP is a step by step (staircase) ADC where SAC ADC is one of the widely used type ADC.

2) RAMP uses a counter to provide the input where SAC uses a register to provide the input.

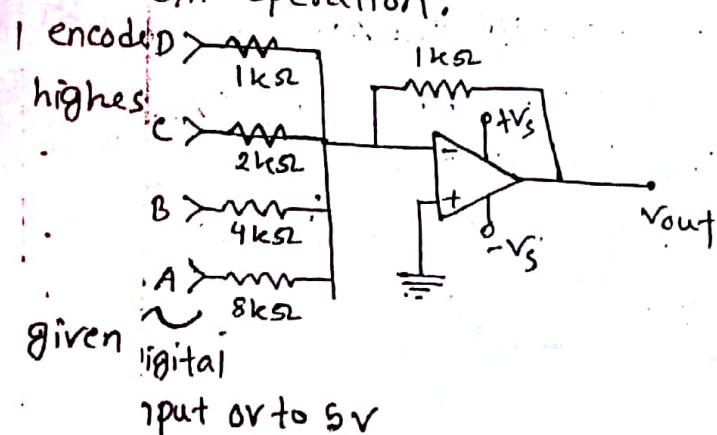
3) Ramp has simple circuitry where SAC has complex.

4) Ramp has the large conversion time than the SAC.

5) Ramp has no fixed value of conversion time where SAC has a fixed value of conversion time that is not dependent on the analog input.

Q, 2V, 336) Draw & explain a DAC using op-amp summing amplifier with weighted resistor.

• with Ans: There are several methods & circuits for producing the low-D/A operation.



or
signals

D	C	B	A	V _{out}
0	0	0	0	0
0	0	0	1	-0.625
0	0	1	0	-1.250
0	1	0	0	-1.875
0	1	0	1	-2.500
0	1	1	0	-3.125
0	1	1	1	-3.750
0	1	1	1	-4.375
1	0	0	0	-5.000
1	0	0	1	-5.625
1	0	1	0	-6.250
1	0	1	1	-6.875
1	1	0	0	-7.500
1	1	0	1	-8.125
1	1	1	0	-8.750
1	1	1	1	-9.375

(38)

Fig shows the basic circuit for four bit DAC. The input A, B, C, D are binary inputs that assumed to have values of 0V or 5V. The op-amp is employed as a summing amplifier which produces the weighted sum of the input voltage. Recall that the summing amplifier multiplies each input voltage by the ratio of the feedback, R_f to the corresponding resistor, R_N . In this circuit $R_f = 1k\Omega$ & input resistors range from 1 to $8k\Omega$.

The D input has $R_N = 1k\Omega$ so the summing amplifier passes the voltage D with no attenuation. The input C has $R_N = 2k\Omega$ so it will be attenuated with $\frac{1}{2}$. Similarly the B input will be attenuated by $\frac{1}{4}$ & A input will be by $\frac{1}{8}$. The amplifier output can be thus expressed as $V_{out} = V_D + \frac{1}{2}V_C + \frac{1}{4}V_B + \frac{1}{8}V_A$

Draw & explain
 Q7. Voltage to frequency conversion ADC.

Ans. It is a device by which we can have output frequency by giving input voltage. Generally the ADC consists with a DAC but voltage controlled ADC does not need any DAC. In lieu of that a VCO (voltage controlled oscillator) is used. The structure of voltage controlled ADC contains two parts:

- ① Parts of General ADC
- ② VCO

sequencing is ...

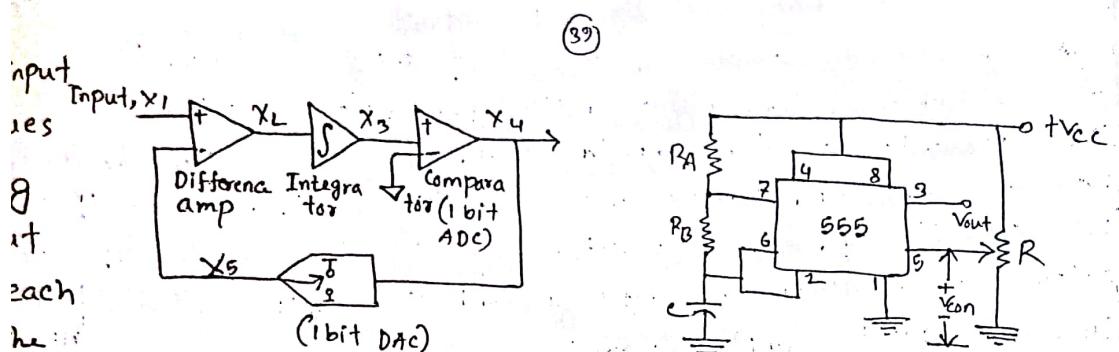


Fig: (a) structure of general adc Fig (b) structure of vco

The voltage which is to be converted is applied to VCO to generate an output frequency. This counter output frequency is sent to a counter to be counted for a fixed time interval. The final output frequency is proportional to the value of analog input voltage.

Ans: Draw & explain a sample & hold circuit.

Ans: when an analog voltage is connected directly to the input of an ADC, the conversion process can be adversely affected if the analog voltage is changing during the conversion time. The stability of the conversion process can be improved by using a sample & hold circuit to hold the analog voltage constant while the A/D conversion is taking place.

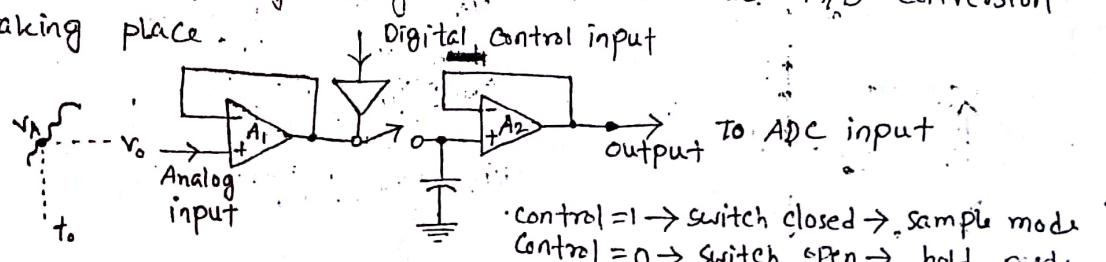


Fig: simplified diagram of a sample & hold

this case, the

(b) output voltage
in the position
open &

Fig shows a simple diagram of sample & hold circuit. The S/H circuit contains a unity gain buffer amplifier A_1 resp. that presents a high impedance to the analog signal & so it has a low output impedance that can rapidly charge the hold capacitor, C_h . The capacitor will be connected to the output of A_1 when the digitally controlled switch is closed. This is called sample operation.

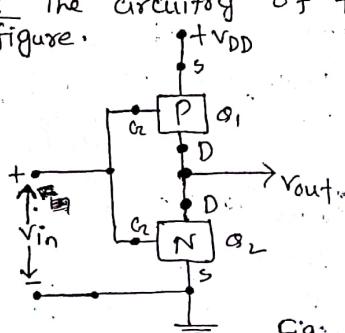
The switch will be closed long enough for C_h charge to the present value of the analog input. For example, if the switch is closed at time t_0 , the A_1 output will quickly charge C_h up to a voltage V_0 . When the switch open, A_1

C_h will hold this voltage so that the output of A_2 will apply this voltage to ADC. The unity gain buffer amplifier A_2 presents a high input impedance that will not discharge the capacitor voltage appreciably during the conversion time of the ADC, & so the ADC will essentially receive a dc input voltage V_0 .

Q1 Logic Families

Q1 Explain the operation of a CMOS inverter.

Ans: The circuitry of the basic CMOS inverter is shown in figure.



V_{in}	Q_1	Q_L	V_{out}
$+V_{DD}$ (logic 1)	OFF $R_{OFF} = 10^{10} \Omega$	ON $R_{ON} = 1 \Omega$	$= 0V$
$0V$ (logic 0)	ON $R_{ON} = 1 \Omega$	OFF $R_{OFF} = 10^{10} \Omega$	$= +V_{DD}$

Fig: Basic CMOS inverter

(4)

t. In figure, Block labeled P & N denote a p-MOS and a n-MOS respectively. The CMOS INVERTER has two MOSFETs in series & so that the p-channel device has its source connected to $+V_{DD}$ & the n-channel device has its source connected to ground. The gates of the two devices are connected together as a common input. The drains of the two devices are connected together as the common output.

The logic levels for CMOS are essentially $+V_{DD}$ for logical 1 & 0V for logical 0. Consider, first, the case where $V_{IN} = +V_{DD}$. In this situation, the gate of Q_1 (p-channel) is at 0V relative to the source of Q_1 . The Q_1 will be in the OFF state with $R_{OFF} \approx 10^{10} \Omega$. The gate of Q_2 (n-channel) will be at $+V_{DD}$ relative to its source. Thus Q_2 will be on with typically $R_{ON} = 1k\Omega$. The voltage divider between Q_1 's R_{OFF} & Q_2 's R_{ON} will produce $V_{out} \approx 0V$.

Next, consider the case where $V_{IN} = 0V$. Q_1 now has its gate at a negative potential relative to its source, while Q_2 has $V_{G2S} = 0V$. Thus, Q_1 will be on with $R_{ON} = 1k\Omega$ & Q_2 will be OFF with $R_{OFF} = 10^{10} \Omega$, producing a V_{out} of approximately $+V_{DD}$. These two operating states are summarized in the table in figure, showing that the circuit does act as a logic Inverter.

~~Explain the internal diagram of TTL NAND gate.~~

Ans: The basic TTL logic circuit is the NAND gate, shown in figure.

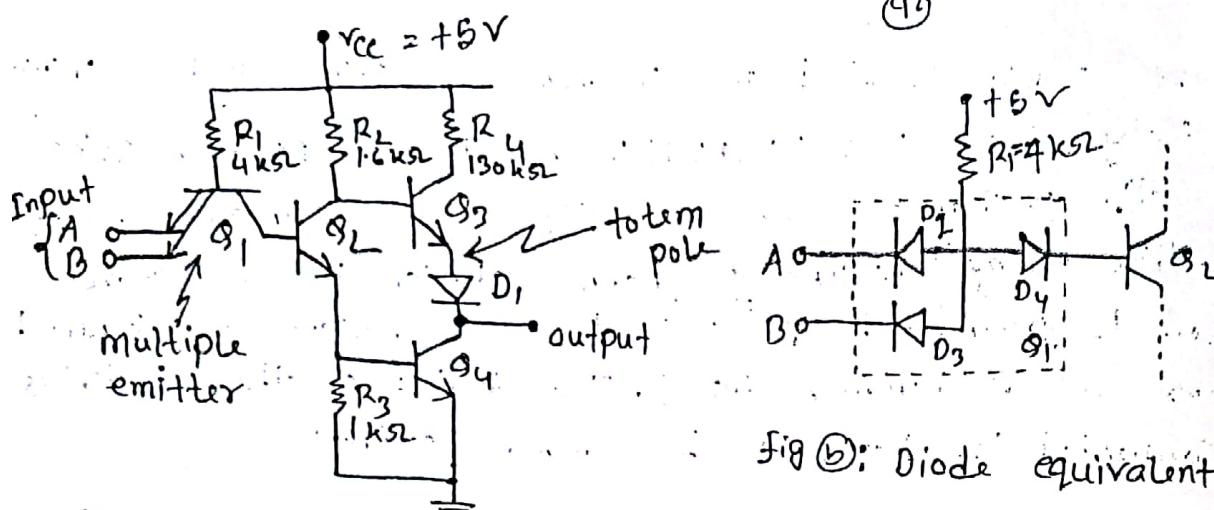


Fig @: Basic TTL NAND Gate

In TTL, the transistor \varnothing_1 has a multiple emitter (diode). ✓
configuration. Forward biasing either of these diode junctions of a
will turn on \varnothing_1 . Only when all junctions are reverse biased,
the transistor will be off. The multiple emitter input
NAND gate.

On the output side of the circuit, transistors \varnothing_3 & \varnothing_4
are in a totem pole arrangement. The totem pole is made
of two transistor switches, \varnothing_3 & \varnothing_4 . The job of \varnothing_3 is to
connect Vcc to the output, making a logic HIGH. The
job of \varnothing_4 is to connect the output to the ground, making a
logic low.

In fig (b), Diodes D_2 & D_3 represent the two E-B junctions of \varnothing_1 , & D_4 is the C-B junction of \varnothing_1 .

~~(4)~~ What is meant by 'Fan out' of TTL device?
Ans: 'FAN-out' is a term that defines the maximum load
number of digital inputs that the output of a single part
can feed

Fig (b): Diode equivalent for I

(43)

"FAN-OUT" of TTL device means that TTL output has a limit, $I_{OL}(\text{max})$ on how much current it can sink in the low state. It also has a limit, $I_{OH}(\text{max})$ on how much current it can source in the high state. These output current limits must not be exceeded if the output voltage level are to be maintained within their specified ranges.

In low state, fanout (low) = $\frac{I_{OL}(\text{Max})}{I_{IL}(\text{Max})}$

In high state, fanout (HIGH) = $\frac{I_{OH}(\text{max})}{I_{IH}(\text{max})}$

(42) Explain, with necessary diagram, the principle of operation of an N-Mos inverter & N-Mos NOR gate.

Ans: N-MOS inverter: Figure shows the N-Mos inverter circuit.

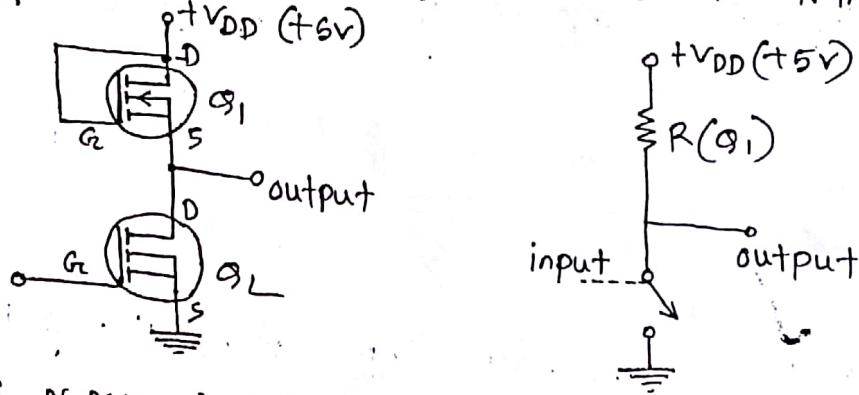


Fig: N-Mos inverter circuit & its equivalent circuit

It contains two N-channel MOSFETs. Q_2 is a switch, Q_1 is a load MOSFET. Q_1 acts as a load resistance (R_d) for Q_2 . As a gate of Q_1 is permanently connected to the V_{DD} , it is always ON & hence minimum load resistance is equal to the R_{ON} of the single. Particularly, Q_1 is designed to have R_{ON} approx

(14)

the R_{ON} of Q_L . To achieve this, channel of Q_1 is made much narrower than channel of Q_L . Typically R_{ON} of Q_1 is $10\text{k}\Omega$, whereas R_{ON} of Q_L is $1\text{k}\Omega$. We know that MOS devices are voltage controlled devices. When positive voltage (High V_{IN}) is applied between gate and source, Q_L is switched ON & it makes the output low. On the other hand, when input is low, Q_L is switched OFF & therefore output is high.

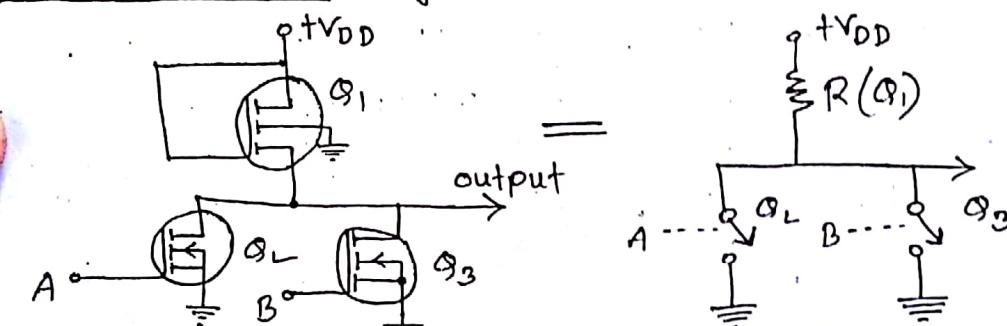
Table summarizes the operation of NMOS Inverter.

V_{IN}	Q_L	$V_o = \overline{V_{IN}}$
0V (logic 0)	OFF	+5V (logic 1)
+5V (logic 1)	ON	0V (logic 0)

1
0
1
1
1

~~Ex:~~
Ans:

N-MOS NOR Gate: Fig shows two input N-MOS NOR gate



number. (a) logic can Fig: 2 input N-MOS NOR gate (b)

$+V_{DD}$
 $-V_{SS}$

Fig:

de
MOSFET
equival
tche

(45)

Q_1 acts as a load register and Q_2 & Q_3 are the switch made MOSFETs controlled by the input A & B. Fig (b) shows the of equivalent switching circuit, consisting of a resistor and two switches connected in parallel. When either or both input are high, the corresponding MOSFETs are ON i.e. Corresponding switches are closed making the output low. If both inputs are low, both MOSFETs are OFF i.e. both switches are open & the output is high.

Q_2

Table summarize the operation of N-MOS NOR Gate:

A	B	Q_2	Q_3	$V_o = \bar{A} + \bar{B}$
0	0	OFF	OFF	1
0	1	OFF	ON	0
1	0	ON	OFF	0
1	1	ON	ON	0

(13) Explain a MOSFET switch.

Ans:

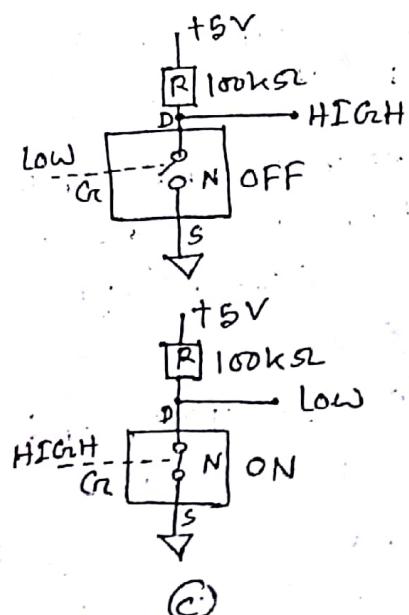
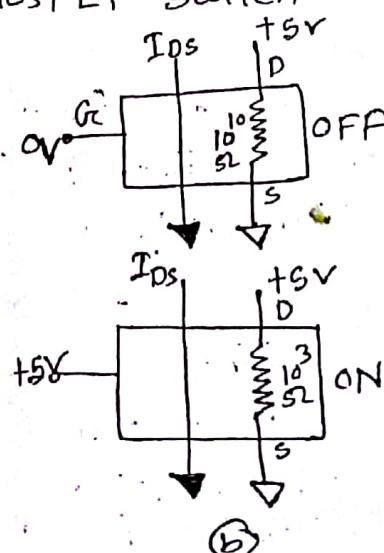
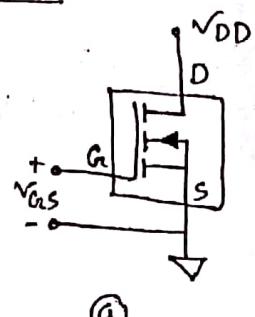


Fig: N Channel MOSFET used as a switch

(a) Symbol; (b) circuit model; (c) N-MOS inverter operation

figure shows the switching operation of an N-channel MOSFET. (44)
the basic for the N-channel device, the drain is always biased positive relative to the source. [The gate to drain voltage V_{GS}] is the input voltage, which is used to control the resistance between drain and source and thereby therefore determines whether the device is on or off.

[When $V_{GS} = 0V$, there is no conductive channel between source & drain, & the device is OFF, as shown in fig ⑥. Typically the resistance of the channel in this OFF state is $10^9 \Omega$ which for most purposes is an open circuit. The MOSFET will remain OFF as long as V_{GS} is zero or negative.] (45)

when V_{GS} is positive (gate positive relative to source), a threshold voltage (V_T) is reached at which point a conductive channel begins to form between drain and source. It makes the device ON. Typically the resistance of the channel in this ON state is 1000Ω which for most purposes is a closed circuit.

In essence, the N-Mos will switch from a very high resistance to a low resistance as the gate voltage switch from a low voltage to a high voltage.

(46) ✓ Compare TTL and MOS devices.

Ans: The comparison between TTL and MOS is given below

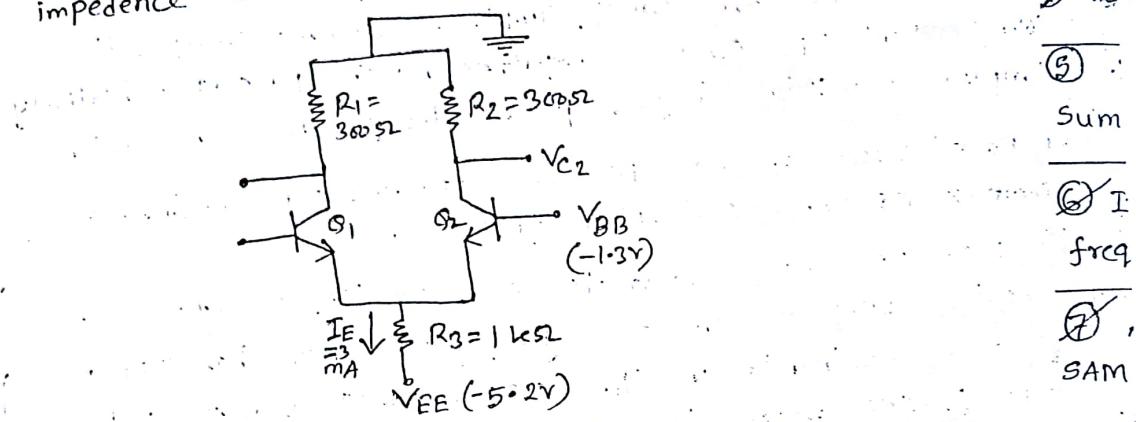
① MOS is a structure of a metal electrode over an oxide insulator over a semiconductor substance.

while, TTL is a name for type of logic circuits which are constructed using the bipolar transistor.

- ② Mos devices are current operated device while TTL are voltage operated device. 49
- ③ Mos devices are small, simple & consume very little power. But TTL circuits requires much space. Its relatively complex & require higher power though they are fast.
- ④ Fabrication of Mos ICs is approximately one-third as complex as the fabrication of TTL.
- ⑤ Mos ICs can accomodate a much larger number of circuits elements on a single chip rather than TTL.
- ⑥ Mos dominants in the SSI and MSI markets. But TTL is still more durable in the lab experiment.
- ⑦ ~~Ans~~ Write down some ECL characteristics.

- Ans: Some ECL characteristics are given below:
- ① The transistors never saturate and so switching speed is very high. Typically, propagation delay time is 360 ps (per second), which makes ECL faster than any TTL or CMOS family members.
- ② The logic levels are nominally -0.8V and -1.7V for the logical 1 and 0 respectively.
- ③ Worst-case ECL noise margins are approximately 150 mV. These low noise margins make ECL somewhat unreliable for use in heavy industrial environments.
- ④ An ECL logic block usually produces an output & its complement. These eliminates the need for inverters.

- (5) Fan-out is typically around 25, owing to the low-
impedance emitter follower outputs.



- (6) Typical power dissipation is 25 mW.
 (7) The total current flow in an ECL circuit remains relatively constant, regardless of its logic state. This helps to maintain unvarying current drain on the power supply and no noise spike will be generated internally.

Q5 Memory System

- (47) What are the differences between the following terms:
 ① RAM and SAM; ② DRAM and SRAM, ③ ROM and RAM,
 ④ EPROM and EEPROM

Ans: ① RAM and SAM:

RAM	SAM
① Random Access Memory ② The actual physical location of a memory has no effect on how long it takes to read from or write into that location.	① Sequential Access memory ② It varies depending on the address location

RAM	SAM
③ It works rapidly.	③ It works slowly.
④ The access time is constant.	④ The access time is not constant.
⑤ It is not time consuming.	⑤ It is time consuming.
⑥ Its working process is more frequent.	⑥ Its working process is slow.
⑦ Access time is smaller than SAM.	⑦ Access time is longer than RAM.

helps ② DRAM and SRAM:

SRAM	DRAM
① static random access memory.	① Dynamic random access memory.
② stores data in FF.	② stores data in small mos capacit
③ It is used as a cache memory.	③ It is used as main memory.
④ No need to writing data periodically.	④ Need to write data periodically.
⑤ No need to refresh cycle.	⑤ Need to refresh cycle.
⑥ It has low capacity.	⑥ It has high capacity.
⑦ It has high power requirement.	⑦ It has low power requirement.
⑧ High speed memory.	⑧ moderate speed memory.
⑨ The design is very simple.	⑨ The design is very complex.
⑩ Density of cell is lower than DRAM.	⑩ Density of cell is higher than SRAM.
⑪ The cost per bit is higher than DRAM.	⑪ The cost per bit is lower.

③ Rom and RAM:

RAM	ROM
① Random Access memory	① Read only memory.
② It stores data temporarily & can be changeable.	② It stores data frequently & can not change frequently
③ It is volatile & will loss all stored data when electrical power is removed.	③ It is non volatile & will restore the data when electrical power is removed.
④ Any memory address location is easily accessible.	④ It is not easily accessible.
⑤ Data can be read & written into RAM.	⑤ Data can be read from a cache.
⑥ It requires fast read & write cycle time	⑥ write operation is more complicated than read operation
⑦ It will not slow down the computer operation	⑦ It will slow down the computer operation.

④ EPROM and EEPROM:

EPROM	EEPROM
① Erasable programmable ROM	① Electrically erasable programmable
② Erasing & Programming of it can be done outside of the circuit.	② Erasing and Programming of it can be done inside the circuit.
③ For erasing, it needs uv lightsource.	③ For uv erasing, it doesn't need <u>any</u> lightsource.
④ For programming it needs a special PROM programmable unit	④ For programming it doesn't need any programming unit.
⑤ It has no memory cell complexity and on-chip support circuitry.	⑤ It has memory cell complexity and on-chip support circuitry.

51

Q8 What is the major drawback of MROM, PROM and EPROM
How is an EPROM erased?

Ans: Drawback of MROM, PROM and EPROM:

mask-programmed Rom (MROM): MROM is very expensive and would not be used except in high volume applications. This ROM cannot be reprogrammed in the event of design change requiring a modification of stored data.

programmable Rom (PROM): Once programmed; however, a PROM is like an MROM because it cannot be changed or reprogrammed. Thus if the program in the PROM is faulty or must be changed, the PROM must be thrown away. For this reason, this device is often called "one time programmable ROMs". These are also expensive.

Erasable PROM (EPROM): (i) They must be removed from the circuitry to erase & reprogrammed. (ii) The erase operation erases the entire chip. There is no way to select only certain address to be erased.

(iii) The erase & reprogramming process typically takes 20 minutes or more.

How is an EPROM erased? Once an EPROM cell has been programmed, it can be erased by exposing ultra-violet (UV) light applied through a window on the chip-package. The UV light produces a photo current from the floating gate back to the silicon substrate, therefore removing the stored charges. It turned the transistor OFF and restoring all cells to logic 1 state. This erasing process typically requires 15 to 20 minutes of exposure to UV rays.

There is no way to erase only selected cells. The UV light erases all cells at the same time. The EPROM can be reprogrammed.

(49) What is the function of memory enable input?

Ans: Many memory system have some means for completely disabling all part of the memory so that it will not respond to other inputs. This is done by memory enable input (ME). It is also called chip enable (CE) or chip select (CS).

When memory enable acts active-high input, it enables the memory to operate normally. A low on this input disables the memory so that it will not respond to the address & R/W inputs.

This type of input is useful when several memory modules are combined to form a large memory.

(50) What is the drawback of DRAM & SRAM?

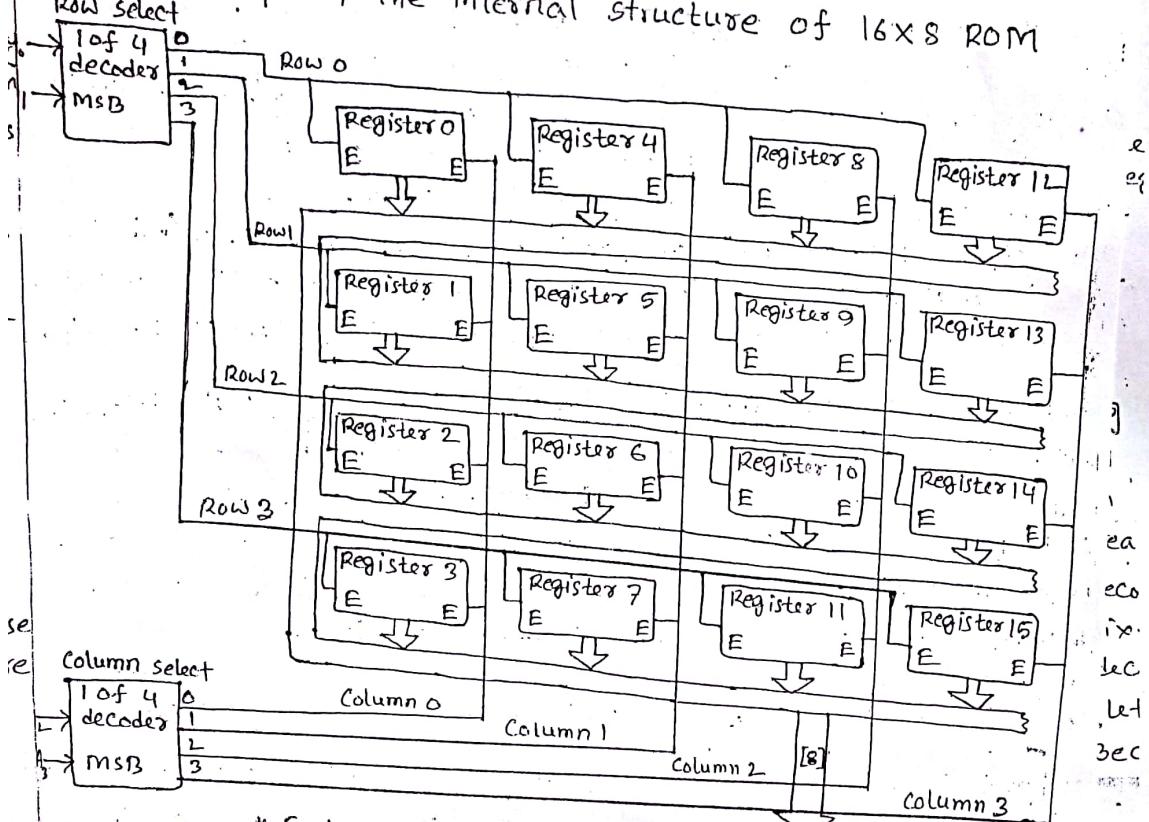
Ans: Drawback of DRAM: DRAM store 1's & 0's as charges on a small MOS capacitor. Because of the tendency for these charges to leak off after a period of time, DRAMs require periodic recharging of the memory cells. This is called refreshing. Each memory cell must be refreshed typically every 2, 4 or 8 ms or its data will be lost. It may require external support circuitry. Some DRAM chips have built-in refresh control circuitry that does not require extra external hardware but does require special timing of the chips input control signals. So designing and using DRAM is more complex system.

(53)

Drawback of SRAM: It has lower capacity than the DRAM.

Its density is lower than the DRAM. Its power requirement is higher & cost per bit also higher than DRAM..

- (51) Draw & Explain the internal structure of 16x8 ROM



* Each register stores one 8-bit word

Fig: Architecture of 16x8 ROM

Ans. A simplified diagram of the internal structure of a 16×8 ROM. There are four basic parts: ① register array, ② row decoder, ③ column decoder, ④ output buffers.

Register Array: The register array stores the data that have been programmed into the ROM. Each register stores an 8-bit word. The registers are arranged in a square matrix array. We can specify the position of each register as being in a specific row & a specific column. For example: register 0 is in row 0, column 0 & register 9 is in row 1, column 2.

The eight data outputs of each register are connected to an internal data bus that runs through the entire circuit. Each register has two enable inputs (E), both must be high.

Address Decoder: The applied address code $A_3A_2A_1A_0$ determines which register in the array will be enabled to place its eight bit data word onto the bus. Address bits A_1A_0 are fed to a 1 of 4 decoder that activates one row-select line & address bit A_3A_2 are fed to a second 1 of 4 decoder that activates one column-select line. Only one register will be in both the row & the column selected by the address input & this will be enabled.

Output Buffer: The register that is enabled by the address input will place its 8-bit data word onto the data bus. These data feed into the output buffers & provided if CS is low. If CS is high the output buffer are in the Hi-Z state & D_7 through D_0 will be floating.

(52) Draw & explain the internal structure of 64×4 RAM

Ans:

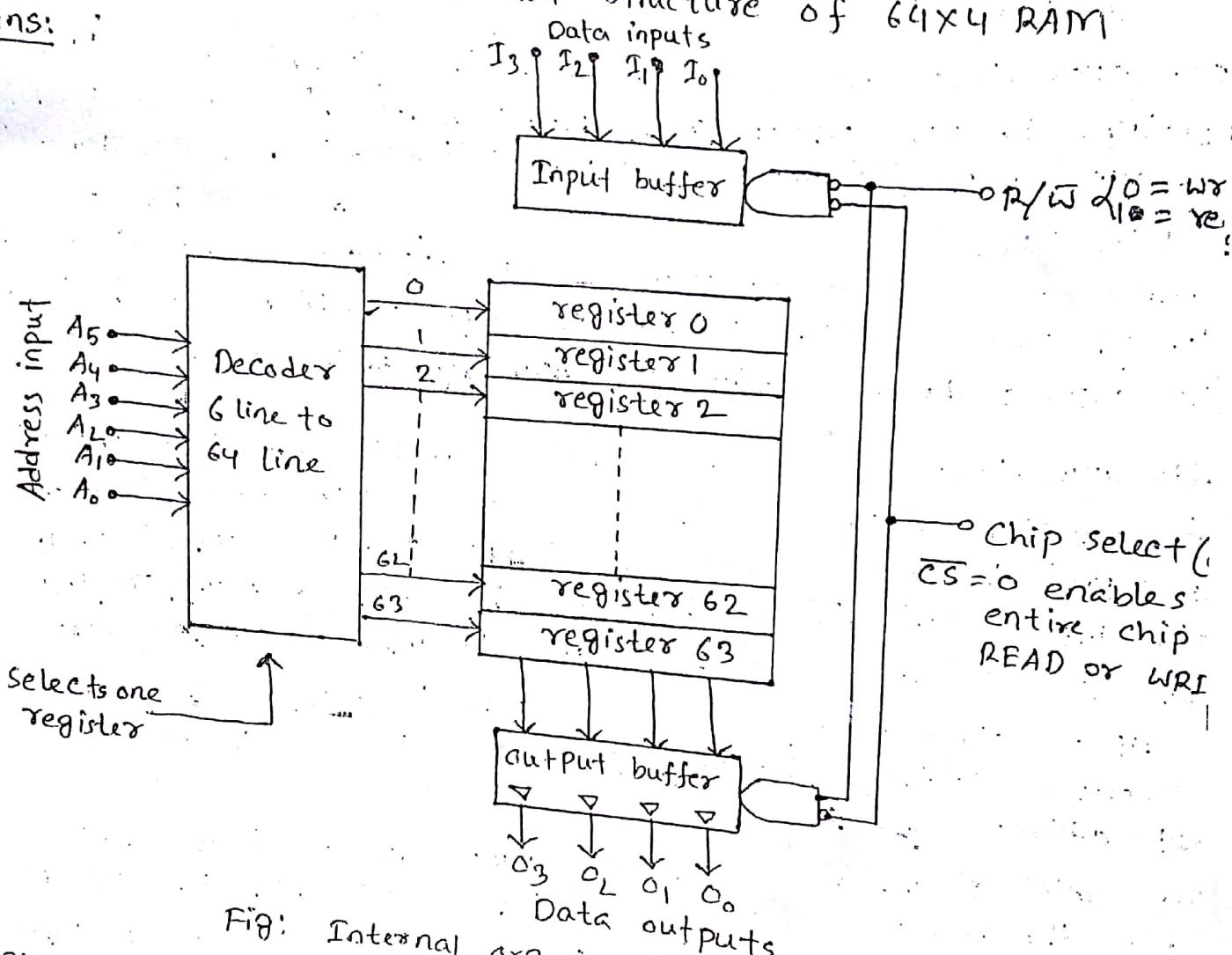


Fig: Internal organization

Fig shows the internal structure of a 64×4 RAM. It stores 64 words of four bits each. Addresses range from 0 to 63. In order to select one of the 64 addresses, a binary address code is applied to a six-bit input code. Because $64 = 2^6$, the decoder requires a six-bit input code. Each address code activates a particular decoder output, which enables its corresponding register. Let, an applied address code is $A_5 A_4 A_3 A_2 A_1 A_0 = 011010$. Because $(11010)_2 = (26)_{10}$, decoder output $26 = 011010$.

Show a Sir 6 for either a read or a write operation.
f 16x8 Row row der. W/R

In order to read the content of the selected for AD/ WRITE (R/W) input must be 1. In addition, Address (ES) input must be activated (0). The combination $\overline{CS} = 0$ enables the output buffer so that the Ac the selected register will appear at the four data wo: outputs. $R/W = 1$ also disables the input buffers so that the IG: data inputs do not affect the memory during a read operation.

Write operations To write a new four bit word into the selected register requires $R/W = 0$ & $\overline{CS} = 0$. This combination enables: the input buffers so that the four bit word applied to the data inputs will be loaded into the selected register. The $R/W = 0$ also disables the output buffers. & output are in Hi-3 state during a write operation. The write operation high of course destroys the word that was previously stored at mar that address.

Chip select: When CS or CE inputs are in their active state, the memory chip is said to be selected. otherwise, it is said to be deselected. $\overline{CS} = 0$ enables entire chip for READ OR WRITE.

Common Input/output Pins: The R/W input controls the function of these I/O pins. During read operation I/O acts as data usi outputs that reproduce selected address location. During write Ans operation, I/O acts as data inputs to which data to be mod written are applied.

(57)

Q. (53) ✓ How many address input, data input and output are required for $16k \times 8$ memory?

Ans: Data input & data output: Eight of each because the word sizes is eight.

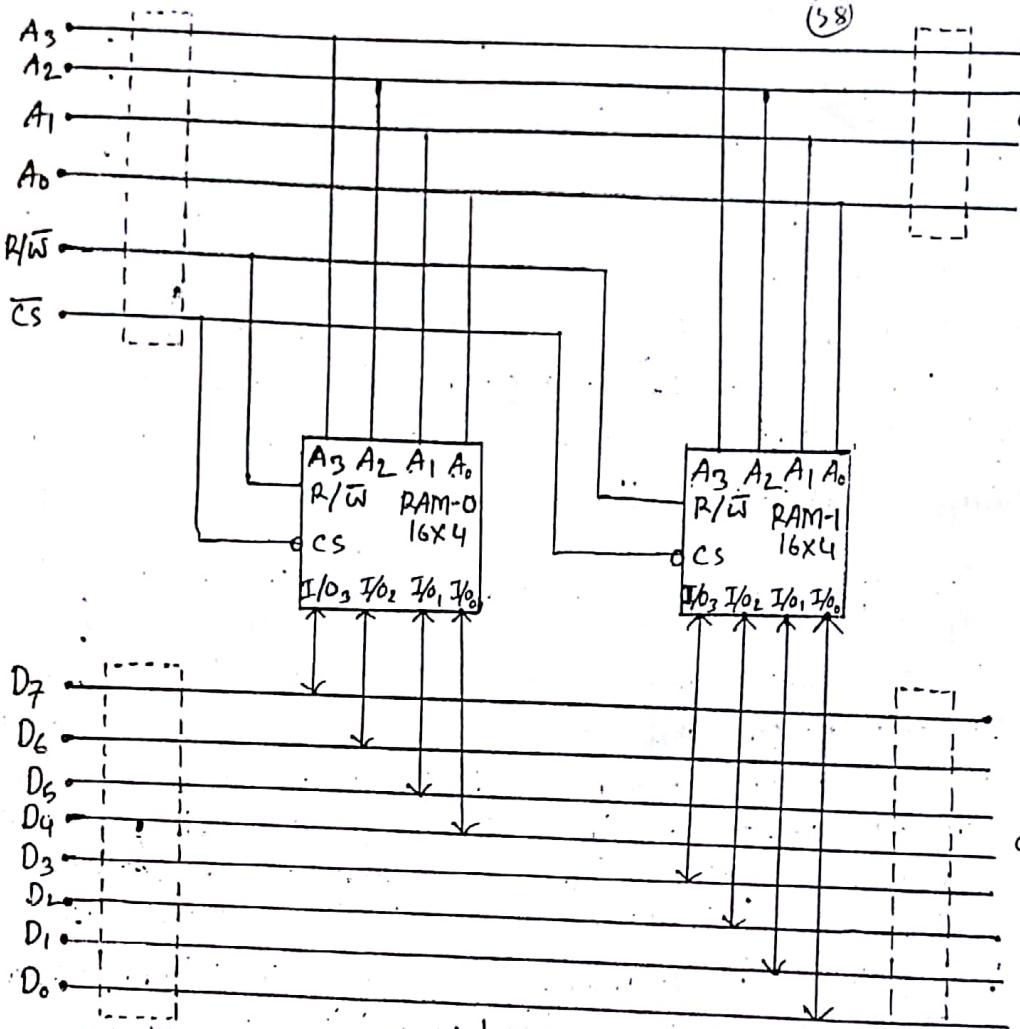
Address input: The memory stores $16k = 16 \times 1024 = 16384$ words. Thus there are 16384 memory address. Because $16384 = 2^{14}$, it requires a 14 bit address code to specify one of 16384 address.

Q. (54) ✓ What is the benefit of address multiplexing? ✓

Ans: The $16k \times 1$ DRAM array would have 14 address input. The $64k \times 1$ DRAM array would have 16 address input. The $1M \times 4$ DRAM array would have 20 address input. The $4M \times 1$ DRAM array would have 22 address input. In high capacity memory chips such as these would require many pins, if each address input required a separate pin. In order to reduce the number of pins on their DRAM chips, manufacturers utilize address multiplexing whereby each address input pin can accommodate two different address bits. The saving in pin count translates to a significant decrease in the IC size.

Q. (55) ✓ Describe the way of realizing 16×8 RAM module by using two 16×4 RAM modules.

Ans: Fig shows 16×8 RAM module by using two 16×4 RAM modules. Each chip has 16 ~~for~~ four bit words and it makes 16 eight bit words. RAM-0 stores the four higher order bits of each of 16 words & RAM-1 stores four lower order bits of each of 16 words. A full eight bit words is available at the RAM output connected to the data bus.



Address range 0000 to 1111 (16 words)
Word size 8 bits

The 4 bit higher order
bit of each word stored
in RAM-0

The 4 lower order bit of it
each word are stored
in RAM-1

Fig: Combining of 16×4 RAMs for a 16×8 module.

any one of the 16 words is selected by address code (A_3, A_2, A_1, A_0) & can read or write at this address under control of Common R/W and CS line.

(58)

address bus^{RC}
on to
selects
The
bit
device
To
as i
data
location

In
a SIR
modul
data bus
(6) Rec
tns:
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four l
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The : 1
ne - F
hi - Q
ne -

To read, $R/W = 1$ & $\overline{CS} = 0$. This causes the RAM I/O lines to act as outputs. RAM-0 places its selected four bit word in the upper four data bus lines, & RAM-1 places its selected four bit word on the lower four data bus lines. The data bus line then contains the full selected eight bit word, which can now be transmitted to some other device.

To write, $R/W = 0$ & $\overline{CS} = 0$, causes the RAM I/O lines to act as inputs. The eight bit word to be written is placed on the data bus. The higher four bits will be written into the select location of RAM-0 & the lower four bit will be written into RAM-1.

In essence, the combination of the two RAM chips acts like a single 16×8 memory chip. We refer to this as a 16×8 memory module.

(b) Realize a 32×4 RAM module by using two 16×4 RAM modules: By combining two 16×4 chips as shown in fig, we can produce the desired memory.

Each RAM is used to store 16 four-bit words. The four I/O pins of each RAM are connected to a common four line data bus. Only one of RAM chips can be selected at one time so that there will be no bus connection problem. This is ensured by driving the respective \overline{CS} input from different logic signals.

The total capacity of this memory module is 32×4 . So there must be 32 different addresses. This requires five address control bus lines. The upper address line A_4 is used to select one RAM & the other that will be read from or written into. The other four address lines A_0 to A_3 are used to select the one memory location out of 16 from the selected RAM.