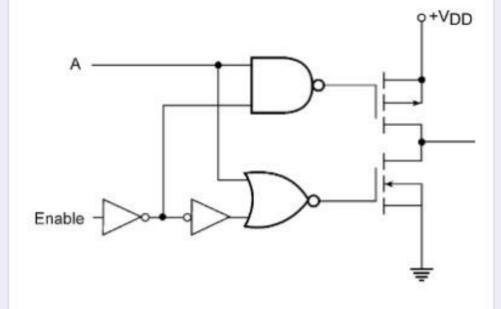


- Integration
- Summation
- Differentiation
- Division

Differentiation

The following circuit is a (an) ------

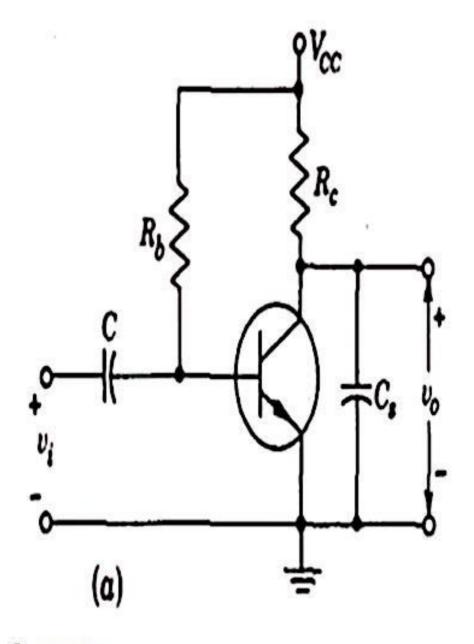
3/3



- Inverter in CMOS
- AND gate in CMOS
- NOR gate in CMOS
- Tristate buffer in CMOS

Tristate buffer in CMOS

If the input is a digital pulse train, Capacitor is 1000 microFarad, Collector load 0/1 is 1 K Ohm, the output of the following circuit is ——



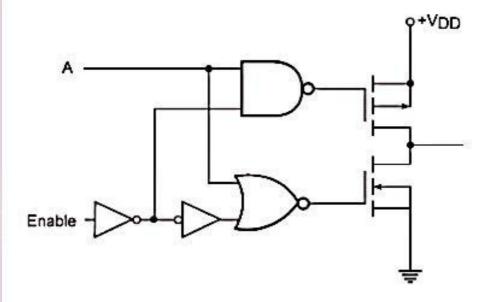
- O Saw tooth wave
- Rectangular wave
- Sinusoidal wave
- exponential wave

Correct answer

Saw tooth wave

With Enable input=1, the output of the circuit is ---

2/2



- Inverted
- O Same as input
- Hi-Z (high impedance)

#### Feedback

Hi-Z (high impedance)

Which among the bipolar logic families is specifically adopted for high speed 1/1 applications?

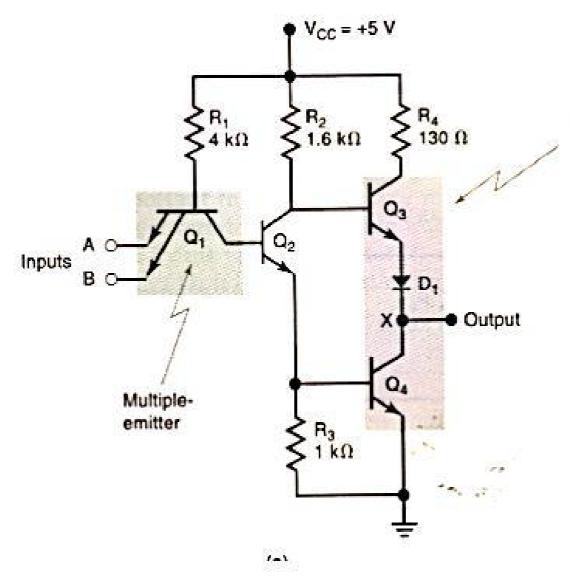
- a. Diode Transistor Logic (DTL)
- b. Transistor Transistor Logic (TTL)
- c. Emitter Coupled Logic (ECL)
- d. Integrated Injection Logic (I\*2L)

#### Feedback

c. Emitter Coupled Logic (ECL)

In the following TTL circuit, which conditions are true for the transistors Q2, Q3 3/3 and Q4 if both of the inputs A and B are set to logic zero or (A=1, B=0) or (A=0, B=1)

In the following TTL circuit, which conditions are true for the transistors Q2, Q3 3/3 and Q4 if both of the inputs A and B are set to logic zero or (A=1, B=0) or (A=0, B=1)



- Q2 ON, Q3 OFF, Q4 OFF
- ( ) Q2 OFF, Q3 OFF, Q4 ON
- Q2 OFF, Q3 ON, Q4 OFF
- Q2 ON, Q3 OFF, Q4 ON

# Feedback

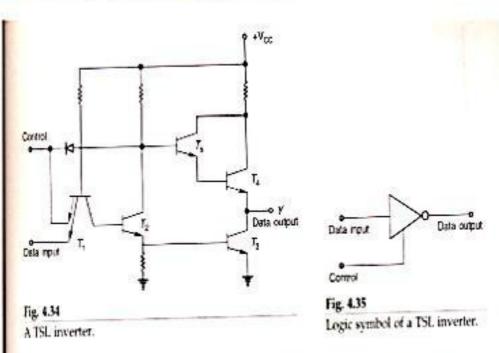
Q2 OFF, Q3 ON, Q4 OFF

In the following TTL circuit, which conditions are true for the transistors Q2, Q3 2/2 and Q4 if both of the inputs A and B set to logic one.

Which type of unipolar logic family exhibits its usability for the applications requiring low power consumption?	1/1
PMOS	
O NMOS	
● cmos	
All of the above	
Feedback	
CMOS	

In the following Tri-state ligic circuit, which conditions are true for the transistors T3, T4, T5 if the control input is zero.

3/3

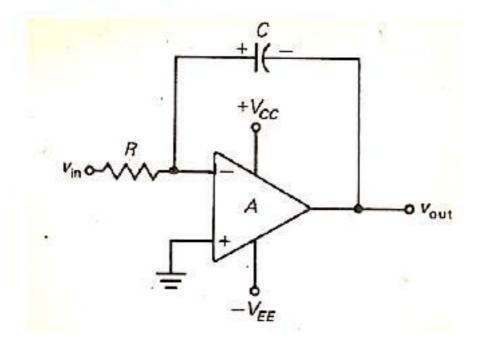


The output and input current specifications of TSL family are given in Table 4.11.

- T3 and T4 are ON but T5 is OFF
- T3, T4, T5 are OFF
- T3 is ON but T4, T5 are OFF
- T3 is OFF but T4, T5 are ON

Feedback

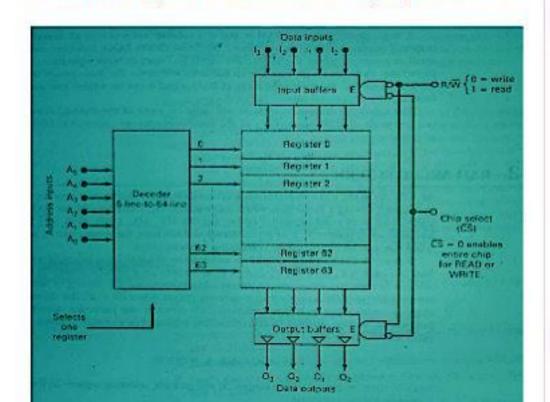
T3, T4, T5 are OFF



- O Comparator
- Integrator
- Differentiator
- O Summing Amplifier

Integrator

Which of the following information is true for the RAM diagram given below? 2/2

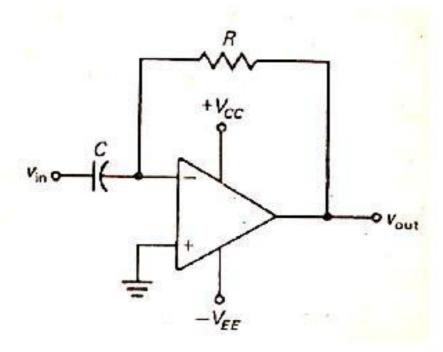


- () Its capacity is 5\*64\*4 bits
- () Its capacity is 6\*64\*4 bits
- Its capacity is 64\*4 bits
- ( ) Its capacity is 64\*8 bits
- () Its capacity is 64\*4 bytes

Its capacity is 64\*4 bits

For constant voltage, the output of the circuit is -----.

2/2

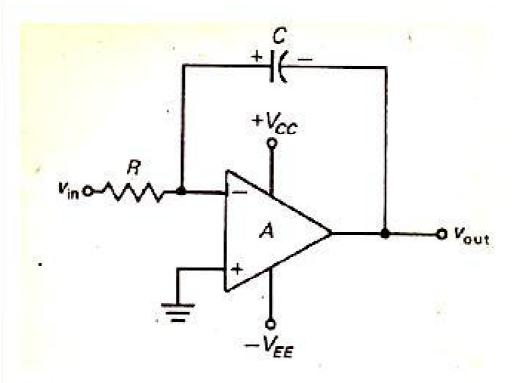


- Time varying voltage
- Negative voltage
- O Positive voltage
- Zero voltage

# Feedback

Zero voltage

If the input voltage is constant, the current through the capacitor of the circuit is 0/3



- Exponential
- Linear
- ( ) Zero
- O Constant

Correct answer

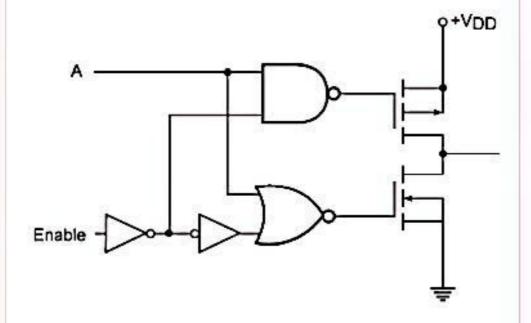
( Constant

Suppose that the digital IC family has a fan out of 6. It implies that the gate can 1/1 supply the current to \_\_\_\_\_ of same family.

- 6 inputs
- 6 outputs
- 12 nodes
- 12 branches

Feedback

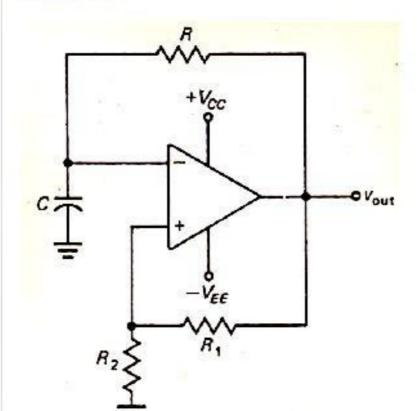
6 inputs



- O Inverted
- Same as input
- Hi-Z (high impedance)

Same as input

Find the frequency of the relaxation oscillator, if R=1 K, C= 0.1 micro Farad, R1= 3/3 2K and R2= 18 K.

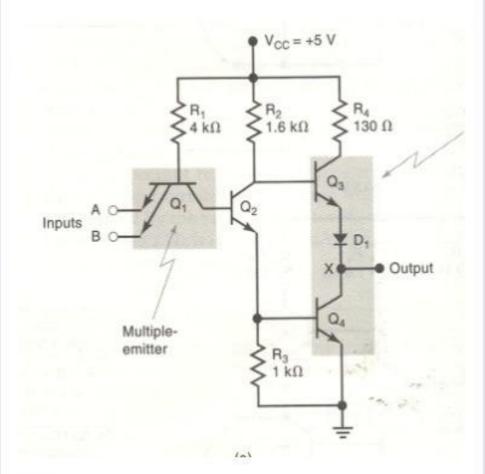




- 10 Hz
- O 1 KHz
- 1.7 KHz
- 100 KHz

1.7 KHz

TTL totem pole outputs should never be tied together, because it can produce 3/3 harmful current through the transistor ------

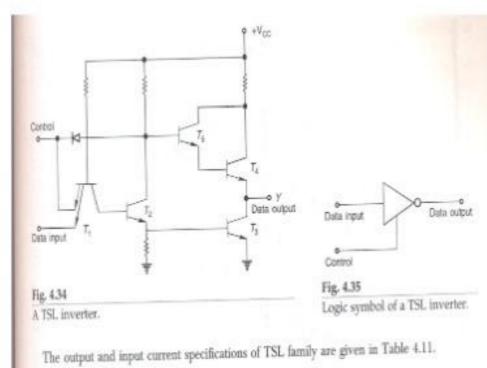


- Q4
- O 03
- O Q1
- O Q2

Feedback

04

In the following Tri-state logic circuit, which conditions are true for the transistors T3, T4, T5 if both of the control input and data input are set to logic one.

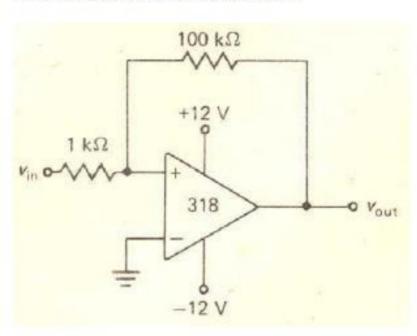


- T3 and T4 are ON but T5 is OFF
- T3 is OFF but T4 and T5 are ON
- T3, T4, T5 are OFF
- T3 is ON but T4 and T5 are OFF

## Feedback

T3 is ON but T4 and T5 are OFF

Find the voltage gain of the non-inverting amplifier.



0/2

2/2

- O 10
- 0
- () 100
- 0.01

Correct answer

100

In the following Tri-state ligic circuit, which conditions are true for the transistors T3, T4, T5 if the control input is logic one but data input is zero.

2/2

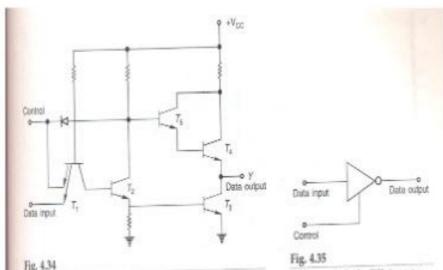


Fig. 4.34 A TSL inverter.

Logic symbol of a TSL inverter.

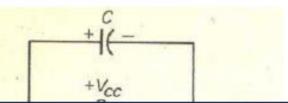
The output and input current specifications of TSL family are given in Table 4.11.

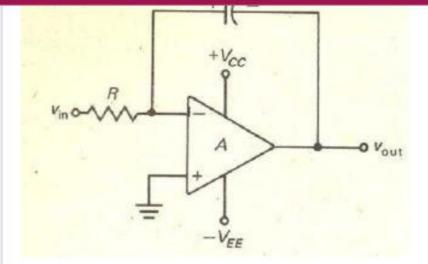
- O T3 and T4 are ON but T5 is OFF
- T3, T4, T5 are OFF
- T3 is ON but T4, T5 are OFF
- T3 is OFF but T4 and T5 are ON

## Feedback

T3 is OFF but T4 and T5 are ON

If the input voltage is constant, the output voltage (voltage across the capacitor)2/2 of the circuit is ------



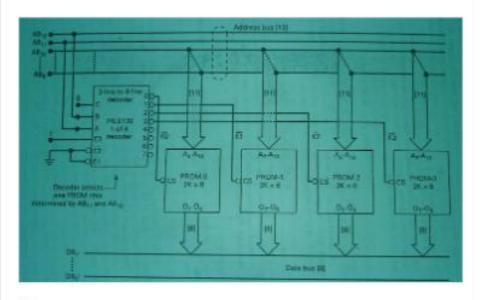


- Exponential function of time
- Linear function of time
- ( ) Zero
- O Constant

Linear function of time

There are four PROM modules in the following ROM diagram. Determine by inspection the exact address range (in hexadecimal) for the PROM-0 module.

3/3



- 0800 to 0FFF
- ( ) 1000 to 17FF
- 1800 to 1FFF
- 0000 to 07FF

### Feedback

0000 to 07FF

E	eedback
0	000 to 07FF
	ch type of output current flows towards or into the output terminal in a logic 1/ uit?
0	Sourcing current
•	Sinking current
0	Both a and b
0	None of the above
F	eedback
S	inking current