EEG SIGNAL ACQUISITION AND ALERT SYSTEM FOR SLEEPING DISORDER PATIENTS USING RISC – V PROCESSOR ON FPGA

Report submitted to GITAM (Deemed to be University) as a partial fulfillment of the requirements for the award of the Degree of Bachelor of Technology in Electronics and Communication Engineering

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DECLARATION

We declare that the project work contained in this report is original and it has been done by me under the guidance of my project guide.

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CERTIFICATE

This is to certify that H Sahana and Priyanka G bearing BU22EECE0100475, BU22EECE0100446 has satisfactorily completed Mini Project Entitled in partial fulfillment of the requirements as prescribed by University for VIIth semester, Bachelor of Technology in "Electrical, Electronics and Communication Engineering" and submitted this report during the academic year 2025-2026.

[Signature of the Guide] [Signature of HOD]

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Chapter 1: Introduction

1.1 Overview of the problem statement

The rapid advancements in digital signal processing and hardware design have made it possible to build real-time biomedical monitoring systems that are both efficient and reliable. Among these, Electroencephalogram (EEG) signal acquisition and processing play a critical role in diagnosing neurological disorders such as sleep apnea and insomnia. Traditional EEG systems often rely on external processors or microcontrollers, which introduce delays and limit real-time performance. To overcome these challenges, Field Programmable Gate Arrays (FPGAs) provide a flexible and parallel computing platform, making them well-suited for high-speed signal capture, filtering, and analysis.

This project focuses on the **implementation of an EEG signal acquisition and processing system using an Artix-7 FPGA**. In the first phase, fundamental FPGA operations such as LED control, clock division, and seven-segment display interfacing were carried out to build a strong hardware foundation. In the second phase, **Serial Peripheral Interface (SPI)** communication is employed to connect the FPGA with an external Analog-to-Digital Converter (ADC) for real-time EEG signal sampling. The captured signals will then be processed through digital filters and displayed for monitoring. This modular approach ensures that each stage—signal acquisition, communication, and processing—can be validated independently, reducing design complexity and increasing reliability.

The long-term objective of the project is to build an efficient hardware-software co-design system capable of detecting abnormal EEG waveforms related to sleep disorders. By leveraging the parallelism of FPGA hardware and the accuracy of digital filters, the design aims to provide a cost-effective, real-time biomedical monitoring solution.

1.2 Objectives and goals:

The objective of this project is to design and implement a real-time EEG signal acquisition and processing system using the Artix-7 FPGA. The primary goal is to establish reliable SPI communication with an external ADC for accurate EEG data capture and to process the signals through digital techniques such as filtering. Additionally, the project aims to validate FPGA-based hardware for biomedical monitoring applications, ensuring low latency, high efficiency, and future scalability for detecting sleep-related disorders.

Specific Objectives:

1. **EEG Signal Acquisition**: To interface the FPGA with an external ADC via SPI for accurate and real-time EEG signal sampling.

2. **Clock and Control Logic**: To design clock dividers and control logic for synchronizing data transfer and ensuring stable operation of the system.

3. **Signal Processing:** To implement digital filters on FPGA to remove noise and extract meaningful brainwave patterns.

4. **Real-Time Visualization**: To display processed EEG signals and detected events using LEDs/7-segment displays for immediate feedback.

5. **Scalability for Healthcare Applications:** To establish a modular FPGA design that can later be extended for advanced medical analysis such as sleep apnea and insomnia detection.

6. **Abnormality Detection Logic:** To design and implement FPGA-based algorithms capable of identifying irregular EEG patterns that may indicate sleep apnea or insomnia.

Goals:

1. **Develop a reliable FPGA-based signal acquisition system** that can capture and digitize both test analog signals and real EEG signals with high accuracy.

2. **Implement real-time EEG signal processing** using a RISC-V soft-core processor on FPGA for efficient pattern recognition and analysis.

3. **Design and integrate an intelligent alert mechanism** (LED, buzzer, or display) to notify users when abnormal brainwave activity such as sleep apnea or insomnia indicators are detected.

4. **Ensure system scalability and portability** by providing a modular architecture that can be extended for advanced biomedical applications and real-world healthcare use.

Chapter 2 : Literature Review

2.1 Introduction

The field of biomedical monitoring, particularly for Electroencephalography (EEG) signal acquisition and processing, is a critical area in modern embedded systems. Reliable, continuous monitoring of neurological signals is vital for diagnosing and managing chronic conditions like sleep disorders, which require high-throughput computational resources. To address the need for portability and real-time processing, three major domains of research are frequently employed: FPGA-based DSP (for signal processing acceleration), Embedded RISC-V Architectures (for flexible, high-performance control), and Bio-Signal Classification Algorithms (for event detection). This chapter reviews key research contributions in these areas, highlighting their techniques and major findings, and positioning them within the scope of the proposed EEG Signal Acquisition and Alert System.

2.2 Embedded Processor Implementation

This section reviews literature relevant to implementing the RISC-V processor core and leveraging FPGA resources for high-speed computation**.**

1. Naveed, M. Z., et al. (2024) – Design & Implementation of 5-Stage 32-bit RISC-V Pipeline Processor on FPGA
    - Technique: Designed and implemented a 32-bit RISC-V processor utilizing a 5-stage pipeline architecture (IF, ID, EX, MEM, WB) using Verilog HDL.
    - Contribution: Validated the **feasibility of integrating complex, modern RISC-V ISAs** into FPGAs for improved instruction throughput and custom SoC development.
    -
2. Ngu Teck Joung, D. (2023) – Design and Simulate RISC-V Processor using Verilog
    - Technique: Developed and simulated a foundational RISC-V processor model exclusively using Verilog HDL, focusing on the verification of core instruction execution and microarchitecture principles.
    - Contribution: Established a verifiable hardware codebase for the RISC-V core, which confirms operational integrity and provides a foundation

for subsequent physical FPGA implementation and customization.

3. Khairullah, S. S. (2022) – Hardware realization of a 5-stage 16-bit RISC processor on FPGA

   - Technique: Implemented a smaller-scale 5-stage pipelined 16-bit RISC processor (non-RISC-V) in hardware on an FPGA, emphasizing the optimization of the instruction execution flow.
   - Contribution: Demonstrated the fundamental hardware realization benefits and performance gains achieved through pipelining in custom embedded processor designs within constrained FPGA resources.

2.3 EEG Signal Processing and Alert Systems

This section reviews papers concerning the signal processing and classification algorithms necessary for the alert system.

1. **Krithiga Sree, R., & Somasundareswari, D. (2024) – Sleep Apnea Detection Based on FPGA Using EEG Signals**
   - **Technique:** Focused on leveraging **FPGA-based Digital Signal Processing (DSP)** for the real-time filtering and analysis of EEG signals, specifically for **sleep apnea detection**.
   - **Contribution:** Confirmed the **high-speed capabilities of FPGAs** for dedicated hardware acceleration of EEG processing algorithms, proving their suitability for critical, low-latency biomedical alerting systems.

2. **Gawhale, S., et al. (2023) – EEG Signal Processing for the Identification of Sleeping Disorder Using Hybrid Deep Learning with Ensemble Classifier**
   - **Technique:** Employed a **Hybrid Deep Learning Model** incorporating an **Ensemble Classifier** to extract features from EEG data and identify sleeping disorders.
   - **Contribution:** Provided **validated algorithmic structures** for accurate identification of sleeping disorders, which informs the design of the C firmware decision-making logic for the embedded RISC-V processor.

3. **de Chazal, P., et al. (2003) – Automatic classification of sleep apnea from ECG signals**

    - **Technique:** Developed an automated classification method for sleep apnea utilizing **ECG (Electrocardiogram) signals** and features derived from heart rate variability.
    - **Contribution:** Highlighted the diagnostic value of **multi-modal sensing**, suggesting that a comprehensive alert system could benefit from integrating auxiliary bio-signals alongside EEG in future system iterations.

4. **Seo, H., et al. (2020) – Sleep quality assessment using wearable ECG-based monitoring**

    - **Technique:** Focused on implementing **sleep quality assessment** using a **wearable device design** that monitored and processed continuous ECG data.
    - **Contribution:** Underscored the crucial design constraints of **portability, power efficiency, and continuous monitoring** that justify the use of highly optimized, single-board solutions like the FPGA-RISC-V SoC over traditional desktop platforms.

Summary

The literature confirms the viability of implementing **complex RISC-V processors on FPGAs** for embedded systems, validating the core architectural choice for this project (Naveed et al., 2024). Research demonstrates that **FPGAs are highly effective for accelerating EEG signal processing** and real-time event detection, which is essential for low-latency alert systems (Krithiga Sree et al., 2024). Furthermore, the review establishes **modern algorithmic requirements** for sleep disorder classification, which informs the firmware development for the RISC-V processor (Gawhale et al., 2023). Ultimately, these works justify the proposed **hybrid FPGA-RISC-V System-on-Chip (SoC) architecture** as the optimal platform for a portable and efficient EEG monitoring solution.

Chapter 3 : Strategic Analysis and Problem Definition

3.1 SWOT Analysis

A SWOT (Strengths, Weaknesses, Opportunities, Threats) analysis provides a structured way to evaluate the project's internal and external factors, defining its positioning and its potential in real-world applications.

Strengths

- **Real-Time Processing:** The **FPGA** provides **inherent parallelism** for DSP tasks, executing EEG filtering and signal processing with extremely low latency, critical for immediate alert generation.
- **Custom SoC Design:** Integrating the **RISC-V soft core** directly on the FPGA creates a highly customized System-on-Chip (SoC) optimized precisely for the EEG application.

Weaknesses

- **Development Complexity:** FPGA development requires proficiency in HDL (Verilog) and complex SoC design tools (Vivado), leading to longer debugging and implementation cycles.
- **Resource Constraints:** The size and complexity of the RISC-V core and DSP filters must be balanced to fit within the limited logic cells and BRAM of the Nexys 4's Artix-7 chip.

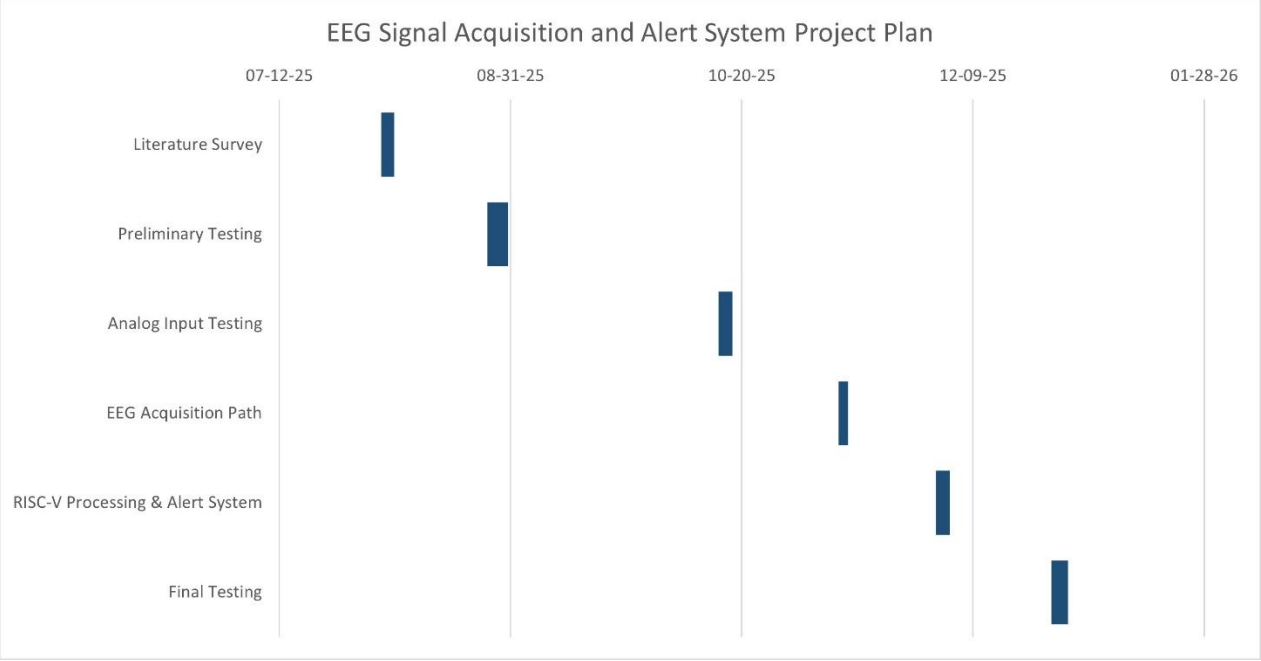
Opportunities

- **Growing Need for Home Monitoring:** There is a strong market demand for portable, non-invasive, and continuous at-home monitoring devices for chronic sleep disorders.
- **Open-Source Ecosystem:** The **RISC-V** architecture is open source and gaining rapid industry support, providing access to a vast and growing library of development tools and soft-core .

Threats

- **Signal Noise and Artifacts:** EEG signals are extremely susceptible to noise (from muscles, movement, 50/60Hz power lines), which can compromise the accuracy of the detection algorithm.
- **Competitive Solutions:** Existing commercial wearable devices are rapidly incorporating simpler sleep monitoring features, requiring this solution to offer superior EEG data quality and proven reliability.

3.2 Project Plan - GANTT Chart



3.3 **Refinement of Problem Statement**

Problem Statement (Refined):

Traditional embedded systems using low-power microcontrollers or DSP chips are limited by sequential processing and insufficient instruction throughput, often failing to meet the concurrent computational demands of real-time EEG filtering, feature extraction, and high-speed data acquisition (SPI) required for reliable chronic monitoring.

To address this gap, the project aims to design and implement a FPGA-based RISC-V System-on-Chip (SoC) Architecture for EEG monitoring that:

1. Integrates custom hardware acceleration (like a high-speed SPI Master and parallel DSP logic) with a RISC-V processor core.
2. Achieves ultra-low latency in processing EEG signals by utilizing the FPGA's inherent parallelism, critical for immediate alert generation.
3. Provides a flexible software platform (RISC-V firmware) for easily updating detection algorithms (e.g., changing threshold parameters or classification models) without redesigning all hardware.
4. Creates a unified, compact SoC solution by eliminating I/O overhead and maximizing resource efficiency on the Nexys 4 board compared to multi-chip solutions.

Chapter 4 : Methodology

4.1 Description of the Approach

The project adopts a Hardware/Software Co-Design approach, implemented as a System-on-Chip (SoC) Architecture on the Nexys 4 FPGA (Artix-7). This methodology leverages the strengths of both hardware (FPGA parallelism) and software (RISC-V control) to overcome the computational limitations of conventional microcontrollers.

The core challenge is achieving reliable, low-latency EEG processing and real-time event alerting. To address this, the implementation strategy is divided into the following sequential and concurrent stages:
Implementation Strategy: FPGA-RISC-V Co-Design

1. High-Speed Data Acquisition (Hardware):
    - SPI Master Protocol: Custom Verilog logic is designed to implement the SPI master, specifically tailored for the high-resolution, multi-channel ADC (e.g., ADS1299).
    - Function: Ensures precise timing and reliable transfer of raw EEG samples from the sensor front-end to the FPGA fabric at high data rates.
    - Output: Continuous stream of 24-bit EEG samples.

2. Data Buffering and Hardware Acceleration (Hardware):

    - Synchronous FIFO/BRAM: A First-In, First-Out buffer (FIFO) is instantiated using FPGA's Block RAM (BRAM) to store acquired samples.
    - Function: Decouples the high-speed SPI acquisition from the RISC-V processor's variable execution speed, preventing data loss.
    - Optional DSP Block: Critical DSP tasks (e.g., 50 Hz/60 Hz Notch Filtering) may be implemented in dedicated parallel hardware before the FIFO to pre-process the data.

3. RISC-V Processor and Control Layer (Software):
   - RISC-V Soft-Core: The RISC-V processor (e.g., PicoRV32) is instantiated as the main control unit, with the FIFO and UART interfaces memory-mapped as peripherals.
   - Function: The processor executes the embedded C firmware, polls the FIFO for new EEG data, executes the final event detection algorithm (e.g., threshold analysis or classification), and manages the alert output.

4.2 Tools and techniques utilized

A. Hardware Design and Implementation

The project relies on specialized tools and techniques for creating and loading the hardware design onto the FPGA.

1. Verilog HDL (Hardware Description Language): This is the core language used for designing all custom digital logic. This includes the fundamental components like the SPI Master (for data acquisition), the UART transmitter (for PC streaming), the FIFO buffers, and the overall structural top module of the system.

2. Xilinx Vivado (IDE): This is the essential integrated design environment (IDE) provided by the FPGA manufacturer. Vivado is used for project management, behavioral simulation, synthesis, place-and-route (P&R), and ultimately generating the final .bit file (bitstream) to configure the Nexys 4 FPGA.

B. Embedded Processing and Software

The software layer requires tools compatible with the customized processor architecture.

1. RISC-V Soft-Core IP (e.g., PicoRV32): This is the processor design itself, instantiated in Verilog within the FPGA logic. It acts as the central control unit for the system.
2. RISC-V GCC Toolchain (GNU Compiler): This is the specialized software required to cross-compile the project's C/Assembly firmware into machine code that the RISC-V processor can execute.

C. **Data Handling and Communication**

Specific protocols and methodologies are used to move data both on and off the chip.

1. SPI Protocol (e.g., ADS1299): This is the high-speed serial protocol chosen for the time-critical task of acquiring high-resolution EEG samples from the external Analog-to-Digital Converter (ADC).
2. Memory-Mapped Peripherals: This is a crucial design technique used to enable the RISC-V processor (software) to interact directly with hardware components (like FIFO status registers or the Alert control line). The hardware registers are assigned specific memory addresses, allowing the processor to control them via standard memory load/store instructions.

D. **Verification and Debugging**

Tools are necessary to ensure the design functions correctly both in simulation and on the physical hardware.

1. Vivado Simulator: Used to verify the behavior of all Verilog modules before loading them onto the FPGA.
2. Logic Analyzer: An external tool used during hardware testing to observe and debug the SPI timing (SCLK, MOSI, MISO) to confirm correct data acquisition.
3. Serial Terminal: Software on the PC used to receive and display the streamed EEG data sent from the FPGA via the UART interface.

4.3Design considerations

While designing the FPGA-based SoC and the overall processing pipeline, the following factors were prioritized:

A. Real-Time Performance and Accuracy

- Computational Efficiency: Critical tasks are partitioned to maximize the FPGA's strengths. Hardware (Verilog) handles parallel, high-speed operations (SPI acquisition and DSP filtering), ensuring the entire processing loop runs in real-time.

- Latency Control: The data path between the ADC and the alert output is minimized. The use of a synchronous FIFO decouples the hardware/software domains to prevent processing delays and guarantee a rapid alert response time.

- Signal Integrity: Robust DSP filtering (e.g., FIR/IIR filters for baseline wander and power-line noise) is integrated into the hardware path to ensure the quality of the EEG data before it reaches the RISC-V classification stage.

B. Architectural and Development Factors

- Resource Management: The RISC-V soft-core IP (e.g., PicoRV32) is carefully configured to be small and efficient, minimizing the consumption of FPGA logic cells (LUTs/FFs) and BRAM to leave room for future hardware accelerators.

- Reproducibility: The project is modular. HDL modules (SPI Master, UART) are designed with parameterized generics (e.g., clock dividers, data widths) to allow easy portability to other FPGA families or different ADC chips.

- Scalability: The architecture is built around a memory-mapped peripheral bus. This allows the seamless addition of new hardware blocks (e.g., a hardware FFT module or a second RISC-V core) or the replacement of the core EEG detection algorithm without altering the main bus structure.

C. System Operation and Debugging

- Reliable Communication: The UART module is designed for robust data streaming at a fixed baud rate (e.g., 115200), allowing for easy PC-based debugging and data logging.
- User Control: Onboard peripherals (buttons, LEDs) are used to provide simple control (e.g., reset system, start/stop acquisition) and visual status feedback to the user or technician.

Chapter 5 : Implementation

5.1 Description of how the project was executed

The EEG Signal Acquisition and Alert System was executed using a Hardware/Software Co-Design methodology implemented within the Xilinx Vivado IDE. The project execution was phased, focusing initially on hardware validation and then on core data acquisition module implementation.

The primary development environment was the Vivado 2023.2 IDE, targeting the Artix-7 FPGA on the Nexys 4 development board. The execution pipeline involved the sequential implementation of the following steps:

Execution Pipeline: FPGA Hardware Implementation

Step 1: Project Setup and Constraint Definition

- Verilog Module Creation: All foundational modules (top.v, spi_master.v, uart_tx.v) were created and imported as design sources.
- Constraint Definition: The Nexys 4 XDC constraints file was meticulously defined and verified, resolving all UCIO-1 (Unconstrained Port) and NSTD-1 (I/O Standard) errors. This step guaranteed correct pin-mapping for clk, LEDs, switches, buttons, and PMOD pins (for SPI/UART).

Step 2: Phase 1 Validation (On-Board I/O Test)

- Logic Implementation: Simple Verilog logic was implemented for Switches → LEDs mirroring and Button-controlled 7-Segment counting (e.g., btnC for reset, btnR for increment).
- Bitstream Generation: The design was run through Synthesis → Implementation → Bitstream Generation in Vivado.
- Visual Verification: The generated bitstream was programmed onto the FPGA. LED and 7-segment functionality was verified on-board, confirming the entire FPGA toolchain was operational and reliable.

Step 3: Core Module Implementation (Phase 2)

- SPI Master Logic: The spi_master.v module was written to implement the Parameterized SPI protocol (CPOL=0, CPHA=0) with configurable data width (24 bits) and clock prescaler (PRESCALE).
- UART Transmitter Logic: The uart_tx.v module was implemented to convert parallel data into a serial stream at 115200 baud, enabling PC data output.

Step 4: Integration and Data Pipeline Setup

- Module Instantiation: The SPI Master, UART TX, and ADC Driver modules were instantiated within the top.v file to establish the sequential data pipeline.
- FIFO Integration: A synchronous FIFO buffer (BRAM-based) was integrated into the pipeline. This ensured that the fast SPI acquisition could be decoupled from the RISC-V processor's reading cycle.
- Final Output Setup: The completed hardware modules were prepared to accept the RISC-V soft-core (future Phase 3) as the control interface, completing the custom hardware platform design.

5.2 Challenges faced and solutions implemented

. Toolchain and Constraint Errors (Phase 1)

- Challenge: Initial Vivado build failed to generate a bitstream due to UCIO-1 (Unconstrained Ports) and NSTD-1 (I/O Standards) errors.
- Solution: The Nexys 4 XDC constraints file was meticulously corrected, providing the exact pin names and specifying IOSTANDARD LVCMOS33 for every top-level port (clk, sw[15:0], led[15:0], an[7:0], seg[6:0], dp).

- Challenge: Button logic failed to detect presses because Nexys 4 pushbuttons are active-low (logic '0' when pressed), while the initial code assumed active-high.
- Solution: The Verilog code was immediately modified to implement active-low checking , ensuring the buttons correctly triggered control logic.

2. SPI Protocol Timing and Verification (Phase 2)

- Challenge: Generating the precise SPI clock (SCLK) required by the external ADC from the 100 MHz system clock was inflexible with a fixed divider.
- Solution: The spi_master.v module was designed with a parameterized prescaler (PRESCALE) to allow the SPI clock frequency (F_SPI) to be precisely tuned for the ADC without modifying core Verilog code.

- Challenge: Debugging the high-speed SPI protocol (MISO/MOSI) on the physical chip was difficult to verify the ADC's data response.
- Solution: A Logic Analyzer was used during hardware testing to

simultaneously observe SCLK, CS, MOSI, and MISO lines, providing external verification of the correct SPI data exchange and timing.

- Challenge: Extracting the precise 10-bit or 24-bit valid ADC sample from the full 24-bit SPI transaction required careful data alignment.
- Solution: The ADC driver (mcp3008_reader.v) was implemented with explicit bit-slicing logic to correctly extract the valid data bits and discard the null bits and padding, ensuring the processor receives a clean sample.

Chapter 6: Results

6.1 outcomes

6.2 Interpretation of results

6.3 Comparison with existing literature or technologies

Chapter 7: Conclusion

Here write Suggestions for further research or development and Potential improvements or extensions

Chapter 8 : Future Work

The next phase will focus on final optimization and transitioning the prototype toward a clinical implementation:

- **Wireless and Clinical Integration:** The immediate next step is integrating the FPGA system with an ergonomic, **wireless headset band** for **EEG acquisition**. This is necessary to enable crucial **real-time testing** and validation of the low-power profile (targeting ≈19mW) using genuine clinical data.

- **Processor Finalization:** We will complete the optimization of the RISC-V core by implementing mechanisms like a **dynamic branch predictor** and integrating key **RISC-V extensions** (e.g., F for floating-point) to improve native acceleration of signal processing algorithms.

- **Model Robustness:** We will move beyond simulation to test the model's reliability on **larger and more diverse clinical datasets**. This step will finalize the validation of the model's performance and generalizability across varied patient populations.

References:

- Krithiga Sree, R., & Somasundareswari, D. (2024). Sleep Apnea Detection Based on FPGA Using EEG Signals. IRJMET, Vol. 6, Issue 7

- de Chazal, P., et al. (2003). Automatic classification of sleep apnea from ECG signals. IEEE Transactions on Biomedical Engineering.
- Seo, H., et al. (2020). Sleep quality assessment using wearable ECG-based monitoring.

- Naveed, M. Z., Amar, M., Hussain, A., & Awan, Z. A. (2024). Design & Implementation of 5-Stage 32-bit RISC-V Pipeline Processor on FPGA. 9th MDSRIC, Pakistan

- Ngu Teck Joung, D. (2023). Design and Simulate RISC-V Processor using Verilog. Master's Dissertation, Universiti Tunku Abdul Rahman

- Khairullah, S. S. (2022). Hardware realization of a 5-stage 16-bit RISC processor on FPGA.

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