

SoC-FPGA Design Guide

Real Time Embedded Systems

LAP – IC – EPFL

Version 0.50 (Preliminary)

Sahand Kashani-Akhavan

René Beuchat

1 TABLE OF CONTENTS

2	List of Figures	4
3	Table of Tables	5
4	Introduction	6
5	Terasic DE1-SoC Board	7
5.1	Specifications	7
5.1.1	FPGA Device	7
5.1.2	Configuration and Debug	7
5.1.3	Memory Device	7
5.1.4	Communication	7
5.1.5	Connectors	8
5.1.6	Display	8
5.1.7	Audio	8
5.1.8	Video Input	8
5.1.9	ADC	8
5.1.10	Switches, Buttons and Indicators	8
5.1.11	Sensors	8
5.1.12	Power	8
5.1.13	Block Diagram	9
5.2	Layout	9
6	Cyclone V Overview	11
6.1	Introduction to the Cyclone V Hard Processor System	11
6.2	Features of the HPS	12
6.3	System Integration Overview	13
6.3.1	MPU Subsystem	13
6.3.2	SDRAM Controller Subsystem	13
6.3.3	Support Peripherals	13
6.3.3.1	System Manager	13
6.3.3.2	FPGA Manager	14
6.3.4	Interface Peripherals	14
6.3.4.1	GPIO Interfaces	14
6.3.5	On-Chip Memory	14
6.3.5.1	On-Chip RAM	14

6.3.5.2	Boot ROM	14
6.4	HPS-FPGA Interfaces	14
6.5	HPS Address Map	15
6.5.1	HPS Address Spaces	15
6.5.2	HPS Peripheral Region Address Map.....	16
6.6	HPS Booting and FPGA Configuration	17
6.6.1	HPS Boot and FPGA Configuration Ordering.....	18
6.6.2	Zooming In On the HPS Boot Process.....	20
6.6.2.1	Preloader.....	20
7	Using the Cyclone V – Possible Configurations	21
7.1	Introduction	21
7.2	FPGA-only.....	21
7.3	HPS & FPGA	21
7.3.1	Choosing the Type of Application	21
7.3.1.1	Bare-metal Application	21
7.3.1.2	Application Over an Operating System (Linux)	22
8	Using the Cyclone V - Hands-On Development Tutorial	23
8.1	Goals.....	23
8.2	Project Structure	23
8.3	Hardware.....	23
8.3.1	General Quartus II Setup.....	23
8.3.2	System Design with Qsys – Nios II.....	24
8.3.3	System Design with Qsys – HPS	26
8.3.3.1	Instantiating the HPS Component.....	26
8.3.3.1.1	FPGA Interfaces Tab	26
8.3.3.1.2	Peripheral Pins Tab	27
8.3.3.1.3	HPS Clocks Tab	28
8.3.3.1.4	SDRAM Tab	28
8.3.3.2	Interfacing with FPGA Peripherals	31
8.3.4	Instantiating the Qsys System.....	32
8.3.5	HPS DDR3 Pin Assignments	34
8.3.6	Programming the FPGA.....	36
8.4	Software	37
8.4.1	FPGA – Nios II	37

8.4.1.1	Project Setup	37
8.4.1.2	Nios II Programming Theory – Accessing Peripherals.....	38
8.4.1.3	Nios II Programming Practice	39
8.4.2	HPS – ARM.....	40
8.4.2.1	Bare-metal Applications	40
8.4.2.1.1	Preloader Generation	40
8.4.2.1.2	Generating a Header File for HPS Peripherals	42
8.4.2.1.3	ARM DS-5	43
8.4.2.1.3.1	Setting Up a New C Project	43
8.4.2.1.3.2	Writing a DS-5 Debug Script.....	44
8.4.2.1.3.3	Setting Up the Debug Configuration.....	45
8.4.2.1.3.4	HPS Programming	47
8.4.2.1.3.4.1	Theory	47
8.4.2.1.3.4.2	Practice	47
8.4.2.2	Linux Applications	48
9	Todo	49
10	Appendix	50
10.1	DE1-SoC Top-level VHDL Entity	50
10.2	DE1-SoC Pin Assignment TCL script.....	54
11	References	67
12	SoC part test	69
12.1	HPS Architecture	69
12.2	Hardware development	69
12.2.1	Qsys integration.....	69
12.3	Software development	71
12.3.1	ARM DS-5 tools	71
12.3.2	Hello World on ARM HPS part.....	71
12.3.2.1	Scatter.scat	71
12.3.2.2	Makefile	72
12.3.3	[4]GPIO access	72
12.3.3.1	Library installation	74
12.3.3.2	Reference files	74

2 LIST OF FIGURES

Figure 5-1. Terasic DE1-SoC Board [1]	7
Figure 5-2. Block Diagram of the DE1-SoC Board [1]	9
Figure 5-3. Back [1]	9
Figure 5-4. Front [1]	10
Figure 6-1. Altera SoC FPGA Device Block Diagram [2, pp. 1-1].....	11
Figure 6-2. HPS Block Diagram [2, pp. 1-3]	12
Figure 6-3. HPS Address Space Relations [2, pp. 1-14]	15
Figure 6-4. Simplified HPS Boot Flow [2, pp. A-3]	18
Figure 6-5. Independent FPGA Configuration and HPS Booting [2, pp. A-2]	18
Figure 6-6. FPGA Configuration before HPS Booting (HPS boots from FPGA) [2, pp. A-2].....	19
Figure 6-7. HPS Boots and Performs FPGA Configuration [2, pp. A-3]	19
Figure 6-8. HPS Boot Flows [2, pp. A-3]	20
Figure 8-1. Project Folder Structure.....	23
Figure 8-2. Basic Nios II System with SDRAM and JTAG UART.....	25
Figure 8-3. Adding LEDs and Switches to the System	26
Figure 8-4. HPS Component Parameters	26
Figure 8-5. HPS_KEY & HPS_LED on DE1-SoC Schematic	27
Figure 8-6. HPS_KEY & HPS_LED on Qsys Peripheral Pins Tab.....	27
Figure 8-7. Using Pin G21 for SPI.....	28
Figure 8-8. Using Pins G21 & A24 as GPIO	28
Figure 8-9. Adding the "Standalone" HPS to the System.....	31
Figure 8-10. Adding Buttons and 7-segment Displays to the Lightweight HPS-to-FPGA Bridge	32
Figure 8-11. Qsys Component Instantiation	33
Figure 8-12. Final Top-level Entity.....	34
Figure 8-13. HPS DDR3 Pin Assignment TCL Script Selection Bug.....	35
Figure 8-14. Correct HPS DDR3 Pin Assignment TCL Script Selection.....	35
Figure 8-15. Quartus II Programmer	36
Figure 8-16. FPGA Selection	36
Figure 8-17. JTAG Scan Chain.....	36
Figure 8-18. Programming the FPGA	37
Figure 8-19. Incorrect Nios II Peripheral Access in C	38

Figure 8-20. Correct Nios II Peripheral Access in C	38
Figure 8-21. nios.c	39
Figure 8-22. Nios II Target Connection Dialog	40
Figure 8-23. New BSP Dialog	41
Figure 8-24. Preloader Settings Dialog.....	41
Figure 8-25. generate_hps_qsys_header.sh	42
Figure 8-26. hps_soc_system.h.....	43
Figure 8-27. New C Project Dialog	44
Figure 8-28. debug_setup.ds.....	45
Figure 8-29. Debug Configuraton "Connection" Tab	46
Figure 8-30. Debug Configuration "Files" Tab.....	46
Figure 8-31. Debug Configuration "Debugger" Tab	47
Figure 8-32. hps_baremetal.c	48
Figure 8-33. Debug Control View	48
Figure 10-1. DE1-SoC Top-level VHDL Entity	52
Figure 10-2. DE1-SoC Pin Assignment TCL Script	66

3 TABLE OF TABLES

Table 6-1. HPS Address Spaces [2, pp. 1-13]	15
Table 6-2. Common Address Space Regions [2, pp. 1-15]	15
Table 6-3. HPS Peripheral Region Address Map [2, pp. 1-16]	17

4 INTRODUCTION

The development of embedded systems based on chips containing one or more microprocessors and hardcore peripherals, as well as an FPGA part is becoming more and more important. This technology gives the designer a lot of freedom and powerful abilities. Classical design flows with microcontrollers are emphasized with the full power of FPGAs.

Mixed designs are becoming a reality. One can now design specific accelerators to greatly improve algorithms, or create specific programmable interfaces with the external world.

Two main HDL (**Hardware Design Language**) languages are available for the design of the FPGA part: **VHDL** and **Verilog**. There also exist other tools that perform automatic translations from C to HDL. New emerging technologies like OpenCL allow compatibility between high-level software design, and low-level hardware implementations such as:

- Compilation for single or multicore processors
- Compilation for GPUs (Graphical Processing Unit)
- Translation and compilation for FPGAs. The latest models use a PCIe interface or some other way of parameters passing between the main processor and the FPGA

*This guide assumes users know how to use **QUARTUS II**, **NIOS II**, **QSYS** and **MODELSIM-ALTERA**.*

*All hardware and software examples in this guide were made with Quartus II, SoC EDS and Nios II Software Build Tools version **14.1**.*

*Some figures in this guide were made with Quartus II, SoC EDS and Nios II Software Build Tools version **14.0**.*

We will be using the Terasic [DE1-SoC](#) board.

5 TERASIC DE1-SoC BOARD

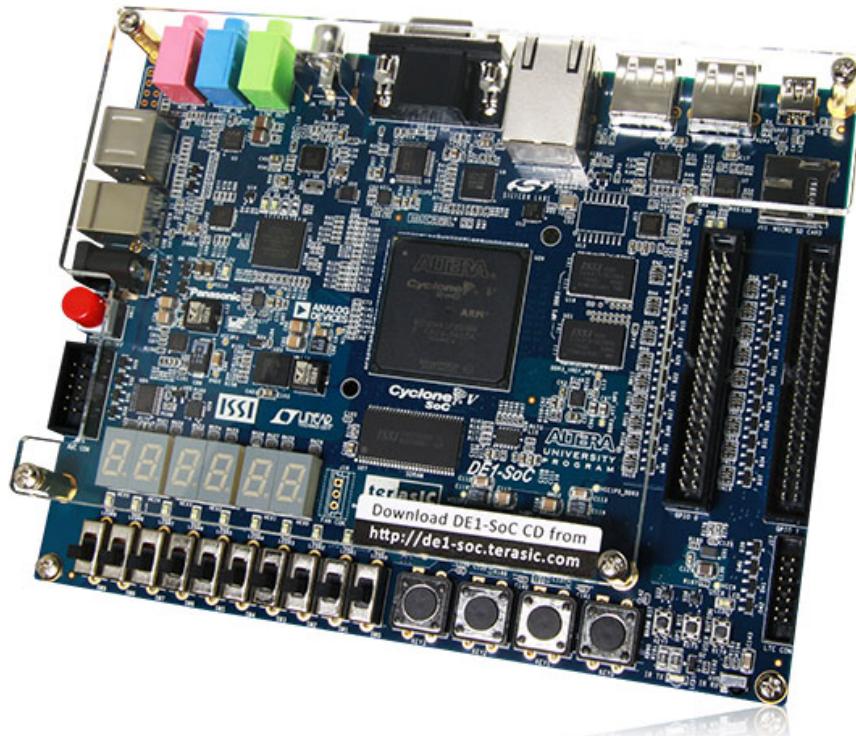


Figure 5-1. Terasic DE1-SoC Board [1]

The DE1-SoC board has many features that allow users to implement a wide range of designed circuits. We will discuss some noteworthy features in this guide.

5.1 SPECIFICATIONS

5.1.1 FPGA Device

- Cyclone V SoC **5CSEMA5F31C6** Device
- Dual-core **ARM CORTEX-A9** (HPS)
- **85K** Programmable Logic Elements
- 4'450 Kbits embedded memory
- 6 Fractional PLLs
- 2 Hard Memory Controllers (only seems to be used for the HPS DDR3 SDRAM, not the FPGA SDRAM)

5.1.2 Configuration and Debug

- Quad Serial Configuration device – **EPCQ256** on FPGA
- On-Board **USB BLASTER II** (Normal type B USB connector)

5.1.3 Memory Device

- **64 MB** (32Mx16) SDRAM on FPGA
- **1 GB** (2x256Mx16) DDR3 SDRAM on HPS
- **MICRO SD** Card Socket on HPS

5.1.4 Communication

- Two Port USB 2.0 Host (ULPI interface with USB type A connector)
- USB to UART (micro USB type B connector)
- 10/100/1000 Ethernet
- PS/2 mouse/keyboard
- IR Emitter/Receiver

5.1.5 Connectors

- Two 40-pin Expansion Headers
- One 10-pin ADC Input Header
- One LTC connector (One Serial Peripheral Interface (SPI) Master, one I2C and one GPIO interface)

5.1.6 Display

- 24-bit VGA DAC

5.1.7 Audio

- 24-bit CODEC, line-in, line-out, and microphone-in jacks

5.1.8 Video Input

- TV Decoder (NTSC/PAL/SECAM) and TV-in connector

5.1.9 ADC

- Fast throughput rate: 1 MSPS
- Channel number: 8
- Resolution: 12 bits
- Analog input range : 0 ~ 2.5 V or 0 ~ 5V as selected via the RANGE bit in the control register

5.1.10 Switches, Buttons and Indicators

- 4 User Keys (FPGA x4)
- 10 User switches (FPGA x10)
- 11 User LEDs (FPGA x10; HPS x 1)
- 2 HPS Reset Buttons (HPS_RST_n and HPS_WARM_RST_n)
- Six 7-segment displays

5.1.11 Sensors

- G-Sensor on HPS

5.1.12 Power

- 12V DC input

5.1.13 Block Diagram

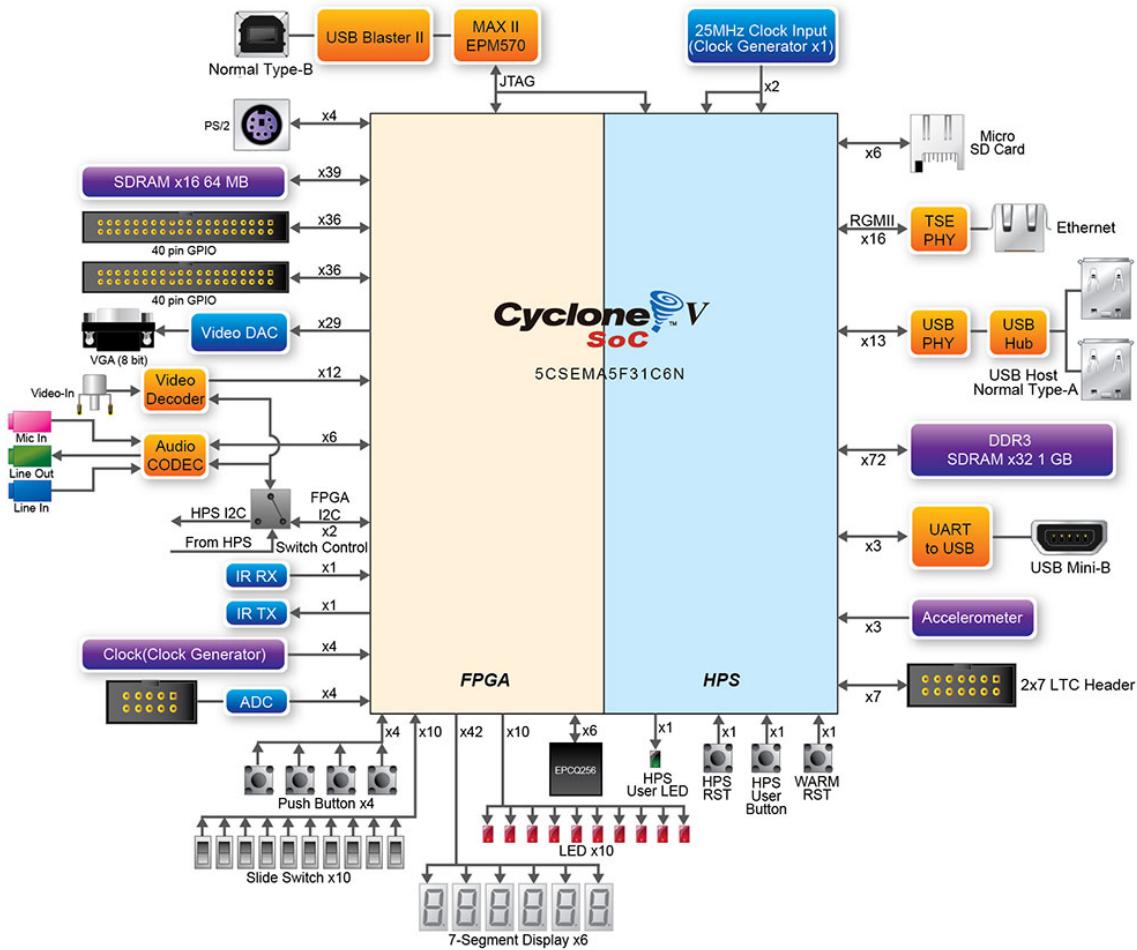


Figure 5-2. Block Diagram of the DE1-SoC Board [1]

5.2 LAYOUT

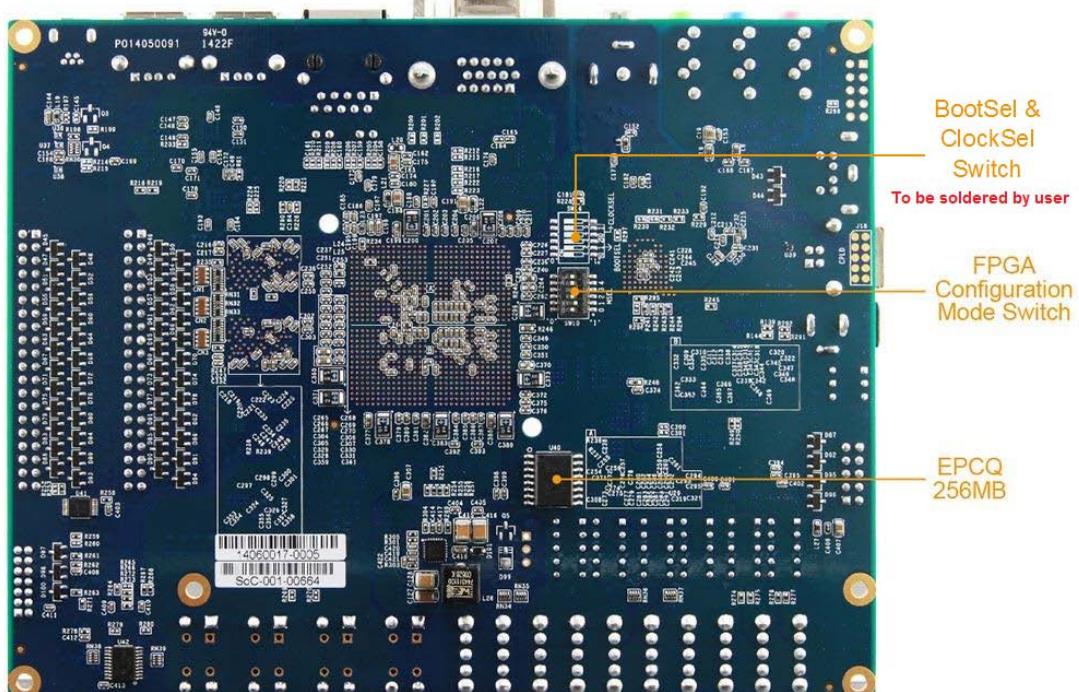


Figure 5-3. Back [1]

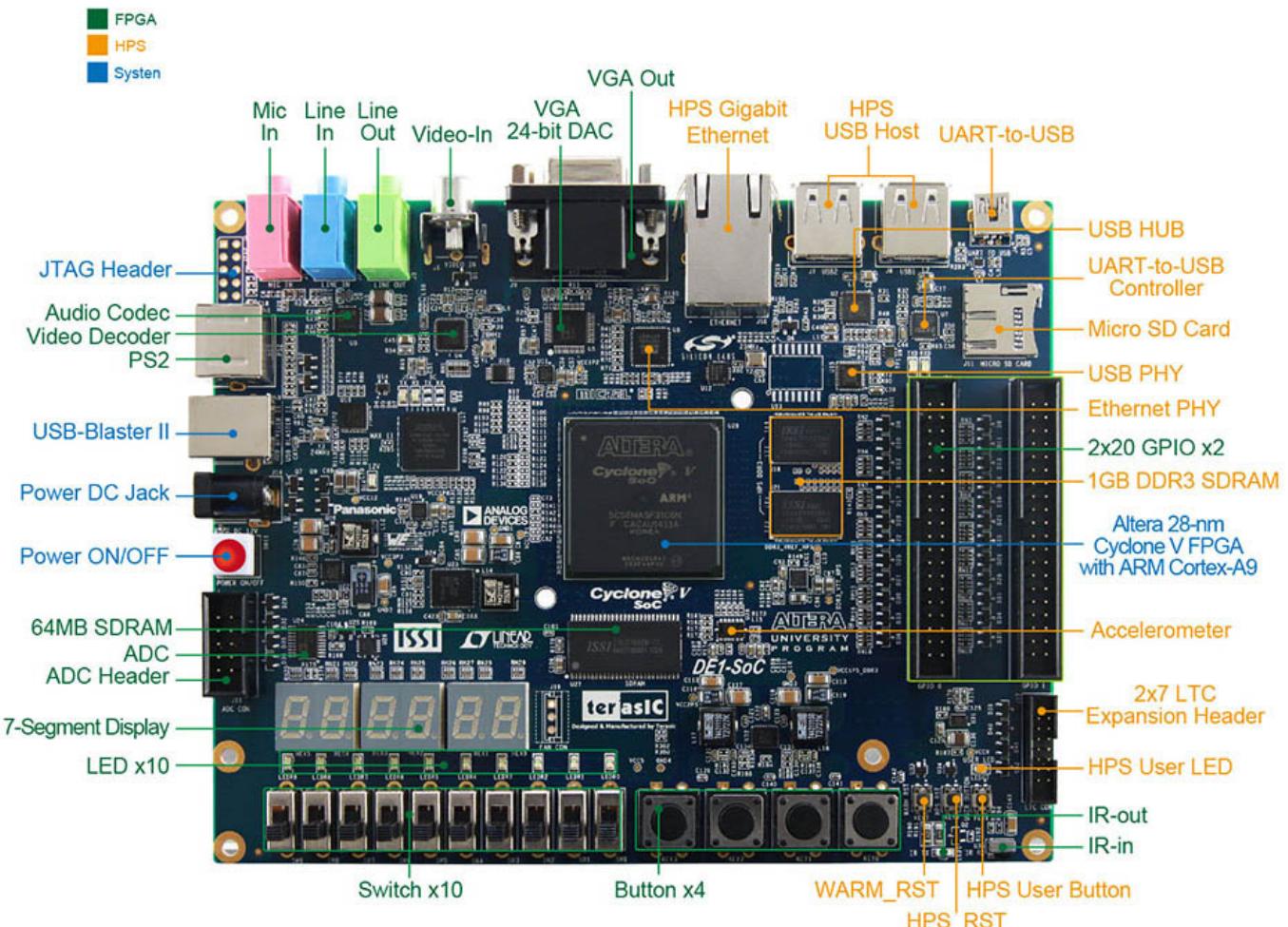


Figure 5-4. Front [1]

- Green for peripherals directly connected to the FPGA
- Orange for peripherals directly connected to the HPS
- Blue for board control

6 CYCLONE V OVERVIEW

This section describes some features of the Cyclone V family of devices. We do not list all features, but only the ones most important to us. All information below, along with the most complete documentation regarding this family can be found in the Cyclone V Device Handbook [2].

6.1 INTRODUCTION TO THE CYCLONE V HARD PROCESSOR SYSTEM

The Cyclone V device is a single-die system on a chip (SoC) that consists of two distinct parts – a hard processor system (HPS) portion and an FPGA portion.

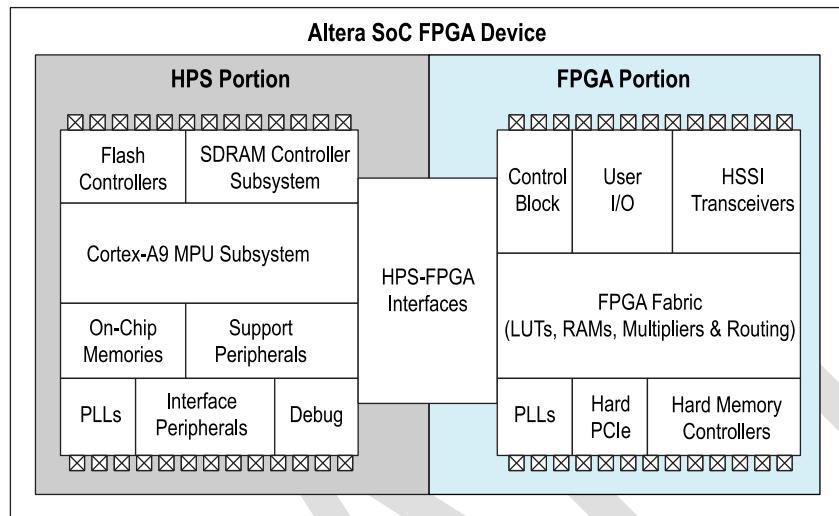


Figure 6-1. Altera SoC FPGA Device Block Diagram [2, pp. 1-1]

The HPS contains a microprocessor unit (MPU) subsystem with single or dual ARM Cortex-A9 MPCore processors, flash memory controllers, SDRAM L3 Interconnect, on-chip memories, support peripherals, interface peripherals, debug capabilities, and phase-locked loops (PLLs). The dual-processor HPS supports symmetric (SMP) and asymmetric (AMP) multiprocessing.

The DE1-SoC has a DUAL-processor HPS.

The FPGA portion of the device contains the FPGA fabric, a control block (CB), phase-locked loops (PLLs), and depending on the device variant, high-speed serial interface (HSSI) transceivers, hard PCI Express (PCIe) controllers, and hard memory controllers.

The DE1-SoC does not contain any HSSI transceivers, or hard PCIe controllers.

The HPS and FPGA portions of the device are distinctly different. The HPS can boot from multiple sources, including the FPGA fabric and external flash. In contrast, the FPGA must be configured through either the HPS or an externally supported device.

The MPU subsystem can boot from flash devices connected to the HPS pins. Or, when the FPGA portion is configured by an external source, the MPU subsystem can boot from memory available on the FPGA portion of the device.

The HPS and FPGA portions of the device each have their own pins. Pins are not freely shared between the HPS and the FPGA fabric. The **FPGA I/O PINS** are configured by an **FPGA CONFIGURATION IMAGE** through the HPS or any external source supported by the device. The **HPS I/O PINS** are configured by **SOFTWARE** executing in the HPS. Software executing on the HPS accesses control registers in the Cyclone V system manager to assign HPS I/O pins to the available HPS modules.

The **SOFTWARE** that configures the **HPS I/O PINS** is called the **PRELOADER**.

The HPS and FPGA portions of the device have separate external power supplies and independently power on. You can power on the HPS without powering on the FPGA portion of the device. However, to power on the FPGA portion, the HPS must already be on or powered on at the same time as the FPGA portion. You can also turn off the FPGA portion of the device while leaving the HPS power on.

6.2 FEATURES OF THE HPS

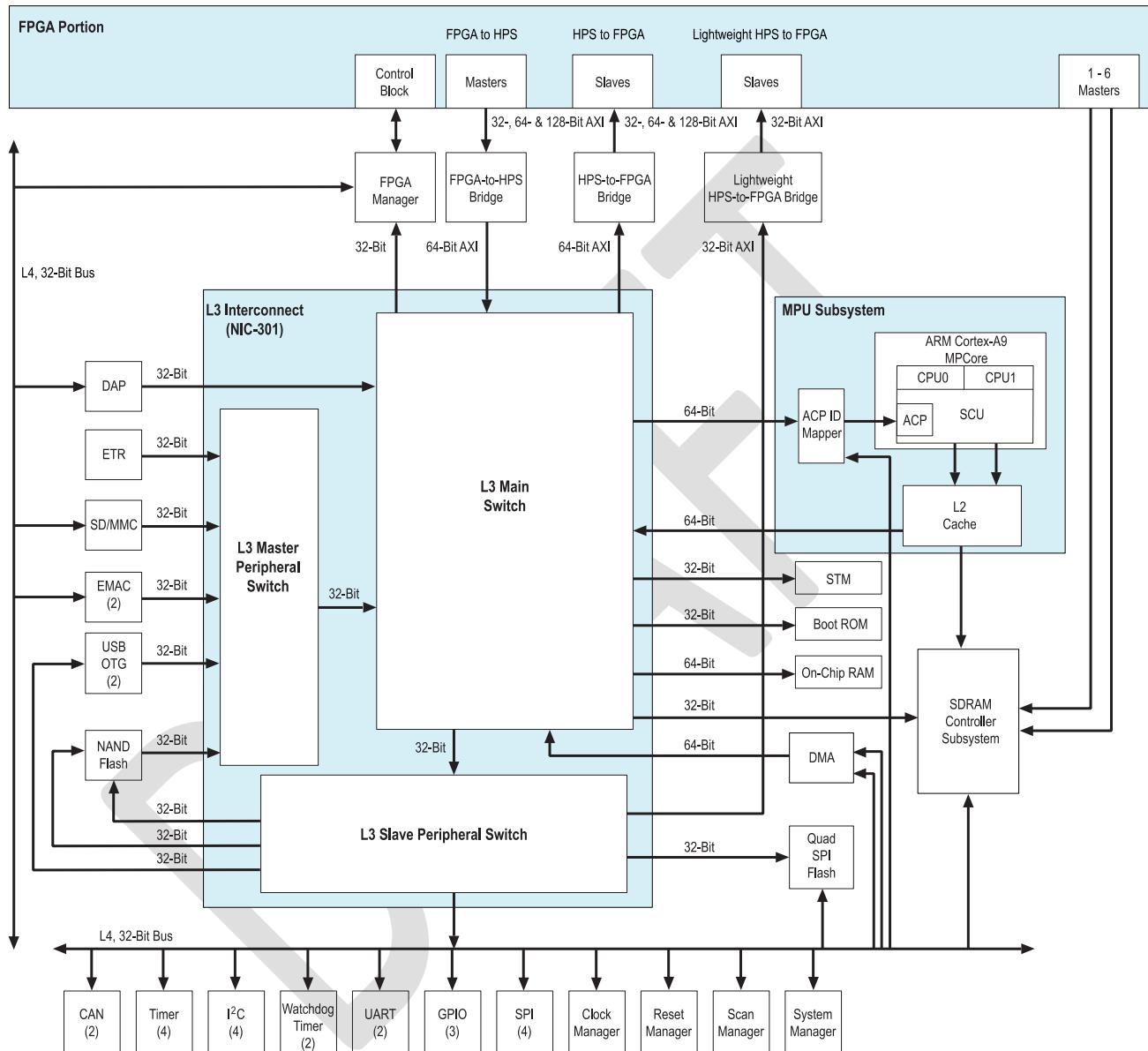


Figure 6-2. HPS Block Diagram [2, pp. 1-3]

The following list contains the main modules of the HPS:

- MPU subsystem featuring dual ARM Cortex-A9 MPCore processors
- General-purpose Direct Memory Access (DMA) controller
- Two Ethernet media access controllers (EMACs)
- Two USB 2.0 On-The-Go (OTG) controllers
- NAND flash controller
- Quad SPI flash controller
- Secure Digital (SD) / MultiMediaCard (MMC) controller

- Two serial peripheral interface (SPI) master controllers
- Two SPI slave controllers
- Four inter-integrated circuit (I^2C) controllers
- 64 KB on-chip RAM
- 64 KB on-chip boot ROM
- Two UARTs
- Four timers
- Two watchdog timers
- Three general-purpose I/O (GPIO) interfaces
- Two controller area network (CAN) controllers
- ARM CoreSight debug components
- System manager
- Clock manager
- Reset manager
- Scan manager
- FPGA manager

6.3 SYSTEM INTEGRATION OVERVIEW

In this part, we briefly go through *some* features provided by the most important HPS components.

6.3.1 MPU Subsystem

Here are a few important features of the MPU subsystem:

- Interrupt controller
- One general-purpose timer and one watchdog timer per processor
- One Memory management unit (MMU) per processor

The HPS masters the L3 interconnect and the SDRAM controller subsystem.

6.3.2 SDRAM Controller Subsystem

The SDRAM controller subsystem is **MASTERED** by **HPS MASTERS** and **FPGA FABRIC MASTERS**. It supports DDR2, DDR3, and LPDDR2 devices. It is composed of 2 parts:

- SDRAM controller
- DDR PHY (interfaces the single port memory controller to the HPS I/O)

The DE1-SoC contains DDR3 SDRAM on the HPS

6.3.3 Support Peripherals

6.3.3.1 System Manager

This is one of the most *essential* HPS components. It offers a few important features:

- **PIN MULTIPLEXING** (term used for the **SOFTWARE** configuration of the **HPS I/O PINS** by the **PRELOADER**)
- Freeze controller that places I/O elements into a safe state for configuration
- Low-level control of peripheral features not accessible through the control and status registers (CSRs)

*The low-level control of some peripheral features that are not accessible through the CSRs is **NOT** externally documented. You will see this type of code when you generate your custom preloader, but must **NOT** use the constructs in your own code.*

6.3.3.2 **FPGA Manager**

The FPGA manager offers the following features:

- Manages the configuration of the FPGA portion of the device
- Monitors configuration-related signals in the FPGA
- Provides 32 general-purpose inputs and 32 general-purpose outputs to the FPGA fabric

6.3.4 Interface Peripherals

6.3.4.1 **GPIO Interfaces**

The HPS provides three GPIO interfaces and offer the following features:

- Supports digital de-bounce
- Configurable interrupt mode
- Supports up to 71 I/O pins and 14 input-only pins, based on device variant
- Supports up to 67 I/O pins and 14 input-only pins

The DE1-SoC has 67 I/O pins and 14 input-only pins

6.3.5 On-Chip Memory

*The following on-chip memories are **DIFFERENT** from any on-chip memories located in the FPGA fabric.*

6.3.5.1 **On-Chip RAM**

The on-chip RAM offers the following features:

- 64 KB size
- High performance for all burst lengths

6.3.5.2 **Boot ROM**

The boot ROM offers the following features:

- 64 KB size
- Contains the code required to support HPS boot from cold or warm reset
- Used **EXCLUSIVELY** for booting the HPS

*The code in the boot ROM **CANNOT** be changed.*

6.4 HPS-FPGA INTERFACES

The HPS-FPGA interfaces provide a variety of communication channels between the HPS and the FPGA fabric.

The HPS-FPGA interfaces include:

- FPGA-to-HPS bridge – a high performance bus with a configurable data width of 32, 64, or 128 bits. It allows the FPGA fabric to master transactions to slaves in the HPS. This interface allows the FPGA fabric to have full visibility into the HPS address space.
- HPS-to-FPGA bridge – a high performance bus with a configurable data width of 32, 64, or 128 bits. It allows the HPS to master transactions to slaves in the FPGA fabric. I will sometimes call this the “*heavyweight*” HPS-to-FPGA bridge to distinguish its “*lightweight*” counterpart (see below).
- Lightweight HPS-to-FPGA bridge – a bus with a 32-bit fixed data width. It allows the HPS to master transactions to slaves in the FPGA fabric.
- FPGA manager interface – signals that communicate with FPGA fabric for boot and configuration.
- Interrupts – allow soft IP to supply interrupts directly to the MPU interrupt controller.
- HPS debug interface – an interface that allows the HPS debug control domain to extend into the FPGA.

6.5 HPS ADDRESS MAP

6.5.1 HPS Address Spaces

The HPS address map specifies the address of slaves, such as memory and peripherals, as viewed by the HPS masters. The HPS has 3 address spaces:

Name	Description	Size
MPU	MPU subsystem	4 GB
L3	L3 interconnect	4 GB
SDRAM	SDRAM controller subsystem	4 GB

Table 6-1. HPS Address Spaces [2, pp. 1-13]

The following figure shows the relationships between the different HPS address spaces. The figure is **NOT** to scale.

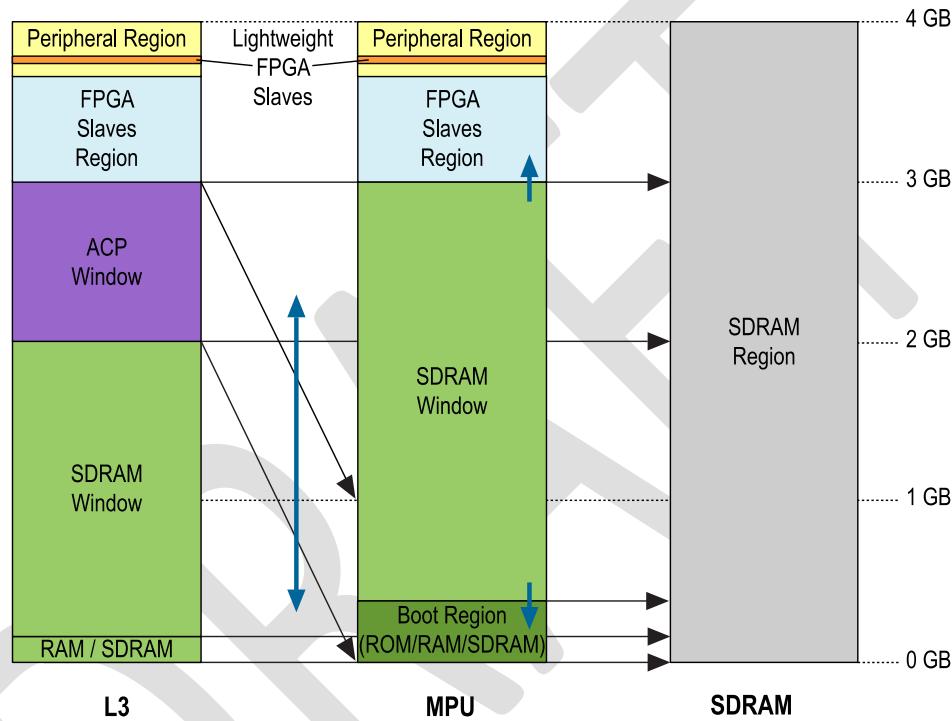


Figure 6-3. HPS Address Space Relations [2, pp. 1-14]

The window regions provide access to other address spaces. The thin black arrows indicate which address space is accessed by a window region (arrows point to accessed address space).

The SDRAM window in the MPU can grow and shrink at the top and bottom (short blue vertical arrows) at the expense of the FPGA slaves and boot regions. The ACP window can be mapped to any 1 GB region in the MPU address space (blue vertical bidirectional arrow), on gigabyte-aligned boundaries.

The following table shows the base address and size of each region that is common to the L3 and MPU address spaces.

Region Name	Description	Base Address	Size
FPGA slaves	FPGA slaves connected to the HPS-to-FPGA bridge	0xC0000000	960 MB
HPS peripherals	Slaves directly connected to the HPS (corresponds to all orange colored elements on Figure 5-4 and Figure 5-3)	0xFC000000	64 MB
Lightweight FPGA slaves	FPGA slaves connected to the lightweight HPS-to-FPGA bridge	0xFF200000	2 MB

Table 6-2. Common Address Space Regions [2, pp. 1-15]

6.5.2 HPS Peripheral Region Address Map

The following table lists the slave identifier, slave title, base address, and size of each slave in the HPS peripheral region. The *Slave Identifier* column lists the names used in the HPS register map file provided by Altera (more on this later).

Slave Identifier	Slave Title	Base Address	Size
STM	STM	0xFC000000	48 MB
DAP	DAP	0xFF000000	2 MB
LWFPGASLAVES	FPGA slaves accessed with lightweight HPS-to-FPGA bridge	0xFF200000	2 MB
LWHPS2FPGAREGS	Lightweight HPS-to-FPGA bridge GPV	0xFF400000	1 MB
HPS2FPGAREGS	HPS-to-FPGA bridge GPV	0xFF500000	1 MB
FPGA2HPSREGS	FPGA-to-HPS bridge GPV	0xFF600000	1 MB
EMAC0	EMAC0	0xFF700000	8 KB
EMAC1	EMAC1	0xFF702000	8 KB
SDMMC	SD/MMC	0xFF704000	4 KB
QSPIREGS	Quad SPI flash controller registers	0xFF705000	4 KB
FPGAMGRREGS	FPGA manager registers	0xFF706000	4 KB
ACPIDMAP	ACP ID mapper registers	0xFF707000	4 KB
GPIO0	GPIO0	0xFF708000	4 KB
GPIO1	GPIO1	0xFF709000	4 KB
GPIO2	GPIO2	0xFF70A000	4 KB
L3REGS	L3 interconnect GPV	0xFF800000	1 MB
NANDDATA	NAND controller data	0xFF900000	1 MB
QSPIDATA	Quad SPI flash data	0xFFA00000	1 MB
USBO	USBO OTG controller registers	0xFFB00000	256 KB
USB1	USB1 OTG controller registers	0xFFB40000	256 KB
NANDREGS	NAND controller registers	0xFFB80000	64 KB
FPGAMGRDATA	FPGA manager configuration data	0xFFB90000	4 KB
CAN0	CAN0 controller registers	0xFFC00000	4 KB
CAN1	CAN1 controller registers	0xFFC01000	4 KB
UART0	UART0	0xFFC02000	4 KB
UART1	UART1	0xFFC03000	4 KB
I2C0	I2C0	0xFFC04000	4 KB
I2C1	I2C1	0xFFC05000	4 KB
I2C2	I2C2	0xFFC06000	4 KB
I2C3	I2C3	0xFFC07000	4 KB
SPTIMER0	SP Timer0	0xFFC08000	4 KB
SPTIMER1	SP Timer1	0xFFC09000	4 KB
SDRREGS	SDRAM controller subsystem registers	0xFFC20000	128 KB
OSC1TIMERO	OSC1 Timer0	0xFFD00000	4 KB
OSC1TIMER1	OSC1 Timer1	0xFFD01000	4 KB
L4WD0	Watchdog0	0xFFD02000	4 KB
L4WD1	Watchdog1	0xFFD03000	4 KB
CLKMGR	Clock manager	0xFFD04000	4 KB
RSTMGR	Reset manager	0xFFD05000	4 KB
SYSMGR	System manager	0xFFD08000	16 KB
DMANONSECURE	DMA nonsecure registers	0FFE00000	4 KB
DMASECURE	DMA secure registers	0FFE01000	4 KB
SPISO	SPI slave0	0FFE02000	4 KB
SPIS1	SPI slave1	0FFE03000	4 KB
SPIMO	SPI master0	0FFF00000	4 KB
SPIM1	SPI master1	0FFF01000	4 KB

SCANMGR	Scan manager registers	0xFFFF02000	4 KB
ROM	Boot ROM	0xFFFFD0000	64 KB
MPUSCU	MPU SCU registers	0xFFFFEC000	8 KB
MPUL2	MPU L2 cache controller registers	0xFFFFEF000	4 KB
OCRAM	On-chip RAM	0xFFFFF0000	64 KB

Table 6-3. HPS Peripheral Region Address Map [2, pp. 1-16]

The programming model for accessing the HPS peripherals in Table 6-3 is the same as for peripherals created on the FPGA fabric. That is, every peripheral has a base address at which a certain number of registers can be found. You can then read and write to a certain set of these registers in order to modify the peripheral's behavior.

When using a HPS peripheral in Table 6-3, you do not need to hard-code any base address or peripheral register map in your programs, as Altera provides a header file for each one.

Two directories contain all **HPS**-related **HEADER FILES**:

1. "<altera_install_directory>/<version>/embedded/ip/altera/hps/altera_hps/hwlib/include"

Contains **HIGH-LEVEL** header files that typically contain a few **FUNCTIONS** which facilitate control over the HPS components.
2. "<altera_install_directory>/<version>/embedded/ip/altera/hps/altera_hps/hwlib/include/socal"

Contains **LOW-LEVEL** header files that provide a peripheral's **BIT-LEVEL REGISTER DETAILS**. For example, any bits in a peripheral's register that correspond to undefined behavior will be specified in these header files.

To illustrate the differences among the high and low-level header files, we can compare the ones related to the FPGA manager peripheral:

1. ".../hwlib/include/alt_fpga_manager.h"


```
ALT_STATUS_CODE alt_fpga_reset_assert(void);
ALT_STATUS_CODE alt_fpga_configure(const void* cfg_buf, size_t cfg_buf_len);
```
2. ".../hwlib/include/socal/alt_fpgamgr.h"


```
/* The width in bits of the ALT_FPGAMGR_CTL_EN register field. */
#define ALT_FPGAMGR_CTL_EN_WIDTH          1
/* The mask used to set the ALT_FPGAMGR_CTL_EN register field value. */
#define ALT_FPGAMGR_CTL_EN_SET_MSK        0x00000001
/* The mask used to clear the ALT_FPGAMGR_CTL_EN register field value. */
#define ALT_FPGAMGR_CTL_EN_CLR_MSK        0xfffffffffe
```

An *important* header file is ".../hwlib/include/socal/hps.h". It contains the HPS component's full **REGISTER MAP**, as provided in Table 6-3.

Note however, that there exists **NO HEADER FILE** for the "*heavyweight*" HPS-to-FPGA bridge, as it is not located in the "HPS peripherals" region in Figure 6-3. Indeed, the "*heavyweight*" HPS-to-FPGA bridge is not considered a HPS peripheral, whereas the "*lightweight*" HPS-to-FPGA bridge is. Therefore, in order to use the "*heavyweight*" HPS-to-FPGA bridge, you will have to define a macro in your code, as follows:

```
#define ALT_HWPGASLVS_OFST    0xc0000000
```

The reason why the "*lightweight*" HPS-to-FPGA bridge is considered a HPS peripheral may be related to the fact that it has a fixed 32-bit bus width (coincidence that this corresponds to the HPS' native data size?)

6.6 HPS BOOTING AND FPGA CONFIGURATION

Before being able to use the Cyclone V SoC, one needs to understand how the HPS boots and how the FPGA is configured. We'll first take a look at the ordering between the HPS and FPGA.

6.6.1 HPS Boot and FPGA Configuration Ordering

The **HPS BOOT** starts when the processor is released from reset (for example, on power up) and executes code in the internal *boot ROM* at the reset exception address. The boot process ends when the code in the boot ROM jumps to the next stage of the boot software. This next stage of the boot software is referred to as the *preloader*. Figure 6-4 illustrates this *initial incomplete* HPS boot flow.

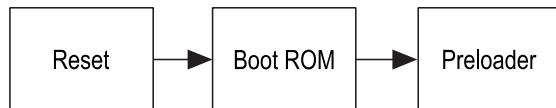


Figure 6-4. Simplified HPS Boot Flow [2, pp. A-3]

The processor can boot from the following sources:

- NAND flash memory through the NAND flash controller
- SD/MMC flash memory through the SD/MMC flash controller
- SPI and QSPI flash memory through the QSPI flash controller using *Slave Select 0*
- FPGA fabric on-chip memory

The choice of the boot source is done by modifying the *BOOTSEL* and *CLKSEL* values **BEFORE THE DEVICE IS POWERED UP**. Therefore, the Cyclone V device normally uses a **PHYSICAL DIP SWITCH** to configure the *BOOTSEL* and *CLKSEL*.

The DE1-SoC can ONLY BOOT from SD/MMC flash memory, as its BOOTSEL and CLKSEL values are hard-wired on the board. Although its HPS contains all necessary controllers, the board doesn't have a physical DIP switch to modify the BOOTSEL and CLKSEL values. The actual location of the DIP switch is present underneath the board, as can be seen in Figure 5-3, but a switch isn't soldered.

CONFIGURATION OF THE FPGA portion of the device starts when the FPGA portion is released from reset state (for example, on power up). The control block (CB) in the FPGA portion of the device is responsible for obtaining an FPGA configuration image and configuring the FPGA. The FPGA configuration ends when the configuration image has been fully loaded and the FPGA enters user mode. The FPGA configuration image is provided by users and is typically stored in non-volatile flash-based memory. The FPGA CB can obtain a configuration image from the HPS through the FPGA manager, or from another external source, such as the *Quartus II Programmer*.

The following three figures illustrate the possible HPS boot and FPGA configuration schemes.

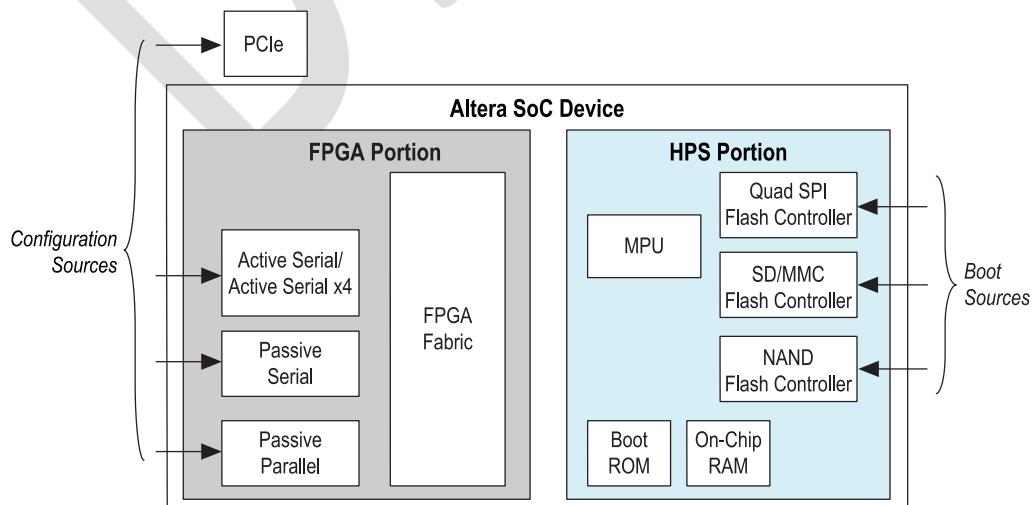


Figure 6-5. Independent FPGA Configuration and HPS Booting [2, pp. A-2]

Figure 6-5 shows the scheme where the FPGA configuration and the HPS boot occur independently. The FPGA configuration obtains its image from a non-HPS source (*Quartus II Programmer*), while the HPS boot obtains its configuration image from a non-FPGA fabric source.

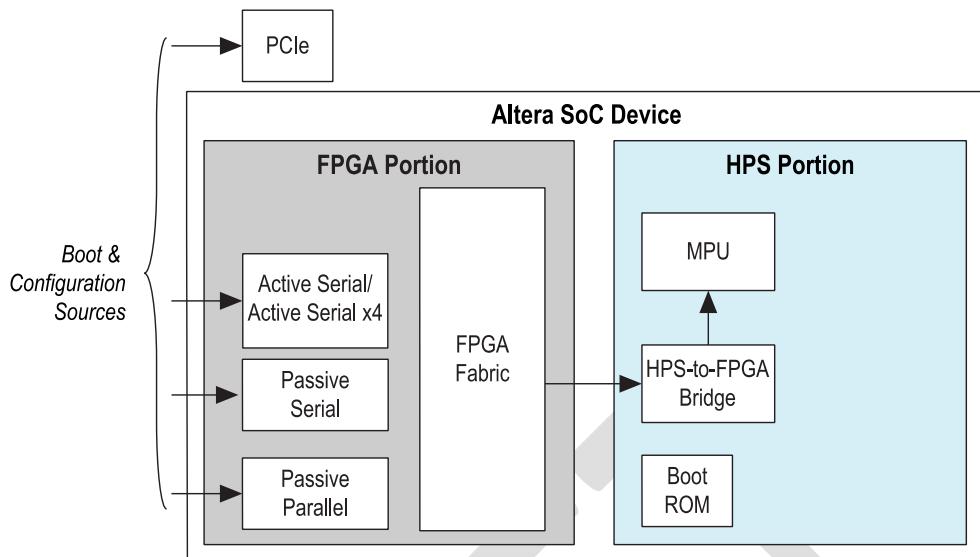


Figure 6-6. FPGA Configuration before HPS Booting (HPS boots from FPGA) [2, pp. A-2]

Figure 6-6 shows the scheme where the FPGA is first configured through the *Quartus II Programmer*, then the HPS boots from the FPGA fabric. The HPS boot waits for the FPGA fabric to be powered on and in user mode before executing. The HPS boot ROM code executes the preloader from the FPGA fabric over the HPS-to-FPGA bridge. The preloader can be obtained from the FPGA on-chip memory, or by accessing an external interface (such as a larger external SDRAM).

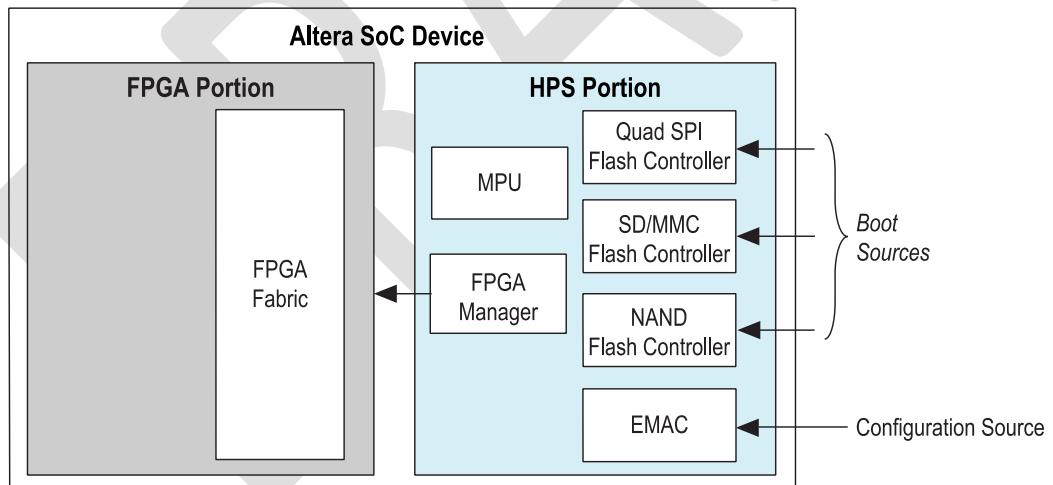


Figure 6-7. HPS Boots and Performs FPGA Configuration [2, pp. A-3]

Figure 6-7 shows the scheme under which the HPS first boots from one of its non-FPGA fabric boot sources, then software running on the HPS configures the FPGA fabric through the FPGA manager. The software on the HPS obtains the FPGA configuration image from any of its flash memory devices or communication interfaces, such as the SD/MMC memory, or the Ethernet port. The software is provided by users and the boot ROM is not involved in configuring the FPGA fabric.

6.6.2 Zooming In On the HPS Boot Process

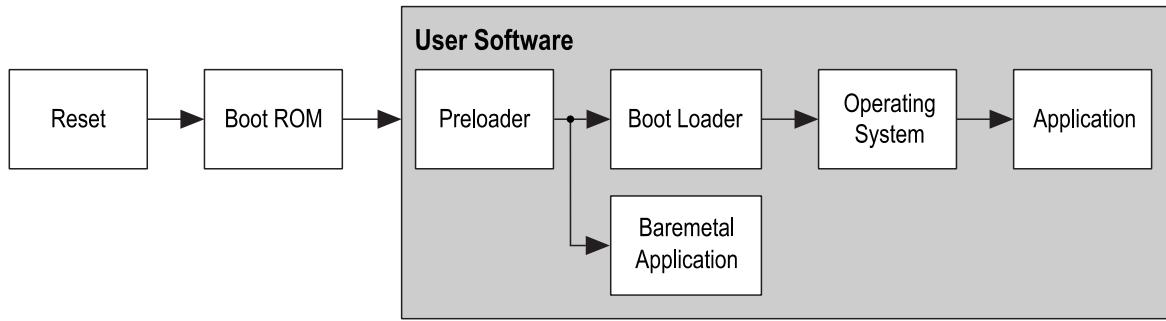


Figure 6-8. HPS Boot Flows [2, pp. A-3]

Booting software on the HPS is a multi-stage process. Each stage is responsible for loading the next stage. The first software stage is the *boot ROM*. The boot ROM code locates and executes the second software stage, called the *preloader*. The preloader locates, and **IF PRESENT**, executes the next software stage. The preloader and subsequent software stages are collectively referred to as *user software*.

The *reset*, *boot ROM*, and *preloader* stages are always present in the HPS boot flow. What comes after the preloader then depends on the type of application you want to run. The HPS can execute 2 types of applications:

- Bare-metal applications (no operating system)
- Applications on top of an operating system (Linux)

Figure 6-8 shows the HPS' available boot flows. The *Reset* and *Boot ROM* stages are the only *fixed* parts of the boot process. Everything in the *user software* stages can be *customized*.

Although the DE1-SoC has a DUAL-processor HPS, CPU1 is under reset, and the boot flow only executes on CPU0. If you want to use both processors of the DE1-SoC, then USER SOFTWARE executing on CPU0 is responsible for releasing CPU1 from reset.

6.6.2.1 Preloader

The preloader is one of the most important boot stages. It is actually what one would call the boot “source”, as all stages before it are unmodifiable. The preloader can be stored on external flash-based memory, or in the FPGA fabric.

The preloader typically performs the following actions:

- Initialize the SDRAM interface
- Configure the HPS I/O through the scan manager
- Configure pin multiplexing through the system manager
- Configure HPS clocks through the clock manager
- Initialize the flash controller (NAND, SD/MMC, QSPI) that contains the next stage boot software
- Load the next boot software into the SDRAM and pass control to it

The preloader does **NOT** release CPU1 from reset. The subsequent stages of the boot process are responsible for it if they want to use the extra processor.

7 USING THE CYCLONE V – POSSIBLE CONFIGURATIONS

7.1 INTRODUCTION

The HPS component is a **SOFT** component, but it does **NOT** mean that the HPS is a softcore processor. In fact, the HPS exclusively contains **HARD LOGIC**. The reason it is considered a softcore component originates from the fact that it enables other soft components to interface with the HPS hard logic. As such, the HPS component has a *small footprint* in the FPGA fabric, as its only purpose is to connect the soft and hard logic together.

Therefore, it is possible to use the Cyclone V SoC in 3 different configurations:

- FPGA-only
- HPS-only
- HPS & FPGA

We will look at the *FPGA-only* and *HPS & FPGA* configurations below. We will not cover the *HPS-only* configuration as it is identical to the *HPS & FPGA* one where you simply don't load any design on the FPGA fabric. The configurations using the HPS are more difficult to set up than the *FPGA-only* one.

7.2 FPGA-ONLY

Exclusively using the FPGA part of the Cyclone V is easy, as the design process is identical to any other Altera FPGA. You can build a complete design in *Quartus II & Qsys*, simulate it in *ModelSim-Altera*, then program the FPGA through the *Quartus II Programmer*. If you instantiated a Nios II processor in *Qsys*, you can use the *Nios II SBT IDE* to develop software for the processor.

The DE1-SoC has a lot of pins, which makes it tedious to start an FPGA design. It is recommended to use the **ENTITY** in Figure 10-1 for your **TOP-LEVEL VHDL FILE**, as it contains all the board's FPGA and HPS pins.

After having defined a top-level module, it is necessary to map your design's pins to the ones available on the DE1-SoC. The **TCL SCRIPT** in Figure 10-2 can be executed in *Quartus II* to specify the board's device ID and all its **PIN ASSIGNMENTS**. In order to execute the TCL script, place it in your quartus working directory, then run it through the “Tools > Tcl Scripts...” menu item in *Quartus II*.

7.3 HPS & FPGA

7.3.1 Choosing the Type of Application

7.3.1.1 Bare-metal Application

On one hand, bare-metal software enjoys the advantage of having no OS overhead. This has many consequences, the most visible of which are that code executes at native speed as no context switching is ever performed, and additionally, that code can directly address the HPS peripherals using their **PHYSICAL** memory-mapped addresses, as no virtual memory system is being used. This is very useful when trying to use the HPS as a high-speed microcontroller. Such a programming environment is very similar to the one used by other microcontrollers, like the TI MSP430.

On the other hand, bare-metal code has one great disadvantage, as the programmer must continue to configure the Cyclone V to use all its resources. For example, we saw in 6.6.2.1 that the preloader does not release CPU1 from reset, and that it is up to the *user software* to perform this, which is the bare-metal application itself in this case. Furthermore, supposing CPU1 is available for use, it is still difficult to run multi-threaded code, as an OS generally handles program scheduling and CPU affinity for the programmer. The programmer must now manually assign code fragments to each CPU.

7.3.1.2 Application Over an Operating System (Linux)

Running code over a Linux operating system has several advantages. First of all, the kernel releases CPU1 from reset upon boot, so all processors are available. Furthermore, the kernel initializes and makes most, if not all HPS peripherals available for use by the programmer. This is possible since the Linux kernel has access to a huge amount of device drivers. Multi-threaded code is also much easier to write, as the programmer has access to the familiar Pthreads system calls. Finally, the Linux kernel is not restricted to running compiled C programs. Indeed, you can always run code written in another programming language providing you first install the runtime environment required.

However, running an “**EMBEDDED**” application on top of an operating system also has disadvantages. Due to the virtual memory system put in place by the OS, a program cannot directly access the HPS peripherals through their physical memory-mapped addresses. Instead, one first needs to map the physical addresses of interest into the running program’s virtual address space. Only then will it be possible to access a peripheral’s registers.

At the end of the day, bare-metal applications and applications running code on top of Linux can do the same things. Generally speaking, programming on top of Linux is superior and much easier compared to bare-metal code, as its advantages greatly outweigh its drawbacks.

8 USING THE CYCLONE V - HANDS-ON DEVELOPMENT TUTORIAL

8.1 GOALS

Let's start by defining what we want to achieve. We want to create a system in which both the HPS and FPGA can do some computation simultaneously. More specifically, we want the following capabilities:

1. A Nios II processor on the **FPGA** must be able to use the 10 LEDs and 10 switches connected to the **FPGA PORTION** of the device. The Nios II processor will create a strobing light effect on the 10 LEDs, with the 10 switches acting as enable signals for the corresponding LEDs.
2. The Nios II processor will use its SDRAM instead of any form of on-chip memory.
3. The **HPS** must be able to use the LED and button that are directly connected to the **HPS PORTION** of the device. Pressing the button should toggle the LED.
4. The **HPS** must be able to use 2 buttons and the six 7-segment displays connected to the **FPGA PORTION** of the device. The HPS will increment and decrement a counter that will be shown on the 7-segment displays. Pressing the first button should invert the counting direction, and pushing the second button should reset the counter to 0.

8.2 PROJECT STRUCTURE

The development process creates a lot more files compared to an FPGA-only design. We will use the folder structure shown in Figure 8-1 to organize our project. In this demo, we will use “DE1_SoC_demo” as the project name.

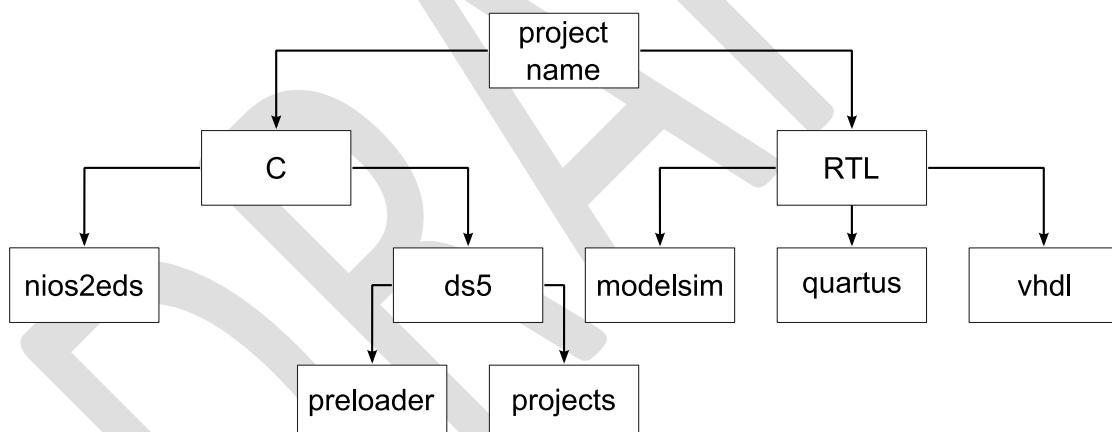


Figure 8-1. Project Folder Structure

A few steps have to be taken in order to configure the Cyclone V before you can use the HPS. The **HARDWARE** design steps are **IDENTICAL** whether you want to write bare-metal applications, or Linux HPS applications. Only the **SOFTWARE** steps **DIFFER** for the **HPS (FPGA SOFTWARE)** is **IDENTICAL**.

8.3 HARDWARE

The details below give step-by-step instructions to create a full system from scratch.

8.3.1 General Quartus II Setup

1. Create a new *Quartus II* project. You only need to specify the project name and destination, as all other settings will be set at a later stage by a TCL script. For this demo, we will call our project “DE1_SoC_demo” and will store it in “DE1_SoC_demo/RTL/quartus”.
2. Download \\lapsrv1.epfl.ch\documentation\Altera\CycloneV\Distribution\DE1_SoC_top_level.vhd and save it in “DE1_SoC_demo/RTL/vhdl1”. We will use this file as the project’s top-level VHDL file, as it contains a complete list of pin names available on the DE1-SoC for use in your designs. Add the file

to the *Quartus II* project by using “Tools > Add/Remove Files in Project...” and set it as your design’s top-level entity.

3. Download \\lapsrv1.epfl.ch\documentation\Altera\CycloneV\Distribution\pin_assignment_DE1_SoC.tcl and save it in “DE1_SoC_demo/RTL/quartus”. This script assigns pin locations and I/O standards to all pins names in “DE1_SoC_top_level.vhd”. Execute the TCL script by using “Tools > Tcl Scripts...” in *Quartus II*.

At this stage, all general *Quartus II* settings have been performed, and we can start creating our design. We want to use the HPS, as well as a Nios II processor in our design, so we will use the *Qsys* tool to create the system.

4. Launch the *Qsys* tool and create a new system. Save it under the name “soc_system.qsys”.

8.3.2 System Design with Qsys – Nios II

In this section, we assemble all system components needed to allow the a Nios II processor to create a strobing light effect on the 10 LEDs with the 10 switches acting as enable signals for the corresponding LEDs.

We want to use a Nios II processor with an SDRAM. To use an SDRAM, we need 2 things:

- An SDRAM controller.
- A PLL to generate a clock for the softcore SDRAM controller and a phase-shifted clock for the off-chip SDRAM component. The reference clocks and timings needed for the SDRAM can be found on its datasheet: [\\lapsrv1.epfl.ch\documentation\Altera\CycloneV\Documentation\terasic\DE1-SoC \(Revision B Board\) System CD\Datasheet\SDRAM\IS42R16320D.pdf](\\lapsrv1.epfl.ch\documentation\Altera\CycloneV\Documentation\terasic\DE1-SoC (Revision B Board) System CD\Datasheet\SDRAM\IS42R16320D.pdf)

5. Add an “Altera PLL” to the system.

- Reference Clock Frequency: 50 MHz
- Operation Mode: normal
- Uncheck “Enable locked output port”

We need to generate 3 clocks:

- 50 MHz clock for the Nios II processor and all its peripherals.
- 100 MHz clock for the SDRAM controller.
- 100 MHz, -3758 ps phase-shifted clock for the off-chip SDRAM component.

In *Qsys*’ “System Contents” tab:

- Export “pll_0.outclk2” under the name “pll_0_sdram”. This clock will be used for the off-chip SDRAM component.

6. Add an softcore SDRAM controller to the system. Use the following settings (taken from the SDRAM’s datasheet):

- Memory Profile
 - Data Width
 - Bits: 16
 - Architecture
 - Chip select: 1
 - Banks: 4
 - Address Width
 - Row: 13
 - Column: 10
- Timing
 - CAS latency cycles: 3
 - Initialization refresh cycles: 2
 - Issue one refresh command every: 7.8125 us

- Delay after powerup, before initialization: 100.0 us
- Duration of refresh command (t_rfc): 70.0 ns
- Duration of precharge command (t_rp): 15.0 ns
- ACTIVE to READ or WRITE delay (t_rcd): 15.0 ns
- Access time (t_ac): 5.4 ns
- Write recovery time (t_wr, no auto precharge): 14.0 ns

In Qsys' "System Contents" tab:

- Rename "new_sdram_controller_0" to "sdram_controller_0".
- Export "sdram_controller_0.wire".

7. Add a Nios II processor to the system. You can choose any variant (Nios II/e, Nios II/s, or Nios II/f).
8. Add a JTAG UART to the system. This will be used to be able to use the `printf()` function when programming the Nios II processor.
9. Connect the system as shown in Figure 8-2 below:

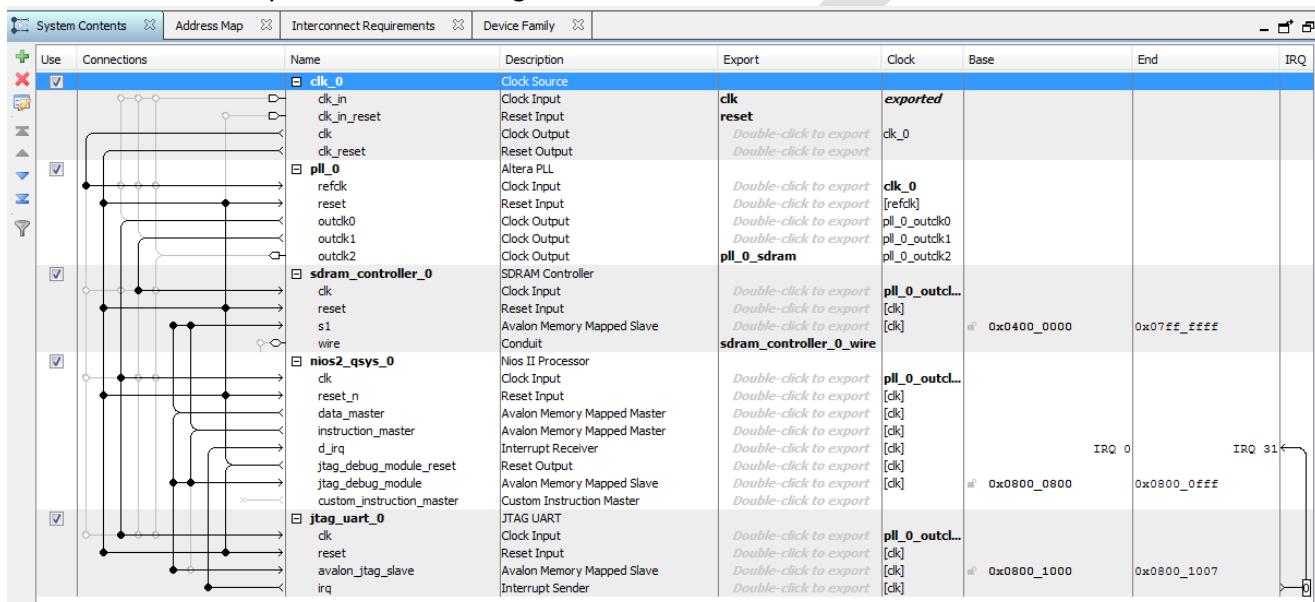


Figure 8-2. Basic Nios II System with SDRAM and JTAG UART

10. Edit the Nios II processor and set "sdram_controller_0.s1" as its Reset and Exception vectors.
11. Add a PIO component to the system for the LEDs. The DE1-SoC has 10 LEDs, so we will use a 10-bit PIO component.

- Width: 10 bits
- Direction: Output
- Output Port Reset Value: 0x00

In Qsys' "System Contents" tab:

- Rename the component to "leds_0"
- Export "leds_0.external_connection"

12. Add a PIO component to the system for the switches. The DE1-SoC has 10 Switches, so we will again use a 10-bit PIO component.
- Width: 10 bits
- Direction: Input

In Qsys' "System Contents" tab:

- Rename the component to "switches_0"
- Export "switches_0.external_connection"

13. Connect the system as shown in Figure 8-3 below:

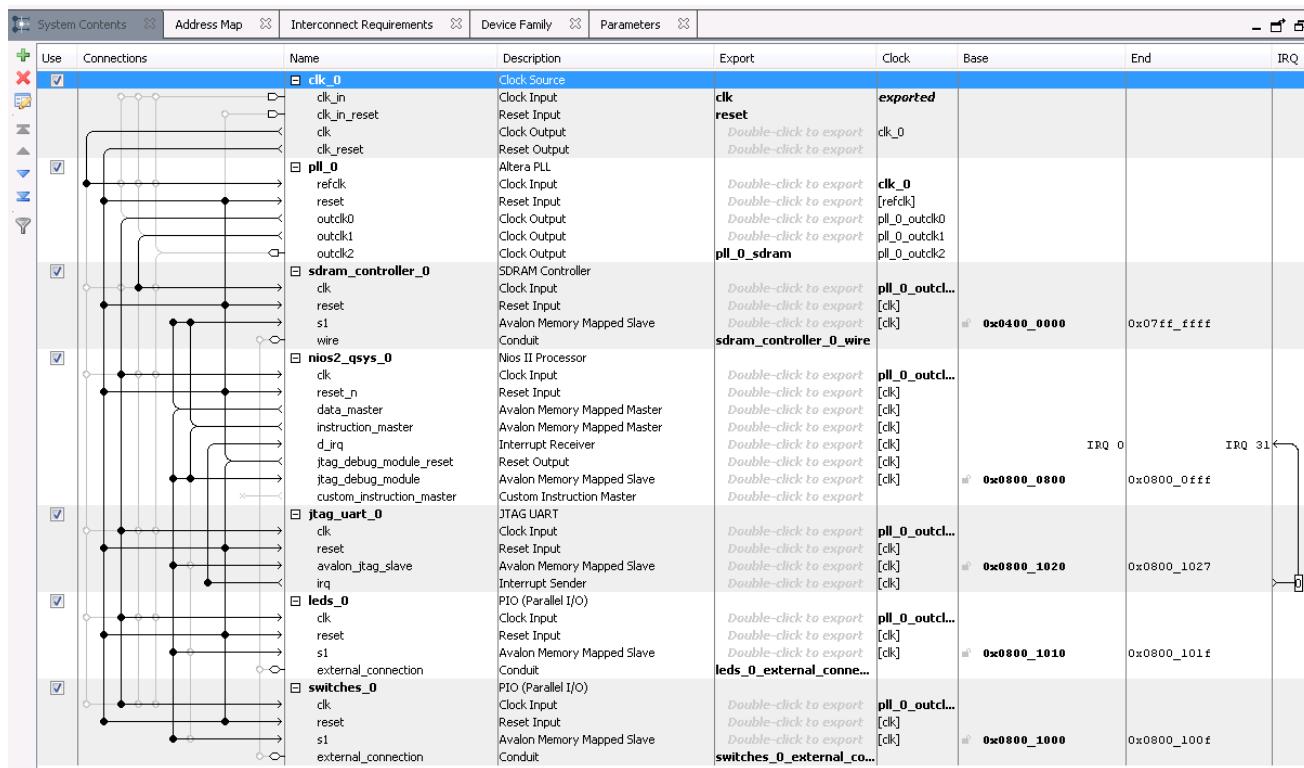


Figure 8-3. Adding LEDs and Switches to the System

At this stage, we have created a system that satisfies goals 1 and 2 defined in 8.1.

8.3.3 System Design with Qsys – HPS

In this section, we assemble all system components needed to allow the HPS to access a button and LED connected directly to itself, as well as a button and the 7-segment displays connected to the FPGA portion of the device.

Note: When using Qsys to manipulate any signal or menu item related to the HPS, the GUI will seem as though it is not responding. However, it is not the case and it is just checking all parameters in the background, which makes the GUI hang momentarily. It is working correctly behind the scenes.

8.3.3.1 Instantiating the HPS Component

14. To use the HPS, add an “Arria V/Cyclone V Hard Processor System” to the system.
15. Open the HPS’ parameters and have a look around. There are 4 tabs that control various aspects of the HPS’ behaviour, as shown on Figure 8-4.

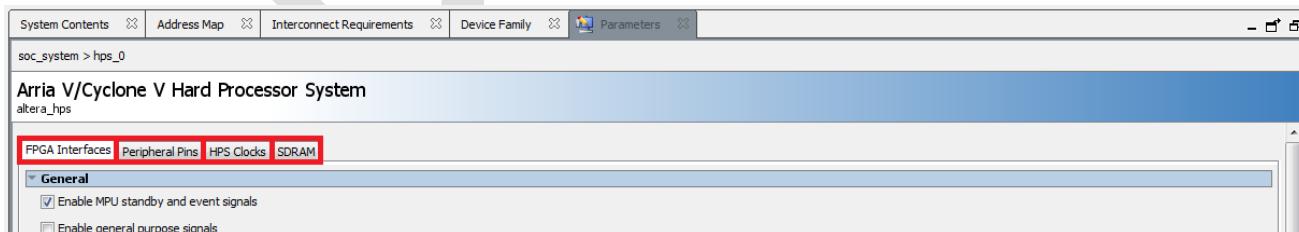


Figure 8-4. HPS Component Parameters

8.3.3.1.1 FPGA Interfaces Tab

This tab configures everything related to the interfaces between the HPS and the FPGA. You can configure which bridges to use, interrupts, ...

16. We want to use the HPS to access FPGA peripherals, so we need to enable one of the following buses:
 - HPS-to-FPGA AXI bridge
 - Lightweight HPS-to-FPGA AXI bridge

Since we are not going to be using any high performance FPGA peripherals in this demo, we'll choose to enable the Lightweight HPS-to-FPGA AXI bridge.

- Set the FPGA-to-HPS interface width to “Unused”.
- Set the HPS-to-FPGA interface width to “Unused”.

By default, Qsys checks “Enable MPU standby and event signals”, but we are not going to use this feature, so

- Uncheck “Enable MPU standby and event signals”.

Qsys also adds an FPGA-to-HPS SDRAM port by default, which we are not going to use either, so

- Remove the port listed under “FPGA-to-HPS SDRAM Interface”.

8.3.3.1.2 Peripheral Pins Tab

This tab configures the physical pins that are available on the device. Most device pins have various sources, and are *multiplexed*. The pins can be configured to be sourced by the FPGA, or by various HPS peripherals.

17. We want to use the HPS to access the button and LED that are directly connected to it. These HPS peripherals correspond to pins “HPS_KEY” and “HPS_LED” on the device’s top-level entity. We need to know how these 2 pins are connected to the HPS to access them. To find out this information, we have to look at the board’s schematics. You can find the schematics

at [\\lapsrv1.epfl.ch\documentation\Altera\CycloneV\Documentation\terasic\DE1-SoC \(Revision B Board\) System CD\Schematic\DE1-SoC.pdf](\\lapsrv1.epfl.ch\documentation\Altera\CycloneV\Documentation\terasic\DE1-SoC (Revision B Board) System CD\Schematic\DE1-SoC.pdf).

The right side of Figure 8-5 shows the area of interest on the DE1-SoC’s schematics. We see that “HPS_KEY” and “HPS_LED” are respectively connected to pins G21 and A24.



Figure 8-5. HPS_KEY & HPS_LED on DE1-SoC Schematic

Figure 8-5 allows us to explain what Qsys’ *Peripheral Pins* tab does. The Qsys GUI doesn’t make any reference to pins G21 and A24, as they depend on the device being used, and cannot be generalized to other Cyclone V devices. However, the GUI does have references to what is displayed on the left side of Figure 8-5. We will examine the details of pin G21, to which “HPS_KEY” is connected. The schematic shows that pin G21 is connected to 4 sources:

- TRACE_D5
- SPIS1_MOSI
- CAN1_TX
- HPS_GPIO54

This can be seen in Qsys, as shown in Figure 8-6.

TRACE_D4	CAN1_RX (Set0)	SPIS1_CLK (Set0)	TRACE_D4 (Set0)	GPIO53	LOANIO53
TRACE_D5	CAN1_TX (Set0)	SPIS1_MOSI (Set0)	TRACE_D5 (Set0)	GPIO54	LOANIO54

Figure 8-6. HPS_KEY & HPS_LED on Qsys Peripheral Pins Tab

Depending on how you configure the Peripheral Pins tab, you can configure pin G21 to use any of the sources above. For example, if you want to use this pin as an SPI slave control signal, you would use the configuration shown in Figure 8-7.

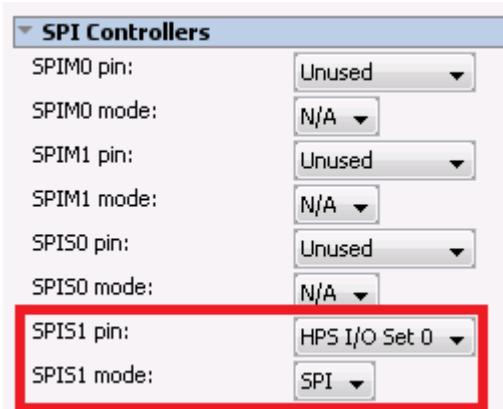


Figure 8-7. Using Pin G21 for SPI

However, if you don't want to use any of the peripherals available at the top of the *Peripheral Pins* tab, then you can always use one of the 2 buttons on the right side of Figure 8-6:

- **GPIOX_Y**: Configures the pin to be connected to the **HPS' GPIO** peripheral.
- **LOANIOX_Y**: Configures the pin to be connected to the **FPGA** fabric. This pin can be exported from Qsys to be used by the FPGA.

In our case, we want the HPS to directly control “HPS_KEY” and “HPS_LED” and don't need any of the controllers listed above for pins G1 and A24. To do this, we will connect pins G21 and A24 to the HPS' GPIO peripheral.

- Click on the “GPIO53” and “GPIO54” buttons shown in Figure 8-6. You should obtain the situation shown in Figure 8-8.

TRACE_D3	I2C1.SCL (Set0)	SPIS0.SSO (Set0)	TRACE_D3 (Set0)	GPIO52	LOANIO52
TRACE_D4	CAN1.RX (Set0)	SPIS1.CLK (Set0)	TRACE_D4 (Set0)	GPIO53	LOANIO53
TRACE_D5	CAN1.TX (Set0)	SPIS1.MOSI (Set0)	TRACE_D5 (Set0)	GPIO54	LOANIO54
TRACE_D6	I2C0.SDA (Set0)	SPIS1.SSO (Set0)	TRACE_D6 (Set0)	GPIO55	LOANIO55

Figure 8-8. Using Pins G21 & A24 as GPIO

18. In Qsys' “System Contents” tab:

- Export “hps_0.hps_io” under the name “hps_0_io”. This is a conduit that contains all the pins configured in the *Peripheral Pins* tab. We will connect these to our top-level entity later.

8.3.3.1.3 HPS Clocks Tab

This tab configures the clocking system of the HPS. We will generally use the default settings here, so no need to change anything.

8.3.3.1.4 SDRAM Tab

This tab configures the memory subsystem of the HPS. Its name is misleading, as the HPS does **NOT** actually have any **SDRAM**, but rather some **DDR3** memory. This is just a graphical misnomer, as the settings all contain references to DDR2 or DDR3 memory. Be aware that the misnomer is repeated in many other parts of the Qsys interface as well.

19. We need to configure all clocks and timings related to the memory used on our system. The DE1-SoC uses DDR3 memory, so we need to consult its datasheet to find all the settings. The datasheet is available at [\\lapsrv1.epfl.ch\\documentation\\Altera\\CycloneV\\Documentation\\terasIC\\DE1-SoC_\(Revision B Board\) System CD\\Datasheet\\DDR3 SDRAM\\43TR16256A-85120AL\(ISSI\).pdf](http://lapsrv1.epfl.ch/documentation/Altera/CycloneV/Documentation/terasIC/DE1-SoC_(Revision_B_Board)_System_CD/Datasheet/DDR3_SDRAM/43TR16256A-85120AL(ISSI).pdf). Based on the

memory's datasheet, we can fill in the following memory settings (you will soon see that it is quite tedious to enter these values):

- SDRAM Protocol: DDR3
- PHY Settings:
 - Clocks:
 - Memory clock frequency: 400.0 MHz
 - PLL reference clock frequency: 25.0 MHz
 - Advanced PHY Settings:
 - Supply Voltage: 1.5V DDR3
- Memory Parameters:
 - Memory vendor: Micron
 - Memory device speed grade: 800.0 MHz
 - Total interface width: 32
 - Number of chip select/depth expansion: 1
 - Number of clocks: 1
 - Row address width: 15
 - Column address width: 10
 - Bank-address width: 3
 - Enable DM pins
 - DQS# Enable
 - Memory Initialization Options:
 - Mirror Addressing: 1 per chip select: 0
 - Mode Register 0:
 - Burst Length: Burst chop 4 or 8 (on the fly)
 - Read Burst Type: Sequential
 - DLL precharge power down: DLL off
 - Memory CAS latency setting: 11
 - Mode Register 1:
 - Output drive strength setting: RZQ/7
 - ODT Rtt nominal value: RZQ/4
 - Mode Register 2:
 - Auto selfrefresh method: Manual
 - Selfrefresh temperature: Normal
 - Memory write CAS latency setting: 8
 - Dynamic ODT (Rtt_WR) value: RZQ/4
- Memory Timing:
 - tIS (base): 180 ps
 - tIH (base): 140 ps
 - tDS (base): 30 ps
 - tDH (base): 65 ps
 - tDQSQ: 125 ps
 - tQH: 0.38 cycles
 - tDQSCK: 255 ps
 - tDQSS: 0.25 cycles
 - tQSH: 0.4 cycles
 - tDSH: 0.2 cycles
 - tDSS: 0.2 cycles
 - tINIT: 500 us
 - tMRD: 4 cycles
 - tRAS: 35.0 ns

- tRCD: 13.75 ns
- tRP: 13.75 ns
- tREFI: 7.8 us
- tRFC: 260.0 ns
- tWR: 15.0 ns
- tWTR: 4 cycles
- tFAW: 30.0 ns
- tRRD: 7.5 ns
- tRTP: 7.5 ns
- Board Settings:
 - Setup and Hold Derating:
 - Use Altera's default settings
 - Channel Signal Integrity:
 - Use Altera's default settings
 - Board Skews:
 - Maximum CK delay to DIMM/device: 0.03 ns
 - Maximum DQS delay to DIMM/device: 0.02 ns
 - Minimum delay difference between CK and DQS: 0.06 ns
 - Maximum delay difference between CD and DQS: 0.12 ns
 - Maximum skew within DQS group: 0.01 ns
 - Maximum skew between DQS groups: 0.06 ns
 - Average delay difference between DQ and DQS: 0.05 ns
 - Maximum skew within address and command bus: 0.02 ns
 - Average delay difference between address and command and CK: 0.01 ns

20. In Qsys' "System Contents" tab:

- Export "hps_0.memory" under the name "hps_0_ddr".

21. Connect the system as shown in Figure 8-9 below:

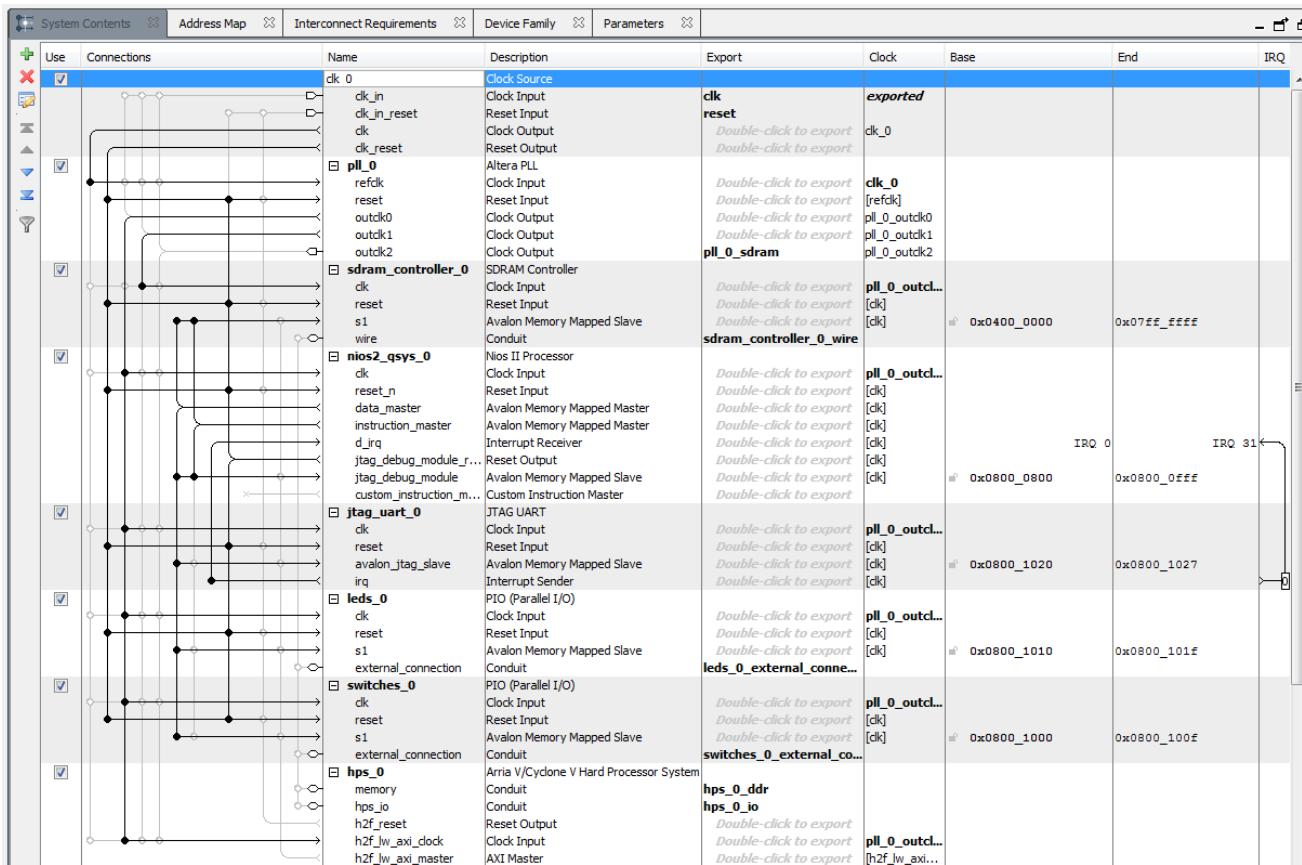


Figure 8-9. Adding the "Standalone" HPS to the System

At this stage, we have a functional HPS unit that can be programmed and that satisfies goals 1, 2, and 3 defined in 8.1. In our current system however, the HPS can only be used “standalone” and cannot access any FPGA peripherals.

8.3.3.2 Interfacing with FPGA Peripherals

The next step is to connect the HPS to FPGA peripherals through one of its interface bridges. The setup we have uses the Lightweight HPS-to-FPGA bridge to communicate with the FPGA.

22. Add a PIO component to the system for the buttons. The DE1-SoC has 4 buttons, so we will use a 4-bit PIO component.

- Width: 4 bits
- Direction: Input

In Qsys’ “System Contents” tab:

- Rename the component to “buttons_0”
- Export “buttons_0.external_connection”

23. Add a PIO component for one of the 7-segment displays. We will use a 7-bit PIO component.

- Width: 7 bits
- Direction: Output
- Output Port Reset Value: 0x7f

In Qsys’ “System Contents” tab:

- Rename the component to “hex_0”
- Export “hex_0.external_connection”

24. Repeat step 23 five more times to obtain a total of six 7-segment displays “hex_0”, “hex_1”, “hex_2”, “hex_3”, “hex_4”, and “hex_5”.

25. Connect the system as shown in Figure 8-10 below (we don't show the full system to make figures hold on one page). Notice that we use "hps_0.h2f_reset" as the reset signal for the components connected to the HPS. This is a design choice so we can separately reset FPGA-only peripherals, and FPGA peripherals connected to the HPS.

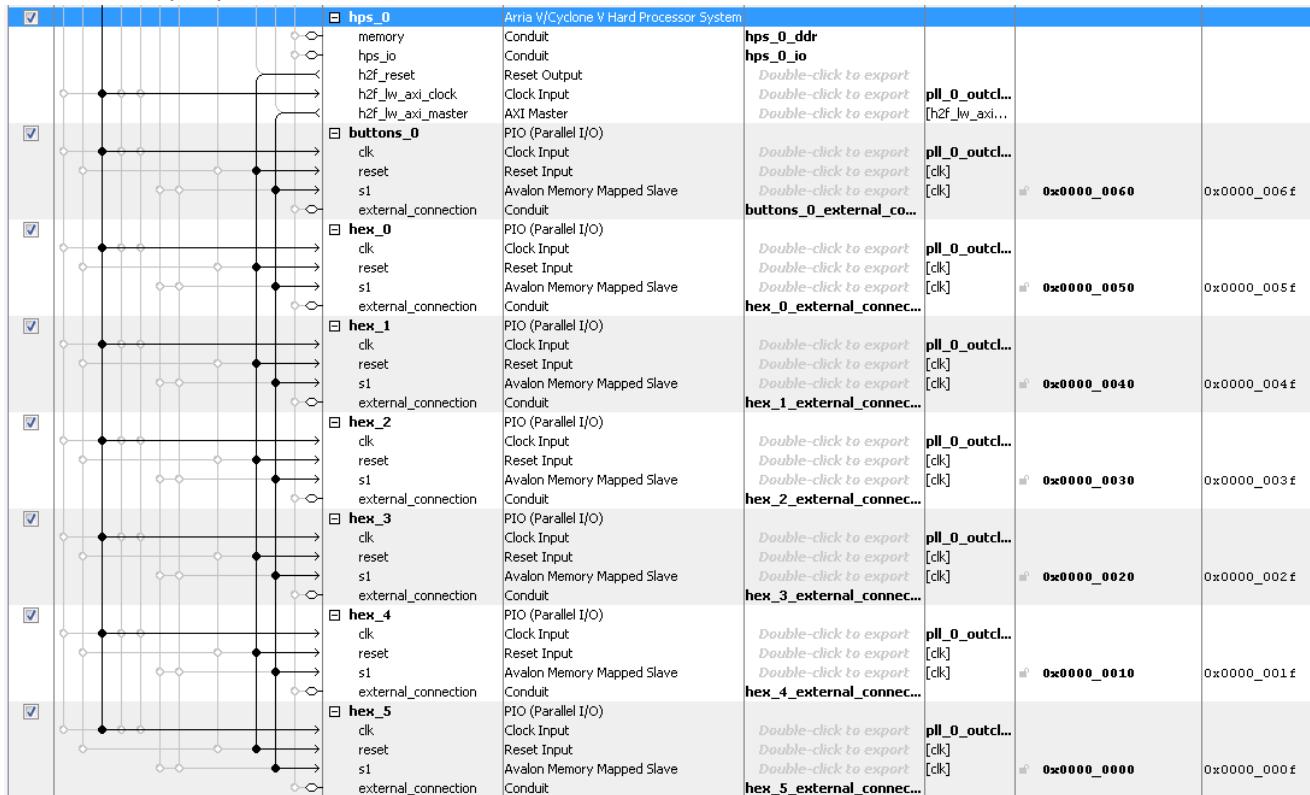


Figure 8-10. Adding Buttons and 7-segment Displays to the Lightweight HPS-to-FPGA Bridge

At this stage, we finally have a system that satisfies goals 1, 2, 3, and 4 defined in 8.1. Our design work with Qsys is now done.

8.3.4 Instantiating the Qsys System

26. Click on the “Generate HDL...” button and choose to generate VHDL files. This will create all the design files that are needed for the specified system.
27. You now have a complete Qsys system. The system will be available as an instantiable component in your design files. However, in order for Quartus II to see the Qsys system, you will have to add the system's files to your Quartus II project.
28. Add “DE1_SoC_demo/RTL/quartus/soc_system/synthesis/soc_system.qip” to the Quartus II project by using “Tools > Add/Remove Files in Project...”. This file contains references to all files generated by Qsys. Adding this single file is very handy, as it pulls in all other files with it. Without this file, you would have had to add every Qsys-generated file to Quartus II manually, which is in the order of hundreds!
29. To use the Qsys system in your design, you have to declare its component, and then instantiate it. Qsys already provides you with a component declaration. You can find it among the numerous files that were generated. The one we are looking for is “DE1_SoC_demo/RTL/quartus/soc_system/soc_system.cmp”.
30. Copy the component declaration code in “..../vhdl/DE1_SoC_top_level.vhd”. Be sure to instantiate the component and assign all the correct pins of the DE1-SoC board. For our demo project, we would use the instantiation shown in Figure 8-11.

```

soc_system_inst : component soc_system
    port map(buttons_0_external_connection_export  => KEY_N,
             clk_clk                                => CLOCK_50,

```

```

hex_0_external_connection_export    => HEX0_N,
hex_1_external_connection_export    => HEX1_N,
hex_2_external_connection_export    => HEX2_N,
hex_3_external_connection_export    => HEX3_N,
hex_4_external_connection_export    => HEX4_N,
hex_5_external_connection_export    => HEX5_N,
hps_0_ddr_mem_a                  => HPS_DDR3_ADDR,
hps_0_ddr_mem_ba                 => HPS_DDR3_BA,
hps_0_ddr_mem_ck                 => HPS_DDR3_CK_P,
hps_0_ddr_mem_ck_n               => HPS_DDR3_CK_N,
hps_0_ddr_mem_cke                => HPS_DDR3_CKE,
hps_0_ddr_mem_cs_n               => HPS_DDR3_CS_N,
hps_0_ddr_mem_ras_n              => HPS_DDR3_RAS_N,
hps_0_ddr_mem_cas_n              => HPS_DDR3_CAS_N,
hps_0_ddr_mem_we_n               => HPS_DDR3_WE_N,
hps_0_ddr_mem_reset_n            => HPS_DDR3_RESET_N,
hps_0_ddr_mem_dq                 => HPS_DDR3_DQ,
hps_0_ddr_mem_dqs                => HPS_DDR3_DQS_P,
hps_0_ddr_mem_dqs_n              => HPS_DDR3_DQS_N,
hps_0_ddr_mem_odt                => HPS_DDR3_ODT,
hps_0_ddr_mem_dm                 => HPS_DDR3_DM,
hps_0_ddr_oct_rzqin              => HPS_DDR3_RZQ,
hps_0_io_hps_io_gpio_inst_GPIO53 => HPS_LED,
hps_0_io_hps_io_gpio_inst_GPIO54 => HPS_KEY,
leds_0_external_connection_export => LEDR,
pll_0_sdram_clk                 => DRAM_CLK,
reset_reset_n                   => '1',
sdram_controller_0_wire_addr     => DRAM_ADDR,
sdram_controller_0_wire_ba       => DRAM_BA,
sdram_controller_0_wire_cas_n   => DRAM_CAS_N,
sdram_controller_0_wire_cke      => DRAM_CKE,
sdram_controller_0_wire_cs_n    => DRAM_CS_N,
sdram_controller_0_wire_dq       => DRAM_DQ,
sdram_controller_0_wire_dqm(1)   => DRAM_UDQM,
sdram_controller_0_wire_dqm(0)   => DRAM_LDQM,
sdram_controller_0_wire_ras_n   => DRAM_RAS_N,
sdram_controller_0_wire_we_n    => DRAM_WE_N,
switches_0_external_connection_export => SW);

```

Figure 8-11. Qsys Component Instantiation

31. After finishing the design, **REMOVE** all unused pins from the top-level VHDL file. Your top-level entity should look like the one shown in Figure 8-12.

```

entity DE1_SoC_top_level is
port(
  -- CLOCK
  CLOCK_50      : in  std_logic;

  -- SDRAM
  DRAM_ADDR      : out std_logic_vector(12 downto 0);
  DRAM_BA        : out std_logic_vector(1 downto 0);
  DRAM_CAS_N     : out std_logic;
  DRAM_CKE        : out std_logic;
  DRAM_CLK        : out std_logic;
  DRAM_CS_N      : out std_logic;
  DRAM_DQ        : inout std_logic_vector(15 downto 0);
  DRAM_LDQM      : out std_logic;
  DRAM_RAS_N     : out std_logic;
  DRAM_UDQM      : out std_logic;

```

```

        DRAM_WE_N      : out  std_logic;

        -- SEG7
        HEX0_N         : out  std_logic_vector(6 downto 0);
        HEX1_N         : out  std_logic_vector(6 downto 0);
        HEX2_N         : out  std_logic_vector(6 downto 0);
        HEX3_N         : out  std_logic_vector(6 downto 0);
        HEX4_N         : out  std_logic_vector(6 downto 0);
        HEX5_N         : out  std_logic_vector(6 downto 0);

        -- KEY_n
        KEY_N          : in   std_logic_vector(3 downto 0);

        -- LED
        LEDR           : out  std_logic_vector(9 downto 0);

        -- SW
        SW              : in   std_logic_vector(9 downto 0);

        -- HPS
        HPS_DDR3_ADDR  : out  std_logic_vector(14 downto 0);
        HPS_DDR3_BA    : out  std_logic_vector(2 downto 0);
        HPS_DDR3_CAS_N : out  std_logic;
        HPS_DDR3_CK_N  : out  std_logic;
        HPS_DDR3_CK_P  : out  std_logic;
        HPS_DDR3_CKE   : out  std_logic;
        HPS_DDR3_CS_N  : out  std_logic;
        HPS_DDR3_DM    : out  std_logic_vector(3 downto 0);
        HPS_DDR3_DQ    : inout std_logic_vector(31 downto 0);
        HPS_DDR3_DQS_N : inout std_logic_vector(3 downto 0);
        HPS_DDR3_DQS_P : inout std_logic_vector(3 downto 0);
        HPS_DDR3_ODT   : out  std_logic;
        HPS_DDR3_RAS_N : out  std_logic;
        HPS_DDR3_RESET_N: out  std_logic;
        HPS_DDR3_RZQ   : in   std_logic;
        HPS_DDR3_WE_N  : out  std_logic;
        HPS_KEY         : inout std_logic;
        HPS_LED         : inout std_logic
    );
end entity DE1_SoC_top_level;

```

Figure 8-12. Final Top-level Entity

8.3.5 HPS DDR3 Pin Assignments

In a normal FPGA design flow, you would be able to compile your design at this stage. However, this isn't possible at the moment in our design. The reason is that the HPS' DDR3 pins assignments have not been performed yet.

How is this possible? We said earlier that our TCL script assigns pin locations and I/O standards to all pins names in "DE1_SoC_top_level.vhd". The truth is that it assigns values for all pin names, except those related to the HPS' DDR3 memory. The reason is that the DDR3 pin assignments depend on how you parameterize the HPS memory timings in Qsys. Our TCL script could not have known what timings you were going to use, so it doesn't set those pin locations and I/O standards.

However, Qsys knows what the parameters are (since you provided it with all the necessary information), and it has generated a custom TCL script for the HPS DDR3 pin assignments.

32. Go to "Tools > Tcl Scripts..." in Quartus II.

IF AT THIS POINT YOU SEE THE SAME THING AS ON Figure 8-13 IN QUARTUS II, THEN CLOSE AND RELAUNCH QUARTUS II AGAIN. SOME VERSIONS OF QUARTUS II SUFFER FROM A BUG, WHERE THE PROGRAM DOESN'T CORRECTLY DETECT TCL FILES GENERATED BY QSYS. YOU SHOULD SEE THE SAME THING AS ON Figure 8-14.



Figure 8-13. HPS DDR3 Pin Assignment TCL Script Selection Bug

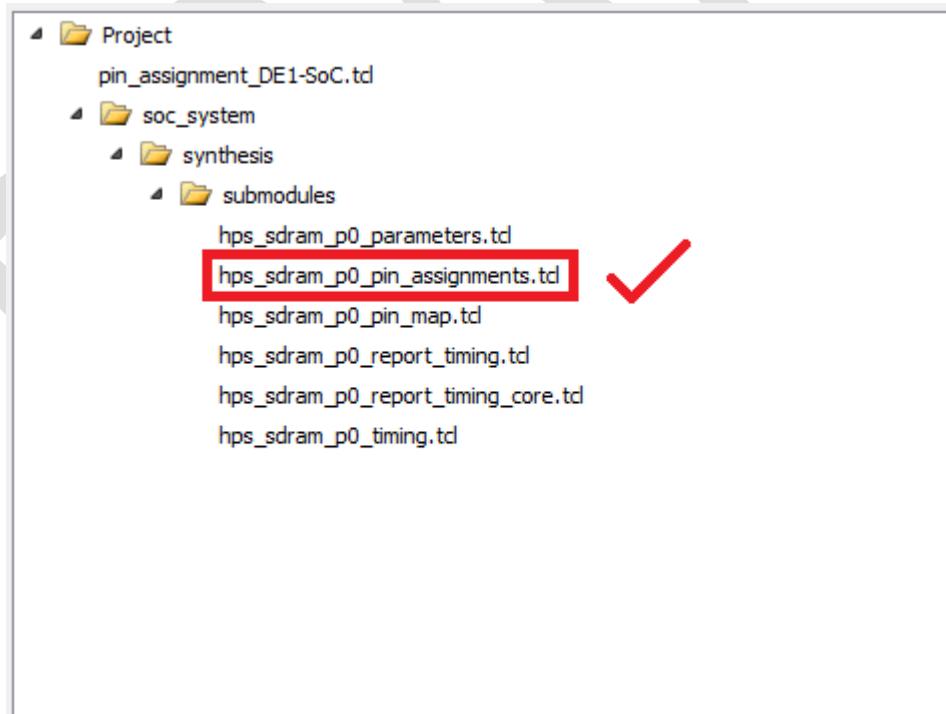


Figure 8-14. Correct HPS DDR3 Pin Assignment TCL Script Selection

33. Execute "hps_sdram_p0_pin_assignments.tcl".
34. You can now compile your design.

IF THE COMPILED FAILS, EXECUTE THE "hps_sdram_p0_pin_assignments.tcl" SCRIPT AGAIN AND RELAUNCH THE COMPILE PROCESS.

At this point, we have finished the hardware design process and can proceed to programming the FPGA.

8.3.6 Programming the FPGA

35. Open the *Quartus II Programmer*.

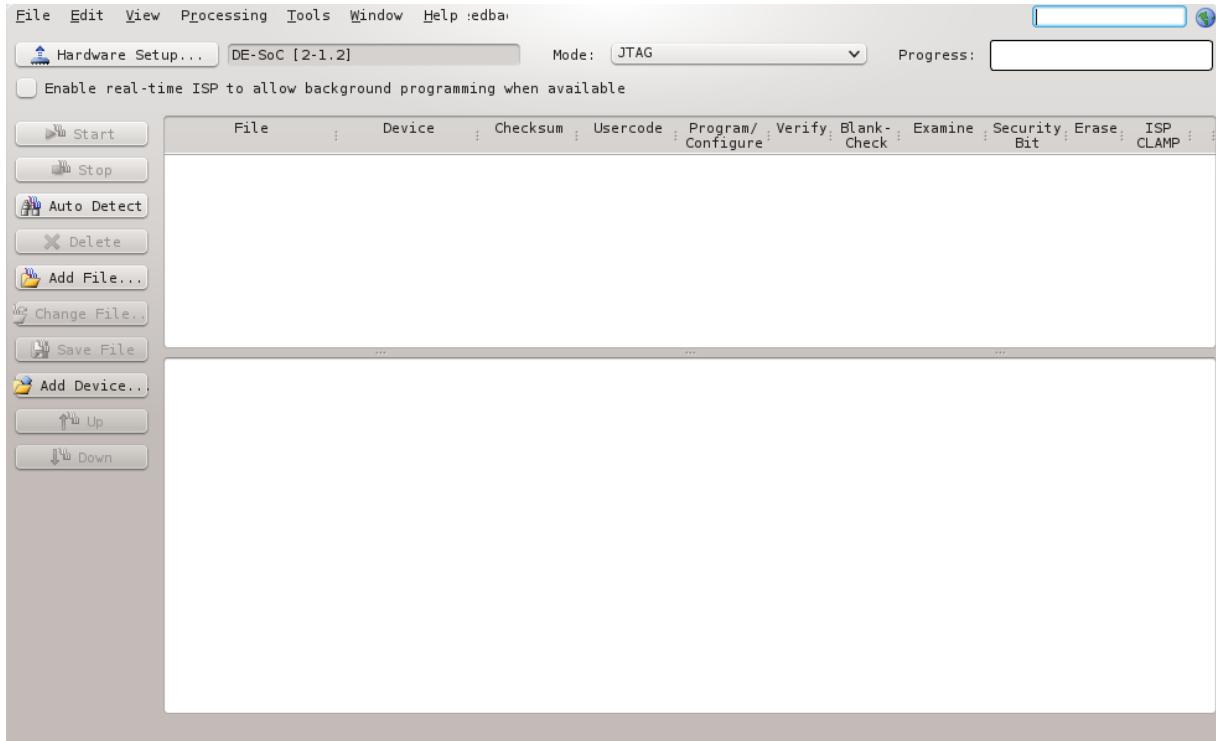


Figure 8-15. Quartus II Programmer

36. Choose the “Auto Detect” button on the left of Figure 8-15, then choose “5CSEMA5”, as shown in Figure 8-16.

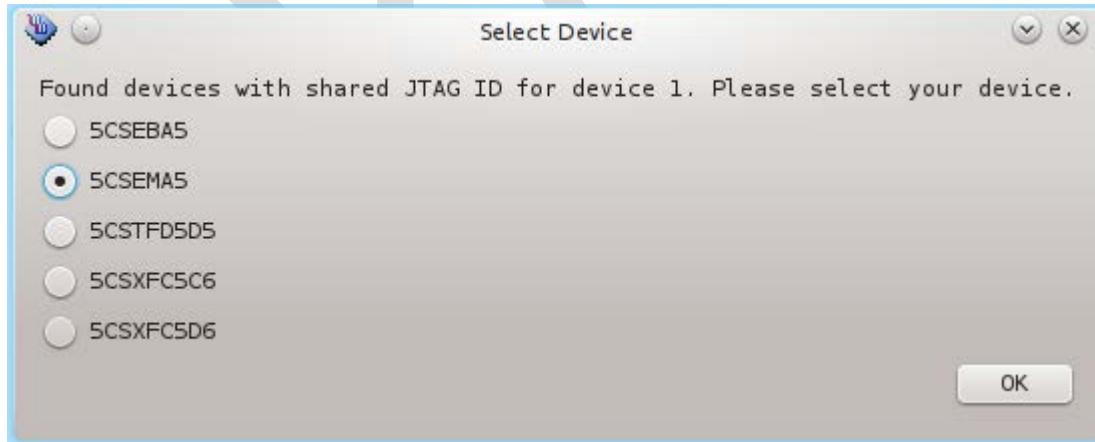


Figure 8-16. FPGA Selection

You should now see 2 devices on the JTAG scan chain, as shown in Figure 8-17.

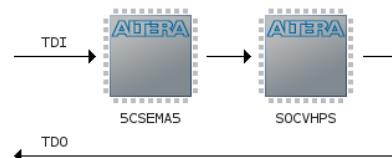


Figure 8-17. JTAG Scan Chain

37. Right-click on the “5CSEMA5” device shown in Figure 8-17 and choose “Edit > Change File”. Then, select “DE1_SoC_demo/RTL/quartus/output_files/DE1_SoC_demo.sof” through the file browser.
38. Enable the “Program/Configure” checkbox for device “5CSEMA5F31”, then press the “Start” button, as shown in Figure 8-18.

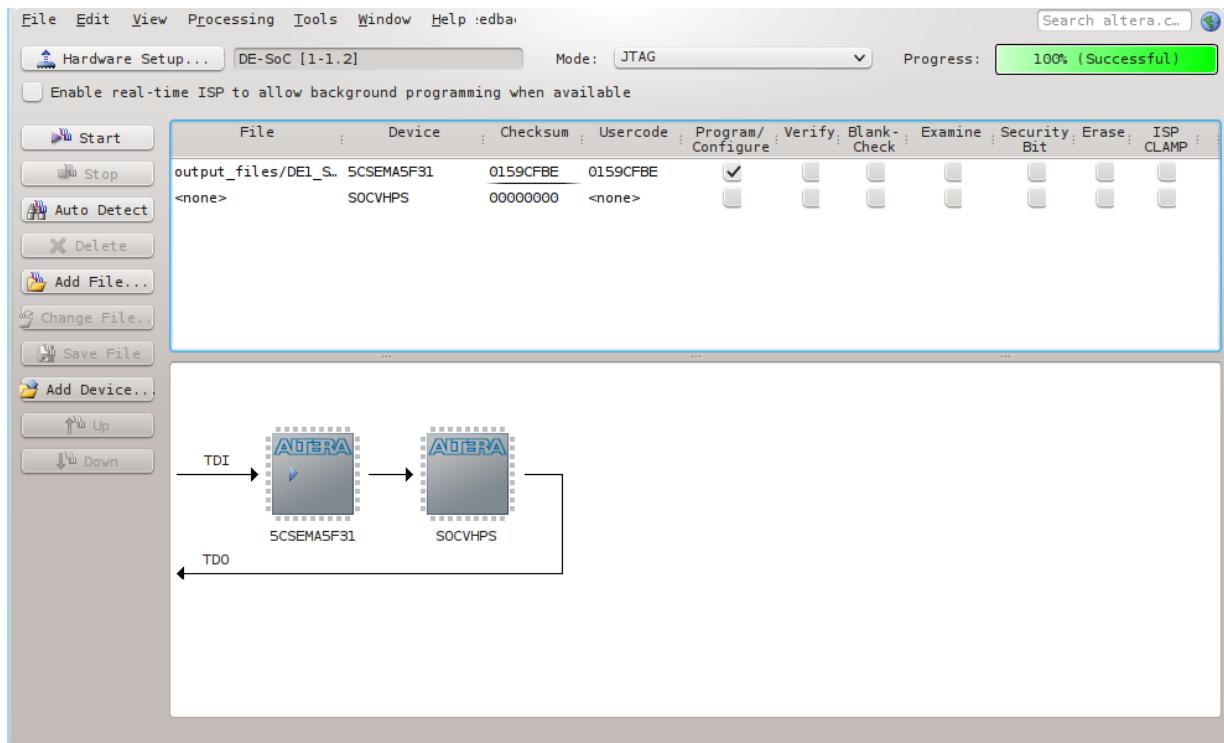


Figure 8-18. Programming the FPGA

We are now done with the *Quartus II* program, and will no longer need it for the rest of this tutorial.

8.4 SOFTWARE

Now that all the hardware has been designed, we need to get to the software aspects of the development process.

8.4.1 FPGA – Nios II

8.4.1.1 Project Setup

1. Launch the *Nios II SBT IDE*.
 - a. On Windows machines, you can find a shortcut to the executable in the Windows Start Menu: “Altera [version] Web Edition > Nios II EDS [version] > Nios II [version] Software Build Tools for Eclipse”.
 - b. On Linux machines, first launch a *Nios II Command Shell*. You can find the executable at “<altera_install_directory>/<version>/nios2eds/nios2_command_shell.sh”. Type “eclipse-nios2” in the *Nios II Command Shell* and press enter.
2. Choose “File > New > Nios II Application and BSP from Template”.
 - a. All the information needed to program a Nios II processor are contained within the “sopcinfo” file created by Qsys. For the “SOPC Information File name” use “DE1_SoC_demo/RTL/quartus/soc_system.sopcinfo”.
 - b. Use “DE1_SoC_demo_nios” as the project name.
 - c. Disable the “Use default location” checkbox
 - d. Use “DE1_SoC_demo/C/nios2eds/DE1_SoC_demo_nios” as the project location.
 - e. Choose the “Blank Project” template.
 - f. Click on the “Finish” button to create the project.

3. Right-click on the “DE1_SoC_demo_nios” project folder and select “New > Source file”. Use the default C source template, and set “nios.c” as the file name.
4. Right-click on the “DE1_SoC_demo_nios_bsp” project, and select “Build Project”. Once the build is completed, a number of files will be generated, the most useful of which is the “system.h” file. This file contains all the details related to the Nios II processor’s various peripherals, as defined in Qsys in 8.3.2.

8.4.1.2 Nios II Programming Theory – Accessing Peripherals

The Nios II processor can be programmed in C similarly to any other microcontroller. However, care must be taken when accessing any of the processor’s peripherals. Depending on which version of the Nios II you instantiated in Qsys, you may not be able to correctly read data at a peripheral’s address space using pointers. The issue arises when your Nios II processor has a *data cache*.

Suppose we use the code in Figure 8-19 to read data from the switches of our Qsys design.

```
int main() {
    alt_u32 *p_switches = SWITCHES_0_BASE;
    while (1) {
        alt_u32 switches_value = *p_switches;
        printf("switches_value = %x\n", (unsigned int) switches_value);
    }
    return 0;
}
```

Figure 8-19. Incorrect Nios II Peripheral Access in C

When this code is run, the initial value of the “switches_value” variable, as obtained from the first iteration of the while loop, will be the correct representation of the switches’ state. However, at each iteration of the while loop, the “switches_value” variable will **NEVER** change again, even if the switches are flipped between each iteration. The issue is that each successive access is being served by the data cache, which doesn’t see that the switches have been modified.

The solution to this issue is to use special instructions that bypass the data cache when reading or writing to peripherals. The available instructions are listed below, and an example of how to correctly access Nios II peripherals is shown in Figure 8-20.

- Reading
 - IORD_8DIRECT(BASE, OFFSET)
 - IORD_16DIRECT(BASE, OFFSET)
 - IORD_32DIRECT(BASE, OFFSET)
- Writing
 - IOWR_8DIRECT(BASE, OFFSET, DATA)
 - IOWR_16DIRECT(BASE, OFFSET, DATA)
 - IOWR_32DIRECT(BASE, OFFSET, DATA)

```
int main() {
    while (1) {
        alt_u32 switches_value = IORD_32DIRECT(SWITCHES_0_BASE, 0);
        printf("switches_value = %x\n", (unsigned int) switches_value);
    }
    return 0;
}
```

Figure 8-20. Correct Nios II Peripheral Access in C

8.4.1.3 Nios II Programming Practice

5. Write the code provided in Figure 8-21 in “nios.c”. The code instructs the Nios II processor to create a strobing light effect on its 10 peripheral LEDs. The processor’s 10 peripheral switches are used as enable signals for each corresponding LED. This corresponds to specification 1 in 8.1.

```
#include <stdio.h>
#include <unistd.h>
#include "io.h"
#include "altera_avalon_pio_regs.h"
#include "system.h"

#define LEDS_MAX_ITERATION (1000)
#define SLEEP_DELAY_US (100 * 1000)

void rotate_leds() {
    int loop_count = 0;
    int leds_mask = 0x01;

    // 0/1 = left/right direction
    int led_direction = 0;

    while (loop_count < LEDS_MAX_ITERATION) {
        alt_u32 switches_value = IORD_ALTERA_AVALON_PIO_DATA(SWITCHES_0_BASE);
        alt_u32 leds_value = ~leds_mask;

        // only turn on leds which have their corresponding switch enabled
        IOWR_ALTERA_AVALON_PIO_DATA(LEDS_0_BASE, leds_value & switches_value);

        usleep(SLEEP_DELAY_US);

        if (led_direction == 0) {
            leds_mask <= 1;
            if (leds_mask == (0x01 << (LEDS_0_DATA_WIDTH - 1))) {
                led_direction = 1;
            }
        } else {
            leds_mask >= 1;
            if (leds_mask == 0x01) {
                led_direction = 0;
                loop_count++;
            }
        }
    }
}

int main() {
    rotate_leds();
    return 0;
}
```

Figure 8-21. nios.c

6. Right-click on “DE1_SoC_demo_nios” project, and select “Build Project”.
7. The code is now ready to be run on the FPGA. Right-click on “DE1_SoC_demo_nios” project, and select “Run As > Nios II Hardware”. You should be able to see a strobing light effect on the 10 FPGA LEDs. You can use the 10 FPGA switches as enable signals for the corresponding LED.
8. In some cases, it is possible that the program will not immediately run on the Nios II processor, and you will be prompted with a “Target Connection” dialog, as shown in Figure 8-22. If your Nios II CPU doesn’t appear in the list of available processors, then

- Click on the “Refresh Connections” button on the right of Figure 8-22.
- Enable the “Ignore mismatched system ID” checkbox under “System ID checks”.
- Enable the “Ignore mismatched system timestamp” checkbox under “System ID checks”.
- Click on the “Run” button to finish.

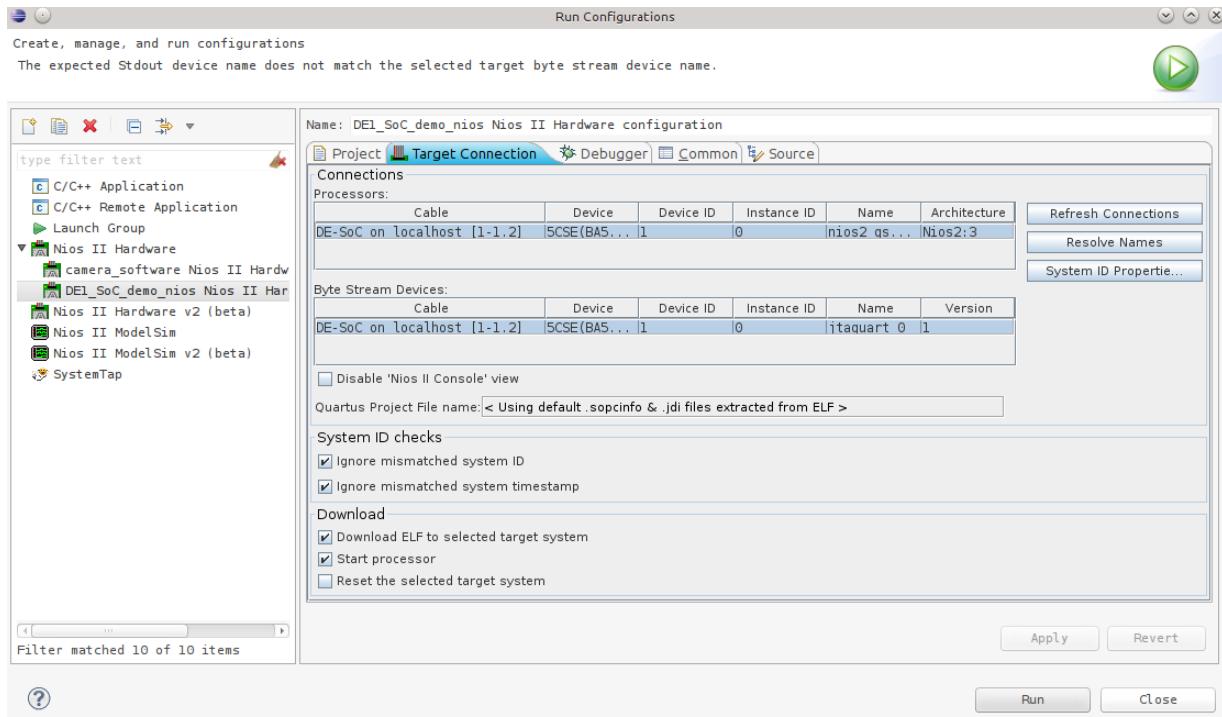


Figure 8-22. Nios II Target Connection Dialog

We now have a programmed Nios II processor on the FPGA. Of course, the design we had specified didn't require the power of a Nios II processor, and could have easily been done in pure VHDL. Nevertheless, the idea was to show that one can have a secondary programmable processor functioning on the FPGA parallelly to the HPS. We are now done with the *Nios II SBT IDE*, and will no longer need it for the rest of this tutorial.

Up until this point, the hardware and software design process has been ***IDENTICAL*** for both ***BARE-METAL*** and ***LINUX HPS*** applications.

8.4.2 HPS – ARM

This is where the design process ***DIVERGES*** between ***BARE-METAL*** and ***LINUX HPS*** applications.

8.4.2.1 Bare-metal Applications

The first thing that needs to be done for bare-metal applications is to generate and compile a preloader for the HPS.

8.4.2.1.1 Preloader Generation

9. Launch a *SoC EDS Embedded Command Shell*.
 - On Windows machines, you can find a shortcut to the executable in the Windows Start Menu: “Altera [version] Web Edition > SoC Embedded Design Suite (EDS) [version] > SoC EDS [version] Command Shell”.
 - On Linux machines, you can find the executable at “<altera_install_directory>/<version>/embedded/embedded_command_shell.sh”.
10. Type “bsp-editor” and press enter.
11. Choose “File > New BSP...”.
 - The preloader will need to know which of the HPS’ peripherals were enabled so it can appropriately initialize them in the boot process. Under “Preloader settings directory”,

- select the “DE1_SoC_demo/RTL/quartus/hps_isw_handoff/soc_system_hps_0” directory. This directory contains settings relative to the HPS’ **HARD** peripherals, as configured in the “Arria V/Cyclone V Hard Processor System” component in Qsys.
- Disable the “Use default locations” checkbox and under the “BSP target directory”, select the “DE1_SoC_demo/C/ds5/preloader” directory. You should have something similar to Figure 8-23.

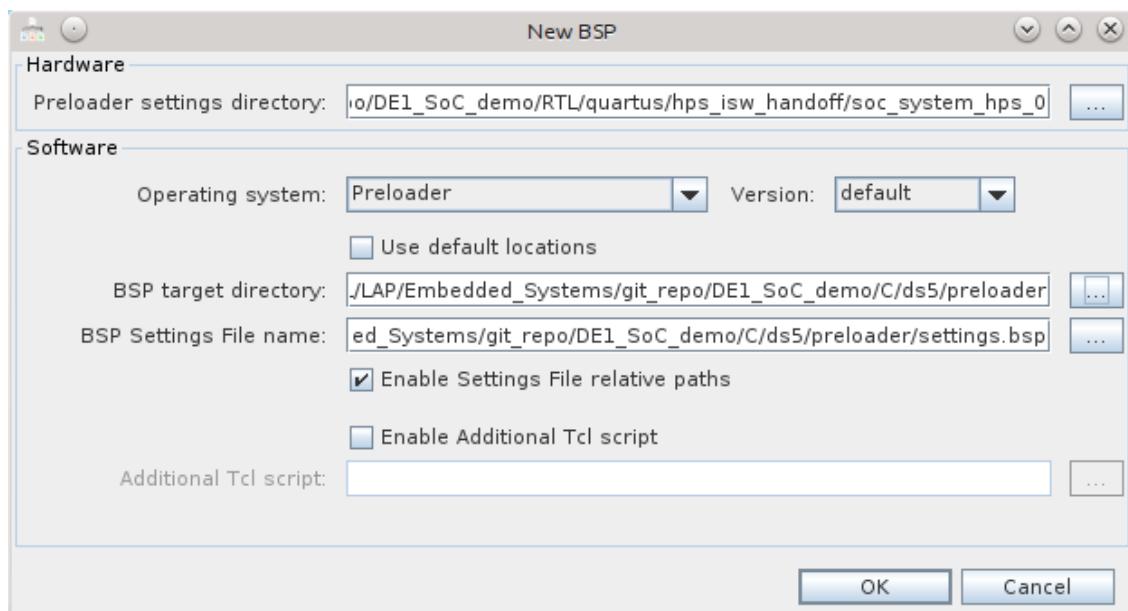


Figure 8-23. New BSP Dialog

- Press the “OK” button. You should then arrive on a page with many settings, as shown on Figure 8-24. Take some time to read through them to see what the preloader has the ability to do.

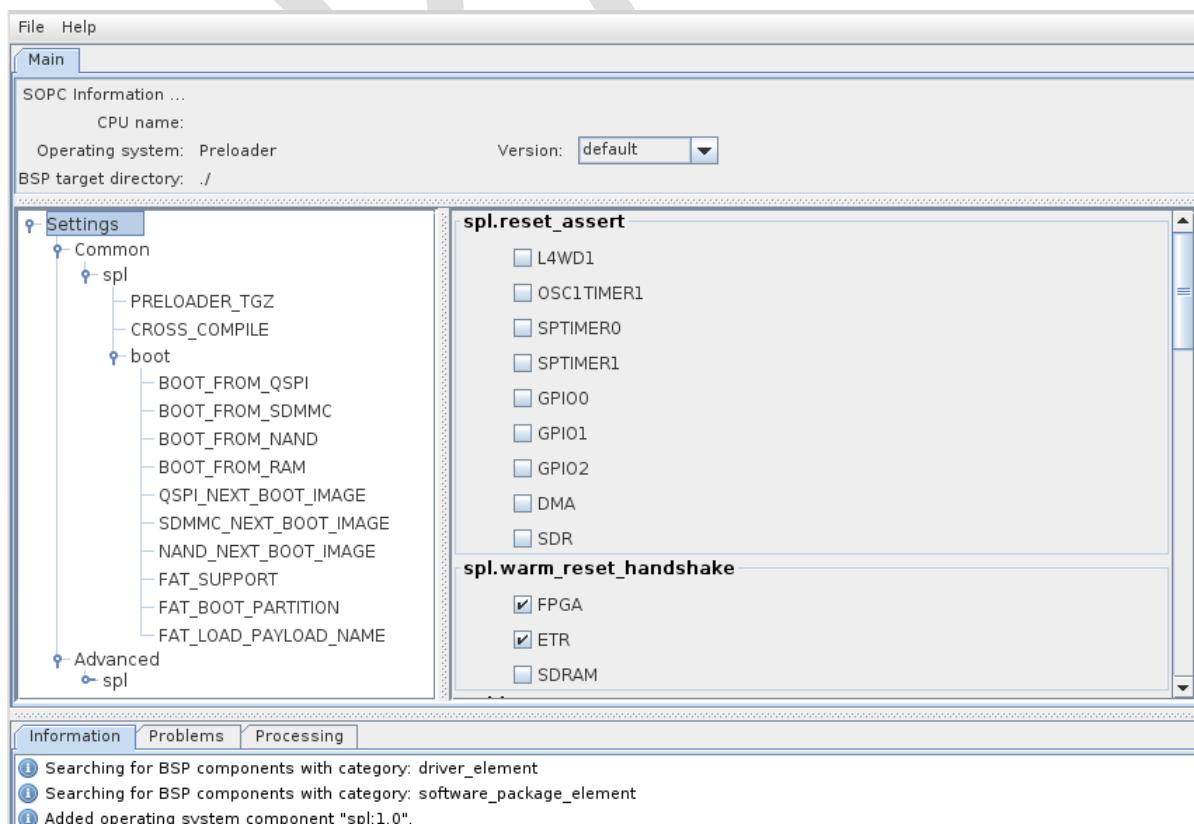


Figure 8-24. Preloader Settings Dialog

12. On the main settings page of Figure 8-24, we will only need to modify 2 parameters for our design.
 - a. Under “spl.boot”, disable the “WATCHDOG_ENABLE” checkbox. This is necessary to prevent the system from being automatically reset after a certain time has elapsed.
 - b. Under “spl.performance”, disable the “SERIAL_SUPPORT” checkbox. This greatly speeds up the time spent in the preloader. The “serial support” implied by this checkbox only concerns serial support while the preloader is running. Once we run our bare-metal application, we will still be able to call the printf() function.
 - c. Press the “Generate” button to finish. You can then exit the bsp-editor.
13. In the *Soc EDS Embedded Command Shell*, navigate to the “DE1_SoC_demo/C/ds5/preloader” directory, and execute “make” to build the preloader.

IF YOU EVER DECIDE TO MOVE THE “DE1_SoC_demo” PROJECT DIRECTORY DEFINED IN FIGURE 8-1, YOU WILL HAVE TO REGENERATE THE PRELOADER. UNFORTUNATELY, THE SCRIPT THAT GENERATES THE PRELOADER HARD-CODES MULTIPLE PATHS DIRECTLY IN THE RESULTING FILES, RENDERING THE FILES USELESS ONCE MOVED.

8.4.2.1.2 Generating a Header File for HPS Peripherals

We need to be able to programmatically access the HPS peripherals that are part of the FPGA fabric. In order to do this, we must generate a header file.

14. Create a new file “DE1_SoC_demo/generate_hps_qsys_header.sh”, and populate it with the code shown in Figure 8-25. This code parses the “DE1_SoC_demo/RTL/quartus/soc_system.sopcinfo” file looking for a module called “hps_0”, and outputs a header file “hps_soc_system.h”. The generated header file is then moved to the “DE1_SoC_demo/C/ds5/projects” directory.

```
#!/bin/sh

sopc-create-header-files \
"RTL/quartus/soc_system.sopcinfo" \
--single "hps_soc_system.h" \
--module "hps_0"

mv "hps_soc_system.h" "C/ds5/projects/"
```

Figure 8-25. generate_hps_qsys_header.sh

15. Execute the “generate_hps_qsys_header.sh” script in the *Soc EDS Embedded Command Shell*. Figure 8-26 shows a short extract of the generated “hps_soc_system.h” header file. At the top of the file, it says that macros for devices connected to master port “h2f_lw_axi_master” of module “hps_0” have been generated.

```
/*
 * This file was automatically generated by the swinfo2header utility.
 *
 * Created from SOPC Builder system 'soc_system' in
 * file 'RTL/quartus/soc_system.sopcinfo'.
 */

/*
 * This file contains macros for module 'hps_0' and devices
 * connected to the following master:
 *   h2f_lw_axi_master
 *
 * Do not include this header file and another header file created for a
 * different module or master group at the same time.
 * Doing so may result in duplicate macro names.
 * Instead, use the system header file which has macros with unique names.
```

```

/*
 *
 * Macros for device 'hex_5', class 'altera_avalon_pio'
 * The macros are prefixed with 'HEX_5_'.
 * The prefix is the slave descriptor.
 */
#define HEX_5_COMPONENT_TYPE altera_avalon_pio
#define HEX_5_COMPONENT_NAME hex_5
#define HEX_5_BASE 0x0
#define HEX_5_SPAN 16
#define HEX_5_END 0xf

```

Figure 8-26. *hps_soc_system.h*

8.4.2.1.3 ARM DS-5

16. Launch the *ARM DS-5* IDE.

- On Windows machines, you can find a shortcut to the executable in the Windows Start Menu: “*ARM DS-5 > Eclipse for DS-5*”.
- On Linux machines, you can find the executable at “*<altera_install_directory>/<version>/embedded/ds-5/bin/eclipse*”. Be sure to launch eclipse from the *SoC EDS Embedded Command Shell* on a Linux machine.

8.4.2.1.3.1 Setting Up a New C Project

17. Create a new C project by going to “File > New > C Project”.

- Use “*DE1_SoC_demo_hps_baremetal*” as the project name.
- Disable the “Use default location” checkbox.
- Set “*DE1_SoC_demo/C/ds5/projects/DE1_SoC_demo_hps_baremetal*” as the target location for the project.
- We want to create a single output executable for our project, so choose “Executable > Empty Project” as the project type.
- Choose “Altera Baremetal GCC” as the Toolchain.
- You should have something similar to Figure 8-27. Then, press the “Finish” button to create the project.

18. When programming the HPS, we will need access to a few standard header and linker files provided by Altera. We need to add these files to the *ARM DS-5* project.

- Right-click on the “*DE1_SoC_demo_hps_baremetal*” project, and go to “Properties”.
- Under “C/C++ Build > Settings > GCC C Compiler > Includes”, add the following paths to the “Include paths (-I)” list:
 - “*<altera_install_directory>/<version>/embedded/ip/altera/hps/altera_hps/hwlib/include*”
 - “*<altera_install_directory>/<version>/embedded/ip/altera/hps/altera_hps/hwlib/include/socal*”
- Since we are not going to be running any operating system, we will need to use a linker script in order to correctly layout our bare-metal program in memory. Altera provides linker scripts for the HPS’ on-chip memory, as well as for its DDR3 memory. We want our code to be loaded in the HPS’ DDR3 memory and will not use any on-chip memory in our design, so we will use the DDR3 linker script. Under “C/C++ Build > Settings > GCC C Linker > Image”, set the linker script to “*<altera_install_directory>/<version>/embedded/host_tools/mentor.gnu/arm/baremetal/arm-altera-eabi/lib/cycloneV-dk-ram-**HOSTED**.ld*”. The “hosted” script allows the bare-metal application to use some of the host’s functionality. In this case, we use the “hosted” script to be able to see the output of the `printf()` function on the host’s console.

- d. Click on the “Apply” button, then on the “Ok” button to close the project properties dialog.

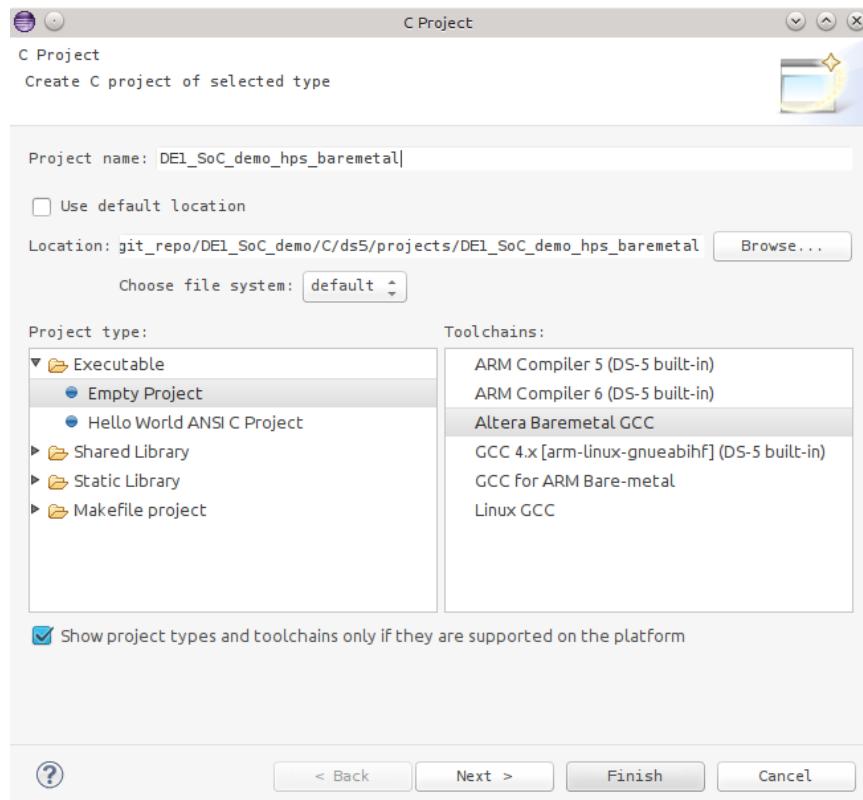


Figure 8-27. New C Project Dialog

8.4.2.1.3.2 Writing a DS-5 Debug Script

In Figure 6-8, we saw that a bare-metal application cannot run immediately upon boot, and that the HPS must first go through the preloader. As such, we cannot instruct the DS-5 debugger to *directly* load our bare-metal application’s compiled binary into the HPS’ memory.

Instead, we will use a **DS-5 DEBUG SCRIPT** to instruct the debugger exactly how to load our application.

19. Create a new file for our DS-5 debug script and save it under “DE1_SoC_demo/C/ds5/projects/DE1_SoC_demo_hps_baremetal/debug_setup.ds”.
20. Populate the file with the code shown in Figure 8-28. This script tells the debugger to load the preloader, then to load our bare-metal application.

This is performed by placing a breakpoint at the very last function executed by the preloader prior to handing control of the cpu to the next boot stage. This function is “spl_boot_device()”, which is responsible for choosing the next boot medium on the DE1-SoC and jumping to its address. For bare-metal applications, we don’t want the boot process to continue on towards another device. Instead, we want to load our bare-metal code and jump to its address. This is exactly what the debug script in Figure 8-28 does.

```
# Reset and stop the system.
stop
wait 5s
reset system
wait 5s

# Delete all breakpoints.
delete breakpoints

# Disable semihosting
```

```

set semihosting enabled false

# Load the preloader.
loadfile "$sdir/../../preloader/u-boot-socfpga/spl/u-boot-spl" 0x0

# Enable semihosting to allow printing even if you don't have a uart module
# available.
set semihosting enabled true

# Set a breakpoint at the "spl_boot_device()" function. This function is the
# last step of the preloader. It looks for a boot device (qspi flash, sdcard,
# fpga), and jumps to that address. For our bare-metal programs, we don't want
# to use any boot device, but want to run our own program, so we want the
# processor to stop here. Then, we will modify its execution to make it run our
# program.
tbreak spl_boot_device

# Set the PC register to the entry point address previously recorded by the
# "load" or "loadfile" command and start running the target.
run

# Instruct the debugger to wait until either the application completes or a
# breakpoint is hit. In our case, it will hit the breakpoint.
wait

# Load our bare-metal program.
loadfile "$sdir/Debug/DE1_SoC_demo_hps_baremetal.axf"

# Set a breakpoint at our program's "main()" function.
tbreak main

# Start running the target.
run

# wait at main().
Wait

```

Figure 8-28. debug_setup.ds

For a comprehensive list of commands supported by the DS-5 debugger, please refer to [3].

NOTE THAT IT IS POSSIBLE FOR THE HPS TO DIRECTLY EXECUTE A BARE-METAL APPLICATION WITHOUT GOING THROUGH THE PRELOADER. HOWEVER, THE APPLICATION WOULD BE FORCED TO FIT IN THE HPS' ON-CHIP MEMORY (WHICH IS QUITE SMALL), AND WOULDN'T BE ABLE TO USE ANY OF THE HPS' PERIPHERALS, AS THEY HAVEN'T BEEN INITIALIZED YET.

8.4.2.1.3.3 Setting Up the Debug Configuration

21. Right-click on the “DE1_SoC_demo_baremetal” project, and go to “Debug As > Debug Configurations...”.
22. Choose to create a new debugger configuration by right-clicking on “DS-5 Debugger” on the left and selecting “New”. Use “DE1_SoC_demo_hps_baremetal” as the name of the new debug configuration.
23. Under the “Connection” tab:
 - a. Use “Altera > Cyclone V SoC (Dual Core) > Bare Metal Debug > Debug Cortex-A9_0” as the target platform.
 - b. Set the “Target Connection” to “USB-Blaster”.
 - c. Use the “Browse” button to select the DE1-SoC that is connected to your machine.
 - d. You should have something similar to Figure 8-29.

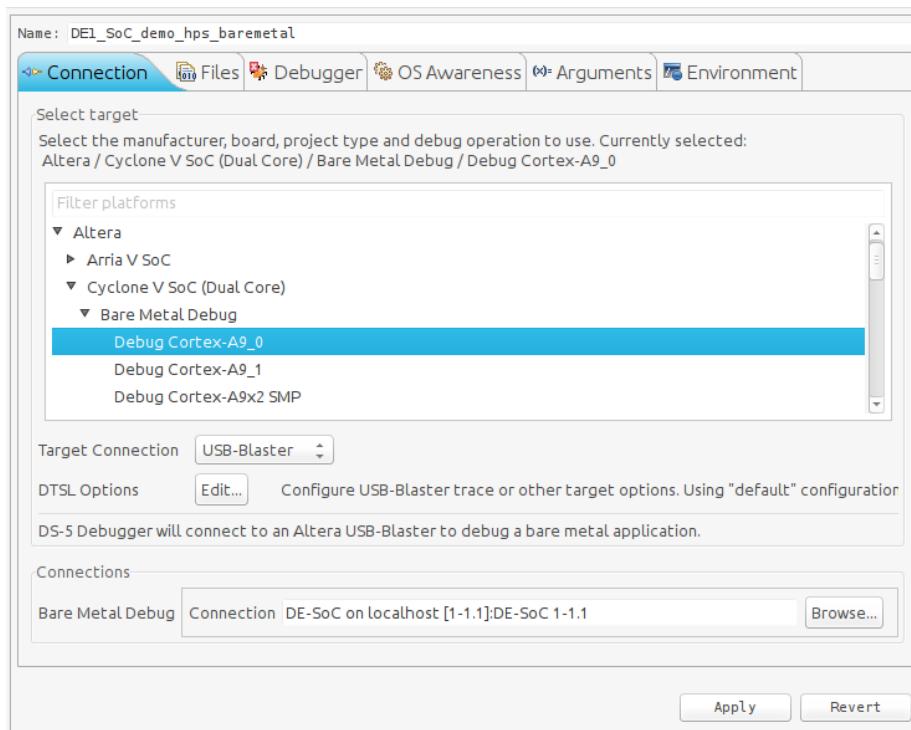


Figure 8-29. Debug Configuration "Connection" Tab

24. Under the "Files" tab:

- Leave the "Application on host to download" empty. We do this since we are using a debug script to instruct the debugger how to load our application.
- In 8.3.3.2, we configured our HPS to use some FPGA peripherals. We can instruct the debugger about this so it can show more detailed information when debugging. To do this, set the combobox to "Add peripheral description files from directory" and set it to the "DE1_SoC_demo/RTL/quartus/soc_system/synthesis" directory, as shown in Figure 8-30. This directory contains a file called "soc_system_hps_0.hps.svd" which has information on all of the HPS' peripherals which are in the FPGA fabric.

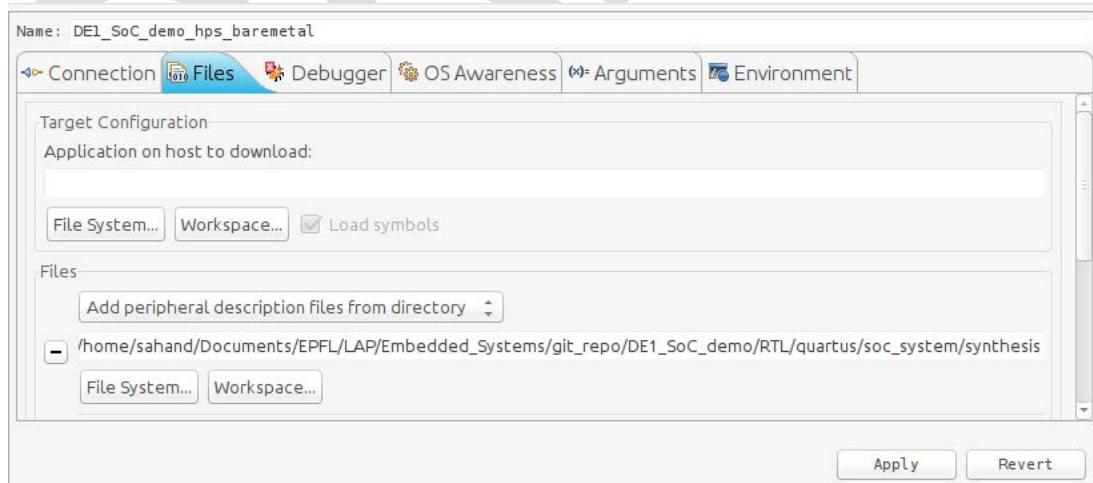


Figure 8-30. Debug Configuration "Files" Tab

25. Under the "Debugger" tab:

- Since we are going to use a debug script to launch the application, we don't need to specify any function to be loaded by the debugger. So, choose "Connect only" under "Run control".

- b. Enable the “Run **DEBUG** initialization debugger script (.ds / .py)” checkbox. Set the debug script to the one we defined for the project in 8.4.2.1.3.2. You should have something similar to Figure 8-31.
26. Click on the “Apply” button, then on the “Close” button to save the debug configuration.

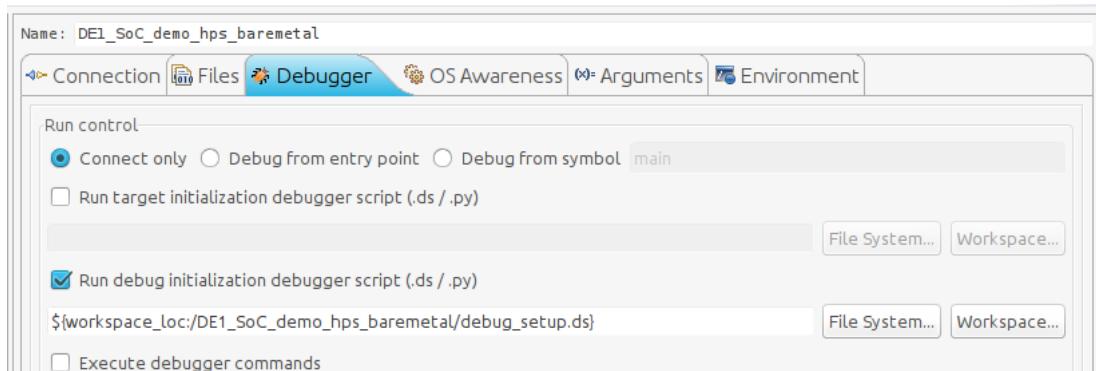


Figure 8-31. Debug Configuration "Debugger" Tab

8.4.2.1.3.4 HPS Programming

We can now start writing code for the HPS.

27. Right-click on the “DE1_SoC_demo_baremetal” project, and go to “New > Source File”. Use “hps_baremetal.c” as the file name, and click on the “Finish” button to create the new source file.

8.4.2.1.3.4.1 Theory

The HPS works just like any other microcontroller.

- If you want to access a peripheral, you have to read at its address.
- If a peripheral is connected to a bus, its address is obtained by adding its offset in the bus to the bus' address.

Altera provides useful utility functions

in “<altera_install_directory>/<version>/embedded/ip/altera/hps/altera_hps/hwlib/include/socal/socal.h”, a few of which are listed below. Most functions exist for multiple sizes (byte, hword, word, dword).

- alt_write_byte(dest, src)
- alt_read_byte(src)
- alt_setbits_byte(dest, bits)
- alt_clrbits_byte(dest, bits)
- alt_xorbits_byte(dest, bits)
- alt_replbits_byte(dest, msk, src)

8.4.2.1.3.4.2 Practice

28. Populate the “hps_baremetal.c” file with the code shown in Figure 8-32.

```
// | ======|=====|=====|=====|
// | Signal Name | HPS GPIO | Register/bit | Function |
// | ======|=====|=====|=====|
// | HPS_LED | GPIO53 | GPIO1[24] | I/O |
// | HPS_KEY | GPIO54 | GPIO1[25] | I/O |
// | ======|=====|=====|=====|
#define HPS_LED_BIT (24)
#define HPS_KEY_BIT (25)
#define HPS_LED_MASK (1 << HPS_LED_BIT)
#define HPS_KEY_MASK (1 << HPS_KEY_BIT)
```

```

// The 7-segment display is active low
#define HEX_DISPLAY_CLEAR (0x7F)
#define HEX_DISPLAY_ZERO (0x40)
#define HEX_DISPLAY_ONE (0x79)
#define HEX_DISPLAY_TWO (0x24)
#define HEX_DISPLAY_THREE (0x30)
#define HEX_DISPLAY_FOUR (0x19)
#define HEX_DISPLAY_FIVE (0x12)
#define HEX_DISPLAY_SIX (0x02)
#define HEX_DISPLAY_SEVEN (0x78)
#define HEX_DISPLAY_EIGHT (0x00)
#define HEX_DISPLAY_NINE (0x18)
#define HEX_DISPLAY_A (0x08)
#define HEX_DISPLAY_B (0x03)
#define HEX_DISPLAY_C (0x46)
#define HEX_DISPLAY_D (0x21)
#define HEX_DISPLAY_E (0x06)
#define HEX_DISPLAY_F (0x0E)

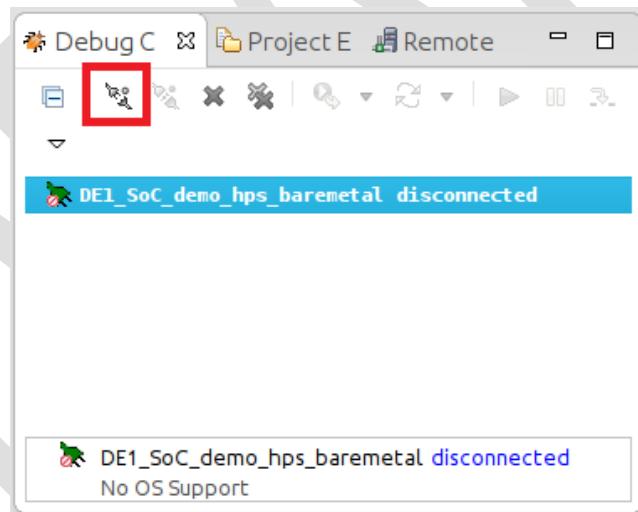
// The HPS will only use HEX_DISPLAY_COUNT of the 6 7-segment displays
#define HEX_DISPLAY_COUNT (6)
#define HEX_COUNTER_MASK ((1 << (4 * HEX_DISPLAY_COUNT)) - 1)

```

Figure 8-32. *hps_baremetal.c*

29. Switch to the *DS-5 Debug* perspective.

30. In the “Debug Control” view, click on “DE1_SoC_demo_hps_baremetal” entry, then click on the “Connect to Target” button, as shown on Figure 8-33.

Figure 8-33. *Debug Control View*

8.4.2.2 Linux Applications

9 TODO

- Explain MSEL when reprogramming the FPGA from the HPS.
- Talk about what the JTAG to Avalon masters are.
- Printing is done in the “App Console” in DS-5.

DRAFT

10 APPENDIX

10.1 DE1-SoC TOP-LEVEL VHDL ENTITY

The DE1-SoC has a lot of pins, which makes it tedious to start an FPGA design. It is recommended to use the following **ENTITY** for your **TOP-LEVEL VHDL FILE**, as it contains all the board's FPGA and HPS pins. The file can be found at \\lapsrv1.epfl.ch\documentation\Altera\CycloneV\Distribution\DE1_SoC_top_level.vhd.

```
-- ##### DE1_SoC_top_level.vhd #####
-- DE1-SoC from Terasic
-- Author : Sahand Kashani-Akhavan from Terasic documentation
-- Revision : 1.1
-- Creation date : 04/02/2015
--
-- Syntax Rule : GROUP_NAME_N[bit]
--
-- GROUP : specify a particular interface (ex: SDR_)
-- NAME : signal name (ex: CONFIG, D, ...)
-- bit : signal index
-- _N : to specify an active-low signal
-- #####
library ieee;
use ieee.std_logic_1164.all;

entity DE1_SoC_top_level is
port(
    -- ADC
    ADC_CS_n      : out  std_logic;
    ADC_DIN       : out  std_logic;
    ADC_DOUT      : in   std_logic;
    ADC_SCLK      : out  std_logic;

    -- Audio
    AUD_ADCDAT   : in   std_logic;
    AUD_ADCLRCK  : inout std_logic;
    AUD_BCLK      : inout std_logic;
    AUD_DACDAT   : out  std_logic;
    AUD_DACLRCK  : inout std_logic;
    AUD_XCK       : out  std_logic;

    -- CLOCK
    CLOCK_50      : in   std_logic;
    CLOCK2_50     : in   std_logic;
    CLOCK3_50     : in   std_logic;
    CLOCK4_50     : in   std_logic;

    -- SDRAM
    DRAM_ADDR     : out  std_logic_vector(12 downto 0);
    DRAM_BA       : out  std_logic_vector(1 downto 0);
    DRAM_CAS_N    : out  std_logic;
    DRAM_CKE      : out  std_logic;
    DRAM_CLK      : out  std_logic;
    DRAM_CS_N     : out  std_logic;
    DRAM_DQ       : inout std_logic_vector(15 downto 0);
    DRAM_LDQM    : out  std_logic;
```

```

DRAM_RAS_N      : out  std_logic;
DRAM_UDQM       : out  std_logic;
DRAM_WE_N       : out  std_logic;

-- I2C for Audio and Video-In
FPGA_I2C_SCLK   : out  std_logic;
FPGA_I2C_SDAT   : inout std_logic;

-- SEG7
HEX0_N          : out  std_logic_vector(6 downto 0);
HEX1_N          : out  std_logic_vector(6 downto 0);
HEX2_N          : out  std_logic_vector(6 downto 0);
HEX3_N          : out  std_logic_vector(6 downto 0);
HEX4_N          : out  std_logic_vector(6 downto 0);
HEX5_N          : out  std_logic_vector(6 downto 0);

-- IR
IRDA_RXD        : in   std_logic;
IRDA_TXD        : out  std_logic;

-- KEY_n
KEY_N           : in   std_logic_vector(3 downto 0);

-- LED
LEDR            : out  std_logic_vector(9 downto 0);

-- PS2
PS2_CLK         : inout std_logic;
PS2_CLK2        : inout std_logic;
PS2_DAT         : inout std_logic;
PS2_DAT2        : inout std_logic;

-- SW
SW              : in   std_logic_vector(9 downto 0);

-- Video-In
TD_CLK27        : inout std_logic;
TD_DATA          : out   std_logic_vector(7 downto 0);
TD_HS            : out   std_logic;
TD_RESET_N       : out   std_logic;
TD_VS            : out   std_logic;

-- VGA
VGA_B            : out   std_logic_vector(7 downto 0);
VGA_BLANK_N      : out   std_logic;
VGA_CLK          : out   std_logic;
VGA_G            : out   std_logic_vector(7 downto 0);
VGA_HS           : out   std_logic;
VGA_R            : out   std_logic_vector(7 downto 0);
VGA_SYNC_N       : out   std_logic;
VGA_VS           : out   std_logic;

-- GPIO_0, GPIO_0 connect to GPIO Default
GPIO_0           : inout std_logic_vector(35 downto 0);

-- GPIO_1, GPIO_1 connect to GPIO Default
GPIO_1           : inout std_logic_vector(35 downto 0);

-- HPS

```

```

HPS_CONV_USB_N : inout std_logic;
HPS_DDR3_ADDR : out std_logic_vector(14 downto 0);
HPS_DDR3_BA : out std_logic_vector(2 downto 0);
HPS_DDR3_CAS_N : out std_logic;
HPS_DDR3_CK_N : out std_logic;
HPS_DDR3_CK_P : out std_logic;
HPS_DDR3_CKE : out std_logic;
HPS_DDR3_CS_N : out std_logic;
HPS_DDR3_DM : out std_logic_vector(3 downto 0);
HPS_DDR3_DQ : inout std_logic_vector(31 downto 0);
HPS_DDR3_DQS_N : inout std_logic_vector(3 downto 0);
HPS_DDR3_DQS_P : inout std_logic_vector(3 downto 0);
HPS_DDR3_ODT : out std_logic;
HPS_DDR3_RAS_N : out std_logic;
HPS_DDR3_RESET_N : out std_logic;
HPS_DDR3_RZQ : in std_logic;
HPS_DDR3_WE_N : out std_logic;
HPS_ENET_GTX_CLK : out std_logic;
HPS_ENET_INT_N : inout std_logic;
HPS_ENET_MDC : out std_logic;
HPS_ENET_MDIO : inout std_logic;
HPS_ENET_RX_CLK : in std_logic;
HPS_ENET_RX_DATA : in std_logic_vector(3 downto 0);
HPS_ENET_RX_DV : in std_logic;
HPS_ENET_TX_DATA : out std_logic_vector(3 downto 0);
HPS_ENET_TX_EN : out std_logic;
HPS_FLASH_DATA : inout std_logic_vector(3 downto 0);
HPS_FLASH_DCLK : out std_logic;
HPS_FLASH_NCSO : out std_logic;
HPS_GPIO : inout std_logic_vector(1 downto 0);
HPS_GSENSOR_INT : inout std_logic;
HPS_I2C_CONTROL : inout std_logic;
HPS_I2C1_SCLK : inout std_logic;
HPS_I2C1_SDAT : inout std_logic;
HPS_I2C2_SCLK : inout std_logic;
HPS_I2C2_SDAT : inout std_logic;
HPS_KEY : inout std_logic;
HPS_LED : inout std_logic;
HPS_SD_CLK : out std_logic;
HPS_SD_CMD : inout std_logic;
HPS_SD_DATA : inout std_logic_vector(3 downto 0);
HPS_SPIM_CLK : out std_logic;
HPS_SPIM_MISO : in std_logic;
HPS_SPIM_MOSI : out std_logic;
HPS_SPIM_SS : inout std_logic;
HPS_UART_RX : in std_logic;
HPS_UART_TX : out std_logic;
HPS_USB_CLKOUT : in std_logic;
HPS_USB_DATA : inout std_logic_vector(7 downto 0);
HPS_USB_DIR : in std_logic;
HPS_USB_NXT : in std_logic;
HPS_USB_STP : out std_logic
);
end entity DE1_SoC_top_level;

architecture rtl of DE1_SoC_top_level is
begin
end;

```

Figure 10-1. DE1-SoC Top-level VHDL Entity

DRAFT

10.2 DE1-SoC PIN ASSIGNMENT TCL SCRIPT

After having defined a top-level module, it is necessary to map your design's pins to the ones available on the DE1-SoC. The following **TCL SCRIPT** can be executed in *Quartus II* to specify the board's device ID and all its **PIN ASSIGNMENTS**. The file can be found

at \\lapsrv1.epfl.ch\documentation\Altera\CycloneV\Distribution\pin_assignment_DE1_SoC.tcl.

```
#####
# pin_assignment_DE1_SoC.tcl
#
# BOARD      : DE1-SoC from Terasic
# Author     : Sahand Kashani-Akhavan from Terasic documentation
# Revision   : 1.0
# Creation date : 04/02/2015
#
# Syntax Rule : GROUP_NAME_N[bit]
#
# GROUP    : specify a particular interface (ex: SDR_)
# NAME     : signal name (ex: CONFIG, D, ...)
# bit      : signal index
# _N       : to specify an active-low signal
#
# You can run this script from Quartus by observing the following steps:
# 1. Place this TCL script in your project directory
# 2. Open your project in Quartus
# 3. Go to the View > Utility Windows -> Tcl Console
# 4. In the Tcl Console type:
#      source pin_assignment_DE1_SoC.tcl
#
# 5. The script will assign pins and return an "assignment made" message.
#####

set_global_assignment -name FAMILY "Cyclone V"
set_global_assignment -name DEVICE 5CSEMA5F31C6
set_global_assignment -name DEVICE_FILTER_PACKAGE FBGA
set_global_assignment -name DEVICE_FILTER_PIN_COUNT 896
set_global_assignment -name DEVICE_FILTER_SPEED_GRADE 6

=====
# ADC
=====
set_location_assignment PIN_AJ4 -to ADC_CS_N
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to ADC_CS_N
set_location_assignment PIN_AK4 -to ADC_DIN
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to ADC_DIN
set_location_assignment PIN_AK3 -to ADC_DOUT
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to ADC_DOUT
set_location_assignment PIN_AK2 -to ADC_SCLK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to ADC_SCLK

=====
# Audio
=====
set_location_assignment PIN_K7 -to AUD_ADCDAT
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to AUD_ADCDAT
set_location_assignment PIN_K8 -to AUD_ADCLRCK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to AUD_ADCLRCK
set_location_assignment PIN_H7 -to AUD_BCLK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to AUD_BCLK
```

```

set_location_assignment PIN_J7 -to AUD_DACDAT
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to AUD_DACDAT
set_location_assignment PIN_H8 -to AUD_DACLRCK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to AUD_DACLRCK
set_location_assignment PIN_G7 -to AUD_XCK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to AUD_XCK

#=====
# CLOCK
#=====
set_location_assignment PIN_AF14 -to CLOCK_50
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to CLOCK_50
set_location_assignment PIN_AA16 -to CLOCK2_50
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to CLOCK2_50
set_location_assignment PIN_Y26 -to CLOCK3_50
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to CLOCK3_50
set_location_assignment PIN_K14 -to CLOCK4_50
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to CLOCK4_50

#=====
# SDRAM
#=====
set_location_assignment PIN_AK14 -to DRAM_ADDR[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[0]
set_location_assignment PIN_AH14 -to DRAM_ADDR[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[1]
set_location_assignment PIN_AG15 -to DRAM_ADDR[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[2]
set_location_assignment PIN_AE14 -to DRAM_ADDR[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[3]
set_location_assignment PIN_AB15 -to DRAM_ADDR[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[4]
set_location_assignment PIN_AC14 -to DRAM_ADDR[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[5]
set_location_assignment PIN_AD14 -to DRAM_ADDR[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[6]
set_location_assignment PIN_AF15 -to DRAM_ADDR[7]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[7]
set_location_assignment PIN_AH15 -to DRAM_ADDR[8]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[8]
set_location_assignment PIN_AG13 -to DRAM_ADDR[9]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[9]
set_location_assignment PIN_AG12 -to DRAM_ADDR[10]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[10]
set_location_assignment PIN_AH13 -to DRAM_ADDR[11]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[11]
set_location_assignment PIN_AJ14 -to DRAM_ADDR[12]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[12]
set_location_assignment PIN_AF13 -to DRAM_BA[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_BA[0]
set_location_assignment PIN_AJ12 -to DRAM_BA[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_BA[1]
set_location_assignment PIN_AF11 -to DRAM_CAS_N
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_CAS_N
set_location_assignment PIN_AK13 -to DRAM_CKE
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_CKE
set_location_assignment PIN_AG11 -to DRAM_CS_N
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_CS_N
set_location_assignment PIN_AH12 -to DRAM_CLK

```

```

set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_CLK
set_location_assignment PIN_AK6 -to DRAM_DQ[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[0]
set_location_assignment PIN_AJ7 -to DRAM_DQ[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[1]
set_location_assignment PIN_AK7 -to DRAM_DQ[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[2]
set_location_assignment PIN_AK8 -to DRAM_DQ[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[3]
set_location_assignment PIN_AK9 -to DRAM_DQ[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[4]
set_location_assignment PIN_AG10 -to DRAM_DQ[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[5]
set_location_assignment PIN_AK11 -to DRAM_DQ[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[6]
set_location_assignment PIN_AJ11 -to DRAM_DQ[7]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[7]
set_location_assignment PIN_AH10 -to DRAM_DQ[8]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[8]
set_location_assignment PIN_AJ10 -to DRAM_DQ[9]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[9]
set_location_assignment PIN_AJ9 -to DRAM_DQ[10]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[10]
set_location_assignment PIN_AH9 -to DRAM_DQ[11]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[11]
set_location_assignment PIN_AH8 -to DRAM_DQ[12]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[12]
set_location_assignment PIN_AH7 -to DRAM_DQ[13]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[13]
set_location_assignment PIN_AJ6 -to DRAM_DQ[14]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[14]
set_location_assignment PIN_AJ5 -to DRAM_DQ[15]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[15]
set_location_assignment PIN_AB13 -to DRAM_LDQM
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_LDQM
set_location_assignment PIN_AE13 -to DRAM_RAS_N
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_RAS_N
set_location_assignment PIN_AK12 -to DRAM_UDQM
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_UDQM
set_location_assignment PIN_AA13 -to DRAM_WE_N
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_WE_N

#=====
# I2C for Audio and Video-In
#=====

set_location_assignment PIN_J12 -to FPGA_I2C_SCLK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to FPGA_I2C_SCLK
set_location_assignment PIN_K12 -to FPGA_I2C_SDAT
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to FPGA_I2C_SDAT

#=====
# SEG7
#=====

set_location_assignment PIN_AE26 -to HEX0_N[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX0_N[0]
set_location_assignment PIN_AE27 -to HEX0_N[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX0_N[1]
set_location_assignment PIN_AE28 -to HEX0_N[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX0_N[2]

```

```

set_location_assignment PIN_AG27 -to HEX0_N[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX0_N[3]
set_location_assignment PIN_AF28 -to HEX0_N[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX0_N[4]
set_location_assignment PIN_AG28 -to HEX0_N[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX0_N[5]
set_location_assignment PIN_AH28 -to HEX0_N[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX0_N[6]
set_location_assignment PIN_AJ29 -to HEX1_N[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX1_N[0]
set_location_assignment PIN_AH29 -to HEX1_N[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX1_N[1]
set_location_assignment PIN_AH30 -to HEX1_N[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX1_N[2]
set_location_assignment PIN_AG30 -to HEX1_N[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX1_N[3]
set_location_assignment PIN_AF29 -to HEX1_N[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX1_N[4]
set_location_assignment PIN_AF30 -to HEX1_N[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX1_N[5]
set_location_assignment PIN_AD27 -to HEX1_N[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX1_N[6]
set_location_assignment PIN_AB23 -to HEX2_N[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX2_N[0]
set_location_assignment PIN_AE29 -to HEX2_N[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX2_N[1]
set_location_assignment PIN_AD29 -to HEX2_N[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX2_N[2]
set_location_assignment PIN_AC28 -to HEX2_N[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX2_N[3]
set_location_assignment PIN_AD30 -to HEX2_N[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX2_N[4]
set_location_assignment PIN_AC29 -to HEX2_N[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX2_N[5]
set_location_assignment PIN_AC30 -to HEX2_N[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX2_N[6]
set_location_assignment PIN_AD26 -to HEX3_N[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX3_N[0]
set_location_assignment PIN_AC27 -to HEX3_N[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX3_N[1]
set_location_assignment PIN_AD25 -to HEX3_N[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX3_N[2]
set_location_assignment PIN_AC25 -to HEX3_N[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX3_N[3]
set_location_assignment PIN_AB28 -to HEX3_N[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX3_N[4]
set_location_assignment PIN_AB25 -to HEX3_N[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX3_N[5]
set_location_assignment PIN_AB22 -to HEX3_N[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX3_N[6]
set_location_assignment PIN_AA24 -to HEX4_N[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX4_N[0]
set_location_assignment PIN_Y23 -to HEX4_N[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX4_N[1]
set_location_assignment PIN_Y24 -to HEX4_N[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX4_N[2]
set_location_assignment PIN_W22 -to HEX4_N[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX4_N[3]
set_location_assignment PIN_W24 -to HEX4_N[4]

```

```

set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX4_N[4]
set_location_assignment PIN_V23 -to HEX4_N[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX4_N[5]
set_location_assignment PIN_W25 -to HEX4_N[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX4_N[6]
set_location_assignment PIN_V25 -to HEX5_N[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX5_N[0]
set_location_assignment PIN_AA28 -to HEX5_N[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX5_N[1]
set_location_assignment PIN_Y27 -to HEX5_N[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX5_N[2]
set_location_assignment PIN_AB27 -to HEX5_N[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX5_N[3]
set_location_assignment PIN_AB26 -to HEX5_N[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX5_N[4]
set_location_assignment PIN_AA26 -to HEX5_N[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX5_N[5]
set_location_assignment PIN_AA25 -to HEX5_N[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX5_N[6]

#=====
# IR
#=====
set_location_assignment PIN_AA30 -to IRDA_RXD
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to IRDA_RXD
set_location_assignment PIN_AB30 -to IRDA_TXD
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to IRDA_TXD

#=====
# KEY_N
#=====
set_location_assignment PIN_AA14 -to KEY_N[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to KEY_N[0]
set_location_assignment PIN_AA15 -to KEY_N[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to KEY_N[1]
set_location_assignment PIN_W15 -to KEY_N[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to KEY_N[2]
set_location_assignment PIN_Y16 -to KEY_N[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to KEY_N[3]

#=====
# LED
#=====
set_location_assignment PIN_V16 -to LEDR[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to LEDR[0]
set_location_assignment PIN_W16 -to LEDR[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to LEDR[1]
set_location_assignment PIN_V17 -to LEDR[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to LEDR[2]
set_location_assignment PIN_V18 -to LEDR[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to LEDR[3]
set_location_assignment PIN_W17 -to LEDR[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to LEDR[4]
set_location_assignment PIN_W19 -to LEDR[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to LEDR[5]
set_location_assignment PIN_Y19 -to LEDR[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to LEDR[6]
set_location_assignment PIN_W20 -to LEDR[7]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to LEDR[7]

```

```

set_location_assignment PIN_W21 -to LEDR[8]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to LEDR[8]
set_location_assignment PIN_Y21 -to LEDR[9]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to LEDR[9]

#=====
# PS2
#=====
set_location_assignment PIN_AD7 -to PS2_CLK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to PS2_CLK
set_location_assignment PIN_AD9 -to PS2_CLK2
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to PS2_CLK2
set_location_assignment PIN_AE7 -to PS2_DAT
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to PS2_DAT
set_location_assignment PIN_AE9 -to PS2_DAT2
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to PS2_DAT2

#=====
# SW
#=====
set_location_assignment PIN_AB12 -to SW[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to SW[0]
set_location_assignment PIN_AC12 -to SW[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to SW[1]
set_location_assignment PIN_AF9 -to SW[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to SW[2]
set_location_assignment PIN_AF10 -to SW[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to SW[3]
set_location_assignment PIN_AD11 -to SW[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to SW[4]
set_location_assignment PIN_AD12 -to SW[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to SW[5]
set_location_assignment PIN_AE11 -to SW[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to SW[6]
set_location_assignment PIN_AC9 -to SW[7]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to SW[7]
set_location_assignment PIN_AD10 -to SW[8]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to SW[8]
set_location_assignment PIN_AE12 -to SW[9]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to SW[9]

#=====
# Video-In
#=====
set_location_assignment PIN_H15 -to TD_CLK27
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to TD_CLK27
set_location_assignment PIN_D2 -to TD_DATA[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to TD_DATA[0]
set_location_assignment PIN_B1 -to TD_DATA[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to TD_DATA[1]
set_location_assignment PIN_E2 -to TD_DATA[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to TD_DATA[2]
set_location_assignment PIN_B2 -to TD_DATA[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to TD_DATA[3]
set_location_assignment PIN_D1 -to TD_DATA[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to TD_DATA[4]
set_location_assignment PIN_E1 -to TD_DATA[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to TD_DATA[5]
set_location_assignment PIN_C2 -to TD_DATA[6]

```

```

set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to TD_DATA[6]
set_location_assignment PIN_B3 -to TD_DATA[7]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to TD_DATA[7]
set_location_assignment PIN_A5 -to TD_HS
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to TD_HS
set_location_assignment PIN_F6 -to TD_RESET_N
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to TD_RESET_N
set_location_assignment PIN_A3 -to TD_VS
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to TD_VS

#=====
# VGA
#=====

set_location_assignment PIN_B13 -to VGA_B[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_B[0]
set_location_assignment PIN_G13 -to VGA_B[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_B[1]
set_location_assignment PIN_H13 -to VGA_B[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_B[2]
set_location_assignment PIN_F14 -to VGA_B[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_B[3]
set_location_assignment PIN_H14 -to VGA_B[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_B[4]
set_location_assignment PIN_F15 -to VGA_B[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_B[5]
set_location_assignment PIN_G15 -to VGA_B[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_B[6]
set_location_assignment PIN_J14 -to VGA_B[7]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_B[7]
set_location_assignment PIN_F10 -to VGA_BLANK_N
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_BLANK_N
set_location_assignment PIN_A11 -to VGA_CLK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_CLK
set_location_assignment PIN_J9 -to VGA_G[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_G[0]
set_location_assignment PIN_J10 -to VGA_G[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_G[1]
set_location_assignment PIN_H12 -to VGA_G[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_G[2]
set_location_assignment PIN_G10 -to VGA_G[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_G[3]
set_location_assignment PIN_G11 -to VGA_G[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_G[4]
set_location_assignment PIN_G12 -to VGA_G[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_G[5]
set_location_assignment PIN_F11 -to VGA_G[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_G[6]
set_location_assignment PIN_E11 -to VGA_G[7]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_G[7]
set_location_assignment PIN_B11 -to VGA_HS
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_HS
set_location_assignment PIN_A13 -to VGA_R[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_R[0]
set_location_assignment PIN_C13 -to VGA_R[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_R[1]
set_location_assignment PIN_E13 -to VGA_R[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_R[2]
set_location_assignment PIN_B12 -to VGA_R[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_R[3]

```



```

set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_GPIO[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_GSENSOR_INT
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_I2C1_SCLK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_I2C1_SDAT
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_I2C2_SCLK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_I2C2_SDAT
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_I2C_CONTROL
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_KEY
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_LED
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_SD_CLK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_SD_CMD
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_SD_DATA[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_SD_DATA[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_SD_DATA[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_SD_DATA[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_SPIM_CLK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_SPIM_MISO
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_SPIM_MOSI
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_SPIM_SS
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_UART_RX
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_UART_TX
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_USB_CLKOUT
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_USB_DATA[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_USB_DATA[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_USB_DATA[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_USB_DATA[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_USB_DATA[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_USB_DATA[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_USB_DATA[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_USB_DATA[7]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_USB_DIR
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_USB_NXT
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_USB_STP
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_CONV_USB_N

#=====
# GPIO_0, GPIO_0 connect to GPIO Default
#=====

set_location_assignment PIN_AC18 -to GPIO_0[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[0]
set_location_assignment PIN_Y17 -to GPIO_0[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[1]
set_location_assignment PIN_AD17 -to GPIO_0[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[2]
set_location_assignment PIN_Y18 -to GPIO_0[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[3]
set_location_assignment PIN_AK16 -to GPIO_0[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[4]
set_location_assignment PIN_AK18 -to GPIO_0[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[5]
set_location_assignment PIN_AK19 -to GPIO_0[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[6]
set_location_assignment PIN_AJ19 -to GPIO_0[7]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[7]
set_location_assignment PIN_AJ17 -to GPIO_0[8]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[8]
set_location_assignment PIN_AJ16 -to GPIO_0[9]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[9]
set_location_assignment PIN_AH18 -to GPIO_0[10]

```

```

set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[10]
set_location_assignment PIN_AH17 -to GPIO_0[11]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[11]
set_location_assignment PIN_AG16 -to GPIO_0[12]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[12]
set_location_assignment PIN_AE16 -to GPIO_0[13]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[13]
set_location_assignment PIN_AF16 -to GPIO_0[14]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[14]
set_location_assignment PIN_AG17 -to GPIO_0[15]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[15]
set_location_assignment PIN_AA18 -to GPIO_0[16]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[16]
set_location_assignment PIN_AA19 -to GPIO_0[17]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[17]
set_location_assignment PIN_AE17 -to GPIO_0[18]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[18]
set_location_assignment PIN_AC20 -to GPIO_0[19]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[19]
set_location_assignment PIN_AH19 -to GPIO_0[20]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[20]
set_location_assignment PIN_AJ20 -to GPIO_0[21]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[21]
set_location_assignment PIN_AH20 -to GPIO_0[22]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[22]
set_location_assignment PIN_AK21 -to GPIO_0[23]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[23]
set_location_assignment PIN_AD19 -to GPIO_0[24]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[24]
set_location_assignment PIN_AD20 -to GPIO_0[25]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[25]
set_location_assignment PIN_AE18 -to GPIO_0[26]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[26]
set_location_assignment PIN_AE19 -to GPIO_0[27]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[27]
set_location_assignment PIN_AF20 -to GPIO_0[28]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[28]
set_location_assignment PIN_AF21 -to GPIO_0[29]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[29]
set_location_assignment PIN_AF19 -to GPIO_0[30]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[30]
set_location_assignment PIN_AG21 -to GPIO_0[31]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[31]
set_location_assignment PIN_AF18 -to GPIO_0[32]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[32]
set_location_assignment PIN_AG20 -to GPIO_0[33]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[33]
set_location_assignment PIN_AG18 -to GPIO_0[34]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[34]
set_location_assignment PIN_AJ21 -to GPIO_0[35]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_0[35]

#=====
# GPIO_1, GPIO_1 connect to GPIO Default
#=====

set_location_assignment PIN_AB17 -to GPIO_1[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[0]
set_location_assignment PIN_AA21 -to GPIO_1[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[1]

```

```
set_location_assignment PIN_AB21 -to GPIO_1[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[2]
set_location_assignment PIN_AC23 -to GPIO_1[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[3]
set_location_assignment PIN_AD24 -to GPIO_1[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[4]
set_location_assignment PIN_AE23 -to GPIO_1[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[5]
set_location_assignment PIN_AE24 -to GPIO_1[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[6]
set_location_assignment PIN_AF25 -to GPIO_1[7]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[7]
set_location_assignment PIN_AF26 -to GPIO_1[8]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[8]
set_location_assignment PIN_AG25 -to GPIO_1[9]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[9]
set_location_assignment PIN_AG26 -to GPIO_1[10]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[10]
set_location_assignment PIN_AH24 -to GPIO_1[11]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[11]
set_location_assignment PIN_AH27 -to GPIO_1[12]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[12]
set_location_assignment PIN_AJ27 -to GPIO_1[13]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[13]
set_location_assignment PIN_AK29 -to GPIO_1[14]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[14]
set_location_assignment PIN_AK28 -to GPIO_1[15]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[15]
set_location_assignment PIN_AK27 -to GPIO_1[16]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[16]
set_location_assignment PIN_AJ26 -to GPIO_1[17]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[17]
set_location_assignment PIN_AK26 -to GPIO_1[18]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[18]
set_location_assignment PIN_AH25 -to GPIO_1[19]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[19]
set_location_assignment PIN_AJ25 -to GPIO_1[20]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[20]
set_location_assignment PIN_AJ24 -to GPIO_1[21]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[21]
set_location_assignment PIN_AK24 -to GPIO_1[22]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[22]
set_location_assignment PIN_AG23 -to GPIO_1[23]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[23]
set_location_assignment PIN_AK23 -to GPIO_1[24]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[24]
set_location_assignment PIN_AH23 -to GPIO_1[25]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[25]
set_location_assignment PIN_AK22 -to GPIO_1[26]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[26]
set_location_assignment PIN_AJ22 -to GPIO_1[27]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[27]
set_location_assignment PIN_AH22 -to GPIO_1[28]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[28]
set_location_assignment PIN_AG22 -to GPIO_1[29]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[29]
set_location_assignment PIN_AF24 -to GPIO_1[30]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[30]
set_location_assignment PIN_AF23 -to GPIO_1[31]
```

```
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[31]
set_location_assignment PIN_AE22 -to GPIO_1[32]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[32]
set_location_assignment PIN_AD21 -to GPIO_1[33]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[33]
set_location_assignment PIN_AA20 -to GPIO_1[34]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[34]
set_location_assignment PIN_AC22 -to GPIO_1[35]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO_1[35]
```

Figure 10-2. DE1-SoC Pin Assignment TCL Script



11 REFERENCES

- [1] Terasic Technologies, "Terasic - DE Main Boards - Cyclone - DE1-SoC Board," [Online]. Available: <http://de1-soc.terasic.com>.
- [2] Altera Corporation, "Cyclone V Device Handbook, Volume 3: Hard Processor System Technical Reference Manual," 31 July 2014. [Online]. Available: http://www.altera.com/literature/hb/cyclone-v/cv_5v4.pdf.
- [3] ARM, "DS-5 Debugger Commands," [Online]. Available: <http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.dui0452c/CIHJIBIH.html>.
- [4] Altera Corporation, "Cyclone V Device Handbook, Volume 1: Device Interfaces and Integration," 22 July 2014. [Online]. Available: http://www.altera.com/literature/hb/cyclone-v/cv_5v2.pdf.
- [5] Altera Corporation, "Documentation: Cyclone V Devices," [Online]. Available: http://www.altera.com/literature/lit-cyclone-v.jsp?ln=devices_fpga&l3=Low-Cost%20FPGAs-Cyclone%20V%20%28E,%20GX,%20GT,%20SE,%20SX,%20ST%29&l4=Documentation.
- [6] Altera Corporation, "Address Map for HPS," [Online]. Available: <http://www.altera.com/literature/hb/cyclone-v/hps.html>.
- [7] Altera Corporation, "A Look Inside: SoC FPGAs Embedded Development Tools (Part 5 of 5)," 25 November 2013. [Online]. Available: <http://www.youtube.com/watch?v=NxZznnf5EKc>.
- [8] Altera Corporation, "A Look Inside: SoC FPGAs Introduction (Part 1 of 5)," 25 November 2013. [Online]. Available: <http://www.youtube.com/watch?v=RVM-ESUMOMU>.
- [9] Altera Corporation, "A Look Inside: SoC FPGAs Reliability and Flexibility (Part 3 of 5)," 25 November 2013. [Online]. Available: <http://www.youtube.com/watch?v=cWlaqt2RU84>.
- [10] Altera Corporation, "A Look Inside: SoC FPGAs System Cost and Power (Part 4 of 5)," 25 November 2013. [Online]. Available: <http://www.youtube.com/watch?v=gUE669XKhUY>.
- [11] Altera Corporation, "A Look Inside: SoC FPGAs System Performance (Part 2 of 5)," 25 November 2013. [Online]. Available: <http://www.youtube.com/watch?v=Ssxf8ggmQk4>.
- [12] Altera Corporation, "Cyclone V Device Datasheet," July 2014. [Online]. Available: http://www.altera.com/literature/hb/cyclone-v/cv_51002.pdf.
- [13] ARM, "DS-5 Altera Edition: Bare-metal Debug and Trace," 21 October 2013. [Online]. Available: http://www.youtube.com/watch?v=u_xKybPhchI.
- [14] ARM, "FPGA-adaptive debug on the Altera SoC using ARM DS-5," 16 December 2013. [Online]. Available: <http://www.youtube.com/watch?v=2NBcUv2Txbl>.
- [15] EE Journal, "OpenCL on FPGAs Accelerating Performance and Design Productivity -- Altera," 28 November 2013. [Online]. Available: http://www.youtube.com/watch?v=M6vpq6s1h_A.
- [16] Altera Corporation, "Bare-Metal Debugging using ARM DS-5 Altera Edition," 3 December 2013. [Online]. Available: <http://www.youtube.com/watch?v=CJ0EHJ9oQ7Y>.

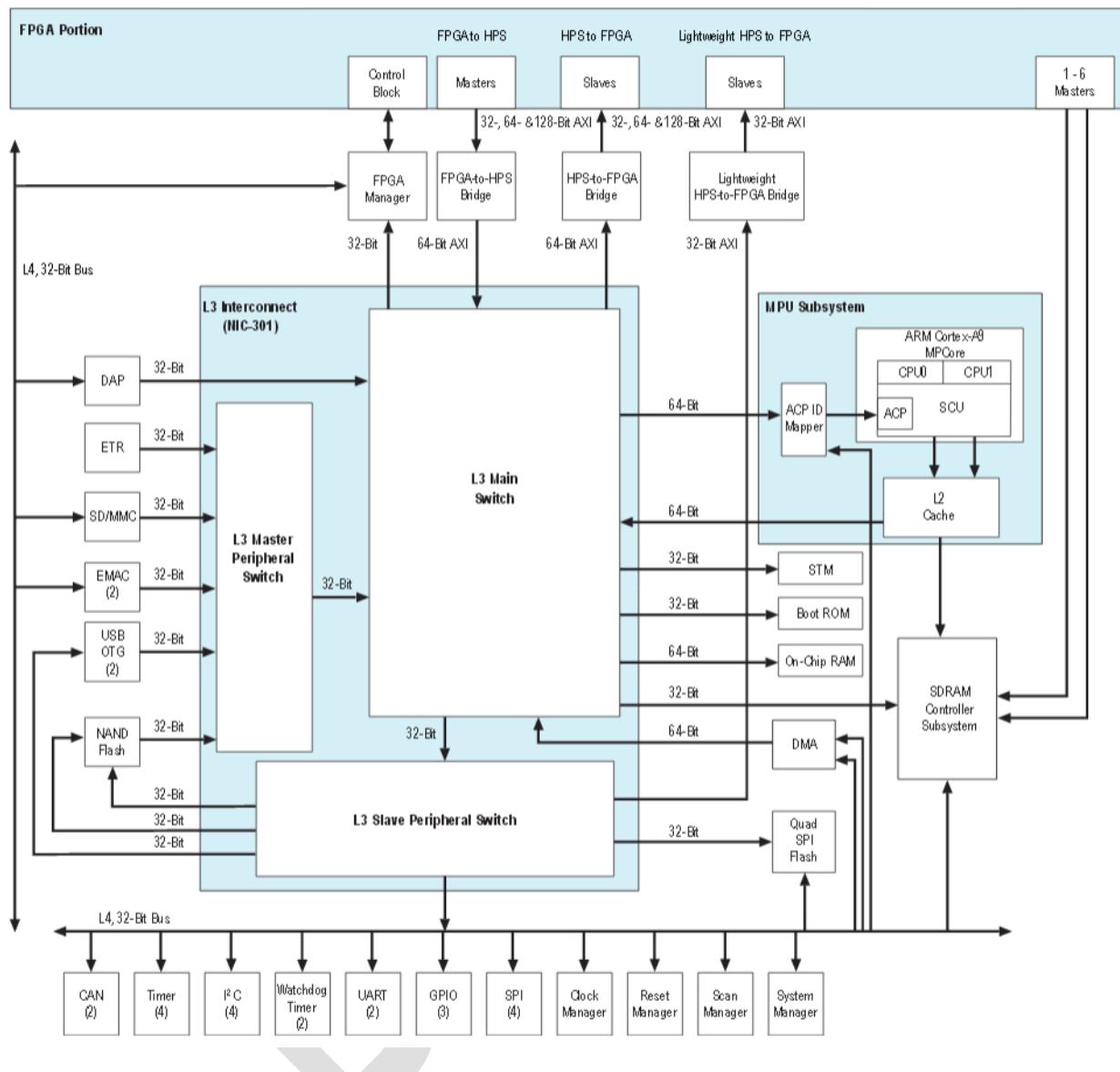
- [17] Altera Corporation, "Cyclone V Device Overview," 7 July 2014. [Online]. Available: http://www.altera.com/literature/hb/cyclone-v/cv_51001.pdf.
- [18] Altera Corporation, "Linux Kernel Debug using ARM DS-5 Altera Edition," 3 December 2013. [Online]. Available: <http://www.youtube.com/watch?v=QcA39O6ofGw>.
- [19] Altera Corporation, "Architecting FPGAs beyond 1M LEs," Altera Corporation, 3 September 2014. [Online]. Available: <http://www.fpl2014.org/fileadmin/w00bpo/www/hutton.pdf>.

DRAFT

12SOC PART TEST

12.1 HPS ARCHITECTURE

To be able to program the ARM9's processors it is almost necessary to have the global view of the HPS architecture.



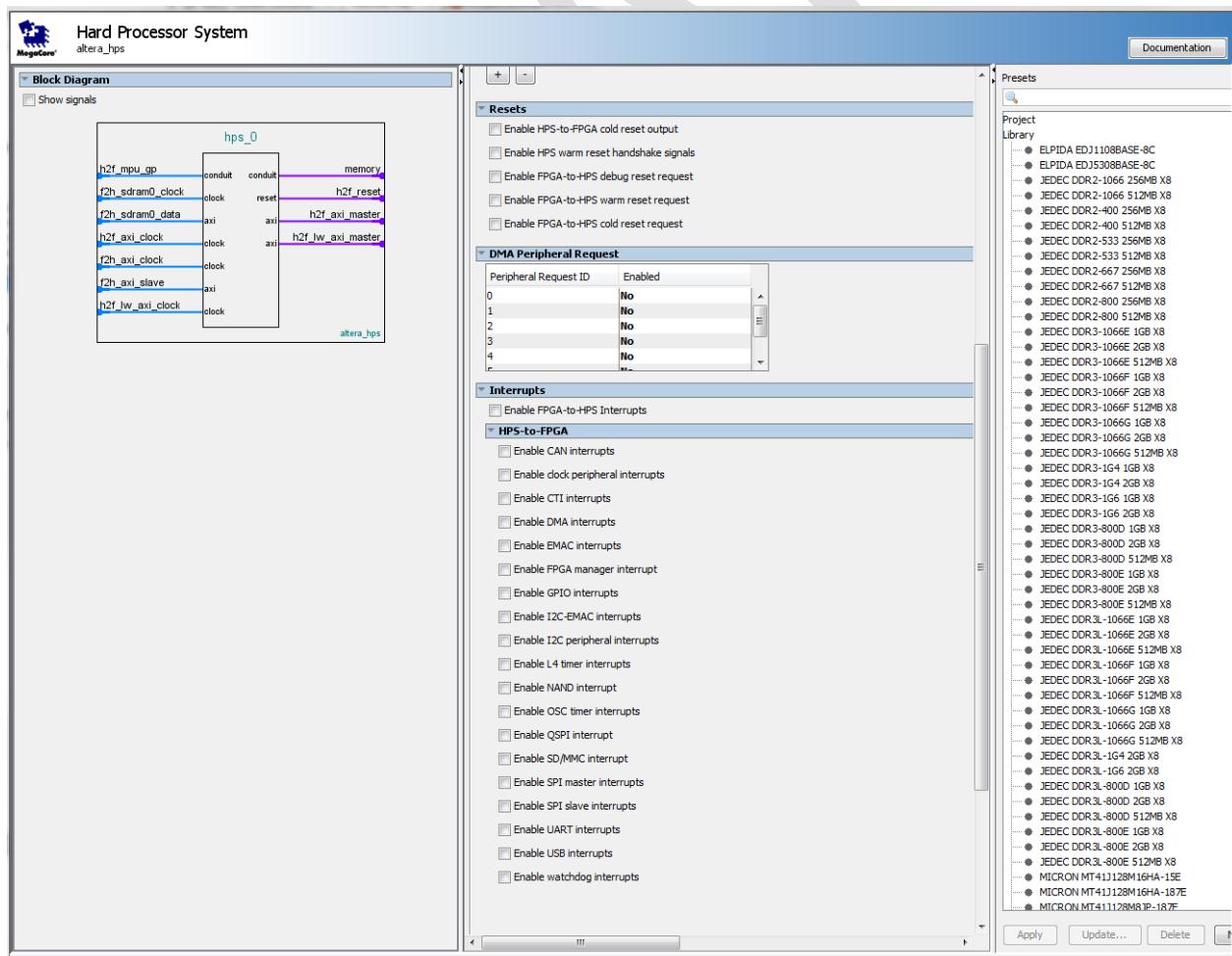
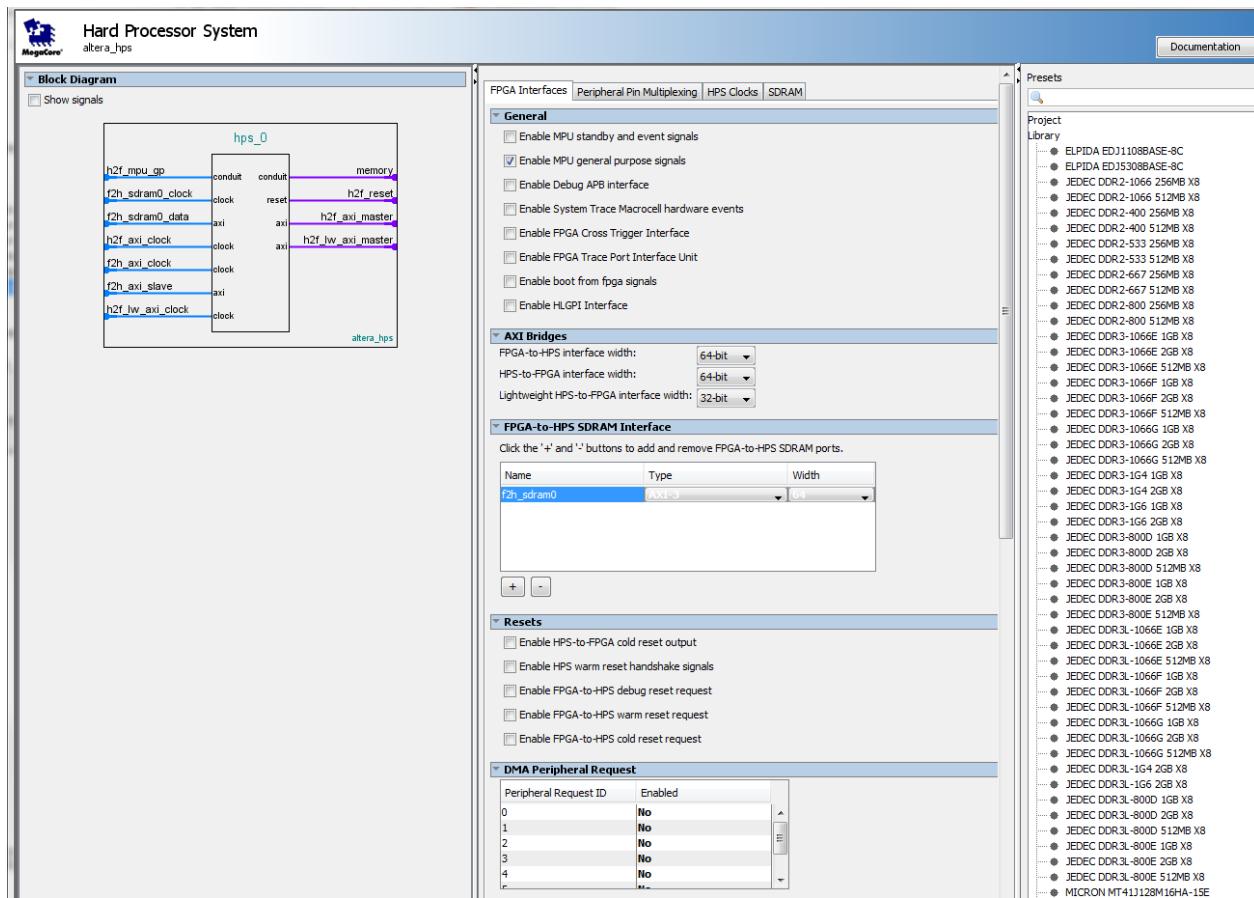
12.2 HARDWARE DEVELOPMENT

12.2.1 Qsys integration

Starting with **QuartusII** and after creating a project, select **Tools → Qsys**

In **Qsys**, open **Library → Embedded Processors → Hard Processor System** the window with description of the parameters for the HPS is open.

The **FPGA Interface** tab allows the access from to the FPGA part with the HPS part.



With the ***Peripheral Pin Multiplexing***, some I/O interface can be used by the HPS part or the FPGA part. The selection is done here.

12.3 SOFTWARE DEVELOPMENT

12.3.1 ARM DS-5 tools

They are some differences between the versions of DS-5.

The one installed for the test is:

ARM DS-5 (DS-5 Altera Edition (Evaluation))
 Version: 5.18.0
 Build number: 5180018

12.3.2 Hello World on ARM HPS part

Copy the directory from Altera examples:

C:\altera\[vers]\embedded\examples\software

And un-gz the file: Altera-SoCFPGA-HelloWorld-Baremetal-ARMCC.tar.gz

Then un-tar it.

The directory **Altera-SoCFPGA-HelloWorld-Baremetal-ARMCC** can then be copied in the Eclipse WorkSpace and Imported as a new project. The files inside are:

- .cproject used by Eclipse
- .project used by Eclipse
- ****.launch ??
- Makefile for the Compiler/Assembler/Linker
 An important info is the flag for the cpu: --cpu=Cortex-A9.no_neon.no_vfp
- scatter.scat Info for the compiler for the Code, Data, Stack and Heap addresses
 in this case in the internal SRAM

12.3.2.1 Scatter.scat

```
*****
; Copyright (c) 2013 Altera All Rights Reserved.
*****

; Scatter-file for OnChip RAM based example
; This scatter-file places application code, data, stack and heap at suitable addresses in the memory map.

; Altera SoC-FPGA has 64kB of internal OnChip RAM

OCRAM 0xFFFF0000 0x10000
{
    APP_CODE +0

    {
        * (+RO, +RW, +ZI)
    }
}
```

```
ARM_LIB_STACKHEAP 0xFFFF8000 EMPTY 0x8000 ; Application heap and stack
{ }
}
```

12.3.2.2 Makefile

Makefile for the ARM compiler

```
# Copyright (C) ARM Limited, 2011. All rights reserved.
#
# This example is intended to be built with the ARM Compiler armcc

TARGET=Altera-SoCFPGA-HelloWorld-Baremetal-ARMCC.axf

CC=armcc
AS=armasm
LD=armlink
AR=armar

# Select build rules based on Windows or Unix
ifdef WINDIR
DONE=@if exist $(1) echo Build completed.
RM=if exist $(1) del /q $(1)
SHELL=$(WINDIR)\system32\cmd.exe
else
ifndef windir
DONE=@if exist $(1) echo Build completed.
RM=if exist $(1) del /q $(1)
SHELL=$(windir)\system32\cmd.exe
else
DONE=@if [ -f $(1) ]; then echo Build completed.; fi
RM=rm -f $(1)
endif
endif

all: $(TARGET)
    $(call DONE,$(TARGET))

rebuild: clean all

clean:
    $(call RM,*.o)
    $(call RM,$(TARGET))

hello.o: hello.c
    $(CC) -c -g --cpu=Cortex-A9.no_neon.no_vfp -O0 hello.c

$(TARGET): hello.o scatter.scat
    $(LD) hello.o -o $(TARGET) --cpu=Cortex-A9.no_neon.no_vfp --scatter=scatter.scat
```

12.3.3 [4]GPIO access

The references for gpio are:

- http://www.altera.com/literature/hb/cyclone-v/cv_54022.pdf

- <http://www.altera.com/literature/hb/cyclone-v/hps.html>
- Supports up to 71 I/O pins and 14 input-only pins depend on device variant

On de1-soc:

- Only 1 Button for HPS GPIO 1
- Only 1 LED for HPS GPIO 1

Pin Name	HPS GPIO	Register [bit]	Function	Address	Dir
HPS_KEY	GPIO54	GPIO1[25]	I/O	0xFF20 9000	In
HPS_LED	GPIO53	GPIO1[24]	I/O	0xFF20 9000	Out

HPS peripherals are mapped to HPS base address space 0xFC00 0000 with 64KB size.

Registers of GPIO0 controller are mapped to the base address 0xFF20 8000 - 0xFF20 8FFF (4KB size)

Registers of GPIO1 controller are mapped to the base address 0xFF20 9000 - 0xFF20 9FFF (4KB size)

Registers of GPIO2 controller are mapped to the base address 0xFF20 A000 - 0xFF20 8FFF (4KB size)

		http://www.altera.com/literature/hb/cyclone-v/cv_5v4.pdf		
GPIO0	0xFF20 8000 - 0xFF20 8FFF	0xFF70 8000		
GPIO1	0xFF20 9000 - 0xFF20 9FFF	0xFF70 9000		
GPIO2	0xFF20 A000 - 0xFF20 8FFF	0xFF70 A000		
LWFGASLAVES		0xFF20 0000		

gpio0	0xFF70 8000	HPS_GPIO0_ADDRESS	HPS_GPIO0_OFFSET	
gpio_swporta_dr	0	HPS_GPIO0_GPIO_SWPORTA_DR_ADDRESS	GPIO_GPIO_SWPORTA_DR_OFFSET	
gpio_swporta_ddr	0x04	HPS_GPIO0_GPIO_SWPORTA_DDR_ADDRESS	GPIO_GPIO_SWPORTA_DDR_OFFSET	
gpio_inten	0x30	HPS_GPIO0_GPIO_INTEN_ADDRESS	GPIO_GPIO_INTEN_OFFSET	
gpio_intmask	0x34	HPS_GPIO0_GPIO_INTMASK_ADDRESS	GPIO_GPIO_INTMASK_OFFSET	
gpio_inttype_level	0x38	HPS_GPIO0_GPIO_INTTYPE_LEVEL_ADDRESS	GPIO_GPIO_INTTYPE_LEVEL_OFFSET	
gpio_int_polarity	0x3c	HPS_GPIO0_GPIO_INT_POLARITY_ADDRESS	GPIO_GPIO_INT_POLARITY_OFFSET	
gpio_intstatus	0x40	HPS_GPIO0_GPIO_INTSTATUS_ADDRESS	GPIO_GPIO_INTSTATUS_OFFSET	
gpio_raw_intstatus	0x44	HPS_GPIO0_GPIO_RAW_INTSTATUS_ADDRESS	GPIO_GPIO_RAW_INTSTATUS_OFFSET	
gpio_debounce	0x48	HPS_GPIO0_GPIO_DEBOUNCE_ADDRESS	GPIO_GPIO_DEBOUNCE_OFFSET	
gpio_porta_eoi	0x4c	HPS_GPIO0_GPIO_PORTA_EOI_ADDRESS	GPIO_GPIO_PORTA_EOI_OFFSET	
gpio_ext_porta	0x50	HPS_GPIO0_GPIO_EXT_PORTA_ADDRESS	GPIO_GPIO_EXT_PORTA_OFFSET	
gpio_ls_sync	0x60	HPS_GPIO0_GPIO_LS_SYNC_ADDRESS	GPIO_GPIO_LS_SYNC_OFFSET	
gpio_id_code	0x64	HPS_GPIO0_GPIO_ID_CODE_ADDRESS	GPIO_GPIO_ID_CODE_OFFSET	
gpio_ver_id_code	0x6c	HPS_GPIO0_GPIO_VER_ID_CODE_ADDRESS	GPIO_GPIO_VER_ID_CODE_OFFSET	
gpio_config_reg2	0x70	HPS_GPIO0_GPIO_CONFIG_REG2_ADDRESS	GPIO_GPIO_CONFIG_REG2_OFFSET	
gpio_config_reg1	0x74	HPS_GPIO0_GPIO_CONFIG_REG1_ADDRESS	GPIO_GPIO_CONFIG_REG1_OFFSET	

12.3.3.1 Library installation

C:\altera\[vers]\embedded\ip\altera\hps\altera_hps\hwlib

HERE

12.3.3.2 Reference files

hps.h		