Digital IC Functionality Duplication Using Neural Networks

RESEARCH PROBLEM

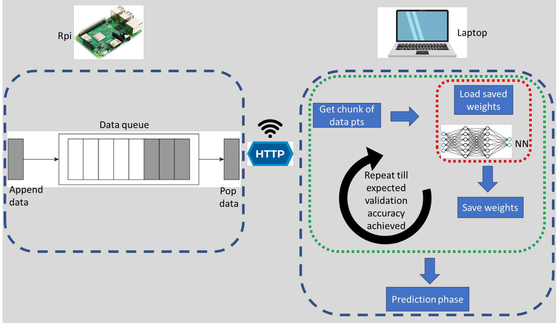
- Novel method for duplicating both known and unknown digital circuits using neural networks (NNs).
- Our approach involves training a common NN model on the inputs and outputs of existing digital circuits, creating a flexible and economical digital twin.

Affordable, Time efficient, Ease of use

OBJECTIVE

- Reverse engineering IC functionality through input-output observation, with a specific emphasis on digital sequential circuits.

METHODOLOGY



Continuous data feed to the Rpi

- Current setup involves transmitting circuit data to a Raspberry Pi using RS232, queuing the data on the Raspberry Pi.
- The Raspberry Pi serves as an intermediate node by queuing the received circuit data.

Transmitting Data from RPi to Laptop

- The Raspberry Pi uses Wi-Fi to transmit queued circuit data to the laptop via HTTP.

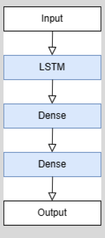
Multi-threading and Data Popping

- To manage the constant stream of data and its processing.
- This facilitates the simultaneous execution of multiple threads, enabling the extraction of data from the queue and its transmission to the laptop, while new data is received and added to the queue.

Neural Network Processing on Laptop

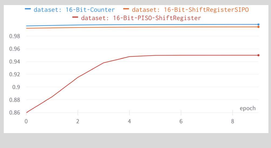
- Runs on the laptop, and efficiently processes the circuit data it receives.

PROPOSED NEURAL NETWORK



- Based on the performance results obtained above, the best model architecture is chosen to be one with **one LSTM layer** containing **32 nodes** and **two hidden dense layers**, each with **64 nodes**.

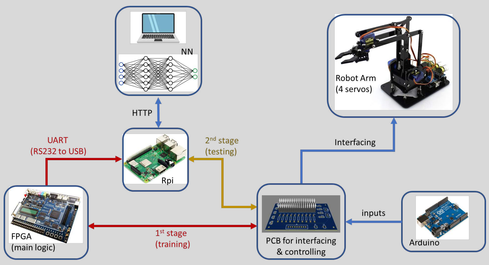
RESULTS

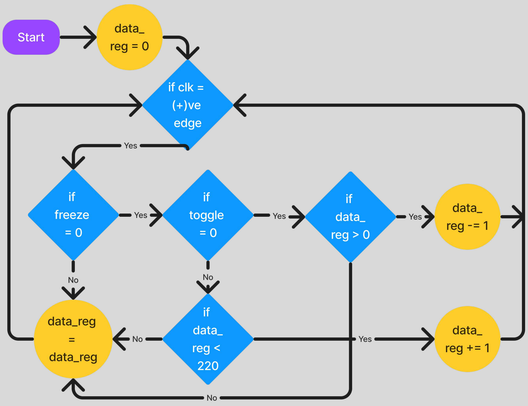


Our results affirm the approach's potential for precise emulation of digital circuit functionality across diverse designs and sizes, confirming its feasibility.

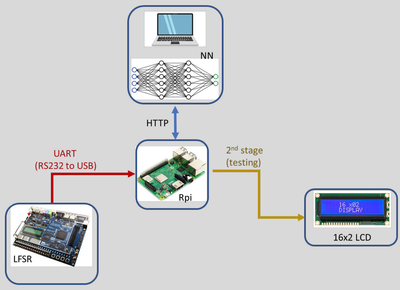
DEMONSTRATION

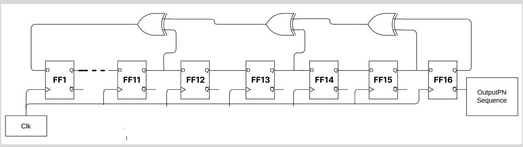
4 DOF Servo Arm



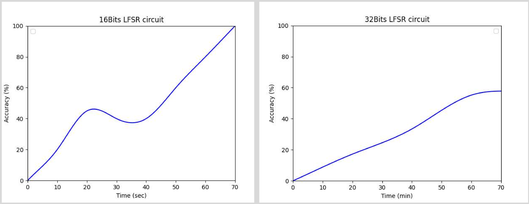


16 Bit LFSR





Converging plots



DELIVERABLES

- A comprehensive system designed to duplicate digital circuits, comprising of continuous **data capturing**, **real-time training**, and **synchronized predictions**.

CONCLUSION

- Results showcase the viability and potential of this approach for precise replication of digital circuit functionality with diverse designs and sizes.
- We anticipate that our findings will inspire further research and development in this field, fostering enhanced efficiency and effectiveness in digital circuit testing.

Group 01 - Members :
H.M.A.M. Bandara
T.M.S. Nayanajith
Y.A.A.W. Rajakaruna
P.S.C. Jayapala

Project Supervisor :
Dr. Thayaparan Subramaniam

ENTC
Electronic and Telecommunication Engineering