BJT AMPLIFIER DESIGN

A report submitted to the

Department of Electrical and Information Engineering

Faculty of Engineering

University of Ruhuna Sri Lanka

On 20th SEP 2023

In completing an assignment for the module

EE 4105 – Electronics Project

By

Group 17

EG/2020/4036	KUMARI H.M.M.S
EG/2020/4038	KURUWITAARACHCHI K.A.D.T.T
EG/2020/4040	LAKPAHANA A.G.S
EG/2020/4044	LAKSHANI P.N.K
EG/2020/4047	LELWALA L.G.S.R

ABSTRACT

This project report primarily revolves around the construction of a common emitter BJT amplifier that meets specific criteria for gain and bandwidth. It encompasses the entire journey of creating this amplifier, starting from the initial idea to the final product. This comprehensive process includes defining design specifications, performing critical calculations, simulating the circuit, designing the PCB layout, physically building the amplifier, analyzing the results, and drawing meaningful conclusions.

PERFACE

In the scope of our EE4105 - Electronic Project module, our team effectively tackled the challenge of crafting a customized BJT amplifier with precise gain and bandwidth specifications. This project provided us with invaluable insights into the intricacies of BJT amplifier design. The following report serves as a detailed record of our discoveries and accomplishments throughout this journey. We would like to express our sincere gratitude to Mr. Saman De Silva, our instructor for the EE4105 module in the Department of Electrical and Electronic Engineering, for granting us the opportunity to compile this report and for his continuous guidance and motivation.

Group 17:

EG/2020/4036	KUMARI H.M.M.S
EG/2020/4038	KURUWITAARACHCHI K.A.D.T.T
EG/2020/4040	LAKPAHANA A.G.S
EG/2020/4044	LAKSHANI P.N.K
EG/2020/4047	LELWALA L.G.S.R

Department of Electrical and Information Engineering,

University of Ruhuna.

TABLE OF CONTENT

ABSTRACT 2

PERFACE 3

TABLE OF CONTENT 4

LIST OF FIGURES 6

1. Introduction 7

1.1. Problem Statement 7

1.2. Objectives 7

1.3. Methodology 8

2. Design of the Amplifier 9

2.1. Top Level Construction of the Design 9

2.1.1. Input Buffer 9

2.1.2. Filter 9

2.1.3. First Amplifier 10

2.1.4. Middle Buffer 10

2.1.5. Second Amplifier 10

2.1.6. Output Buffer 11

2.2. Transistor Selection 11

2.3. Calculations 11

2.3.1. Input Buffer 12

2.3.2. Filter 14

2.3.3. First Amplifier 19

2.3.4. Middle Buffer 23

2.3.5. Second Amplifier 25

2.3.6. Output Buffer 28

2.3.7. Assembles Amplifier Design 31

3. Implementation of the Circuit 32

3.1. Schematic Diagram of the Amplifier 32

3.2. PCB Layout of the Amplifire 32

3.3. 3D Visualizer Views of the Amplifier 33
3.4. Copper Traces of PCB Layout 34
3.5. Physical Implementation 35
4. Result and Discussion 36
4.1. Simulation Result 36
4.2. Experimental Results 38
4.3. Discussion 39
- Temperature Effects: 39

LIST OF FIGURES

Figure 1 : Block Diagram of the Amplifier Circuit 9
Figure 2 : Input Buffer Circuit 12
Figure 3 : Frequency Response of the Input Buffer Circuit 14
Figure 4 : Second Order Low Pass Butterworth Filter General Configuration 14
Figure 5 : Filter Circuit 18
Figure 6 : Frequency Response of the Filter Circuit 19
Figure 7 : First Amplifier (20Gain) Circuit 22
Figure 8 : Frequency Response up to First Amplifire Output 22
Figure 9 : Middle Buffer Circuit 24
Figure 10 : Second Amplifier (20 Gain) Circuit 27
Figure 11 : Frequency Response up to Second Amplifier Output 28
Figure 12 : Output Buffer Circuit 30
Figure 13 : Assembled Amplifier Design 31
Figure 14 : Frequency Response of the Assembled Amplifier 31
Figure 15 : Final Schematic Design of the Circuit 32
Figure 16 : Final PCB Layout of the Circuit 32
Figure 17 : 3D Visualizer View of the Final Circuit 33
Figure 18 : Component Placement with Copper Traces 34
Figure 19 : Copper Traces 34
Figure 20: Photo of the PCB 35
Figure 21 : Simulation Oscilloscope Result 36
Figure 22 : Simulation of Frequency Response 37

1. Introduction

The common emitter amplifier, which is a voltage amplification circuit, consists of a three-terminal bipolar junction transistor in a single-stage configuration. In this setup, it acquires its input signal via the base terminal, collects the amplified output from the collector terminal, and links the emitter terminal to both the input and output sides.

This single-stage common emitter amplifier circuit relies on Voltage Divider Biasing, a specific biasing technique. Within this method, two resistors form a voltage division network across the power supply, and the midpoint of this network generates the necessary base bias voltage for the transistor. Voltage divider biasing is a widely adopted strategy when designing amplifier circuits based on bipolar transistors.

1.1. Problem Statement

The project task was to implement a Common Emitter BJT amplifier with the following Specifications.

- Voltage gain = 400
- Bandwidth of Low Pass Filter = 1.5kHz

This amplifier is designed to amplify weak audio signals, eliminate unwanted high-frequency noise, and invert the signal's phase as needed in audio applications.

1.2. Objectives

- By having a knowledge about how BJT is amplify by controlling the current flow we have to understand the construction and working principle of BJT amplifiers
- Component values like resistors and capacitors are calculated based on given specifications to ensure the circuit's intended performance
- Sketch and simulate the designed common emitter amplifier circuit by proteus for insights into its behavior.
- Implementation on a PCB layout requires precision in component placement and routing, often visualized in 3D.
- Comparing the theoretical and experimental results checks the design and helps make it better, showing how electronics engineering often involves trying, testing, and improving

1.3. Methodology

- Gather information like how much it should amplify the signal, what frequencies it should work with on the BJT common emitter amplifier to compute component values.
- Select an appropriate transistors based on the calculated voltage and current values.
- Develop a block diagram that illustrates the amplifier and filter stages.
- Perform the necessary calculations to determine component values according to specified characteristics.
- Utilize Proteus software to simulate the designed circuit. This helps you to see the design works on the computer properly and if there are any issues, fix them through troubleshooting.
- Implement the circuit design on a printed circuit board
- Concluding the theoretical and practical performances of the design by mentioning the conclusions of this report.
- Preparing and presenting the final design and the report.

2. Design of the Amplifier

2.1. Top Level Construction of the Design

In the amplifier design, it is expected the amplifier gain should be 400 and the bandwidth should be 1.5kHz.

The 400 gain is somewhat higher gain than the normal cases. So we cannot achieve this through only one amplifier. So here two amplifiers are used cascading. Then for the achieve bandwidth requirement, filter is used and the buffer circuits ensure the input/output impedance matching at various stages as the beginning, middle of two amplifiers and the end of the amplifier in the amplifier circuit.

The block diagram of the amplifier circuit as follows.

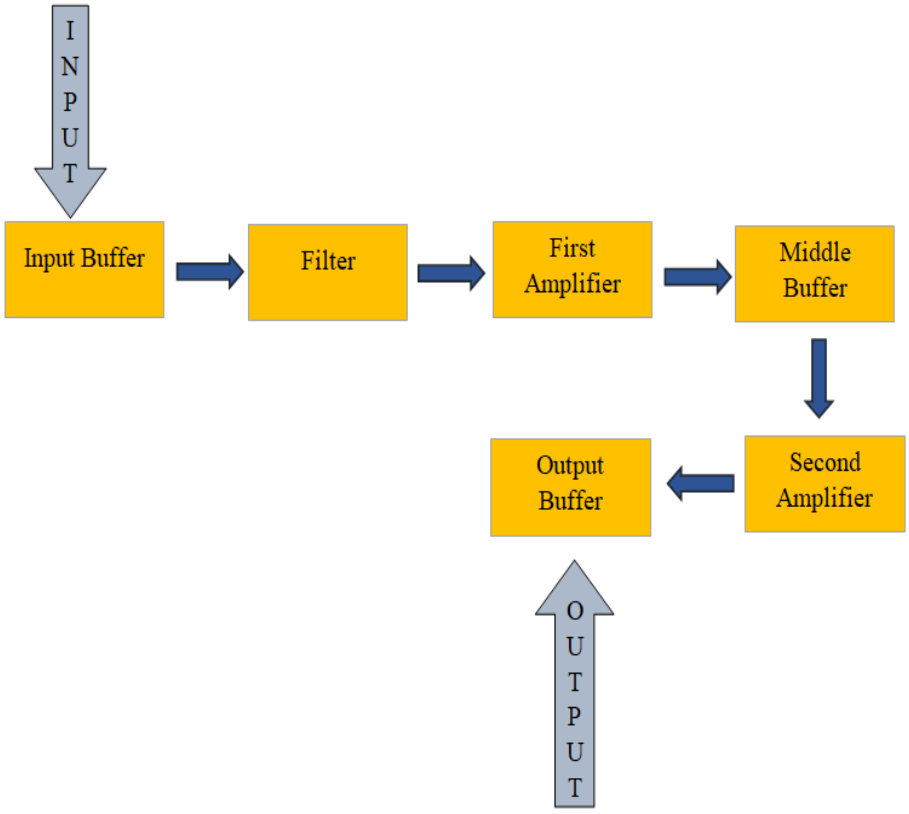


Figure 1 : Block Diagram of the Amplifier Circuit

2.1.1. Input Buffer

The BJT Common collector amplifier is used as input buffer to match the impedance of input signal source with the amplifier. The gain is nearly about 1 and the bandwidth is much higher than 1.5kHz.

2.1.2. Filter

Second order low pass Butterworth filter is used for achieve the bandwidth of 1.5kHz. The filter gain is about 1. Then bandwidth is 1.5kHz.

2.1.3. First Amplifier

The BJT Common-emitter amplifier is used as first amplifier for the circuit. The gain of the first amplifier is 20. Bandwidth is much more than 1.5kHz.

2.1.4. Middle Buffer

The BJT Common collector amplifier is use as middle buffer to match the output impedance of the first filter and the input of the second filter. The gain is about 1 and bandwidth is much more than 1.5kHz.

2.1.5. Second Amplifier

The BJT Common-emitter amplifier is used as second amplifier for the circuit. The gain of the second amplifier is 20. Bandwidth is much more than 1.5kHz.

2.1.6. Output Buffer

The BJT Common collector amplifier is use as output buffer to match the output impedance of the second filter and the output source. The gain is about 1 and bandwidth is much more than 1.5kHz.

2.2. Transistor Selection

The 2N3904 NPN transistor is used for all the stages as transistor for this amplifier circuit. This 2N3904 transistor is used for input buffer, filter, first amplifier, middle buffer, second amplifier and output amplifier in the circuit.

Common properties for this transistor is as follow.

- Continuous Collector Current - 200mA
- DC Current Gain(Minimum) - 100
- Input Capacitive - 8pF

2.3. Calculations

Calculations for the all the buffers, filter and the amplifiers are able to done isolating each section form others because the effect of one section is not depend on other stages.

It is chose 12V as power supply for the amplifier circuit. All the parts in the amplifier is powered by 12V DC power supply.

2.3.1. Input Buffer

As above mentioned Common Collector amplifier is used as input buffer for the circuit. The construction of the common collector amplifier as shown in the below.

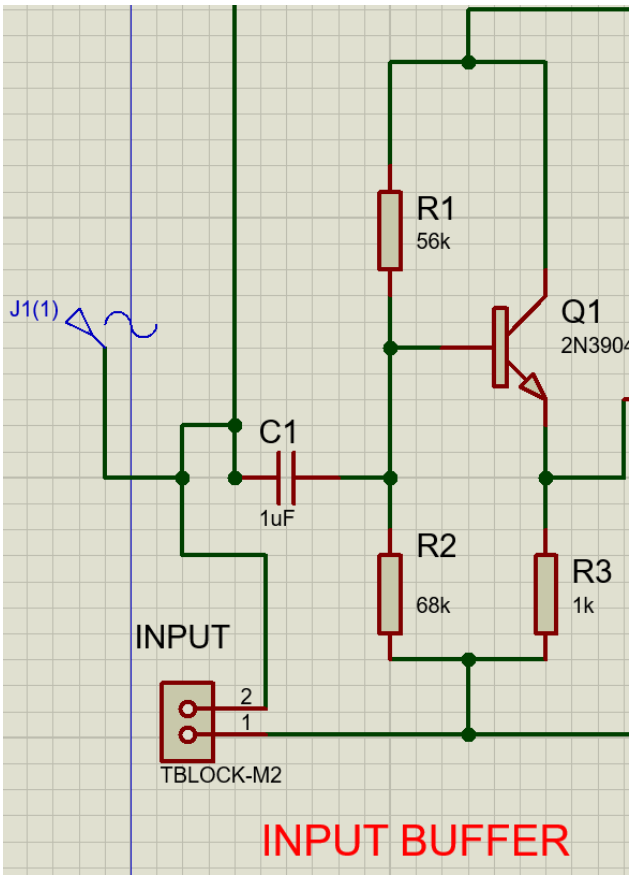


Figure 2 : Input Buffer Circuit

Calculations:

For a largest possible symmetric output voltage swing,

$$V_E = \frac{1}{2}V_{CC}$$

$$V_E = \frac{1}{2} \times 12V$$

$$V_E = 6V$$

Then the Q point used for the calculations,

$$V_{CE} = 6V$$

$$I_C = 6mA$$

Normally $I_C \approx I_E$,

Then Emitter resistor value,

$$R_E = \frac{V_E}{I_E}$$

$$R_3 = \frac{6V}{6mA}$$

$$R_3 = 1k\Omega$$

Base voltage of Q_1 transistor,

$$V_B = V_E + 0.7V$$

$$V_B = 6V + 0.7V$$

$$V_B = 6.7V$$

Then R_1 and R_2 values are,

$$V_B = \frac{R_2 \times V_{CC}}{R_1 + R_2}$$

$$V_B = 6.7\text{V}$$

$$6.7V = \frac{R_2 \times 12V}{R_1 + R_2}$$

$$\frac{R_1}{R_2} = \frac{5.3}{6.7}$$

$$R_1 = 56k\Omega$$

$$R_2 = 68k\Omega$$

Input impedance of the buffer

$$Z_{in} = R_1 \parallel R_2 \parallel [\beta r_E + (1+\beta)]R_E$$

Hence $r_E \ll R_E$

$$Z_{in} = R_1 \parallel R_2 \parallel \beta R_E$$

$$Z_{in} = 56k\Omega \parallel 68k\Omega \parallel 100 \times 1k\Omega$$

$$Z_{in} = 23.5k\Omega$$

To get lower cutoff frequency around 10Hz,

$$C_1 = \frac{1}{2\pi \times f \times Z_{in}}$$

$$C_1 \approx 1\mu F$$

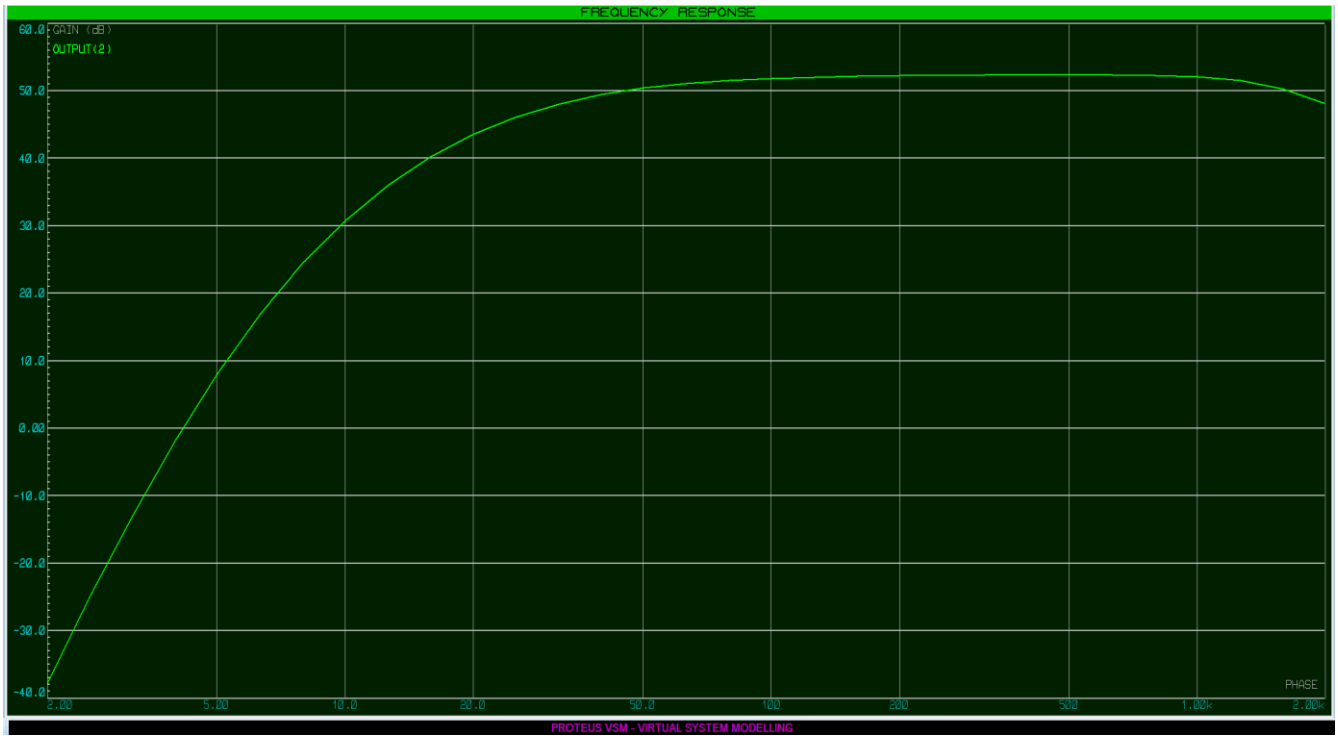


Figure 3 : Frequency Response of the Input Buffer Circuit

2.3.2. Filter

In this design second order active low pass filter is used since it is very similar to the ideal low pass filter. This will decide the higher cutoff frequency of the circuit. Following is the general configuration for the Second Order Low Pass Butterworth Filter.

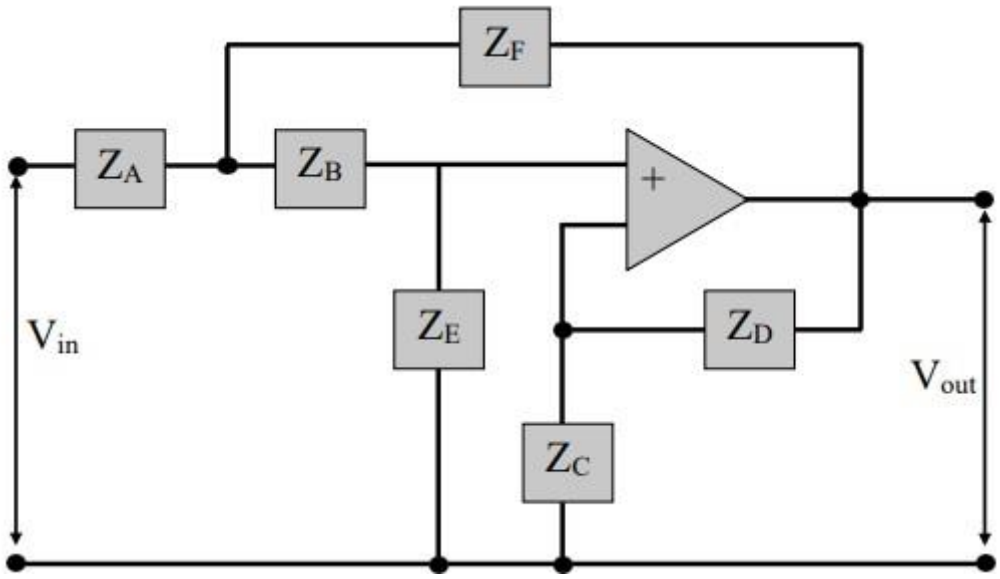


Figure 4 : Second Order Low Pass Butterworth Filter General Configuration

Here the gain from the filter should be unity and bandwidth should be around 1.5kHz. Then using the filter coefficient table, the components values are calculated.

Calculations:

The value of the capacitance C is chosen as 33ηF as a standard value. Then the coefficient vale is,

$$Z_F = C_4$$

$$C_4 = 33\eta\text{F}$$

$$K = \frac{10^{-4}}{f \times C}$$

$$K = \frac{10^{-4}}{1500 \times 33 \times 10^{-9}}$$

$$K = 2.0202$$

Then,

$$Z_A = R_4$$

$$R_4 = 2.0202 \times 1.422$$

$$R_4 = 2.87k\Omega$$

In designing the circuit R_4 value is chosen as 2.7 $k\Omega$.

$$Z_B = R_5$$

$$R_5 = 2.0202 \times 5.399$$

$$R_5 = 10.907 \ k\Omega$$

Value of R_5 is 10 $k\Omega$ in the circuit.

For Unit gain Second Order Low Pass Butterworth Filter,

$$Z_C - open$$

$$Z_D = 0$$

$$Z_E = C_3$$

$$C_3 = 0.33 \times 33\eta\text{F}$$

$$C_3 = 10.89\eta\text{F}$$

Since it is difficult to find $10.89\eta F$ capacitor we have chosen it as $10\eta F$. Then using those values filter can be implemented.

Then for the op amp in the filter it is used Darlington pair. Because it has high input impedance and low output impedance which is the same characteristics of the ideal op amp.

Calculations:

For a largest possible symmetric output voltage swing,

$$V_E = \frac{1}{2}V_{CC}$$

$$V_E = \frac{1}{2} \times 12V$$

$$V_E = 6V$$

Output impedance of the buffer,

$$Z_{out} = R_E \parallel r_E$$

But $r_E \ll R_E$

$$Z_{out} = r_E$$

$$r_E = \frac{26mA}{I_E}$$

To get very low output impedance,

$$I_E = 26mA$$

$$R_E = \frac{V_E}{I_E}$$

$$R_8 = \frac{6V}{26mA}$$

$$R_8 = 220\Omega$$

Base voltage of Q_2 transistor,

$$V_B = V_E + 0.7V + 0.7V$$

$$V_B = 6V + 1.4V$$

$$V_B = 7.4V$$

Then R_6 and R_7 values are,

$$V_B = \frac{R_6 \times V_{CC}}{R_6 + R_7}$$

$$V_B = 7.4\text{V}$$

$$7.4V = \frac{R_6 \times 12V}{R_6 + R_7}$$

$$\frac{R_7}{R_6} = \frac{4.6}{7.4}$$

$$R_6 = 820k\Omega$$

$$R_7 = 470k\Omega$$

Input impedance of the buffer

$$Z_{in} = R_7 \parallel R_6 \parallel [\beta r_E + (1+\beta)]R_E$$

Hence $r_E \ll R_E$

$$Z_{in} = R_7 \parallel R_6 \parallel \beta R_E$$

$$Z_{in} = 470k\Omega \parallel 820k\Omega \parallel 100 \times 220\Omega$$

$$Z_{in} = 22k\Omega$$

To get lower cutoff frequency around 10Hz,

$$C_1 = \frac{1}{2\pi \times f \times Z_{in}}$$

$$C_1 \approx 1\mu F$$

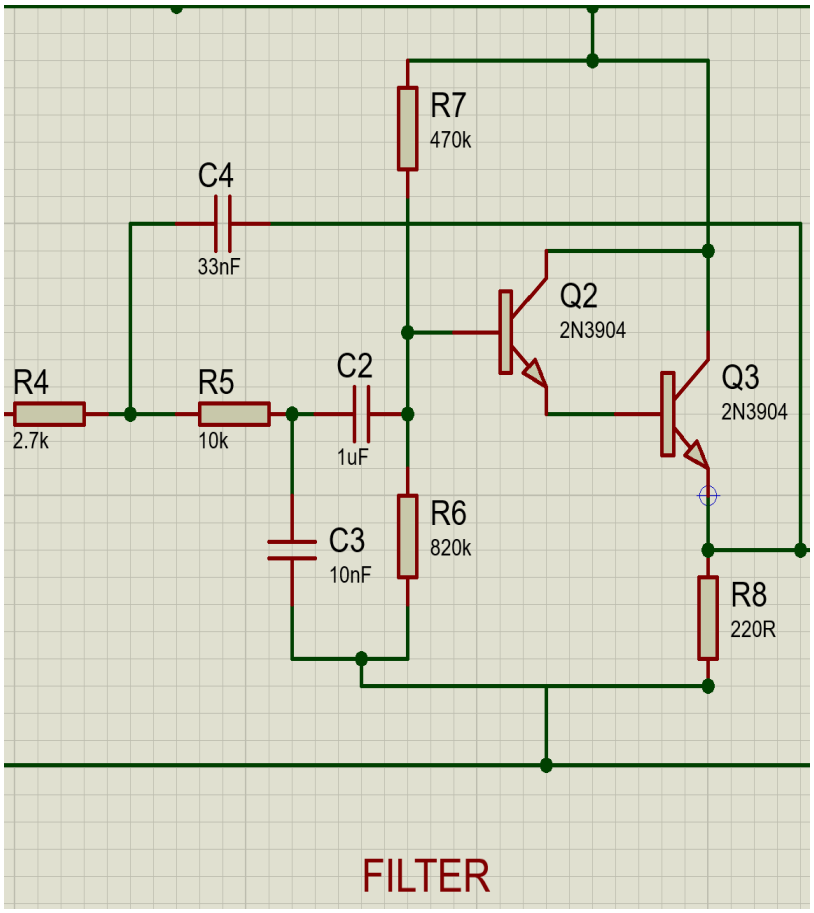


Figure 5 : Filter Circuit

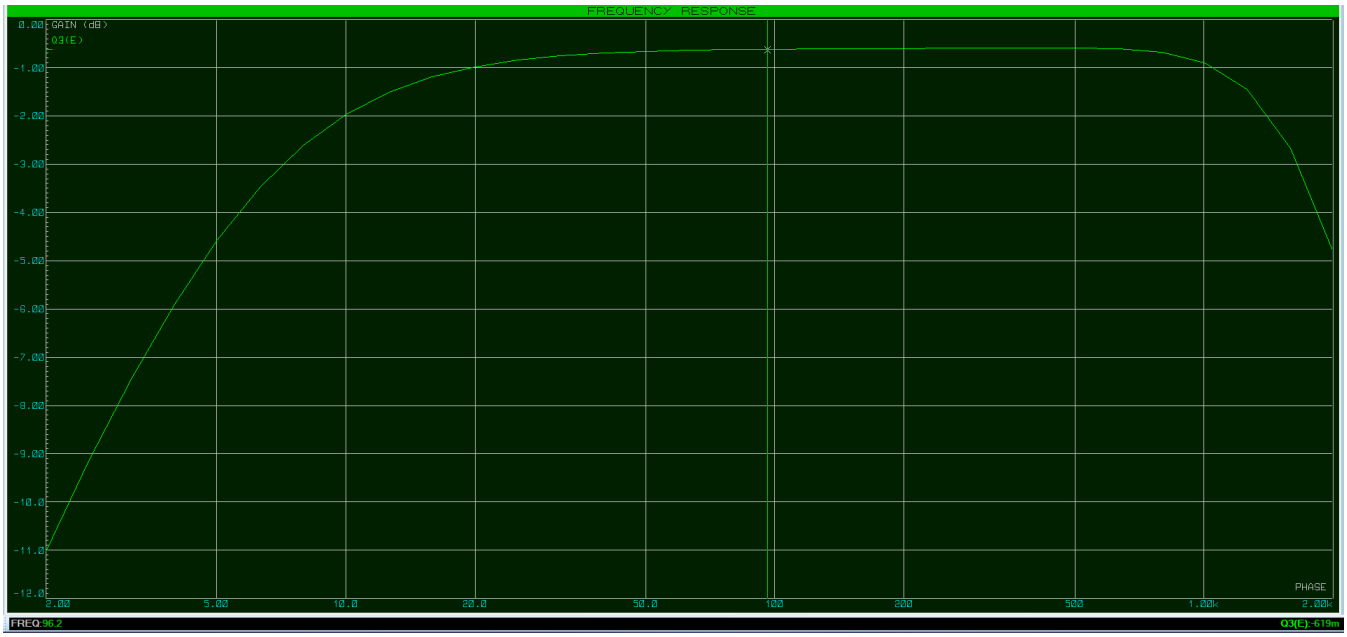


Figure 6 : Frequency Response of the Filter Circuit

2.3.3. First Amplifier

In this amplifier circuit it used two Common Emitter amplifiers to obtain high gain value of 400. Since the each stages are independent form each other stages it can calculate the components values only for this stage independently. For the first amplifier it used 20 gain Common Emitter amplifier.

Calculations:

AC Analysis:

$$V_O = -i_C \times R_C$$

$$i_C = \beta i_B$$

$$V_O = -\beta i_B \times R_C$$

$$i_B = \frac{V_{in}}{r_{in}}$$

$$r_{in} = \beta r_e$$

$$V_O = -\frac{V_{in}}{r_e} \times R_C$$

$$\frac{V_{out}}{V_{in}} = A_V$$

$$A_V = -\frac{R_C}{r_e}$$

$$R_C = |A_V| \times r_e$$

DC Analysis:

Using Kirchhoff law,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

Assuming that V_{CE} = 5V and $I_C \approx I_E$=2.6mA

$$r_E = \frac{26mV}{I_E}$$

$$r_E = 10\Omega$$

Then using AC analysis equation,

$$R_C = R_{11}$$

$$R_{11} = 20 \times 10\Omega$$

$$R_{11} = 200\Omega$$

$$R_{11} = 100\Omega + 100\Omega \text{ (Since the availability)}$$

Using Kirchhoff law equation,

$$12V = (2.6mA \times 220\Omega) + 5V + (2.6mA \times R_E)$$

$$R_{12} = 2.2K\Omega$$

Base voltage,

$$V_B = V_E + V_{BE}$$

$$V_B = (I_E \times R_E) + 0.7V$$

$$V_B = 6.42 \text{ V}$$

Then using voltage divider rule,

$$V_B = \frac{R_{10} \times V_{CC}}{R_9 + R_{10}}$$

$$6.42V = \frac{R_{10} \times 12V}{R_9 + R_{10}}$$

$$\frac{R_9}{R_{10}} = \frac{5.58}{6.42}$$

$$R_9 = 1.2k\Omega$$

$$R_{10} = 1.8k\Omega$$

Calculate the value for C_5

$$Z_{in} = R_9 \parallel R_{10} \parallel \beta r_E$$

$$Z_{in} = 1.2k\Omega \parallel 1.8k\Omega \parallel 100 \times 10\Omega$$

$$Z_{in} = 420\Omega$$

To get lower cutoff frequency around 10Hz,

$$C_5 = \frac{1}{2\pi \times f \times Z_{in}}$$

$$C_5 \approx 33\mu F$$

Calculate the value for C_7

$$Z_E = R_{22} \parallel R_{23} \parallel r_E$$

$$Z_E = 1.2k\Omega \parallel 1.8k\Omega \parallel 10\Omega$$

$$Z_E = 10\Omega$$

To get lower cutoff frequency around 10Hz,

$$C_7 = \frac{1}{2\pi \times f \times Z_E}$$

$$C_7 = 1591\mu F$$

$$C_7 \approx 1500\mu F$$

The first common emitter 20 gain amplifiers is designed as below while considering the availability of the components,

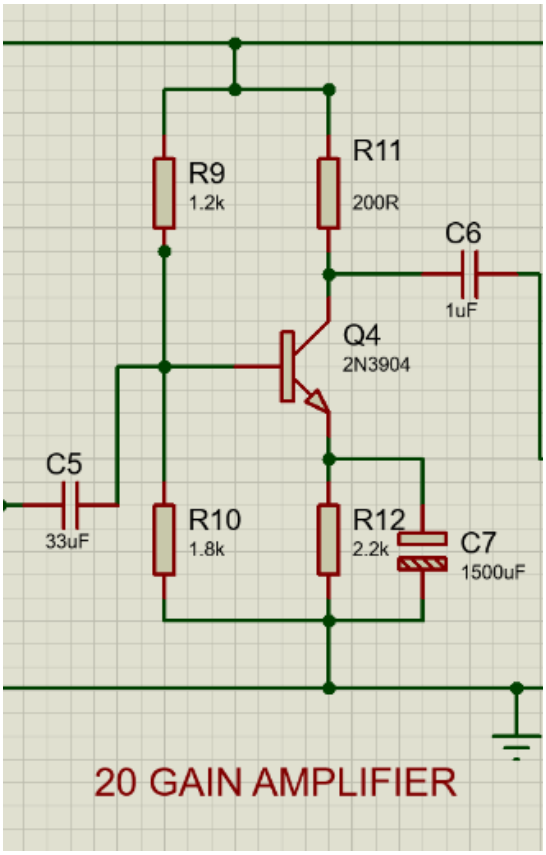


Figure 7 : First Amplifier (20Gain) Circuit

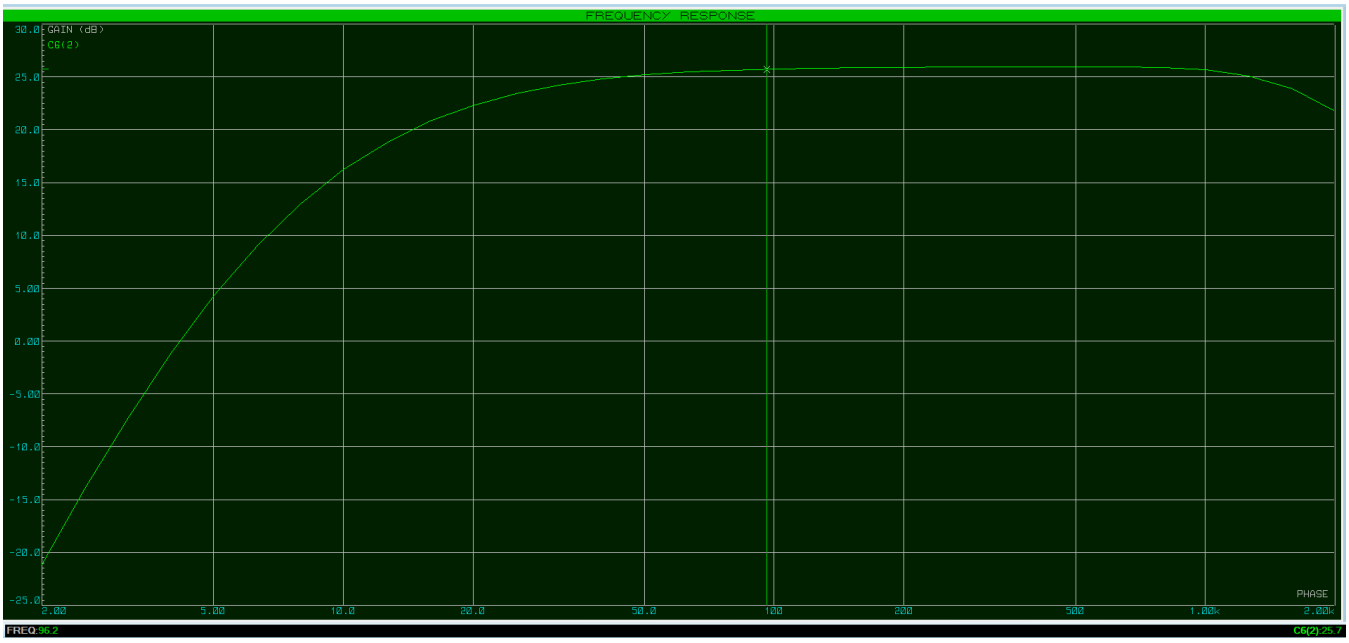


Figure 8 : Frequency Response up to First Amplifire Output

2.3.4. Middle Buffer

As above mentioned Common Collector amplifier is used as middle buffer for the circuit. This buffer will handle the impedance mismatch between first amplifier output and the second amplifier input.

Calculations:

For a largest possible symmetric output voltage swing,

$$V_E = \frac{1}{2}V_{CC}$$

$$V_E = \frac{1}{2} \times 12V$$

$$V_E = 6V$$

Then the Q point used for the calculations,

$$V_{CE} = 6V$$

$$I_C = 6mA$$

Normally $I_C \approx I_E$,

Then Emitter resistor value,

$$R_E = \frac{V_E}{I_E}$$

$$R_{15} = \frac{6V}{6mA}$$

$$R_{15} = 1k\Omega$$

Base voltage of Q_{10} transistor,

$$V_B = V_E + 0.7V$$

$$V_B = 6V + 0.7V$$

$$V_B = 6.7V$$

Then R_{13} and R_{14} values are,

$$V_B = \frac{R_{13} \times V_{CC}}{R_{13} + R_{14}}$$

$$V_B = 6.7\text{V}$$

$$6.7V = \frac{R_{14} \times 12V}{R_{13} + R_{14}}$$

$$\frac{R_{13}}{R_{14}} = \frac{5.3}{6.7}$$

$$R_{13} = 56k\Omega$$

$$R_{14} = 68k\Omega$$

Input impedance of the buffer

$$Z_{in} = R_{13} \parallel R_{14} \parallel [\beta r_E + (1+\beta)]R_E$$

Hence $r_E \ll R_E$

$$Z_{in} = R_{13} \parallel R_{14} \parallel \beta R_E$$

$$Z_{in} = 56k\Omega \parallel 68k\Omega \parallel 100 \times 1k\Omega$$

$$Z_{in} = 23.5k\Omega$$

To get lower cutoff frequency around 10Hz,

$$C_6 = \frac{1}{2\pi \times f \times Z_{in}}$$

$$C_6 = 0.677\mu F$$

$$C_6 \approx 1\mu F$$

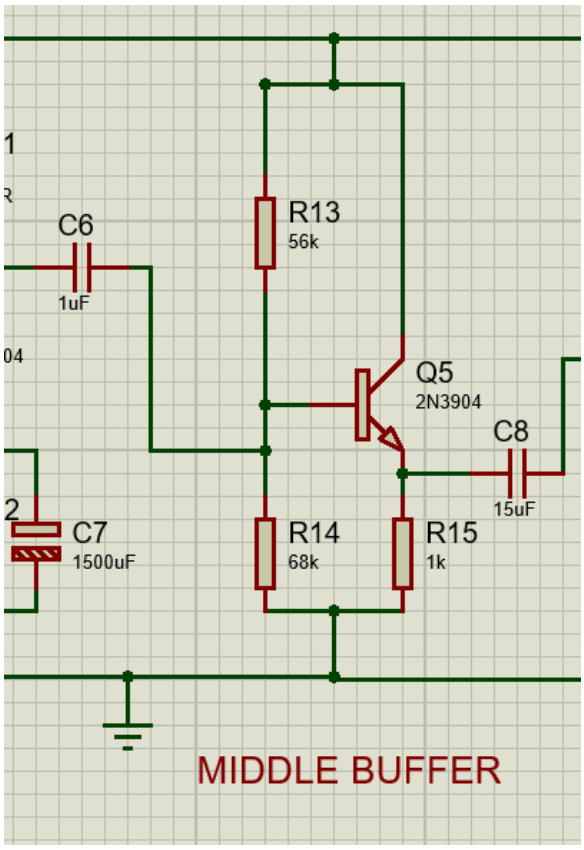


Figure 9 : Middle Buffer Circuit

2.3.5. Second Amplifier

In this amplifier circuit it used two Common Emitter amplifiers to obtain high gain value of 400. Since the each stages are independent form each other stages it can calculate the components values only for this stage independently. For the second amplifier it also used 20 gain Common Emitter amplifier.

Calculations:

AC Analysis:

$$V_O = -i_C \times R_C$$

$$i_C = \beta i_B$$

$$V_O = -\beta i_B \times R_C$$

$$i_B = \frac{V_{in}}{r_{in}}$$

$$r_{in} = \beta r_e$$

$$V_O = -\frac{V_{in}}{r_e} \times R_C$$

$$\frac{V_{out}}{V_{in}} = A_V$$

$$A_V = -\frac{R_C}{r_e}$$

$$R_C = |A_V| \times r_e$$

DC Analysis:

Using Kirchhoff law,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

Assuming that V_{CE} = 5V and $I_C \approx I_E$=2.6mA

$$r_E = \frac{26mV}{I_E}$$

$$r_E = 10\Omega$$

Then using AC analysis equation,

$$R_C = R_{18}$$

$$R_{18} = 20 \times 10\Omega$$

$$R_{18} = 200\Omega$$

$$R_{18} \approx 220\Omega \text{ (Since availability)}$$

Using Kirchhoff law equation,

$$12V = (2.6mA \times 220\Omega) + 5V + (2.6mA \times R_E)$$

$$R_{19} = 2.2K\Omega$$

Base voltage,

$$V_B = V_E + V_{BE}$$

$$V_B = (I_E \times R_E) + 0.7V$$

$$V_B = 6.42 \text{ V}$$

Then using voltage divider rule,

$$V_B = \frac{R_{17} \times V_{CC}}{R_{16} + R_{17}}$$

$$6.42V = \frac{R_{17} \times 12V}{R_{16} + R_{17}}$$

$$\frac{R_{16}}{R_{17}} = \frac{5.58}{6.42}$$

$$R_{16} = 1.2k\Omega$$

$$R_{17} = 1.8k\Omega$$

Calculate the value for C_{12}

$$Z_{in} = R_{16} \parallel R_{17} \parallel \beta r_E$$

$$Z_{in} = 1.2k\Omega \parallel 1.8k\Omega \parallel 100 \times 10\Omega$$

$$Z_{in} = 418.60\Omega$$

$$Z_{in} \approx 420\Omega$$

To get lower cutoff frequency around 10Hz,

$$C_8 = \frac{1}{2\pi \times f \times Z_{in}}$$

$$C_8 \approx 15\mu F$$

Calculate the value for C_{16}

$$Z_E = R_{16} \parallel R_{17} \parallel r_E$$

$$Z_E = 1.2k\Omega \parallel 1.8k\Omega \parallel 10\Omega$$

$$Z_E = 10\Omega$$

To get lower cutoff frequency around 10Hz,

$$C_{10} = \frac{1}{2\pi \times f \times Z_E}$$

$$C_{10} \approx 1500\mu F$$

The second common emitter 20 gain amplifiers is designed as below while considering the availability of the components,

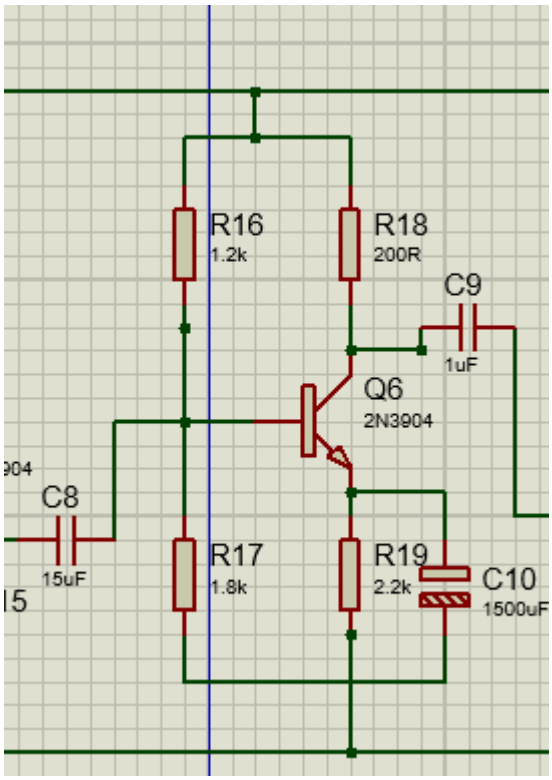


Figure 10 : Second Amplifier (20 Gain) Circuit

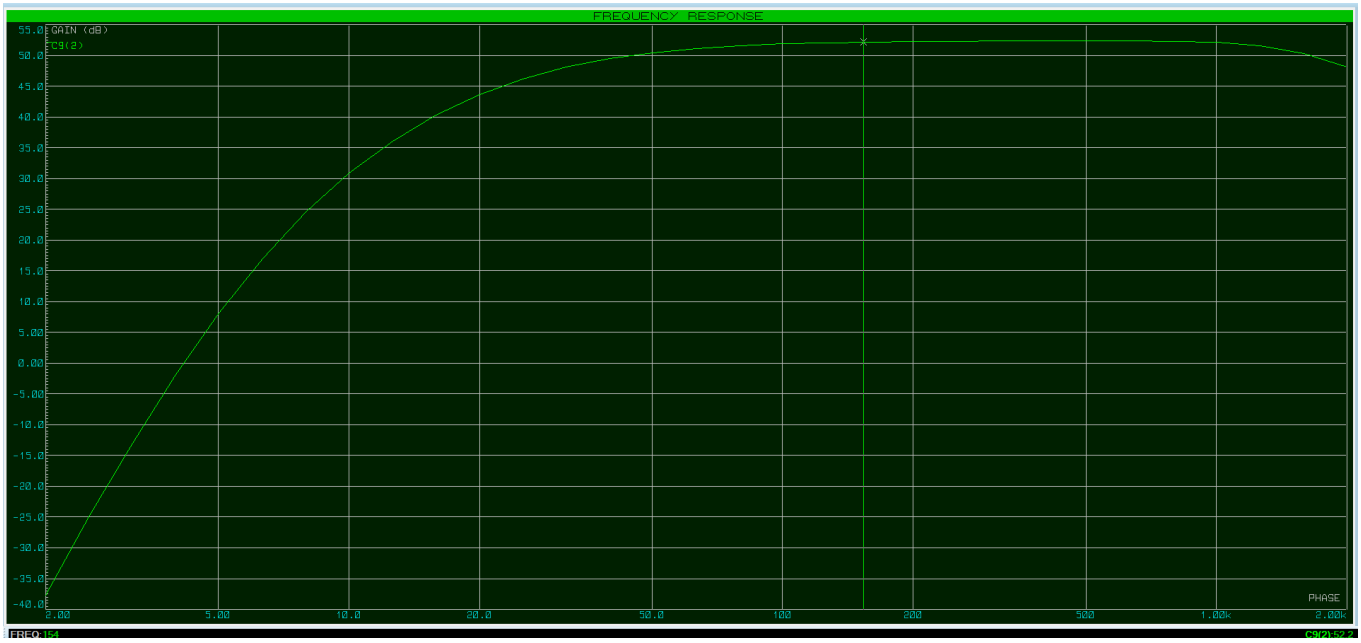


Figure 11 : Frequency Response up to Second Amplifier Output

2.3.6. Output Buffer

As above mentioned Common Collector amplifier is used as output buffer for the circuit. This buffer will handle the impedance mismatch between second amplifier output and the output source.

Calculations:

For a largest possible symmetric output voltage swing,

$$V_E = \frac{1}{2}V_{CC}$$

$$V_E = \frac{1}{2} \times 12V$$

$$V_E = 6V$$

Then the Q point used for the calculations,

$$V_{CE} = 6V$$

$$I_C = 6mA$$

Normally $I_C \approx I_E$,

Then Emitter resistor value,

$$R_E = \frac{V_E}{I_E}$$

$$R_{22} = \frac{6V}{6mA}$$

$$R_{22} = 1k\Omega$$

Base voltage of Q_6 transistor,

$$V_B = V_E + 0.7V$$

$$V_B = 6V + 0.7V$$

$$V_B = 6.7V$$

Then R_{20} and R_{21} values are,

$$V_B = \frac{R_{21} \times V_{CC}}{R_{20} + R_{21}}$$

$$V_B = 6.7\text{V}$$

$$6.7V = \frac{R_{21} \times 12V}{R_{20} + R_{21}}$$

$$\frac{R_{16}}{R_{17}} = \frac{5.3}{6.7}$$

$$R_{20} = 56k\Omega$$

$$R_{21} = 68k\Omega$$

Input impedance of the buffer

$$Z_{in} = R_{20} \parallel R_{21} \parallel [\beta r_E + (1+\beta)]R_E$$

Hence $r_E \ll R_E$

$$Z_{in} = R_{20} \parallel R_{21} \parallel \beta R_E$$

$$Z_{in} = 56k\Omega \parallel 68k\Omega \parallel 100 \times 1k\Omega$$

$$Z_{in} = 23.5k\Omega$$

To get lower cutoff frequency around 10Hz,

$$C_9 = \frac{1}{2\pi \times f \times Z_{in}}$$

$$C_9 \approx 1\mu F$$

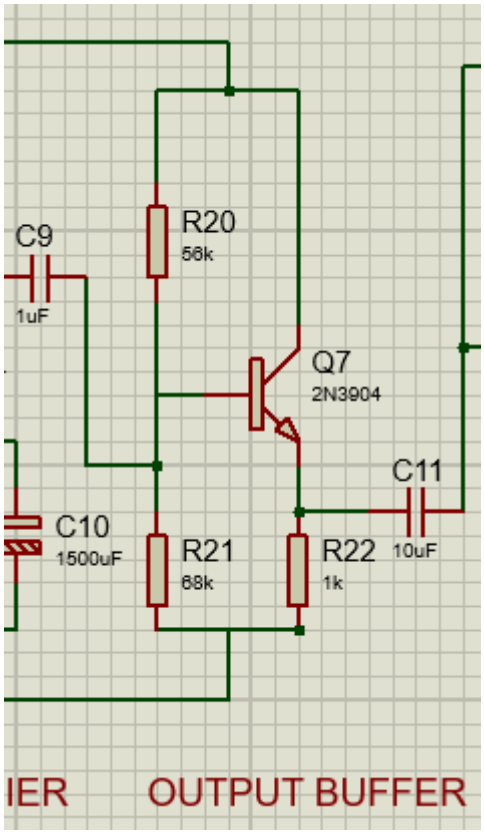


Figure 12 : Output Buffer Circuit

2.3.7. Assembles Amplifier Design

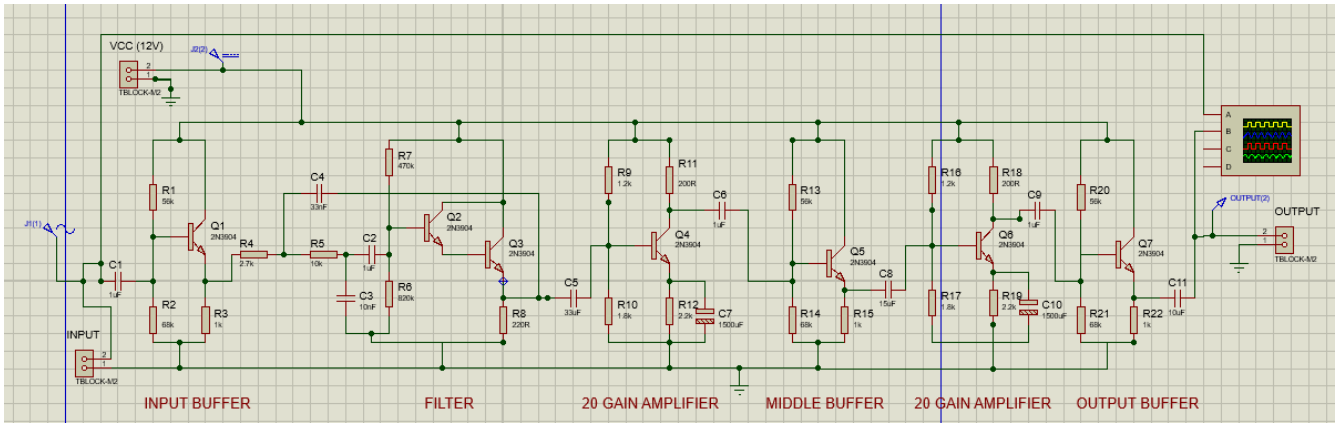


Figure 13 : Assembled Amplifier Design

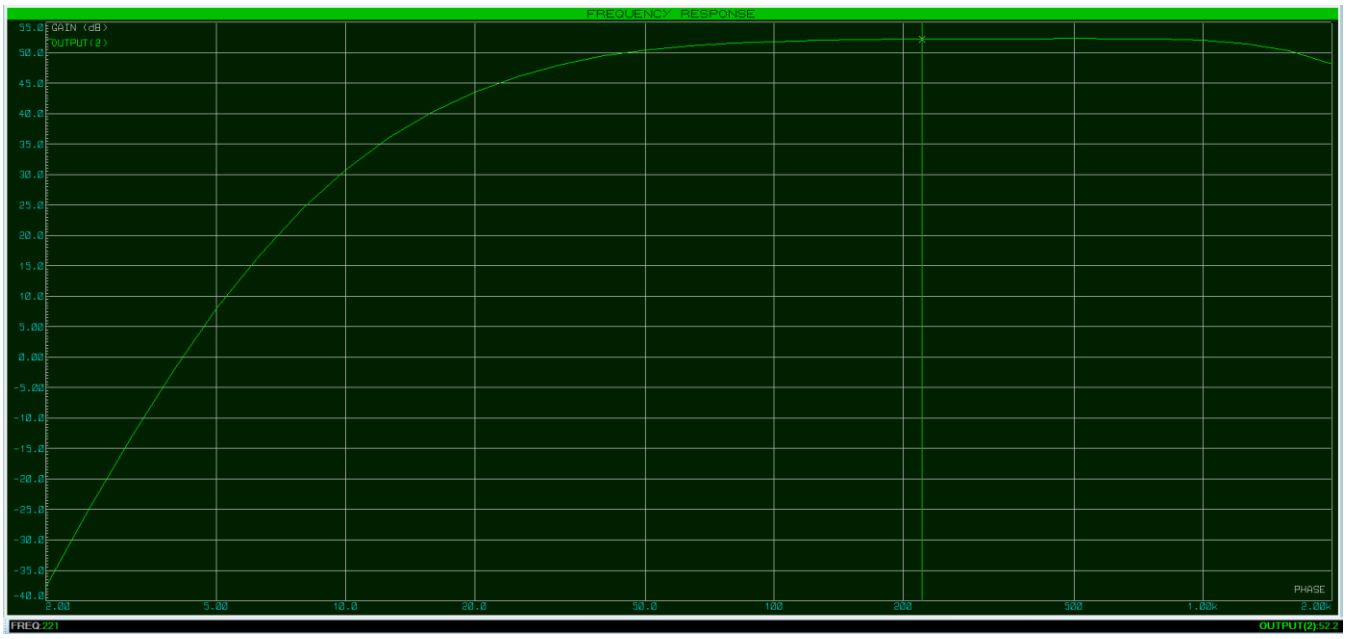


Figure 14 : Frequency Response of the Assembled Amplifier

3. Implementation of the Circuit

3.1. Schematic Diagram of the Amplifier

The schematic diagram of the circuit is designed by using PROTEUS software. The final circuit is shown in the below figure.

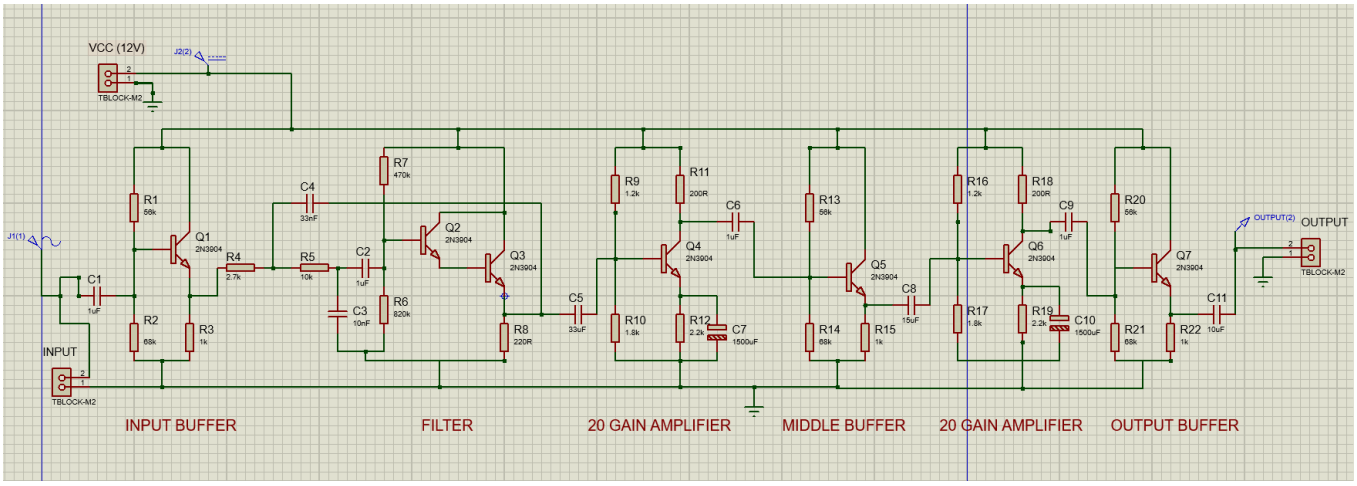


Figure 15 : Final Schematic Design of the Circuit

3.2. PCB Layout of the Amplifire

Also for the PCB design the PROTEUS software is used. The final design is shown below.

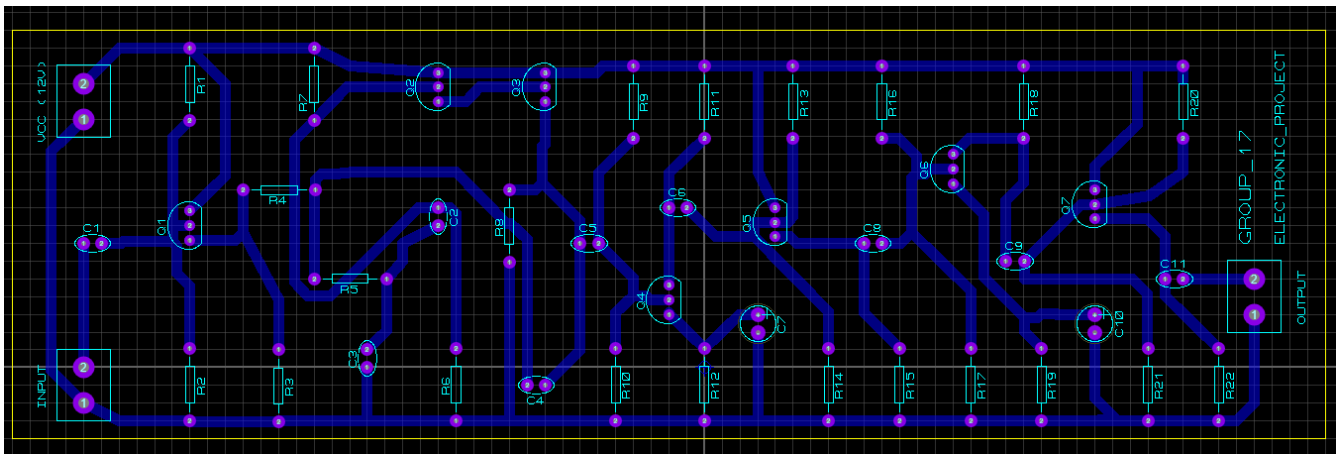


Figure 16 : Final PCB Layout of the Circuit

3.3. 3D Visualizer Views of the Amplifier

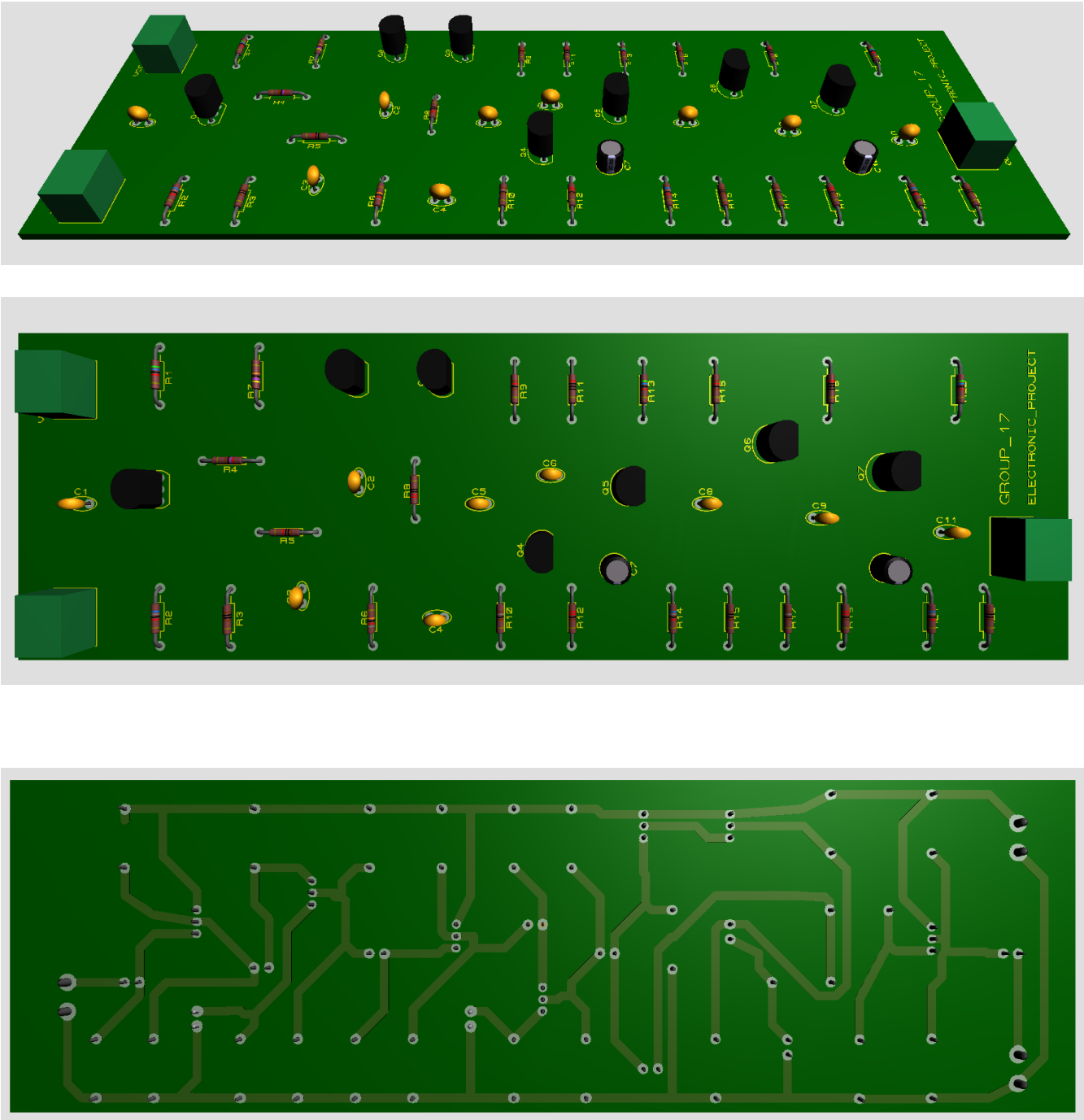


Figure 17 : 3D Visualizer View of the Final Circuit

3.4. Copper Traces of PCB Layout

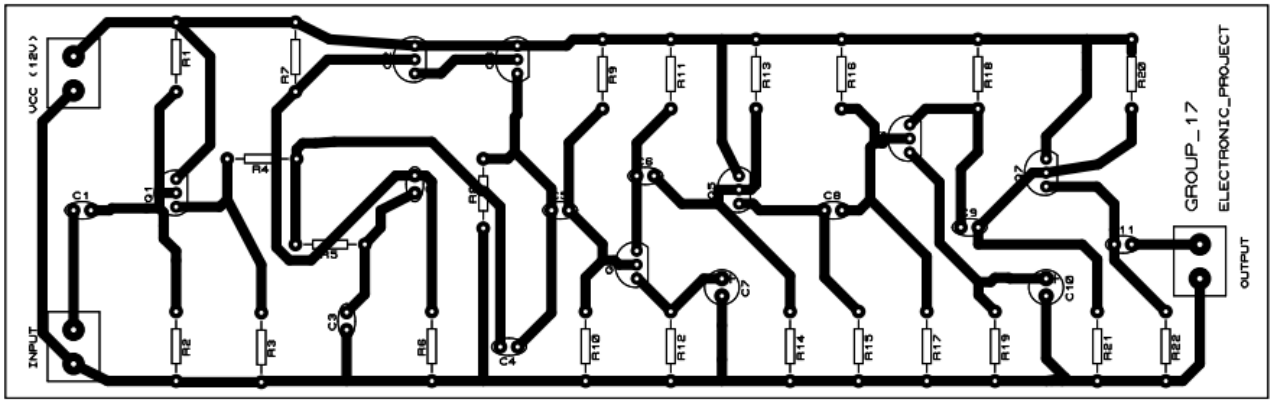


Figure 18 : Component Placement with Copper Traces

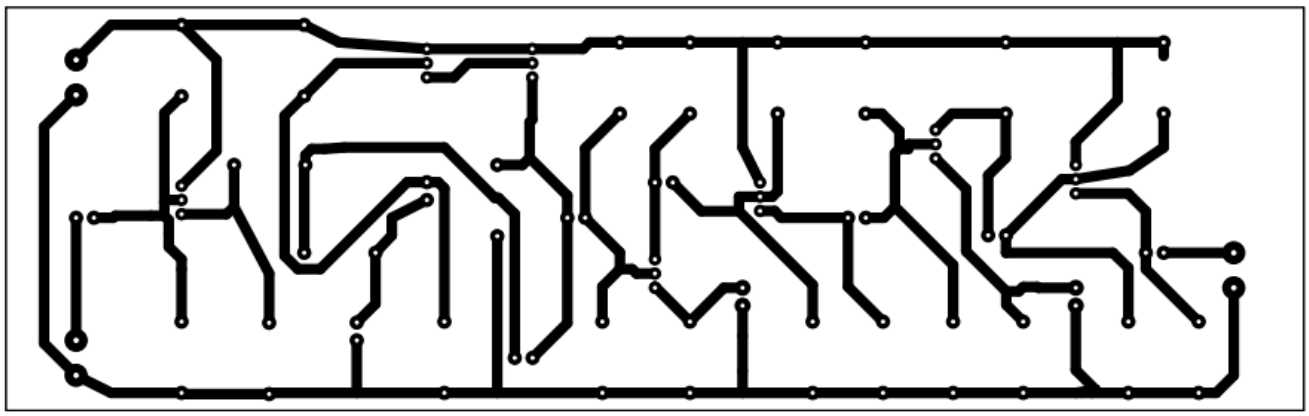


Figure 19 : Copper Traces

3.5. Physical Implementation

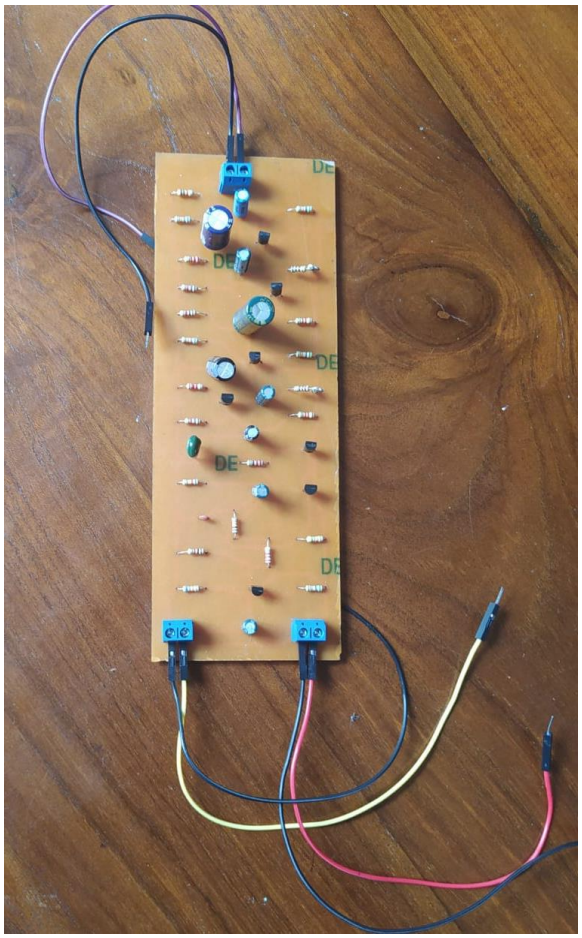


Figure 20: Photo of the PCB

4. Result and Discussion

4.1. Simulation Result

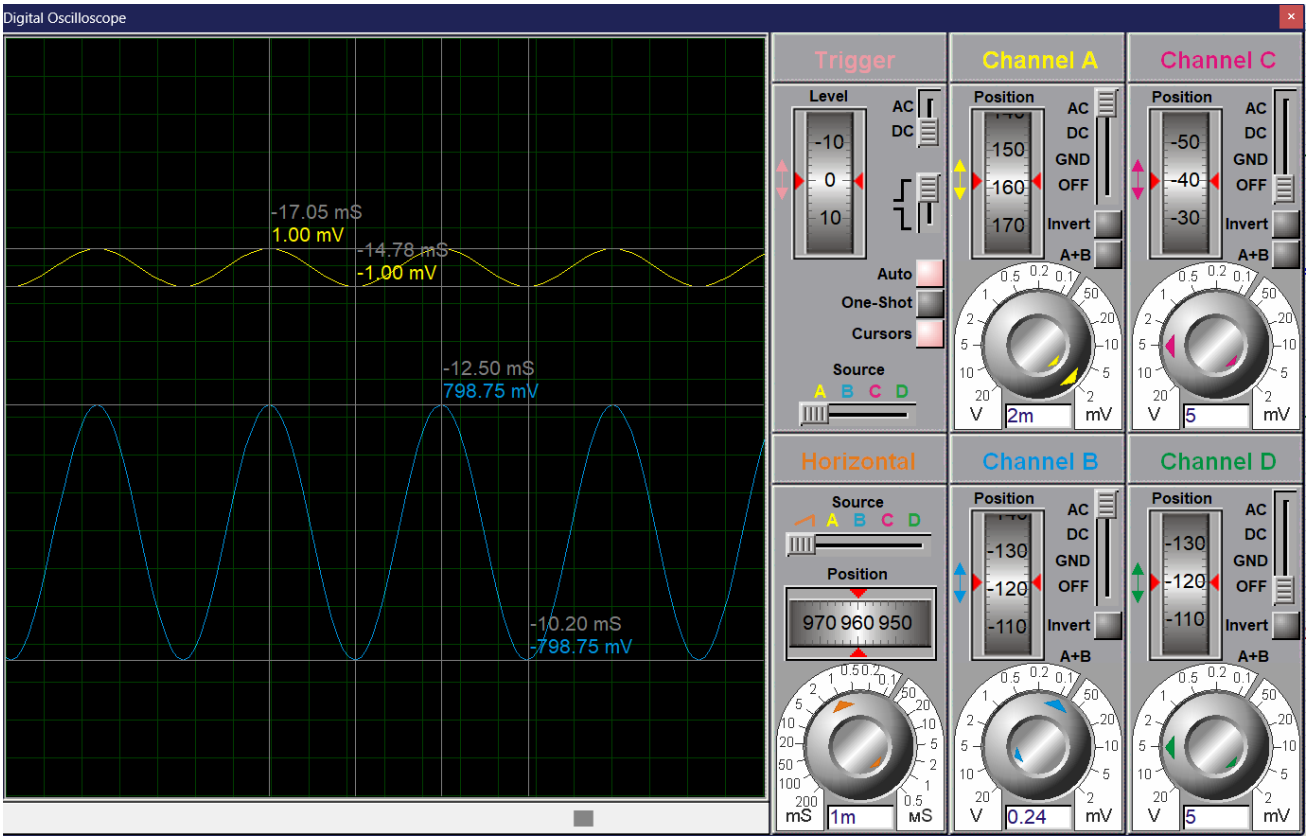


Figure 21 : Simulation Oscilloscope Result

Test input signal (V_{IN}) = 2mV$_{PP}$ and 220Hz

Test output signal (V_{OUT}) = 798mV$_{PP}$ and 220Hz

Gain obtain from the simulation = A_V

$$A_V = \frac{V_{OUT}}{V_{IN}}$$

$$= \frac{798mV}{2mV}$$

$$= 399$$

From the above amplifier circuit, we were able to obtain 400 gain roughly

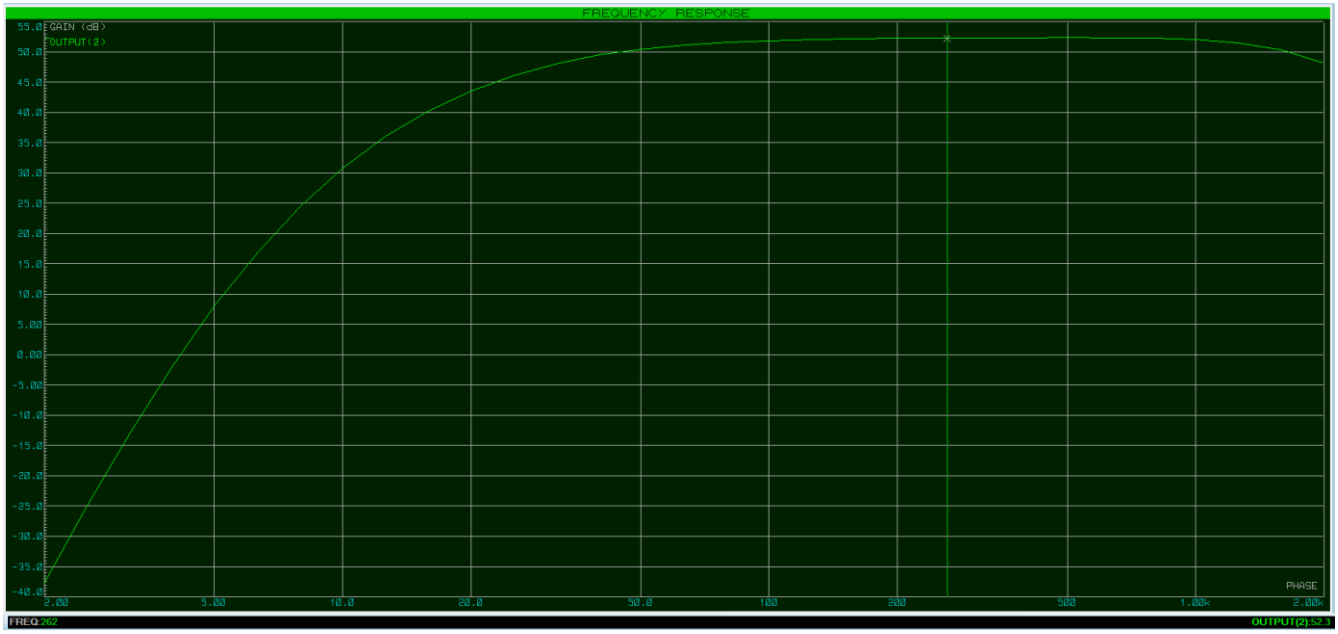
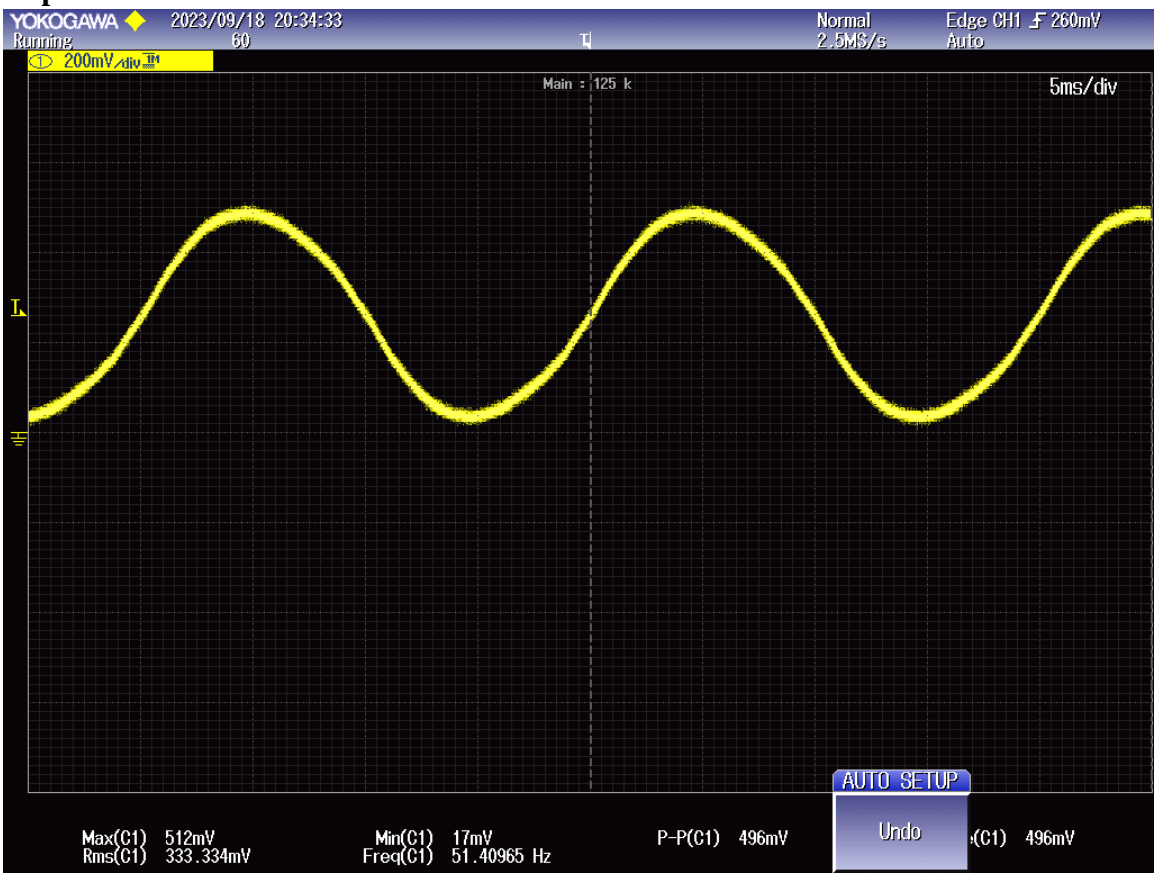


Figure 22 : Simulation of Frequency Response

Pass band gain	= 52.3 dB (Equivalent to 400)
Higher cutoff frequency	= 49.3 dB at 1.77kHz
Lower cutoff frequency	= 49.3 dB at 39.1 Hz
Bandwidth of the amplifier	= 1.77k – 39.1 Hz
	= 1.73 kHz

4.2. Experimental Results



4.3. Discussion

Certainly, here's a more detailed discussion of the factors contributing to the deviation between theoretical and practical values in the common emitter BJT amplifier design. A common emitter BJT amplifier was designed with specified gain of 400 and a bandwidth of 1.5kHz.

- Component Availability and Approximations:

To meet the desired gain and bandwidth specifications, we initially performed theoretical calculations to determine component values. However, in practice, it's often challenging to find components with exact values as calculated. We have to make this with available components that closely approximated to our requirements. These approximations could introduce some difference.

- Impedance Mismatch:

During the experimentation phase, we used a signal generator to provide the input signal and an oscilloscope to measure the output. However, these instruments were not accounted for the theoretical simulations that we did using proteus. The impedance of the signal generator and the load impedance of the oscilloscope can significantly affect the circuit's performance. The impedance mismatch could explain some of the differences observed.

- Real-World Component Properties:

Real-world electronic components may not have ideal characteristics. Components can have noise and tolerances that deviate from their specified values, and exhibit non-ideal behaviors, such as capacitance and inductance. These imperfections in components can lead to variations between theoretical and practical results of voltage gain.

- Temperature Effects:

The operating temperature of electronic components can vary in real-world conditions, impacting their electrical properties. Resistors, for example, can exhibit resistance variations with temperature changes. This thermal drift can cause deviations from the expected circuit behavior.

- Tolerance of Components:

The tolerance specified for resistors and capacitors can affect the observed voltage gain and bandwidth. Components with tolerances outside the expected range can introduce variations in performance.

- Instrumental Errors:

During the experimentation, instrumental errors, such as noise in the components or the measurement instruments, can influence the observed gain and bandwidth. These errors may not be present in theoretical simulations but can significantly impact real-world results.

- Random Experimental Errors:

Random errors in any experimental setup can contribute to the deviation between theoretical and practical values. These errors can include factors like measurement uncertainties and fluctuations in the power supply voltage.