LAB 9

PART 1: gm/ID Design Charts

We would like to design a differential input, single-ended output two-stage Miller-compensated OTA.

-Using ADT Device Xplore, I plotted the following design charts vs gm/ID for both PMOS and NMOS. Set VDS =VDD/3= 600m and

L = 0.18u,0.5u:0.5u:2u as shown in figures 1.1 , 1.2 , 1.3 , 1.4.

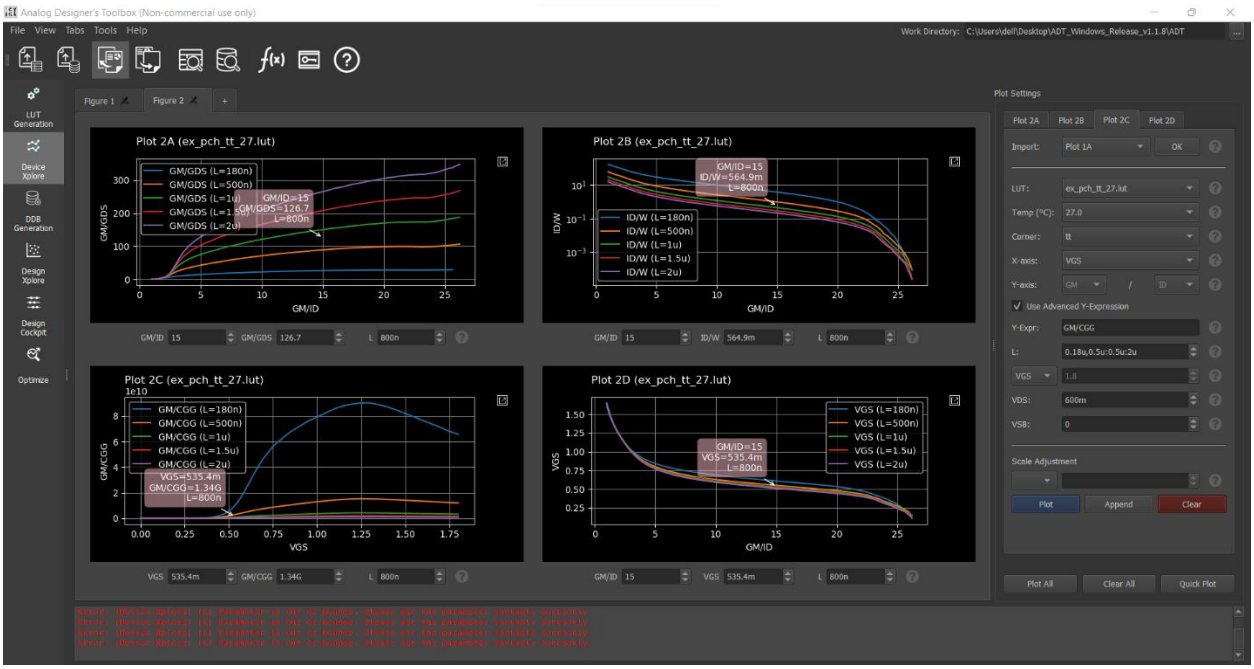

Figure 1.1(PMOS for input pair)

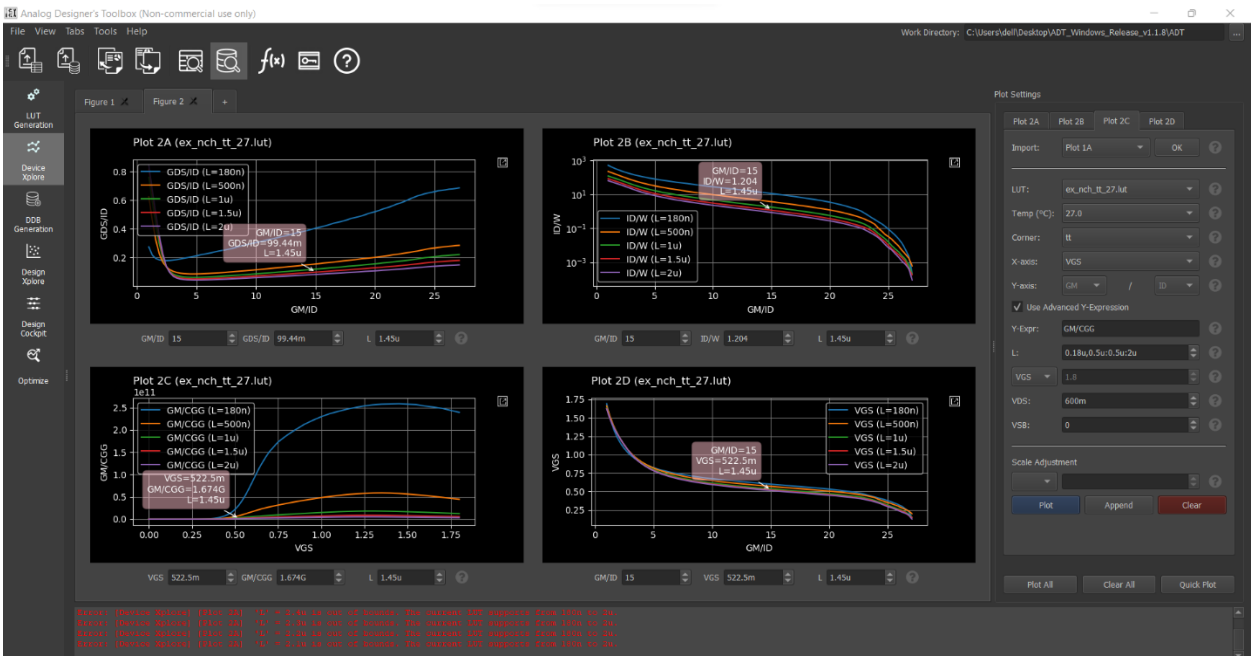

Figure 1.2(NMOS for current mirror load)

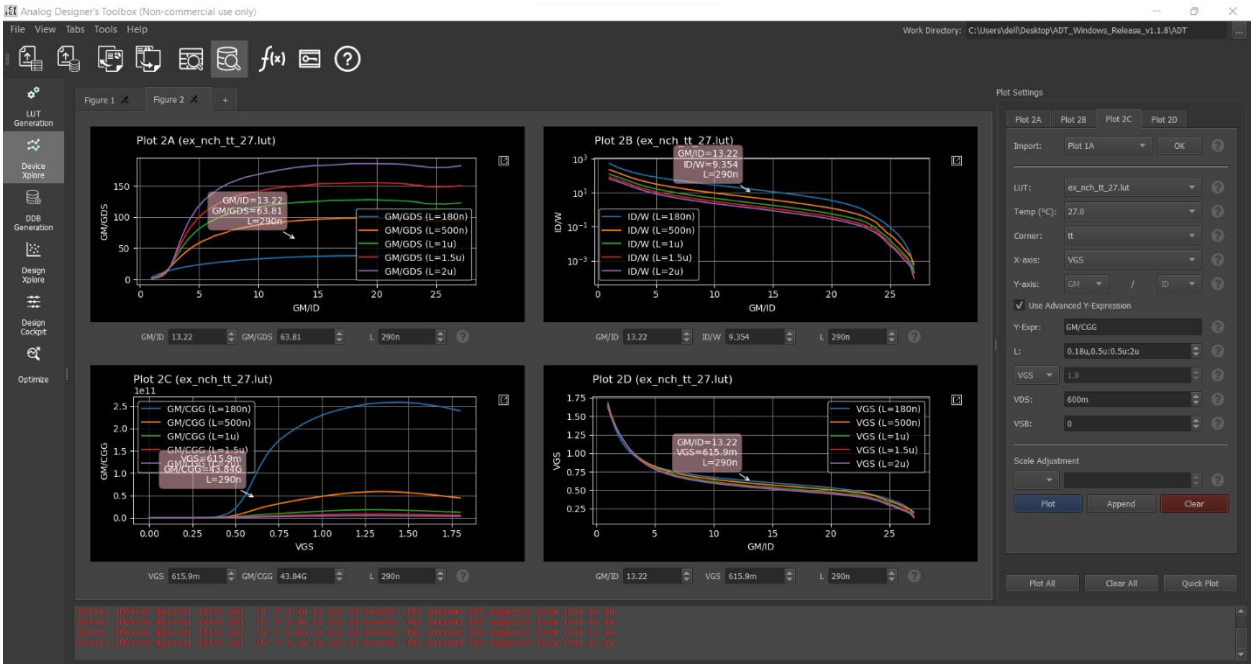

Figure 1.3(NMOS for 2nd stage input)

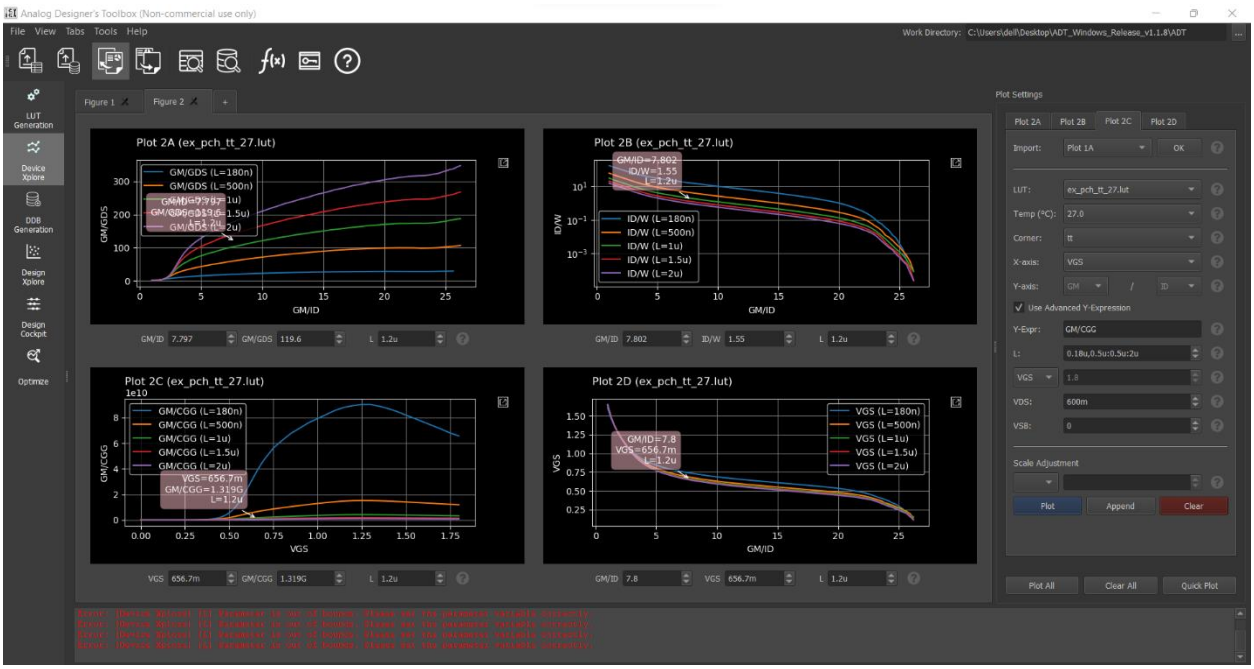

Figure 4.1(PMOS for the tail CS)

PART 2: OTA Design

-I used gm/ID methodology to design differential input, single-ended output two-stage Miller-compensated OTA that achieves the required specs and I used an ideal external 10uA DC current source in my test bench.

- The required gain is high (only 66 dB = 2000) so it can be achieved by a 2 stages OTA.

- Since the required CMIR is close to the ground rail, we need to use a PMOS input stage.

-I used NMOS for the input pair of the 2nd stage because we want VGS of 1st stage load = VGS of 2nd stage input.

-So , the architecture that I implemented is as shown in figure 2.1.

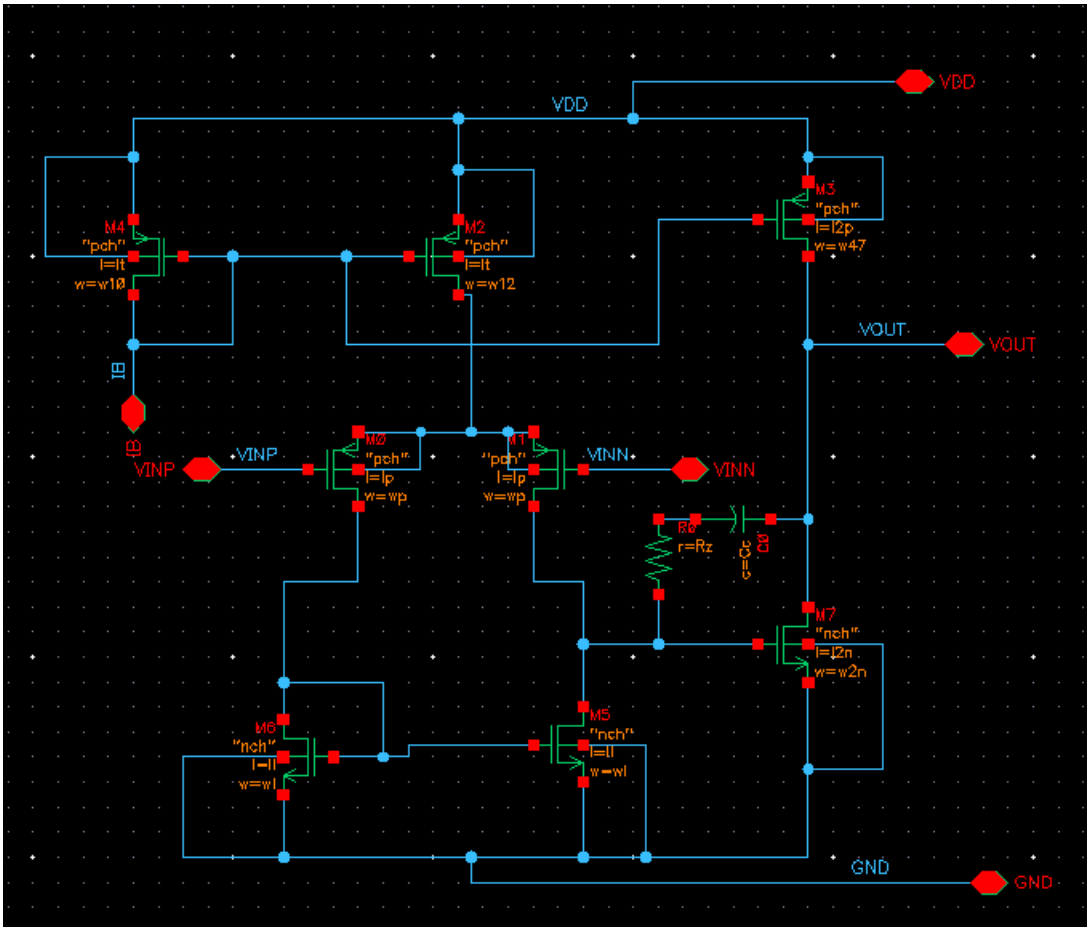

Figure 2.1

1- Detailed design procedure and hand analysis:

As $$\mathrm{UGF} = \frac{\mathrm{gm1,2}}{2\pi \mathrm{Cc}}$$

$$\mathrm{gm1,2} = 2\pi \times 2.5\,\mathrm{p} \times 5\,\mathrm{M} \approx 78.5\,\mu\mathrm{S}$$

And $$\mathrm{SR} = \frac{\mathrm{IB1}}{\mathrm{Cc}} = 5\mathrm{V}/\mu\mathrm{S}$$

$$\mathrm{IB1} = 12.5\mu\mathrm{A}$$

So

$$\mathrm{IB2} = 60 - 12.5 = 47.5\mu\mathrm{A}$$

And $$\frac{\mathrm{gm1,2}}{\mathrm{ID1}} = 12.56$$ ➔ let it = 15

As $\varepsilon s \approx \frac{1}{LG} \approx \frac{1}{\beta Aol} = \frac{0.05}{100}$ and $\beta = 1$ So, Aol = 2000 ➔66dB

I assumed the first stage gain is twice that of the second stage (6dB difference) so, A1 = 36dB and A2 = 30dB.

As $A1 = \frac{gm1ro}{2} = 36dB = 63$ ➔ $\frac{gm1}{gds1} = 2A1 = 126.2$

So, I found that L1,2= 800nm as shown in figure 1.1 and I found that W1,2 = 11.06 um.

I assumed input and load have the same gds and $\frac{gm}{ID}$ = 15 and given gds/ID of the first stage current mirror load= 0.9952 I selected L= 1.45um and W= 5.19um as shown in figure 1.2.

As PM >= 70, I assume ωp2 = 4ωu ➔ $\frac{Gm2}{CL} = \frac{4Gm1}{Cc}$ ➔Gm2 = 8Gm1=628us ➔$(\frac{gm}{ID})2 = 13.22$

As $A2 = \left(\frac{gmro}{2}\right)2 = 30dB = 31.6$ ➔ $(\frac{gm}{gds})2 = 2A2 = 63.25$, I found that L of the 2nd stage NMOS = 290nm and W = 5.078um as shown in figure 1.3.

Given the CMIR-high and Swing-high specs, I found that VDD-VSG1-VICM>Vov2 ➔ max Vdsat2 = 1.8-545.1m-1= 0.255V

V*= 0.255V ➔ $(\frac{gm}{ID})tailCS = 7.8$

I assumed gm/ID = 10 for first stage current mirror load ➔ gm5,6 = 62.5us

As CMRR = $\frac{Av}{AvCM} \geq 74dB$ ➔ $\frac{gm1ro}{2} \times 2 \times gm5,6 \times ro2 = 74dB$ ➔ gds2= 1.57us

So, $\left(\frac{gm}{gds}\right)\text{tailCS} = 120$ ➔ I found that L of the tail CS = 1.2um and W2= 8.06um as shown in figure 1.4.

So, W4 = 6.448um and W3 = 30.628um.

I found that Rz = $\frac{1}{\text{Gm2}} = 1592.36\ \text{ohm}$.

-A table showing W, L, gm,ID, gm/ID, vdsat, Vov = VGS − VTH, and V∗ = 2ID/gm of all transistors:

	W	L	gm	ID	gm/ ID	Vdsat	Vov	V*
M0 ,1	11.0 6u	800 n	78.5u	6.2 5u	15	0.1082V	0.1082V	0.1335V
M5 ,6	5.19 u	1.4 5u	62.5u	6.2 5u	7.8	0.105V,0.1 602V	0.105V,0.1 602V	0.134V, 0.2V
M2	8.06 u	1.2 u	97.5u	12. 5u	10	0.2566V	0.2566V	0.336V
M4	6.44 8u	1.2 u	100u	10u	10	0.2559V	0.2559V	0.3365V
M3	30.6 3u	1.2 u	475u	47. 5u	10	0.2591V	0.2591V	0.336V
M7	5.07 8u	290 n	627.9 5u	47. 5u	13. 22	0.1156V	0.1156V	0.1499V

PART 3: Open-Loop OTA Simulation1

1) I created a testbench as shown in figure 3.1.

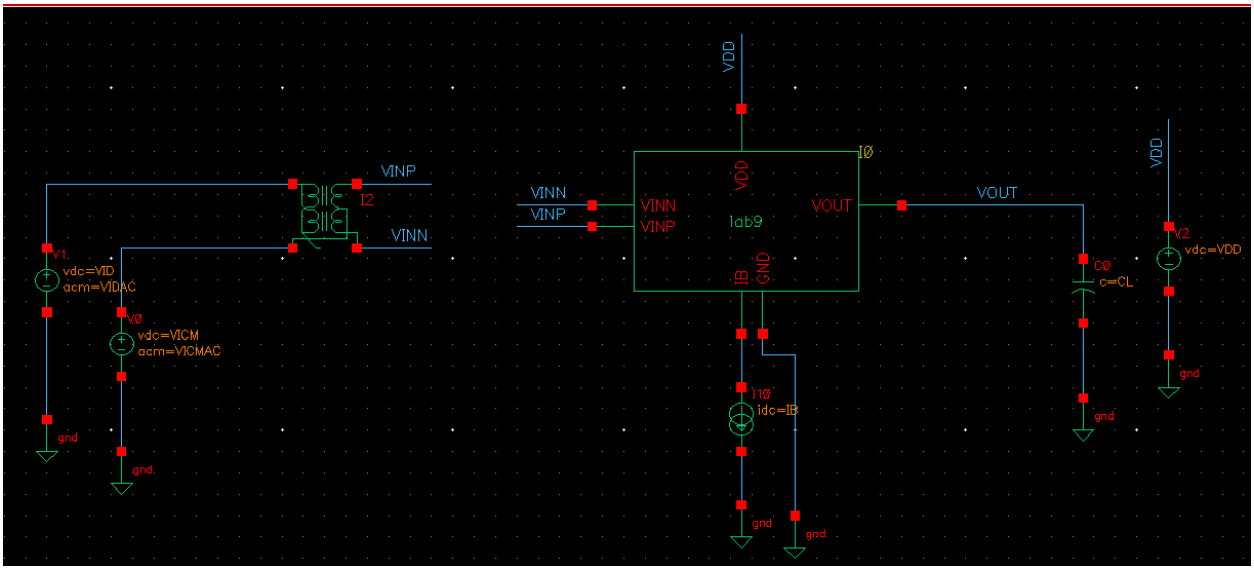

Figure 3.1

-I got the parameters for all transistors as shown in figures 3.2 , 3.3 , 3.4 , 3.5 , 3.6 , 3.7, 3.8 , 3.9.

Test	Output	Nominal
lab999:lab9tb:1	ID	-6.252u
lab999:lab9tb:1	VGS	-535.7m
lab999:lab9tb:1	VDS	-612.3m
lab999:lab9tb:1	VDSAT	-108.2m
lab999:lab9tb:1	VTH	-418.6m
lab999:lab9tb:1	GM	93.62u
lab999:lab9tb:1	GMB	29.83u
lab999:lab9tb:1	GDS	735.3n
lab999:lab9tb:1	REGION	2

Figure 3.2 (M0)

Test	Output	Nominal
lab999:lab9tb:1	ID	-6.252u
lab999:lab9tb:1	VGS	-535.7m
lab999:lab9tb:1	VDS	-612.3m
lab999:lab9tb:1	VDSAT	-108.2m
lab999:lab9tb:1	VTH	-418.6m
lab999:lab9tb:1	GM	93.62u
lab999:lab9tb:1	GMB	29.83u
lab999:lab9tb:1	GDS	735.3n
lab999:lab9tb:1	REGION	2

Figure 3.3 (M1)

Test	Output	Nominal
lab999:lab9tb:1	ID	-12.5u
lab999:lab9tb:1	VGS	-717.2m
lab999:lab9tb:1	VDS	-664.3m
lab999:lab9tb:1	VDSAT	-256.6m
lab999:lab9tb:1	VTH	-395.4m
lab999:lab9tb:1	GM	74.33u
lab999:lab9tb:1	GMB	24.54u
lab999:lab9tb:1	GDS	515.6n
lab999:lab9tb:1	REGION	2

Figure 3.4 (M2)

Test	Output	Nominal
lab999:lab9tb:1	ID	-47.59u
lab999:lab9tb:1	VGS	-717.2m
lab999:lab9tb:1	VDS	-506.5m
lab999:lab9tb:1	VDSAT	-259.1m
lab999:lab9tb:1	VTH	-395.5m
lab999:lab9tb:1	GM	283u
lab999:lab9tb:1	GMB	94.26u
lab999:lab9tb:1	GDS	2.383u
lab999:lab9tb:1	REGION	2

Figure 3.5 (M3)

Test	Output	Nominal
lab999:lab9tb:1	ID	-10u
lab999:lab9tb:1	VGS	-717.2m
lab999:lab9tb:1	VDS	-717.2m
lab999:lab9tb:1	VDSAT	-255.9m
lab999:lab9tb:1	VTH	-395.4m
lab999:lab9tb:1	GM	59.43u
lab999:lab9tb:1	GMB	19.57u
lab999:lab9tb:1	GDS	401.9n
lab999:lab9tb:1	REGION	2

Figure 3.6 (M4)

Test	Output	Nominal
lab999:lab9tb:1	ID	6.251u
lab999:lab9tb:1	VGS	523.4m
lab999:lab9tb:1	VDS	523.4m
lab999:lab9tb:1	VDSAT	105m
lab999:lab9tb:1	VTH	392.6m
lab999:lab9tb:1	GM	93.29u
lab999:lab9tb:1	GMB	26.4u
lab999:lab9tb:1	GDS	634.8n
lab999:lab9tb:1	REGION	2

Figure 3.7 (M5)

Test	Output	Nominal
lab999:lab9tb:1	ID	6.251u
lab999:lab9tb:1	VGS	605.6m
lab999:lab9tb:1	VDS	605.6m
lab999:lab9tb:1	VDSAT	160.2m
lab999:lab9tb:1	VTH	392m
lab999:lab9tb:1	GM	61.17u
lab999:lab9tb:1	GMB	16.81u
lab999:lab9tb:1	GDS	440.7n
lab999:lab9tb:1	REGION	2

Figure 3.8 (M6)

Test	Output	Nominal
lab999:lab9tb:1	ID	47.59u
lab999:lab9tb:1	VGS	605.6m
lab999:lab9tb:1	VDS	1.293
lab999:lab9tb:1	VDSAT	115.6m
lab999:lab9tb:1	VTH	465m
lab999:lab9tb:1	GM	633.7u
lab999:lab9tb:1	GMB	162.6u
lab999:lab9tb:1	GDS	8.773u
lab999:lab9tb:1	REGION	2

Figure 3.9 (M7)

-From figures 3.2 and 3.3, I found that the current (and gm) in the input pair exactly equal because of the symmetry of the circuit.

-I found that the DC voltage at the output of the first stage = 0.5234V as VOUT = VDD – |VDS1|-|VDS2|=1.8 – 0.6123-0.6643= 0.5234V and it is equal to the voltage of the mirror node because of the symmetry of the cct.

And the DC voltage at the output of the second stage = 1.2935V as VOUT= VDD – |VDS3|= 1.8 – 0.5065 = 1.2935V.

2)Diff small signal ccs:

-I used AC analysis (1Hz:10GHz, logarithmic, 10 points/decade),set VIDAC = 1 and VICMAC = 0 and used VICM at the middle of the CMIR to calculate circuit parameters (Ao, Ao in dB, BW,GBW, UGF) as shown in figure 3.10.

Test	Output	Nominal	Spec	Weight	Pass/Fail
lab999:lab9tb:1	Ao	2.44k			
lab999:lab9tb:1	Ao_dB	67.75			
lab999:lab9tb:1	BW	2.234k			
lab999:lab9tb:1	fu	5.369M			
lab999:lab9tb:1	GBW	5.452M			

Figure 3.10

-I plotted diff gain (in dB) vs frequency as shown in figure 3.11.

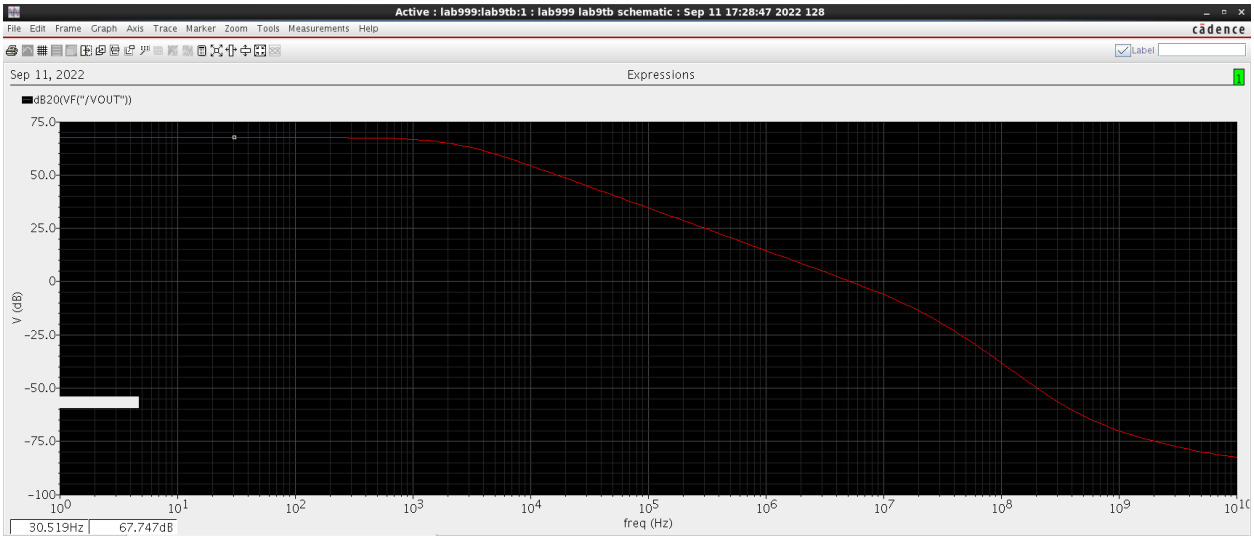

Figure 3.11

-I compared simulation results with hand calculations.

	Simulation	Hand calculations
Avd	67.75dB	$Av = Gm1Rout1 \times Gm2Rout2 = \frac{gm1,2}{2gds3} \times gm7(ro7\backslash\backslash ro3) = 67dB$
Wu	5.369M	$\frac{Gm1}{Cc} = 5.4M$
GBW	5.452M	Ao*BW=5.4M

2)CM small signal ccs:

-I used AC analysis (1Hz:10GHz, logarithmic, 10 points/decade) ,set VICMAC = 1 and VIDAC = 0 and used VICM at the middle of the CMIR.

-I Plotted CM gain in dB vs frequency as shown in figure 3.12

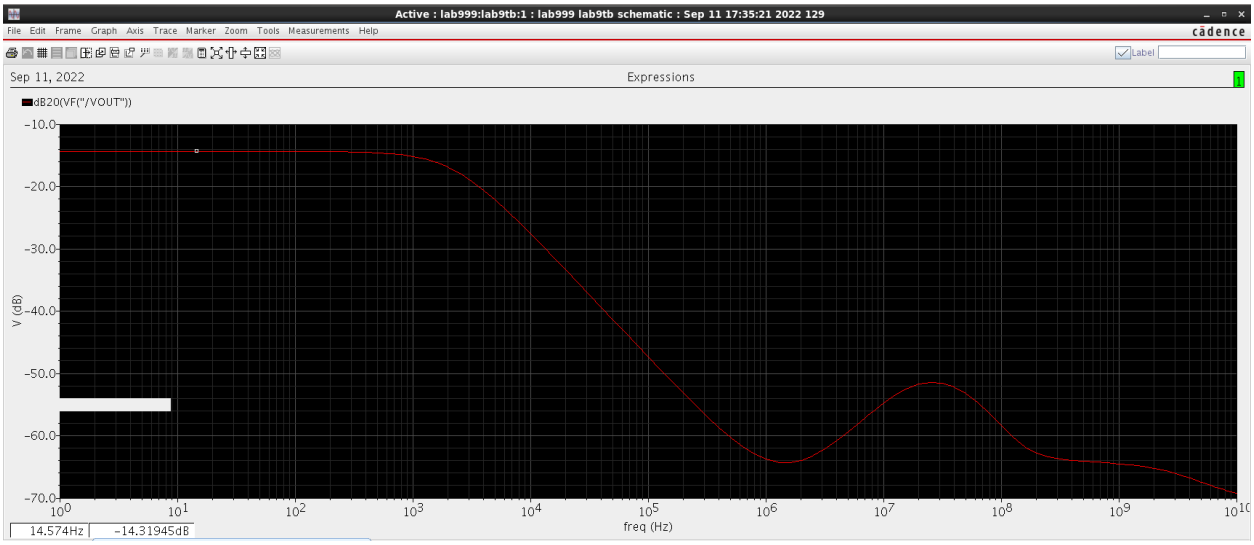

Figure 3.12

-I compared simulation results with hand calculations :

	Simulation	Hand calculaion
AvCM	-14dB	$\|\text{AvCM}\| = \left\|\frac{\text{Vout}}{\text{ViCM}}\right\| \approx \left\|-\frac{1}{2\text{gm3,4} \times \text{ro5}} * \text{Av2}\right\| = -14\text{dB}$

4) CM large signal ccs (region vs VICM):

-I plotted “region” OP parameter vs VICM for the input pair and the tail current source as shown in figure 3.13.

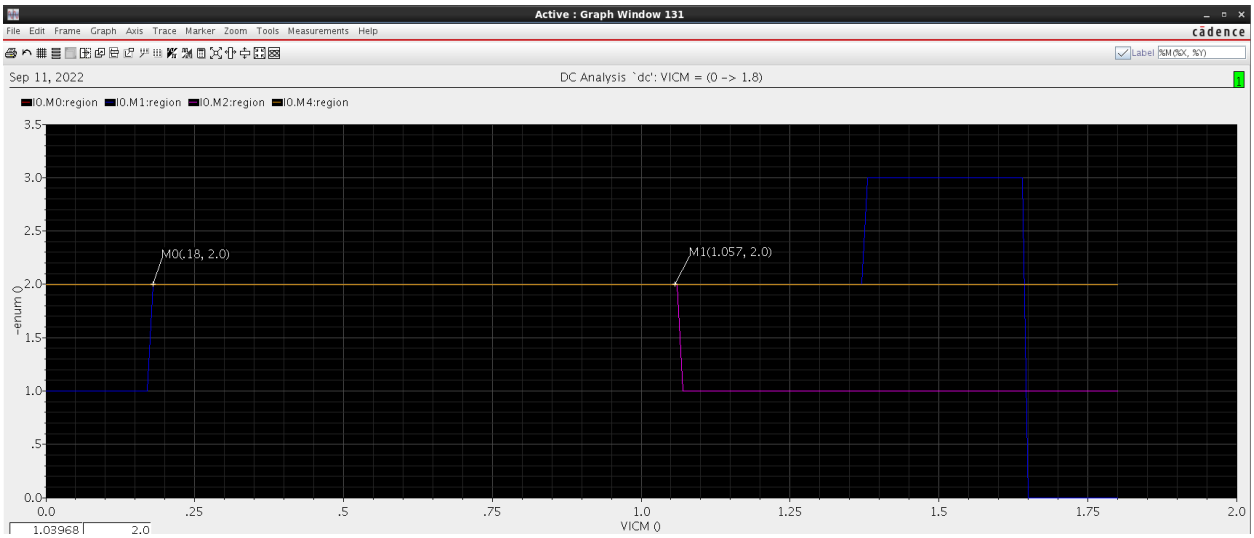

Figure 3.13

-I compared simulation results with hand calculations :

	Simulation	Hand calculations
CMIR	1.057 - 0.18 = 0.877 V	CMIRhigh = VDD− |VGS0|- Vdsat2 = 1.1V CMIRlow = VGS5 -Vth = 0.19V ➔ CMIR = 0.91V

PART 4: Closed-Loop OTA Simulation

-I created a testbench as shown in figure 4.1.

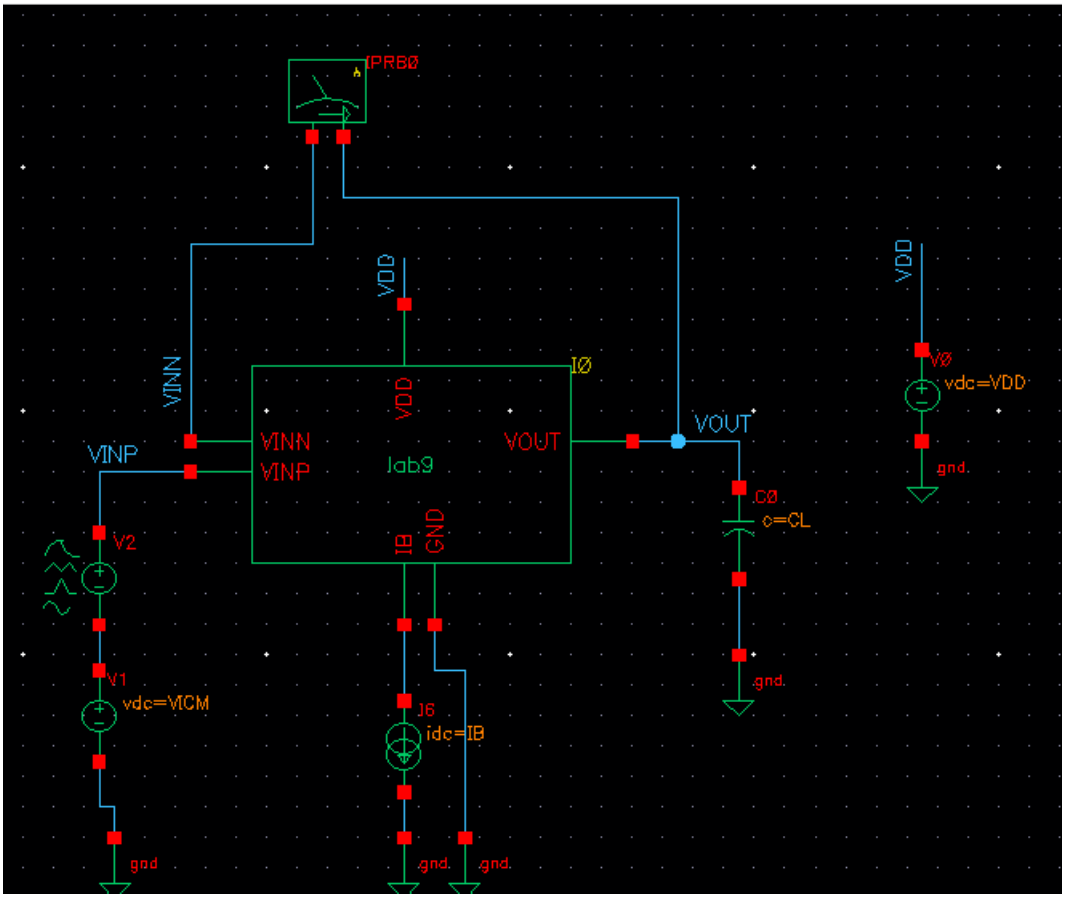

Figure 4.1

-I got the DC OP point for all transistors as shown in figures 4.2, 4.3 , 4.4 , 4.5 , 4.6 , 4.7 , 4.8 , 4.9.

Test	Output	Nominal
lab999:lab9tb2:1	ID	-6.273u
lab999:lab9tb2:1	VGS	-541.7m
lab999:lab9tb2:1	VDS	-538.3m
lab999:lab9tb2:1	VDSAT	-114.6m
lab999:lab9tb2:1	VTH	-414.5m
lab999:lab9tb2:1	GM	89.67u
lab999:lab9tb2:1	GMB	28.63u
lab999:lab9tb2:1	GDS	673.9n
lab999:lab9tb2:1	REGION	2

Figure 4.2(M0)

Test	Output	Nominal
lab999:lab9tb2:1	ID	-6.263u
lab999:lab9tb2:1	VGS	-541.5m
lab999:lab9tb2:1	VDS	-545.9m
lab999:lab9tb2:1	VDSAT	-114.5m
lab999:lab9tb2:1	VTH	-414.5m
lab999:lab9tb2:1	GM	89.59u
lab999:lab9tb2:1	GMB	28.61u
lab999:lab9tb2:1	GDS	671.2n
lab999:lab9tb2:1	REGION	2

Figure 4.3(M1)

Test	Output	Nominal
lab999:lab9tb2:1	ID	-12.53u
lab999:lab9tb2:1	VGS	-657m
lab999:lab9tb2:1	VDS	-658.5m
lab999:lab9tb2:1	VDSAT	-205.2m
lab999:lab9tb2:1	VTH	-405.4m
lab999:lab9tb2:1	GM	97.41u
lab999:lab9tb2:1	GMB	31.7u
lab999:lab9tb2:1	GDS	791.6n
lab999:lab9tb2:1	REGION	2

Figure 4.4(M2)

Test	Output	Nominal
lab999:lab9tb2:1	ID	-49.58u
lab999:lab9tb2:1	VGS	-657m
lab999:lab9tb2:1	VDS	-1.2
lab999:lab9tb2:1	VDSAT	-207.1m
lab999:lab9tb2:1	VTH	-405.6m
lab999:lab9tb2:1	GM	382.1u
lab999:lab9tb2:1	GMB	125.6u
lab999:lab9tb2:1	GDS	2.837u
lab999:lab9tb2:1	REGION	2

Figure 4.5(M3)

Test	Output	Nominal
lab999:lab9tb2:1	ID	-10u
lab999:lab9tb2:1	VGS	-657m
lab999:lab9tb2:1	VDS	-657m
lab999:lab9tb2:1	VDSAT	-204.6m
lab999:lab9tb2:1	VTH	-405.4m
lab999:lab9tb2:1	GM	77.75u
lab999:lab9tb2:1	GMB	25.24u
lab999:lab9tb2:1	GDS	632.2n
lab999:lab9tb2:1	REGION	2

Figure 4.6(M4)

Test	Output	Nominal
lab999:lab9tb2:1	ID	6.263u
lab999:lab9tb2:1	VGS	603.2m
lab999:lab9tb2:1	VDS	595.6m
lab999:lab9tb2:1	VDSAT	157.8m
lab999:lab9tb2:1	VTH	393.1m
lab999:lab9tb2:1	GM	62.32u
lab999:lab9tb2:1	GMB	17.14u
lab999:lab9tb2:1	GDS	458n
lab999:lab9tb2:1	REGION	2

Figure 4.6(M5)

Test	Output	Nominal
lab999:lab9tb2:1	ID	6.267u
lab999:lab9tb2:1	VGS	603.2m
lab999:lab9tb2:1	VDS	603.2m
lab999:lab9tb2:1	VDSAT	157.9m
lab999:lab9tb2:1	VTH	393.1m
lab999:lab9tb2:1	GM	62.35u
lab999:lab9tb2:1	GMB	17.15u
lab999:lab9tb2:1	GDS	456.5n
lab999:lab9tb2:1	REGION	2

Figure 4.7(M6)

Test	Output	Nominal
lab999:lab9tb2:1	ID	49.58u
lab999:lab9tb2:1	VGS	595.6m
lab999:lab9tb2:1	VDS	599.8m
lab999:lab9tb2:1	VDSAT	98.56m
lab999:lab9tb2:1	VTH	483.3m
lab999:lab9tb2:1	GM	752.8u
lab999:lab9tb2:1	GMB	183.1u
lab999:lab9tb2:1	GDS	17.84u
lab999:lab9tb2:1	REGION	2

Figure 4.8(M7)

-I found that the DC voltages at the input terminals of the op-amp aren't exactly equal because the DC loop gain has a finite value so, the DC voltages at the input terminals can't be exactly equal.

-I found that the DC voltage at the output of the first stage isn't exactly equal to the value in the open-loop as the DC voltage at the output of the first stage = 1.8-(0.5459+0.6585)= 0.5956 V and that is because of the feedback.

-I found that the current (and gm) in the input pair are not exactly equal, because of the negative feedback between the output node and VINN node so any incremental variation in input will exactly appear in output and there is a change in DC level because of the negative feedback that made an offset and that causes the mismatch in ID and gm.

2)Loop gain:

-I used STB analysis (1Hz:10Gz, logarithmic, 10 points/decade) in unity gain buffer configuration, used VICM at the middle of the CMIR and plotted loop gain in dB and phase vs frequency as shown in figure 4.9.

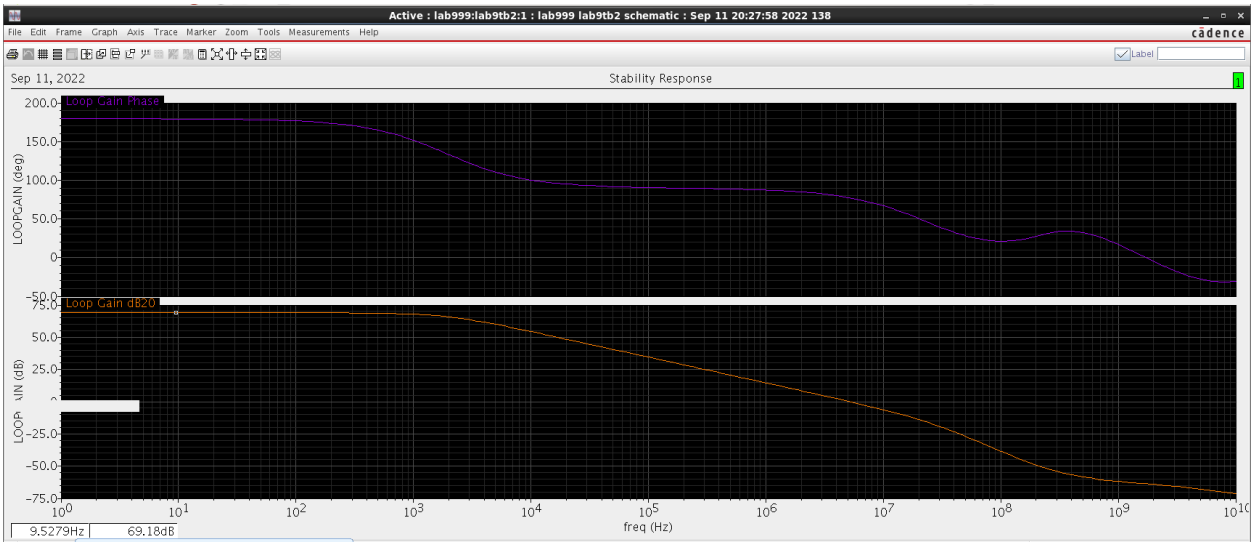

Figure 4.9

-I found that DC gain, fu, and GBW as shown in figure 4.10.

Test	Output	Nominal	Spec	Weight	Pass/Fail
lab999:lab9tb2:1	Ao	2.877k			
lab999:lab9tb2:1	Ao_dB	69.18			
lab999:lab9tb2:1	BW	1.901k			
lab999:lab9tb2:1	fu	5.387M			
lab999:lab9tb2:1	GBW	5.469M			

Figure 4.10

-I found that They are approximately equal in magnitude as this is unity gain buffer so β = 1, $loopgain = Aol * \beta = Aol$ And also they have approximately same bandwidth as β Is independent on frequency so also have approximately same $UGF\ and\ GBW$.

-I found that PM = 76.89

-I compared simulation results with hand calculations.

	simulation	Hand analysis
PM	76.89	$\frac{\text{wp2}}{\text{wu}} = 4.34$ PM=77

2)Slew rate:

-I applied a step input with the following parameters (delay = 1us, initial value = CMIR-low + 50mV, final

value = CMIR-high – 50mV, rise time = 1ns, period = 1s, width = 1s) and run transient analysis (stop = 5us and step = 0.1ns)

-I reported Vin and Vout overlaid as shown in figure 4.11.

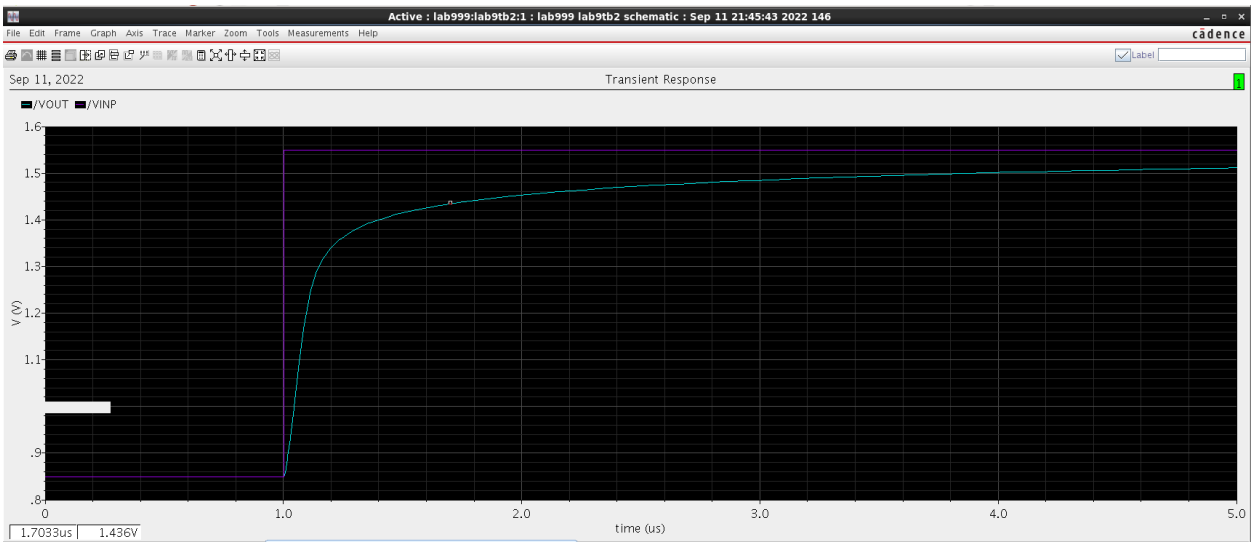

Figure 4.11

-I found that the SR is 4.31V/us as shown in figure 4.12.

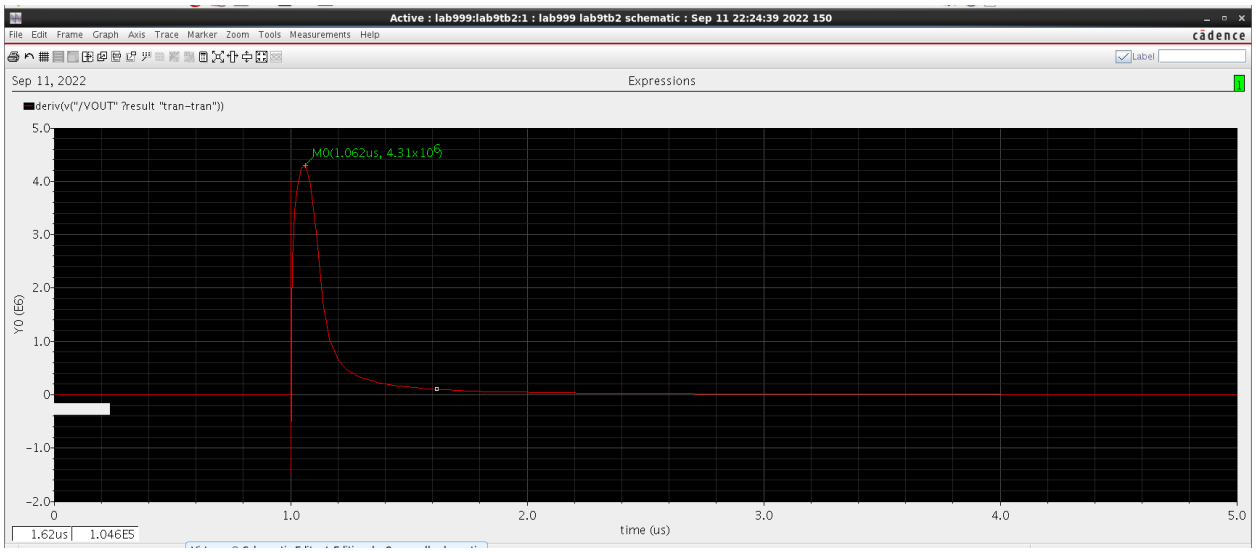

Figure 4.12

-I compared simulation results with hand calculations.

	Simulation	Hand analysis
SR	4.31 V/us	$\frac{IB1}{Cc} = 5$ V/us

4) Settling time:

-I applied a small signal step input with the following parameters (delay = 1us, initial value = the middle of the CMIR, final value = the middle of the CMIR + 5mV, rise time = 1ns, period = 1s, width = 1s).

-I reported Vin and Vout overlaid as shown in figure 4.12.

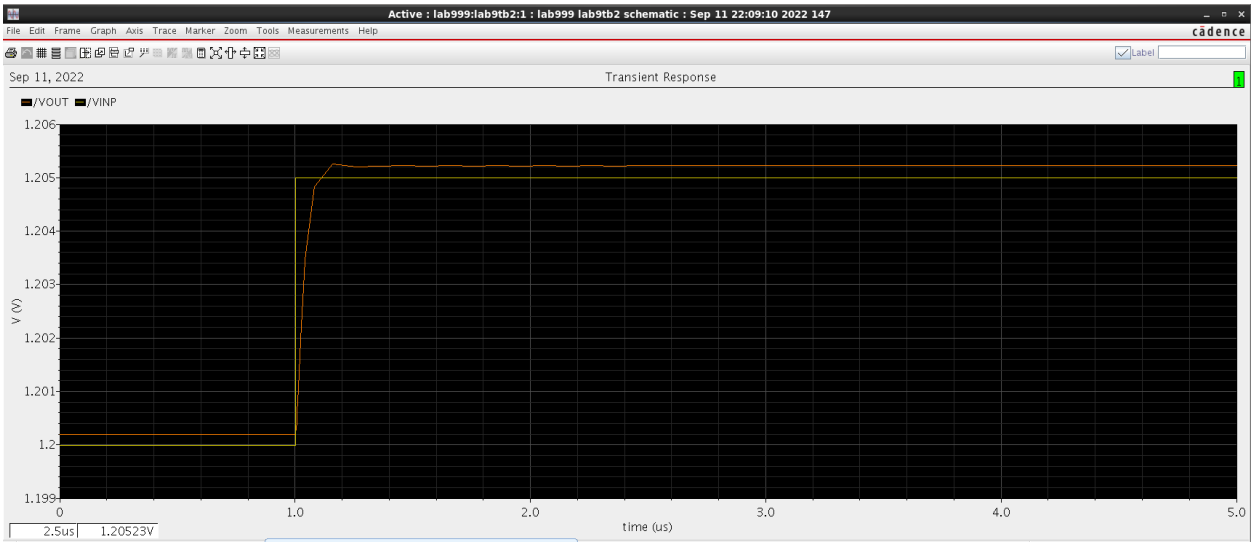

Figure 4.12

-I found that the output rise time as shown in figure 4.13.

Test	Output	Nominal
lab999:lab9tb2:1	riseTime(VT("/VOUT") 0 t 5e-...	68.71n

Figure 4.13

-I Compared simulation results with hand calculations

	simulation	Hand anaysis
Risetime	68.71n	$2.2 \times \frac{1}{2\pi \times \mathrm{wcl}} = 65\mathrm{n}$

-I found that there is very small ringing in time domain is at Cc=2.5pf as decreasing Cc increases UGF which decreases settling time and also decreases phase margin and it can be considered only overshoot not ringing as PM>45 degrees.