Design Challenge

PART 1: OTA Design

We would like to design and simulate a Digitally Controlled Variable Gain Amplifier (VGA).

-Using ADT DDB generation and design cockpit , I designed the OTA to meet all the required specs as shown in figures 1.1 , 1.2.

-I used in my design Two-Stage Miller OTA as it has high DC gain and maximum output swing.

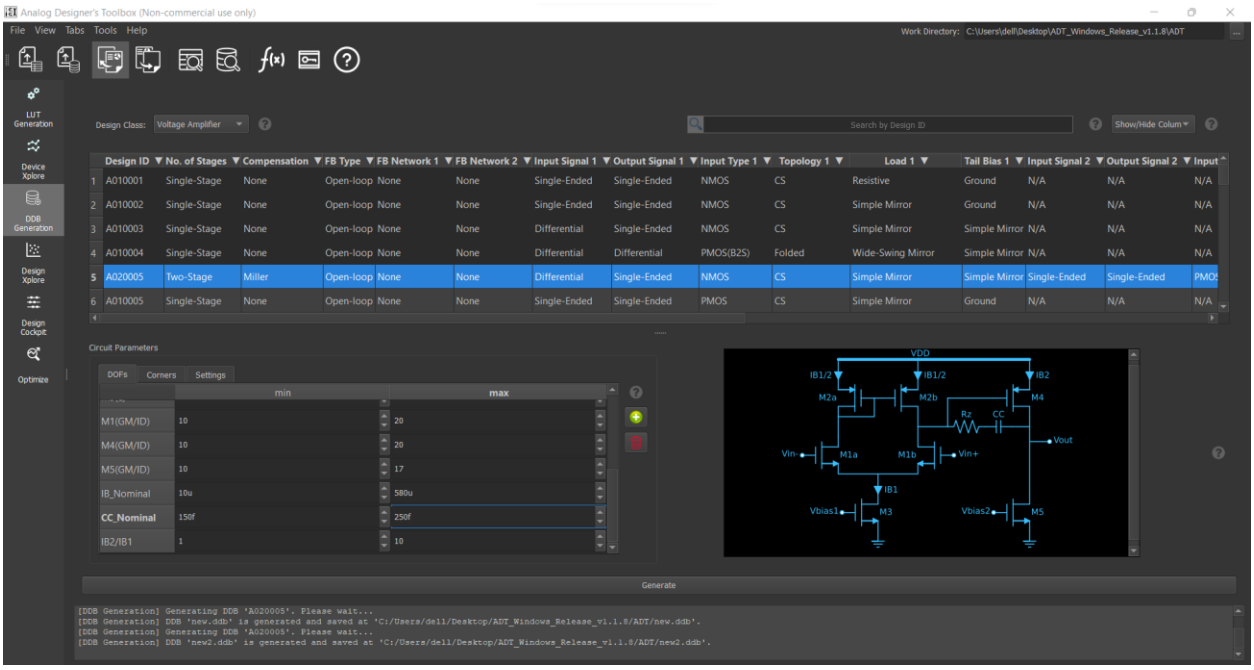

Figure 1.1

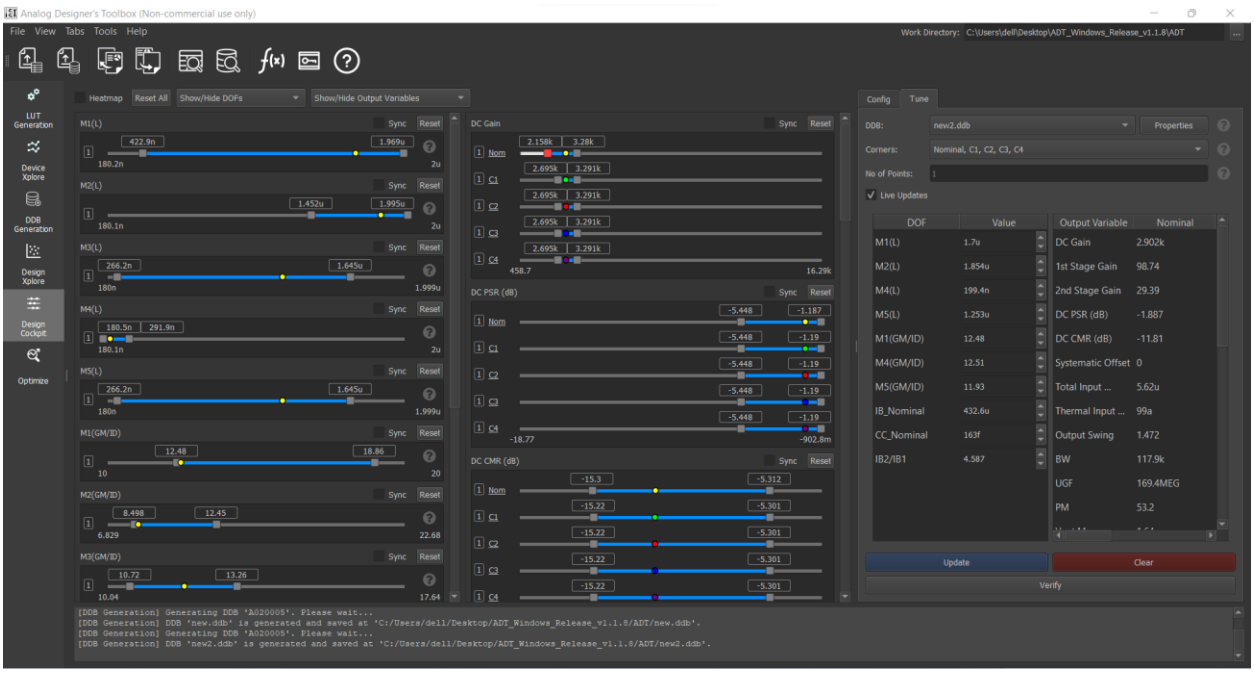

Figure 1.2

- Since the required CMIR is close to the VDD rail, I used an NMOS input stage.

-I used Cc = 250f and Rz = 284.1ohm.

-So , the architecture that I implemented is as shown in figure 1.3.

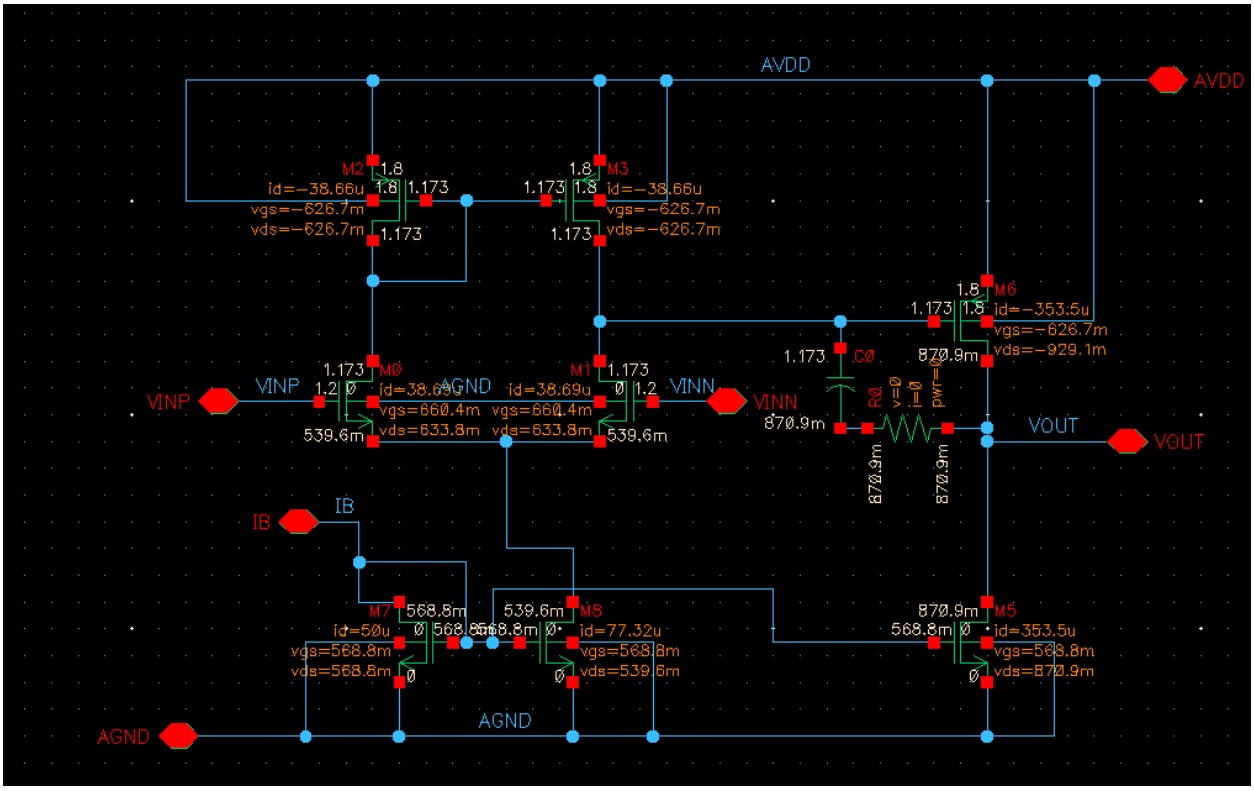

Figure 1.3

	L	W	gm/id	id
M0,1	1.7u	21.88u	12.48	38.715u
M2,3	1.854u	46.19u	12.51	38.715u
M5	1.253u	140.4u	11.93	355.17u
M6	199.4n	62.25u	12.51	355.17u
M7	1.253u	20.44u	11.93	50u
M8	1.253u	31.66u	11.93	77.43u

-I checked that all transistors operate in saturation as shown in figure 1.4.

Test	Output	Nominal
challenge:challengeswitch:1	OP("/I0/M0" "region")	2
challenge:challengeswitch:1	OP("/I0/M1" "region")	2
challenge:challengeswitch:1	OP("/I0/M2" "region")	2
challenge:challengeswitch:1	OP("/I0/M3" "region")	2
challenge:challengeswitch:1	OP("/I0/M5" "region")	2
challenge:challengeswitch:1	OP("/I0/M6" "region")	2
challenge:challengeswitch:1	OP("/I0/M7" "region")	2
challenge:challengeswitch:1	OP("/I0/M8" "region")	2

Figure 1.4

PART 2: Open-Loop OTA Simulation

-I created a testbench as shown in figure 2.1.

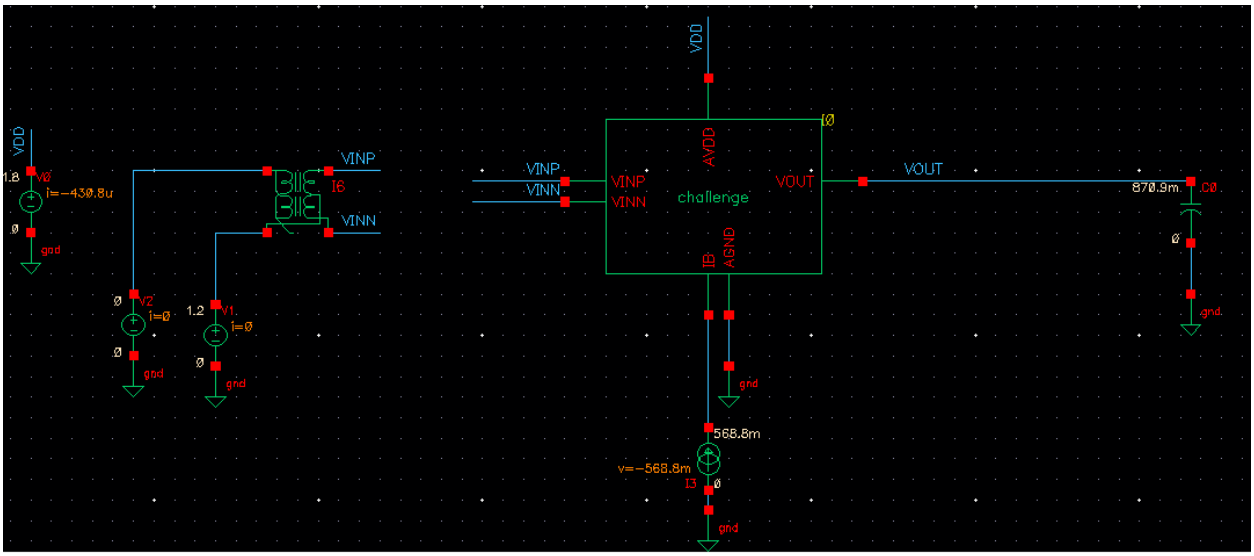

Figure 2.1

-I used AC analysis (1Hz:10Gz, logarithmic, 10 points/decade), set VIDAC = 1 and VICMAC = 0 and I used VICM = 1.2V.

-I used Cadence calculator expressions to calculate circuit parameters (Ao, Ao in dB ,UGF , PM) for all corners of Cc and Rz as shown in figure 2.2.

	Parameter	Nominal					C0	C1	C2	C3
	Cc	250f					225f	225f	275f	275f
	Rz	284.1					227.3	340.9	227.3	340.9

Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max	C0	C1	C2	C3
challenge:challenge1:1	Ao	2.571k				2.571k	2.571k	2.571k	2.571k	2.571k	2.571k
challenge:challenge1:1	Ao_dB	68.2				68.2	68.2	68.2	68.2	68.2	68.2
challenge:challenge1:1	fu	171.3M				159.1M	183.3M	182.8M	183.3M	159.1M	159.7M
challenge:challenge1:1	PM	55.84				54.12	57.5	54.12	55.36	56.07	57.5
challenge:challenge1:1	dB20(VF("/VOUT"))										
challenge:challenge1:1	phase(VF("/VOUT"))										

Figure 2.2

-I plotted diff gain (in dB) and phase vs frequency as shown in figures 2.3 , 2.4 , 2.5.

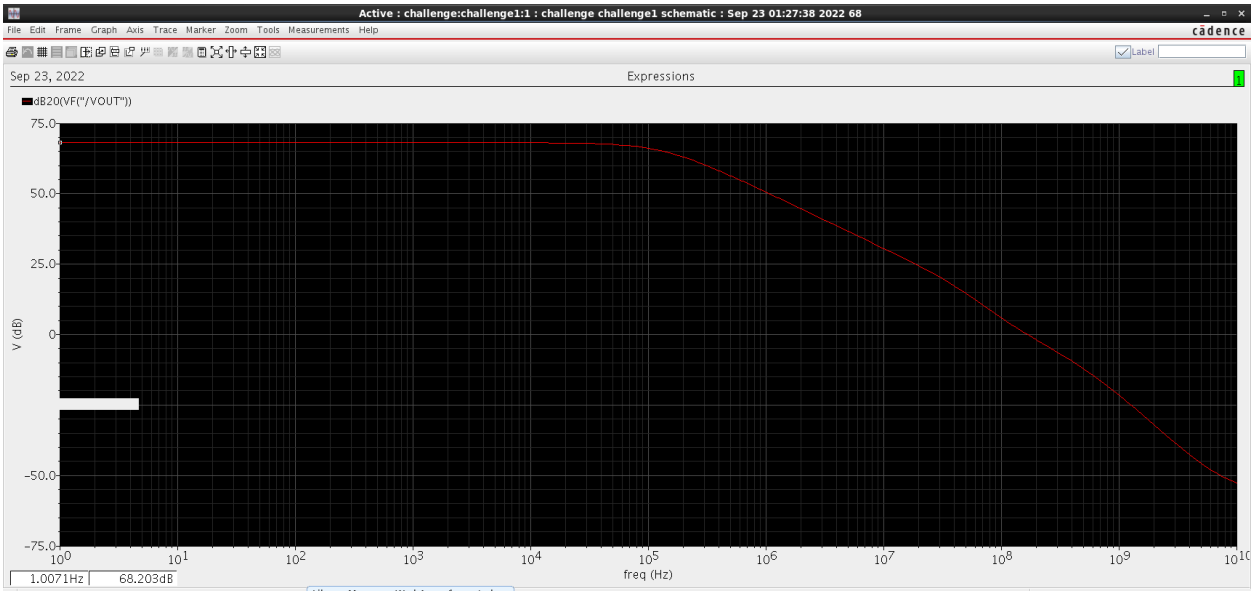

Figure 2.3

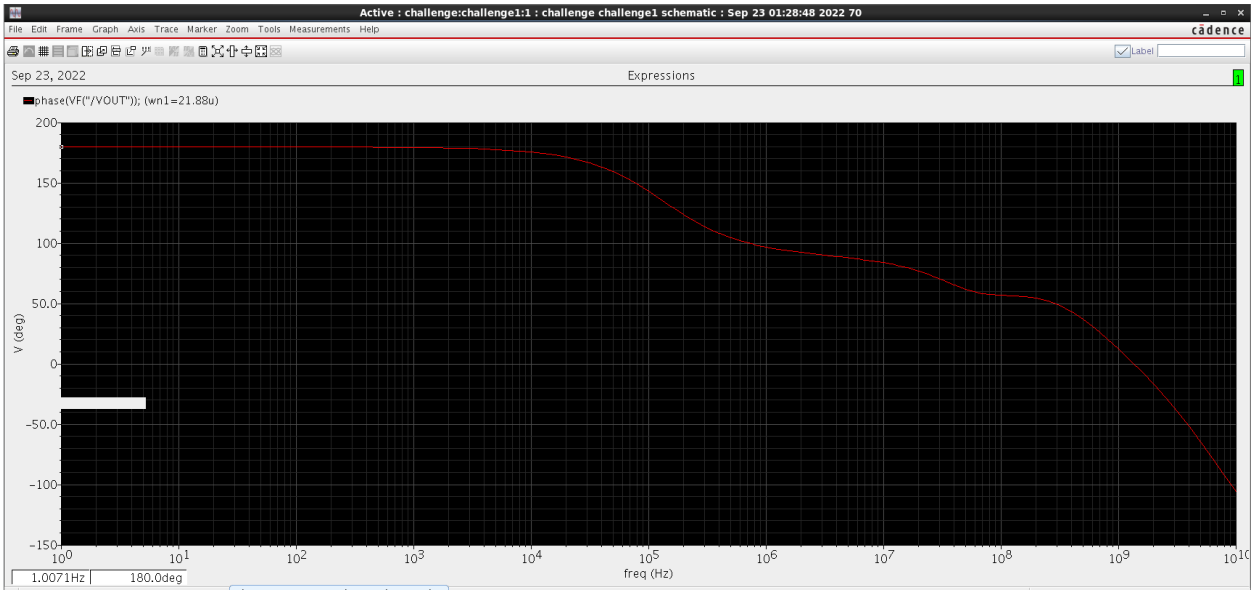

Figure 2.4

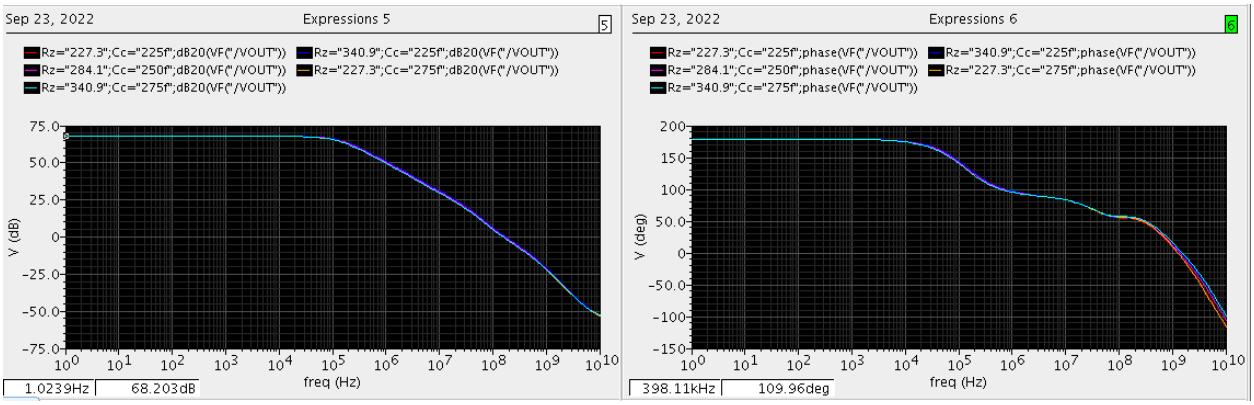

Figure 2.5

-I found that the open lop gain , UGF and PM meet the required specs across all required corners.

PART 3: Closed-Loop OTA Simulation

-I created a new testbench with a switch as shown in figure 3.1.

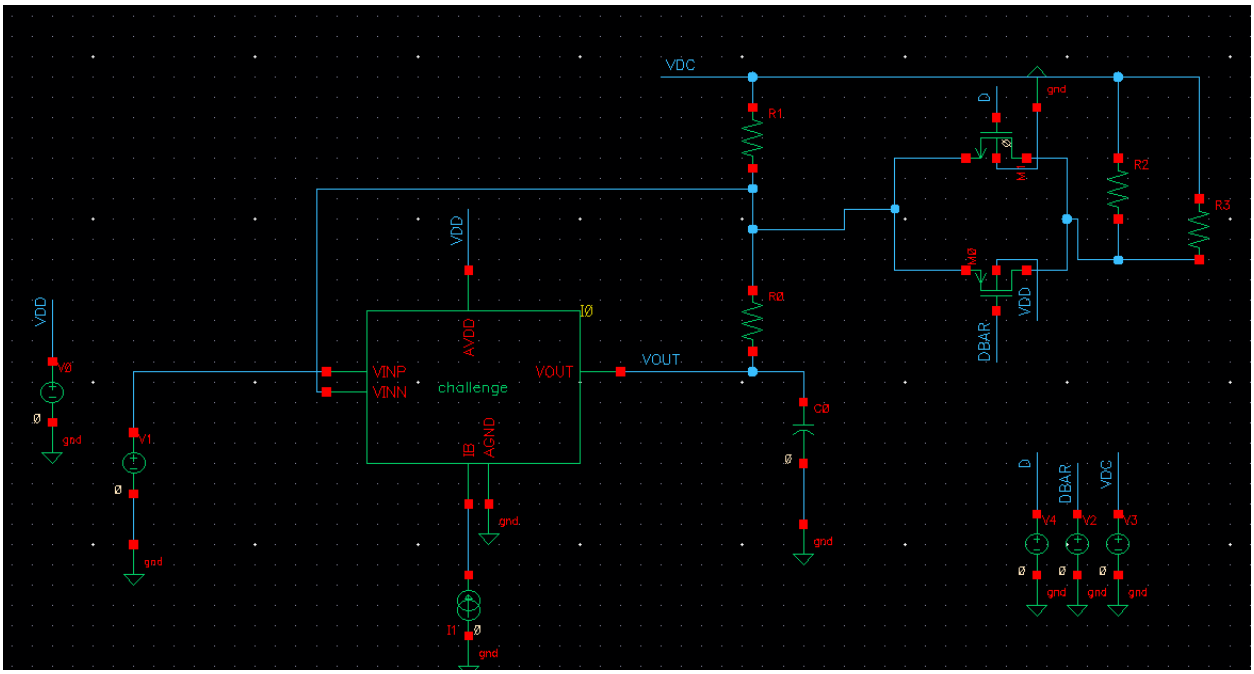

Figure 3.1

-I used AC analysis (1Hz:10Gz, logarithmic, 10 points/decade),set

VICMAC = 1 and I used VICM = 1.2V.

-I used Cadence calculator expressions to calculate circuit parameters (ACL, ACL in dB , UGF , PM) at the two different gain settings and across all required corners of Cc and Rz and as shown in figure 3.2.

		Parameter	Nominal						C0	C1	C2	C3
		Cc	250f						225f	225f	275f	275f
		Rz	284.1						227.3	340.9	227.3	340.9
Point	Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max	C0	C1	C2	C3
Parameters: D=0												
1	challenge:challengeswitch:1	dB20(VF("/VOUT"))										
1	challenge:challengeswitch:1	unityGainFreq(VF("/VOUT"))	126.8M				121.9M	136.6M	136.1M	136.6M	121.9M	122.1M
1	challenge:challengeswitch:1	phaseMargin(VF("/VOUT"))	49.71				48.69	50.4	48.69	49.81	49.07	50.4
Parameters: D=1												
2	challenge:challengeswitch:1	dB20(VF("/VOUT"))										
2	challenge:challengeswitch:1	unityGainFreq(VF("/VOUT"))	140.4M				131.8M	148.7M	148.3M	148.7M	131.8M	132.3M
2	challenge:challengeswitch:1	phaseMargin(VF("/VOUT"))	51.42				50.41	52.49	50.41	51.55	51.16	52.49

Figure 3.2

-I plotted closed loop gain (in dB) vs frequency as shown in figures 3.3

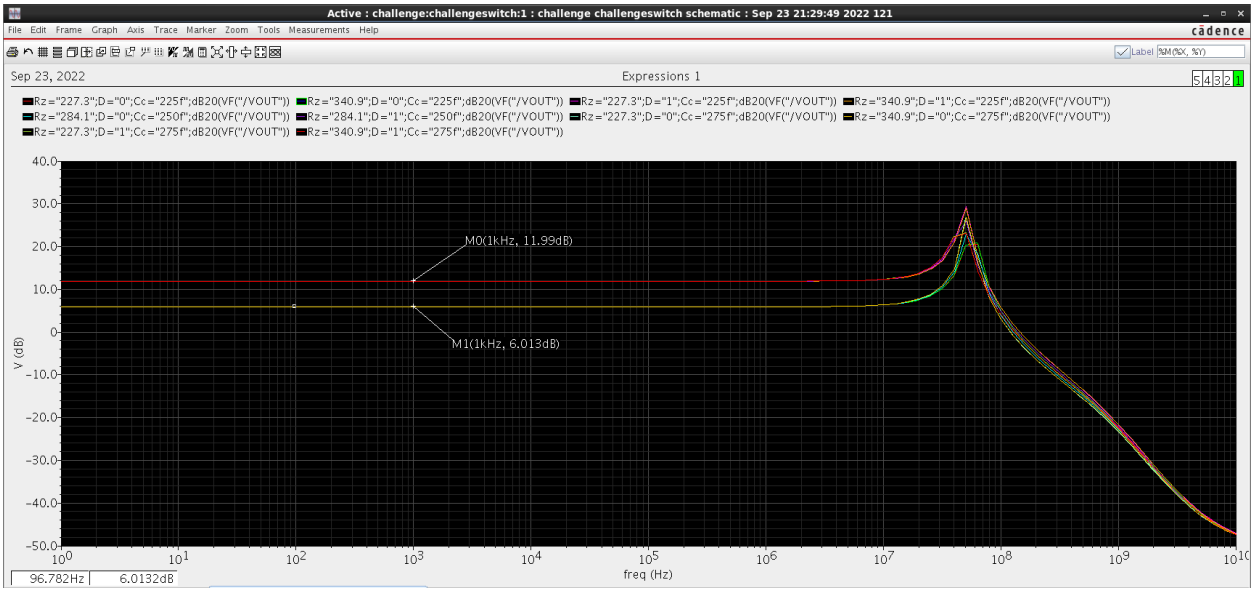

Figure 3.3

-I found that at D=0 the closed loop gain = 6dB and at D=1 the closed loop gain = 12dB and that meet the required Closed loop gain spec across all required corners.

-I found that UGF and PM decreased compared to the case of open loop and that is because of the effect of the -ve feedback (resistive FB) as the gain decreased and there is peaking because there are 2 poles are close to each other.

-I run STB analysis (in addition to AC analysis 1Hz:10Gz, logarithmic, 10 points/decade) using iprobe in the VOUT path.

-I plotted loop gain in dB and phase vs frequency as shown in figure 3.4.

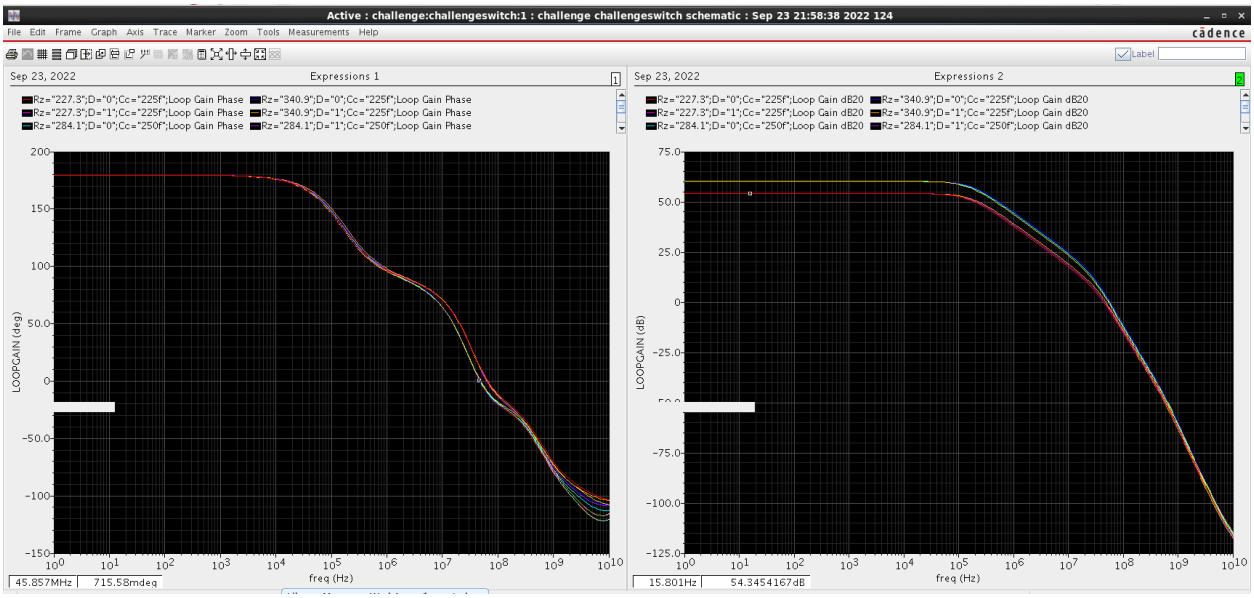

Figure 3.4

-I found that at D=0(ACL = 6dB) the loop gain = 60dB as $\beta = 0.5$ and at D=1(ACL = 12dB) the loop gain = 54dB as $\beta = 0.25$ and OL gain = 2000.

PART 4: Closed Loop Simulation (Transient Analysis)

-I applied a differential sinusoidal input with freq = 1MHz and amplitude = 100mV.

-I run transient analysis for three periods (3us) with 0.1us max time step.

-I plotted the transient signals at VOUT as shown in figure 4.1.

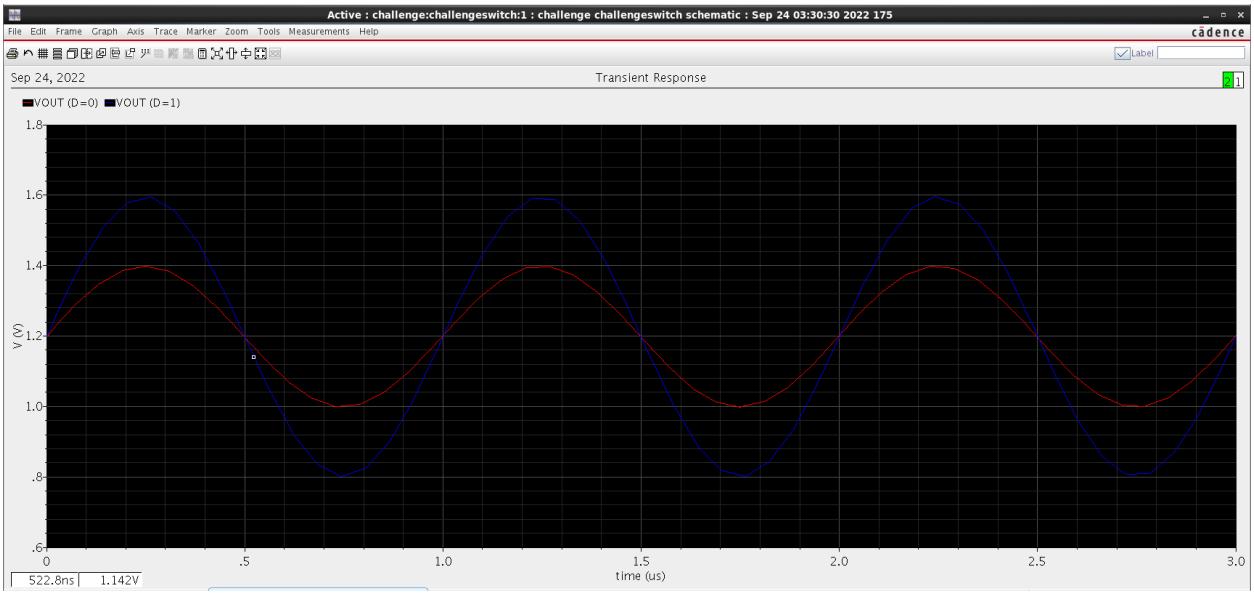

Figure 4.1

-I calculated the output peak-to-peak swing as shown in figure 4.2.

Point	Test	Output	Nominal	Spec	Weight	Pass/Fail
Parameters: D=0						
1	challenge:challengeswitch:1	/VOUT				
1	challenge:challengeswitch:1	peakToPeak(v("/VOUT" ?res...	400m			
Parameters: D=1						
2	challenge:challengeswitch:1	/VOUT				
2	challenge:challengeswitch:1	peakToPeak(v("/VOUT" ?res...	794.8m			

Figure 4.2