LAB 11

PART 1: gm/ID Design Charts

We would like to design a fully-differential folded cascode OTA with capacitive feedback.

-Using ADT Device Xplore, I plotted the following design charts vs gm/ID for both PMOS and NMOS. Set VDS =VDD/3= 600m and

L = 0.18u,0.5u:0.5u:2u as shown in figures 1.1 , 1.2 , 1.3 , 1.4, 1.5.

Figure 1.1(PMOS for input pair)

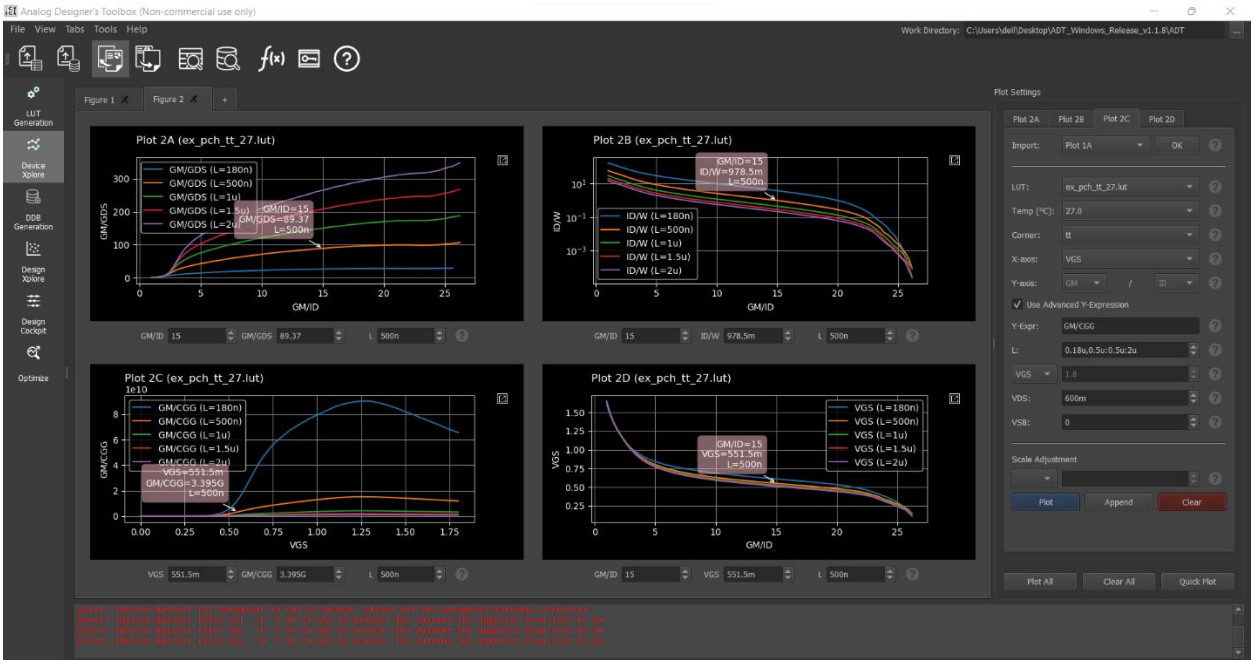

Figure 1.2(PMOS for tail current source)

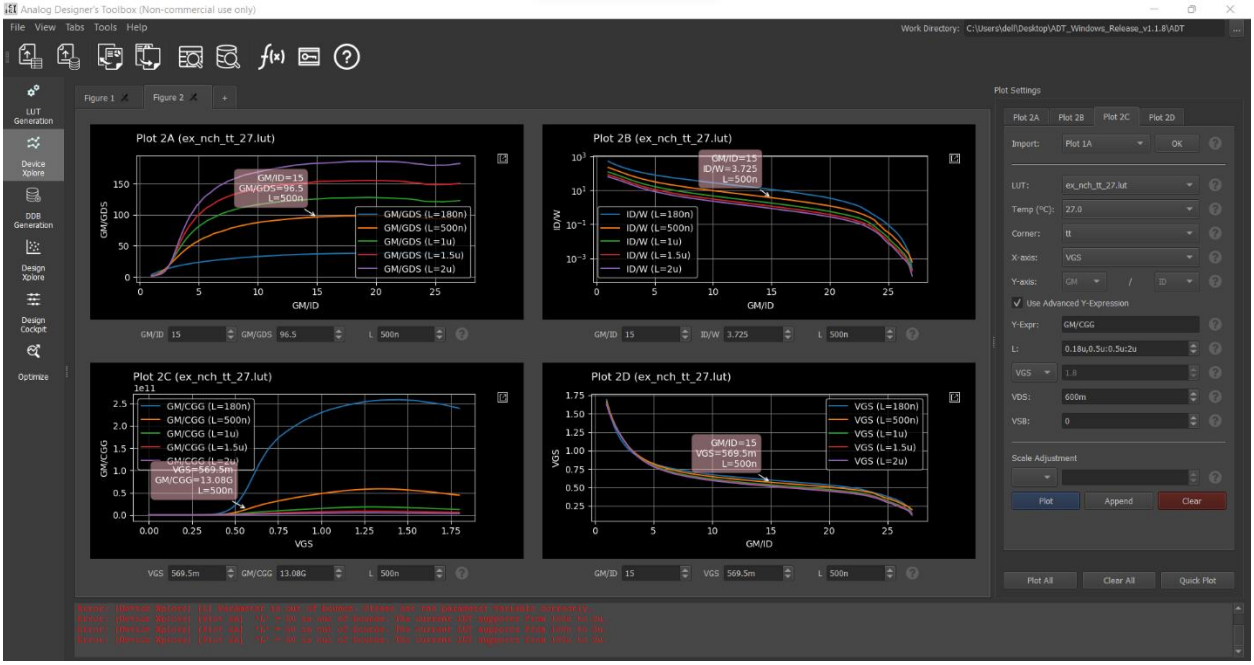

Figure 1.3(NMOS for current mirror load)

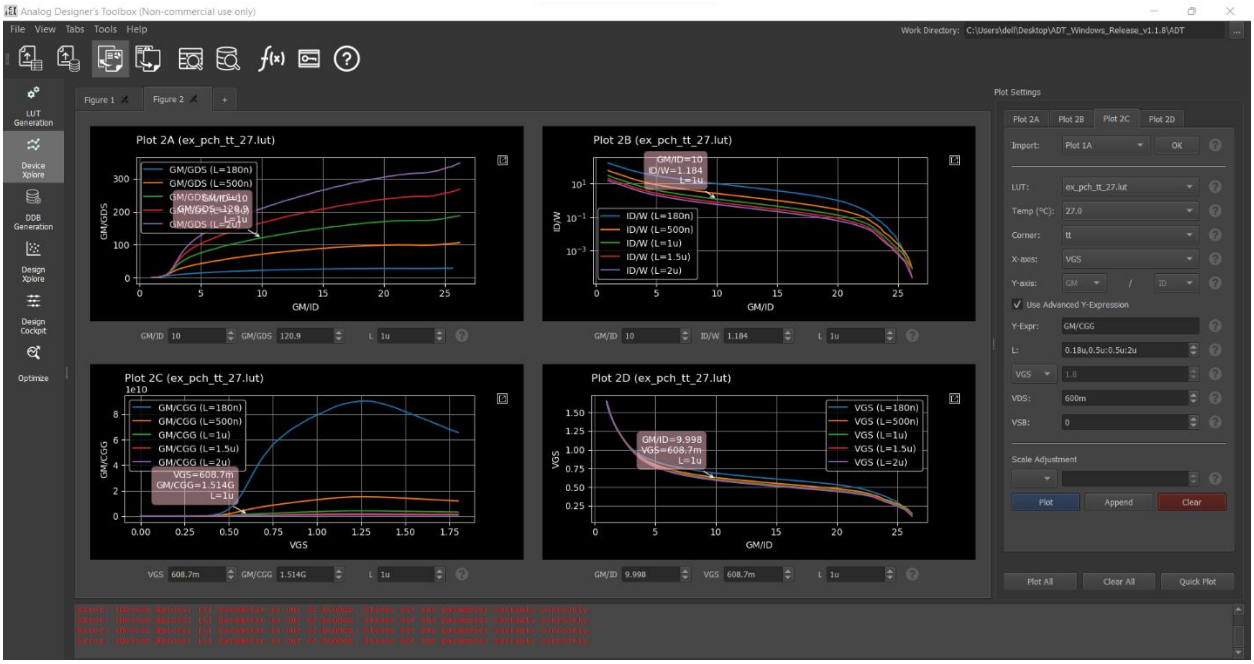

Figure 1.4(PMOS for cascode trans.)

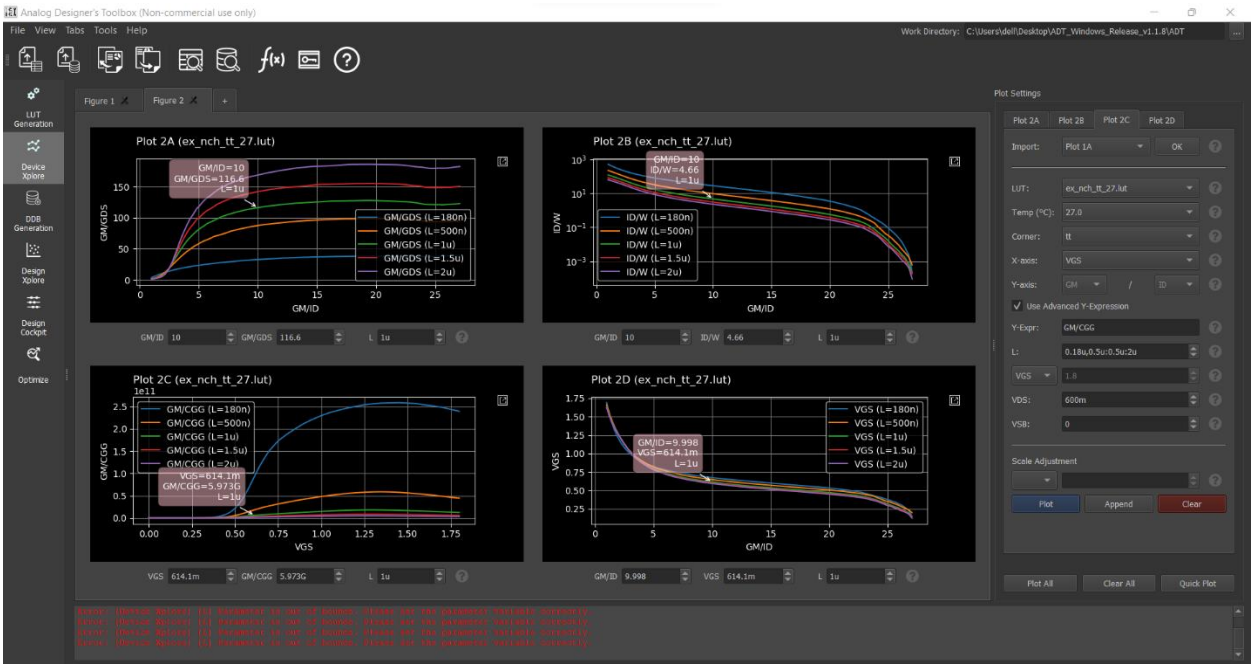

Figure 1.5(NMOS for cascode trans.)

PART 2: OTA Design

From the CMIR spec you will find that I need a PMOS input stage.

The OTA current will be divided as follows: ISS = 40uA for the input pair (CS), and 40uA for the cascode branches (CG). The NMOS current sources in the bottom needs to sink 80uA (2 x 40uA).

For the input pair I used short L and bias it in MI or WI, e.g., L = 0.2um and gm/ID = 15 as shown in figure 1.1.

For the current source transistors I used relatively long L and bias them in SI, e.g., L = 1um and gm/ID =10 as shown in figures 1.2 , 1.3.

For the cascode transistors I used moderate L and bias them in MI or WI, e.g., L = 0.5um and gm/ID =15 as shown in figures 1.4 , 1.5.

From the assumed L and gm/ID (V*) I used the charts to find the sizing (W) of all transistors.

I Set VCASCN ≈ VGSN + V* = 0.7028V and VCASCP ≈ VDD - |VGSP| - V*= 1.115V.

-I designed a fully-differential folded cascode OTA as shown in figure 2.1.

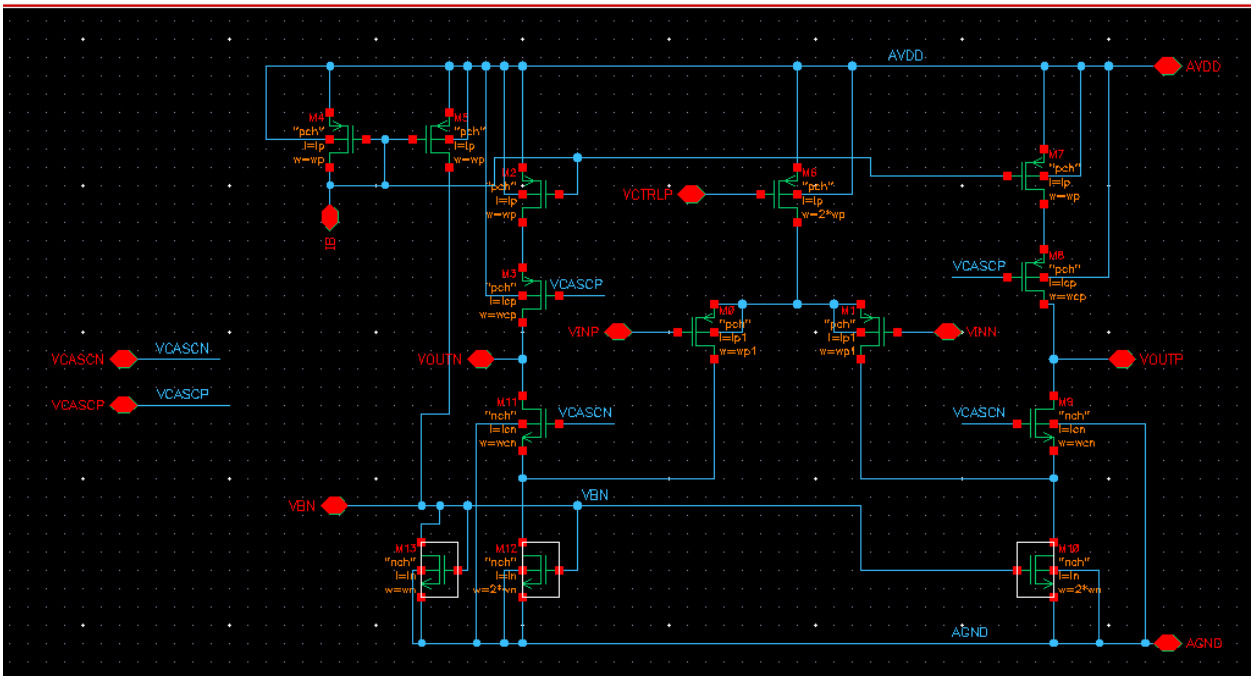
AVDD
AVDD
M4
"pch"
l=lp
w=wp
M5
"pch"
l=lp
w=wp
M6
"pch"
l=lp
w=wp
VCTRLP
M6
"pch"
l=lp
w=2*wp
M7
"pch"
l=lp
w=wp
ID
M3
"pch"
l=lcp
w=wcp
VCASCP
VCASCP
M8
"pch"
l=lcp
w=wcp
VINP
M9
"pch"
l=lp1
w=wp1
M1
"pch"
l=lp1
w=wp1
VINN
VCASCN
VCASCN
VOUTN
VOUTP
VCASCP
VCASCP
M11
"nch"
l=lcn
w=wcn
VCASCN
VCASCN
M9
"nch"
l=lcn
w=wcn
VBN
VBN
M13
"nch"
l=ln
w=wn
M12
"nch"
l=ln
w=2*wn
M10
"nch"
l=ln
w=2*wn
AGND
AGND

Figure 2.1

PART 3: Open-Loop OTA Simulation (Behavioral CMFB)

-I started with a behavioral CMFB network as shown in figure 3.1.

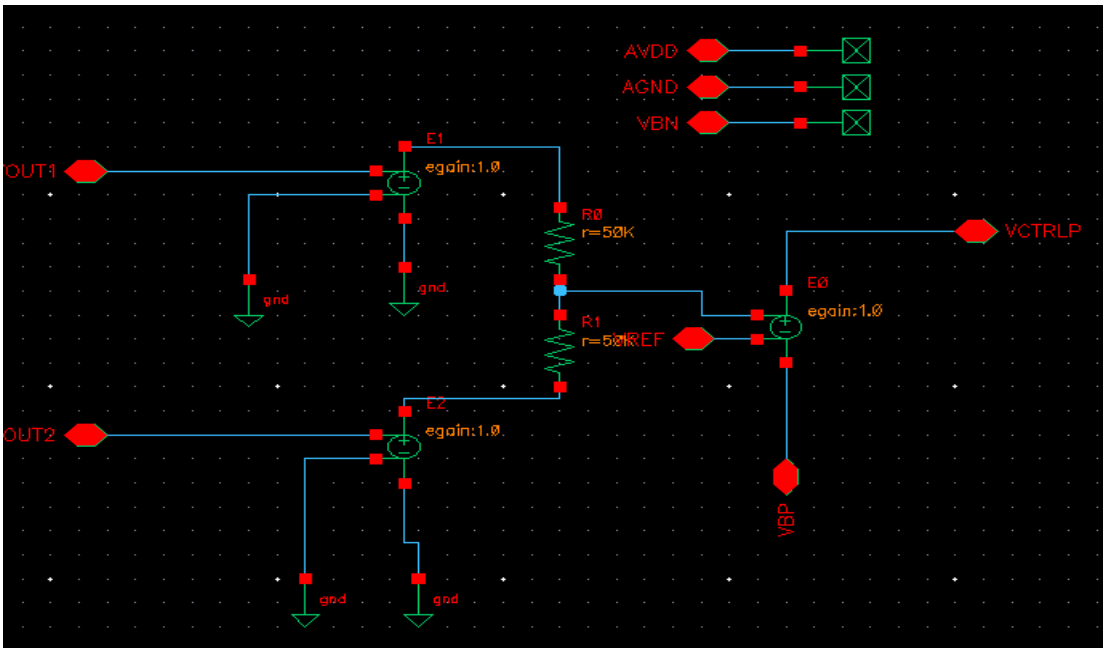

Figure 3.1

-I created a testbench as shown in figure 3.2.

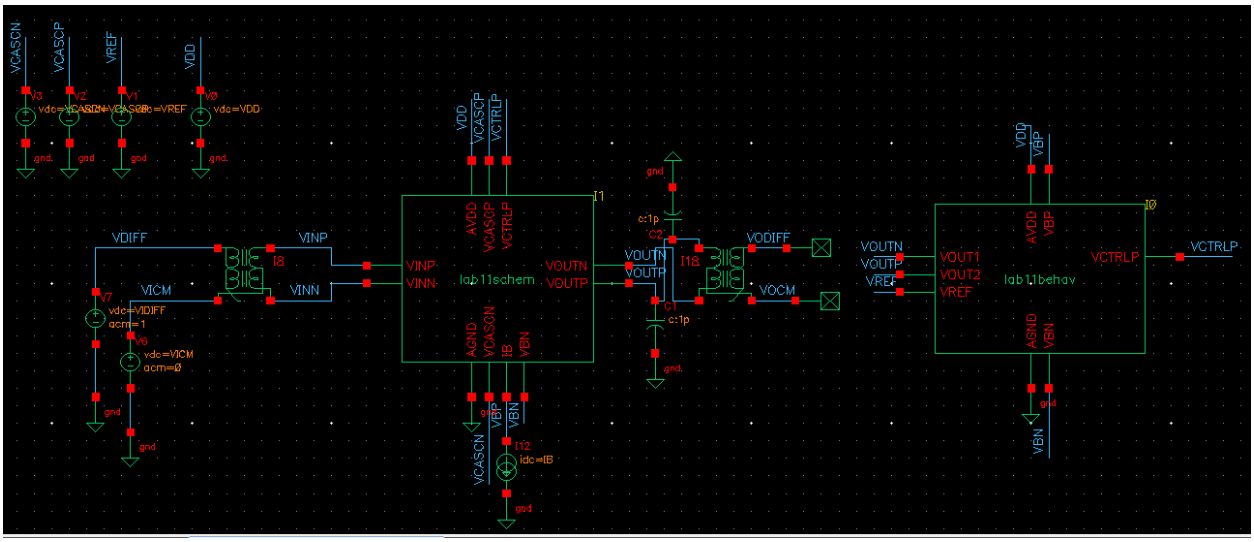

Figure 3.2

-I got the parameters for all transistors as shown in figures 3.3 , 3.4 , 3.5 , 3.6 , 3.7, 3.8 , 3.9 , 3.10 , 3.11 , 3.12 , 3.13 , 3.14 , 3.15 , 3.16 .

Test	Output	Nominal
lab11:lab11tb:1	ID	-20.7u
lab11:lab11tb:1	VGS	-532.3m
lab11:lab11tb:1	VDS	-819.3m
lab11:lab11tb:1	VDSAT	-83.84m
lab11:lab11tb:1	VTH	-463.8m
lab11:lab11tb:1	GM	370.3u
lab11:lab11tb:1	GMB	114.1u
lab11:lab11tb:1	GDS	6.168u
lab11:lab11tb:1	REGION	2

Figure 3.3(M0)

Test	Output	Nominal
lab11:lab11tb:1	ID	-20.7u
lab11:lab11tb:1	VGS	-532.3m
lab11:lab11tb:1	VDS	-819.3m
lab11:lab11tb:1	VDSAT	-83.84m
lab11:lab11tb:1	VTH	-463.8m
lab11:lab11tb:1	GM	370.3u
lab11:lab11tb:1	GMB	114.1u
lab11:lab11tb:1	GDS	6.168u
lab11:lab11tb:1	REGION	2

Figure 3.4 (M1)

Test	Output	Nominal
lab11:lab11tb:1	ID	-19.53u
lab11:lab11tb:1	VGS	-608.6m
lab11:lab11tb:1	VDS	-346.3m
lab11:lab11tb:1	VDSAT	-166.1m
lab11:lab11tb:1	VTH	-411.1m
lab11:lab11tb:1	GM	195.5u
lab11:lab11tb:1	GMB	63.2u
lab11:lab11tb:1	GDS	2.212u
lab11:lab11tb:1	REGION	2

Figure 3.5 (M2)

Test	Output	Nominal
lab11:lab11tb:1	ID	-19.53u
lab11:lab11tb:1	VGS	-653.6m
lab11:lab11tb:1	VDS	-555.9m
lab11:lab11tb:1	VDSAT	-113.9m
lab11:lab11tb:1	VTH	-541.8m
lab11:lab11tb:1	GM	292.2u
lab11:lab11tb:1	GMB	82.04u
lab11:lab11tb:1	GDS	3.265u
lab11:lab11tb:1	REGION	2

Figure 3.6 (M3)

Test	Output	Nominal
lab11:lab11tb:1	ID	-20u
lab11:lab11tb:1	VGS	-608.6m
lab11:lab11tb:1	VDS	-608.6m
lab11:lab11tb:1	VDSAT	-166.1m
lab11:lab11tb:1	VTH	-411.1m
lab11:lab11tb:1	GM	199.7u
lab11:lab11tb:1	GMB	64.59u
lab11:lab11tb:1	GDS	1.644u
lab11:lab11tb:1	REGION	2

Figure 3.7 (M4)

Test	Output	Nominal
lab11:lab11tb:1	ID	-20.9u
lab11:lab11tb:1	VGS	-608.6m
lab11:lab11tb:1	VDS	-1.181
lab11:lab11tb:1	VDSAT	-166.1m
lab11:lab11tb:1	VTH	-411.1m
lab11:lab11tb:1	GM	206.5u
lab11:lab11tb:1	GMB	66.87u
lab11:lab11tb:1	GDS	1.541u
lab11:lab11tb:1	REGION	2

Figure 3.8 (M5)

Test	Output	Nominal
lab11:lab11tb:1	ID	-41.4u
lab11:lab11tb:1	VGS	-610.9m
lab11:lab11tb:1	VDS	-717.7m
lab11:lab11tb:1	VDSAT	-168.3m
lab11:lab11tb:1	VTH	-411.1m
lab11:lab11tb:1	GM	408u
lab11:lab11tb:1	GMB	132.4u
lab11:lab11tb:1	GDS	3.268u
lab11:lab11tb:1	REGION	2

Figure 3.9 (M6)

Test	Output	Nominal
lab11:lab11tb:1	ID	-19.53u
lab11:lab11tb:1	VGS	-608.6m
lab11:lab11tb:1	VDS	-346.3m
lab11:lab11tb:1	VDSAT	-166.1m
lab11:lab11tb:1	VTH	-411.1m
lab11:lab11tb:1	GM	195.5u
lab11:lab11tb:1	GMB	63.2u
lab11:lab11tb:1	GDS	2.212u
lab11:lab11tb:1	REGION	2

Figure 3.10 (M7)

Test	Output	Nominal
lab11:lab11tb:1	ID	-19.53u
lab11:lab11tb:1	VGS	-653.6m
lab11:lab11tb:1	VDS	-555.9m
lab11:lab11tb:1	VDSAT	-113.9m
lab11:lab11tb:1	VTH	-541.8m
lab11:lab11tb:1	GM	292.2u
lab11:lab11tb:1	GMB	82.04u
lab11:lab11tb:1	GDS	3.265u
lab11:lab11tb:1	REGION	2

Figure 3.11 (M8)

Test	Output	Nominal
lab11:lab11tb:1	ID	19.53u
lab11:lab11tb:1	VGS	637.1m
lab11:lab11tb:1	VDS	634.8m
lab11:lab11tb:1	VDSAT	106.9m
lab11:lab11tb:1	VTH	519.4m
lab11:lab11tb:1	GM	298.8u
lab11:lab11tb:1	GMB	74.8u
lab11:lab11tb:1	GDS	3.093u
lab11:lab11tb:1	REGION	2

Figure 3.12(M9)

Test	Output	Nominal
lab11:lab11tb:1	ID	40.23u
lab11:lab11tb:1	VGS	618.9m
lab11:lab11tb:1	VDS	262.9m
lab11:lab11tb:1	VDSAT	160m
lab11:lab11tb:1	VTH	408.1m
lab11:lab11tb:1	GM	393.1u
lab11:lab11tb:1	GMB	109.4u
lab11:lab11tb:1	GDS	8.755u
lab11:lab11tb:1	REGION	2

Figure 3.13 (M10)

Test	Output	Nominal
lab11:lab11tb:1	ID	19.53u
lab11:lab11tb:1	VGS	637.1m
lab11:lab11tb:1	VDS	634.8m
lab11:lab11tb:1	VDSAT	106.9m
lab11:lab11tb:1	VTH	519.4m
lab11:lab11tb:1	GM	298.8u
lab11:lab11tb:1	GMB	74.8u
lab11:lab11tb:1	GDS	3.093u
lab11:lab11tb:1	REGION	2

Figure 3.14 (M11)

Test	Output	Nominal
lab11:lab11tb:1	ID	40.23u
lab11:lab11tb:1	VGS	618.9m
lab11:lab11tb:1	VDS	262.9m
lab11:lab11tb:1	VDSAT	160m
lab11:lab11tb:1	VTH	408.1m
lab11:lab11tb:1	GM	393.1u
lab11:lab11tb:1	GMB	109.4u
lab11:lab11tb:1	GDS	8.755u
lab11:lab11tb:1	REGION	2

Figure 3.15 (M12)

Test	Output	Nominal
lab11:lab11tb:1	ID	20.9u
lab11:lab11tb:1	VGS	618.9m
lab11:lab11tb:1	VDS	618.9m
lab11:lab11tb:1	VDSAT	161m
lab11:lab11tb:1	VTH	405.9m
lab11:lab11tb:1	GM	203.6u
lab11:lab11tb:1	GMB	56.4u
lab11:lab11tb:1	GDS	1.745u
lab11:lab11tb:1	REGION	2

Figure 3.16 (M13)

-I set VICM at the middle of the CMIR = 0.55V and Selected VREF to maximize the symmetrical output swing = 0.9V.

-I tuned gm/ID of the input pair to be = 18 to achieve the CL bandwidth spec.

-I tuned Vcascp to be = 0.7V and Vcascn to be = 1V to keep cascode transistors in saturation.

-I found that the CM level at the OTA output = 0.8959V.

-I found that the differential input = Vref – Vocm= 4.1mV

and the differential output = VBP- VCTRLP = 4.1mV of the error amplifier and the relation between them is the differential gain of the error amp and it is = 1.

	W	L	gm/ID
M0,1	18.7u	270n	18
M2,4,5,7,6	16.89u,33.78u	1u	10
M3,8	20.439u	500n	15
M9,11	5.369u	500u	15
M10,12,13	8.58u,4.29u	1u	10

2) Diff small signal ccs:

-I used AC analysis (1Hz:10Gz, logarithmic, 10 points/decade) , set VIDAC = 1 and VICMAC = 0 and set VICM at the middle of the CMIR.

-I plotted diff gain (magnitude in dB and phase) vs frequency as shown in figures 3.17 and 3.18.

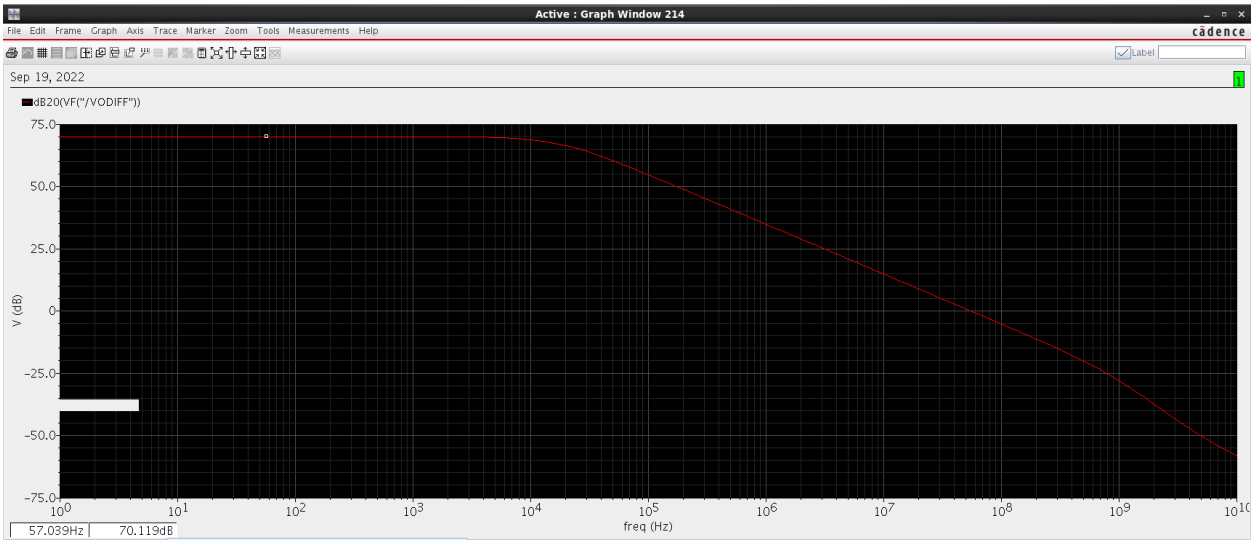

Figure 3.17

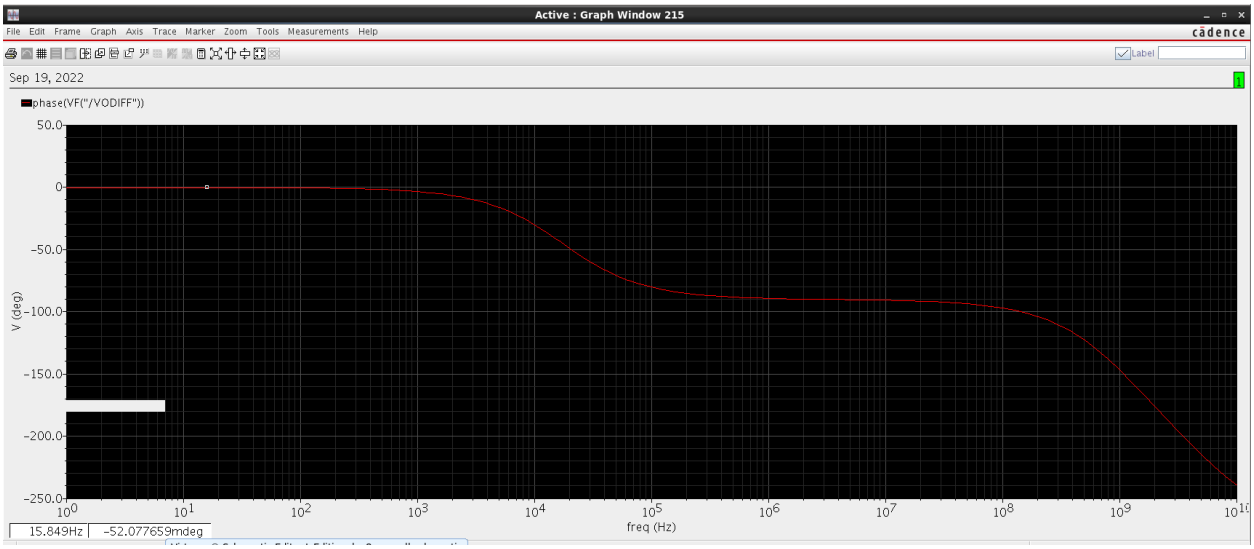

Figure 3.18

-I calculated circuit parameters (DC gain, BW, GBW, UGF, and PM) as shown in figure 3.19.

Test	Output	Nominal	Spec	Weight	Pass/Fail
lab11:lab11tb:1	Ao	3.206k			
lab11:lab11tb:1	Ao_dB	70.12			
lab11:lab11tb:1	BW	17.45k			
lab11:lab11tb:1	fu	56.56M			
lab11:lab11tb:1	GBW	55.95M			
lab11:lab11tb:1	PM	86.16			

Figure 3.19

-I compared simulation results with hand calculations.

	Simulation	Hand calculations
Avd	3.206k=70.119dB	Av = $gm1(ro7ro8gm8\\ (ro9(ro1\\ ro10)gm9)) = 3200 = 70.1dB$
GBW	55.95M	$\frac{\mathrm{gm1}}{2\pi\mathrm{CL}} = 57\mathrm{M}$
BW	17.45kHz	$\frac{\mathrm{GBW}}{\mathrm{Ao}} = 17.9\mathrm{kHz}$
Fu	56.56M	$\frac{\mathrm{gm1}}{2\pi\mathrm{CL}} = 57\mathrm{M}$
PM	86.16deg	$\mathrm{wt} = \frac{\mathrm{gm1}}{\mathrm{Cgg}}$ $= 9.402\mathrm{G}, \mathrm{wp2}$ $= \frac{\mathrm{wt}}{3}, \mathrm{PM}$ $= 90 - \tan^{-1}\left(\frac{\mathrm{wu}}{\mathrm{wp2}}\right)$ $= 88.966\mathrm{deg}$

PART 4: Open-Loop OTA Simulation (Actual CMFB)

-I create a new schematic view for the actual CMFB circuit as shown in figure 4.1.

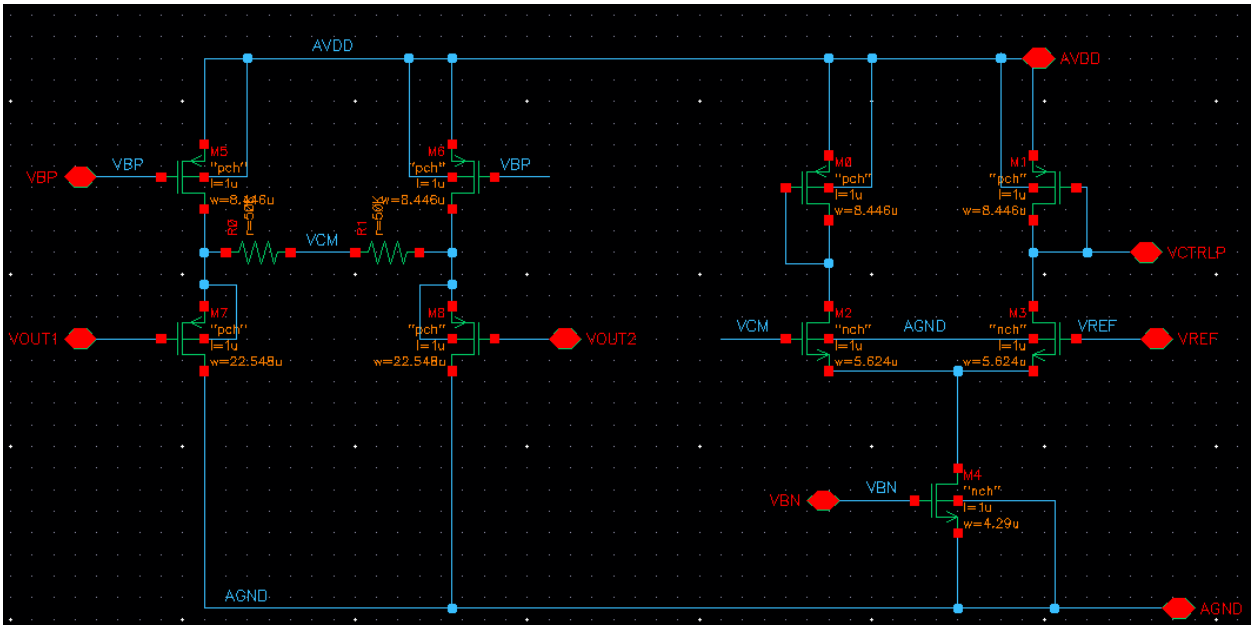

Figure 4.1

- The 40uA current is divided between the four CMFB branches so every branch should have 10uA.

-I assumed L = 1um and gm/ID =15 for all transistors with unknown L or gm/ID for simplicity .

- L and gm/ID for some transistors are already known as they are similar to the current source transistors of the folded cascode OTA.

-I got W for every transistor from charts.

-I got the parameters for all transistors as shown in figures 4.2 , 4.3 , 4.4 , 4.5 , 4.6, 4.7 , 4.8 , 4.9 , 4.10 .

Test	Output	Nominal
lab11:lab11tb2:1	ID	-10.45u
lab11:lab11tb2:1	VGS	-613.5m
lab11:lab11tb2:1	VDS	-613.5m
lab11:lab11tb2:1	VDSAT	-168.8m
lab11:lab11tb2:1	VTH	-411m
lab11:lab11tb2:1	GM	101.8u
lab11:lab11tb2:1	GDS	848.7n
lab11:lab11tb2:1	REGION	2

Figure 4.2(M0)

Test	Output	Nominal
lab11:lab11tb2:1	ID	-10.36u
lab11:lab11tb2:1	VGS	-612.6m
lab11:lab11tb2:1	VDS	-612.6m
lab11:lab11tb2:1	VDSAT	-168.2m
lab11:lab11tb2:1	VTH	-411m
lab11:lab11tb2:1	GM	101.4u
lab11:lab11tb2:1	GDS	843n
lab11:lab11tb2:1	REGION	2

Figure 4.3(M1)

Test	Output	Nominal
lab11:lab11tb2:1	ID	10.45u
lab11:lab11tb2:1	VGS	683.5m
lab11:lab11tb2:1	VDS	619.4m
lab11:lab11tb2:1	VDSAT	111.5m
lab11:lab11tb2:1	VTH	564.9m
lab11:lab11tb2:1	GM	158.2u
lab11:lab11tb2:1	GDS	1.283u
lab11:lab11tb2:1	REGION	2

Figure 4.4(M2)

Test	Output	Nominal
lab11:lab11tb2:1	ID	10.36u
lab11:lab11tb2:1	VGS	682.9m
lab11:lab11tb2:1	VDS	620.3m
lab11:lab11tb2:1	VDSAT	111.1m
lab11:lab11tb2:1	VTH	564.9m
lab11:lab11tb2:1	GM	157.3u
lab11:lab11tb2:1	GDS	1.275u
lab11:lab11tb2:1	REGION	2

Figure 4.5(M3)

Test	Output	Nominal
lab11:lab11tb2:1	ID	20.81u
lab11:lab11tb2:1	VGS	618.9m
lab11:lab11tb2:1	VDS	567.1m
lab11:lab11tb2:1	VDSAT	160.8m
lab11:lab11tb2:1	VTH	406.2m
lab11:lab11tb2:1	GM	203u
lab11:lab11tb2:1	GDS	1.792u
lab11:lab11tb2:1	REGION	2

Figure 4.6(M4)

Test	Output	Nominal
lab11:lab11tb2:1	ID	-9.902u
lab11:lab11tb2:1	VGS	-608.6m
lab11:lab11tb2:1	VDS	-549.4m
lab11:lab11tb2:1	VDSAT	-165.1m
lab11:lab11tb2:1	VTH	-411m
lab11:lab11tb2:1	GM	98.97u
lab11:lab11tb2:1	GDS	836.9n
lab11:lab11tb2:1	REGION	2

Figure 4.7(M5)

Test	Output	Nominal
lab11:lab11tb2:1	ID	-9.902u
lab11:lab11tb2:1	VGS	-608.6m
lab11:lab11tb2:1	VDS	-549.4m
lab11:lab11tb2:1	VDSAT	-165.1m
lab11:lab11tb2:1	VTH	-411m
lab11:lab11tb2:1	GM	98.97u
lab11:lab11tb2:1	GDS	836.9n
lab11:lab11tb2:1	REGION	2

Figure 4.8(M6)

Test	Output	Nominal
lab11:lab11tb2:1	ID	-9.902u
lab11:lab11tb2:1	VGS	-524.1m
lab11:lab11tb2:1	VDS	-1.251
lab11:lab11tb2:1	VDSAT	-105.3m
lab11:lab11tb2:1	VTH	-411.1m
lab11:lab11tb2:1	GM	150.2u
lab11:lab11tb2:1	GDS	907.8n
lab11:lab11tb2:1	REGION	2

Figure 4.9(M7)

Test	Output	Nominal
lab11:lab11tb2:1	ID	-9.902u
lab11:lab11tb2:1	VGS	-524.1m
lab11:lab11tb2:1	VDS	-1.251
lab11:lab11tb2:1	VDSAT	-105.3m
lab11:lab11tb2:1	VTH	-411.1m
lab11:lab11tb2:1	GM	150.2u
lab11:lab11tb2:1	GDS	907.8n
lab11:lab11tb2:1	REGION	2

Figure 4.10(M8)

	W	L	gm/ID
M0,1	11.06u	1u	10
M2,3	5.624u	1u	15
M4	4.29u	1u	10
M5,6	8.446u	1u	10
M7,8	22.548u	1u	15

-I found that the CM level at the OTA output = 879.6mV as it is equal to (voutp+voutn)/2= 879.6mV and The feedback network forces the CM level of Vout1 and Vout2 to approach VREF.

-I found that the differential input = Vcm – Vref = 1.877mV

and the differential output = VBP- VCTRLP= 4.0757mV of the error amplifier and the relation between them is the differential gain of the error amp and it is = 2.17.

2) Diff small signal ccs:

-I used AC analysis (1Hz:10Gz, logarithmic, 10 points/decade) , set VIDAC = 1 and VICMAC = 0 and set VICM at the middle of the CMIR.

-I plotted diff gain (magnitude in dB and phase) vs frequency as shown in figures 4.11 and 4.12.

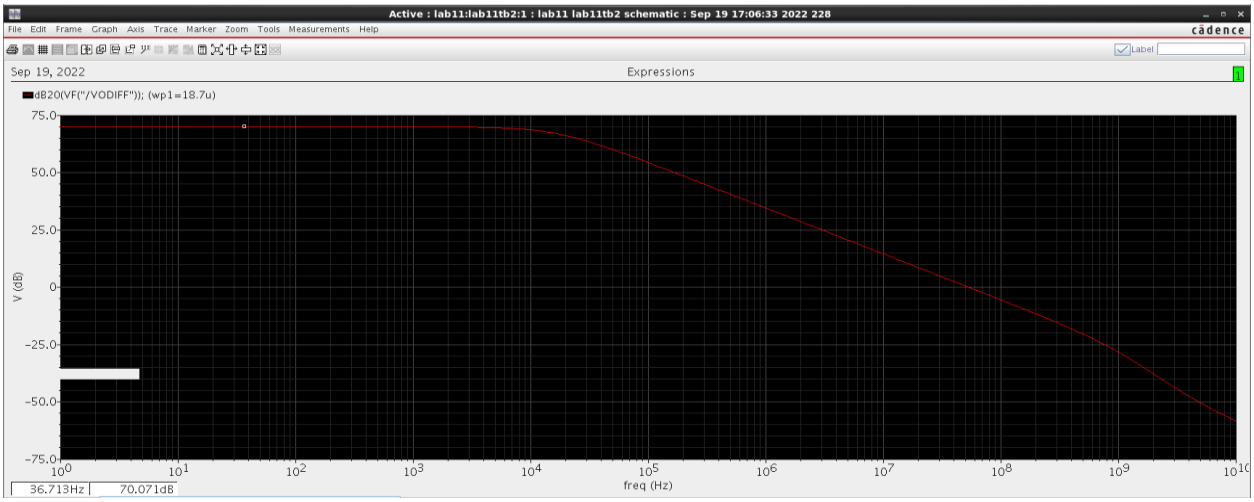

Figure 4.11

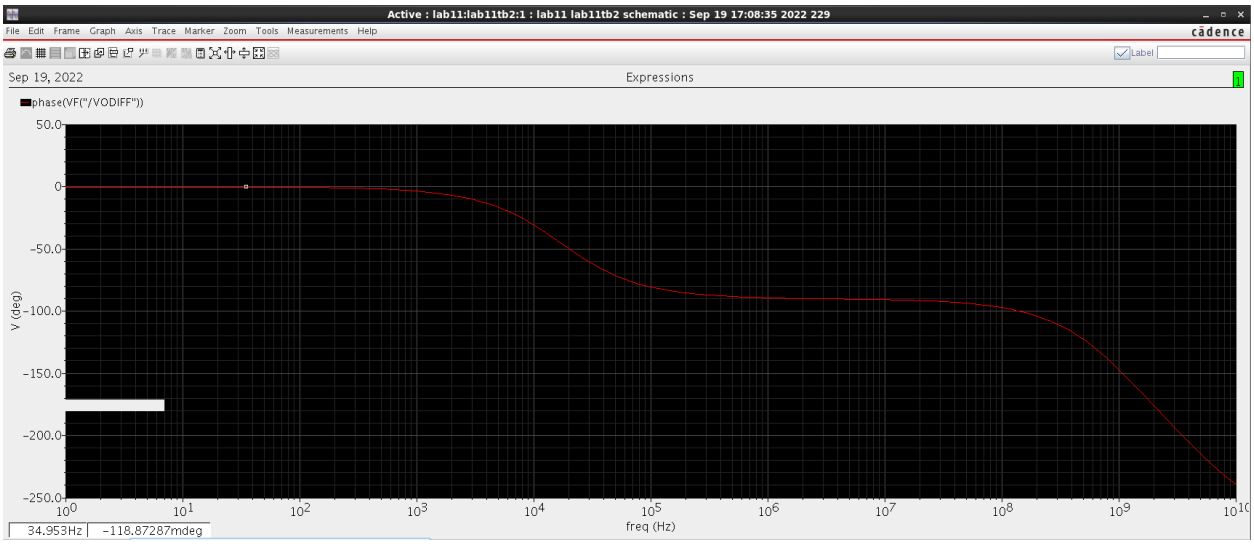

Figure 4.12

-I calculated circuit parameters (DC gain, BW, GBW, UGF, and PM) as shown in figure 4.13.

Test	Output	Nominal
lab11:lab11tb2:1	Ao	3.188k
lab11:lab11tb2:1	Ao_dB	70.07
lab11:lab11tb2:1	BW	16.97k
lab11:lab11tb2:1	fu	54.62M
lab11:lab11tb2:1	GBW	54.1M
lab11:lab11tb2:1	PM	86.22
lab11:lab11tb2:1	dB20(VF("/VODIFF"))	

Figure 4.13

PART 5: Closed Loop Simulation (AC and STB Analysis)

-I created a new testbench with the OTA connected in closed-loop feedback configuration using capacitive feedback as shown in figure 5.1.

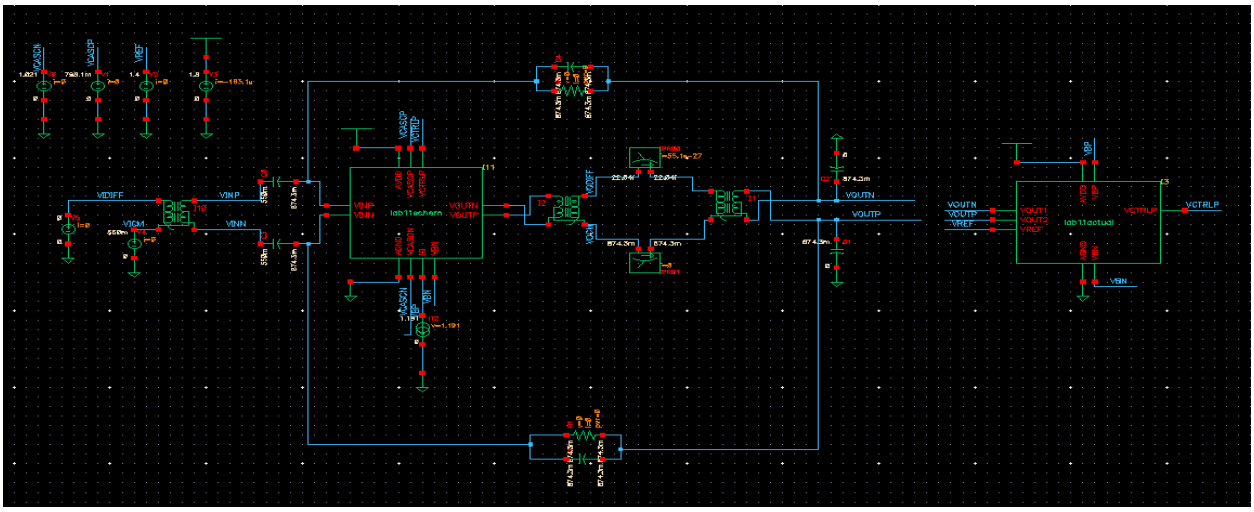

Figure 5.1

-I got schematic of the OTA and the CMFB circuit with DC OP point clearly annotated as shown in figure 5.2.

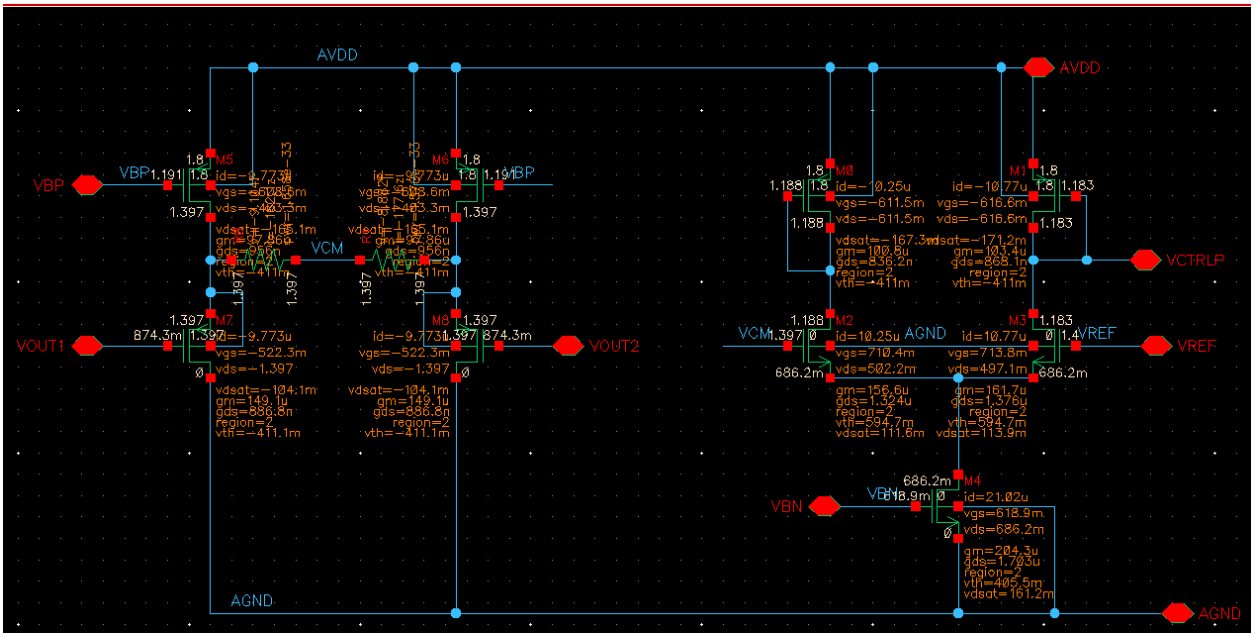

Figure 5.2

-I found that the CM level at the OTA output = 875.3mV as The feedback network forces the CM level of Vout1 and Vout2 to approach VREF.

-I found that the CM level at the OTA input = 875.3mV as the CM DC level provided before the input balun is useless because it is blocked by the capacitor.

2)Differential closed-loop response:

-I used AC analysis (1Hz:10Gz, logarithmic, 10 points/decade) and set VIDAC = 1 and VICMAC = 0.

-I Plotted VODIFF vs frequency as shown in figure 5.3.

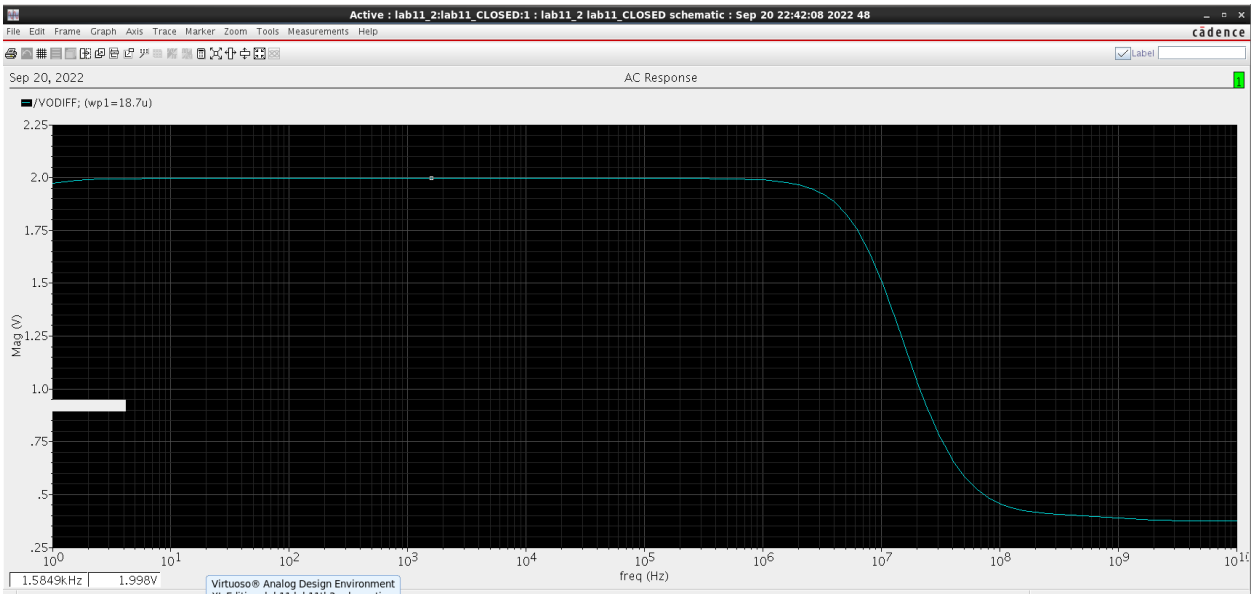

Figure 5.3

-I used Measures or cursors to calculate circuit parameters (DC gain, CL BW, CL GBW) as shown in figure 5.4.

Test	Output	Nominal	Spec	Weight	Pass/Fail
lab11_2:lab11_CLOSED:1	Ao	1.998			
lab11_2:lab11_CLOSED:1	BW_CL	11.95M			
lab11_2:lab11_CLOSED:1	GBW_CL	23.88M			
lab11_2:lab11_CLOSED:1	/VODIFF				

Figure 5.4

3)Differential and CMFB loops stability (STB analysis):

-I run STB analysis (in addition to AC analysis 1Hz:10Gz, logarithmic, 10 points/decade) .

-I plotted loop gain (diff) in dB and phase of vs frequency as shown in figures 5.5 , 5.6.

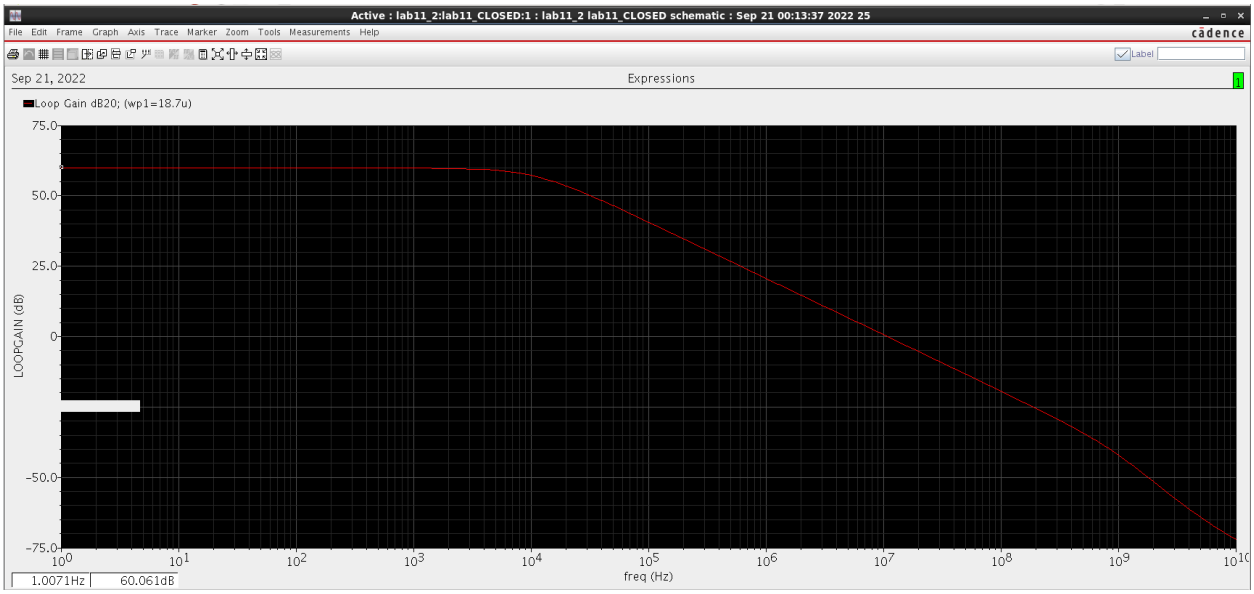

Figure 5.5

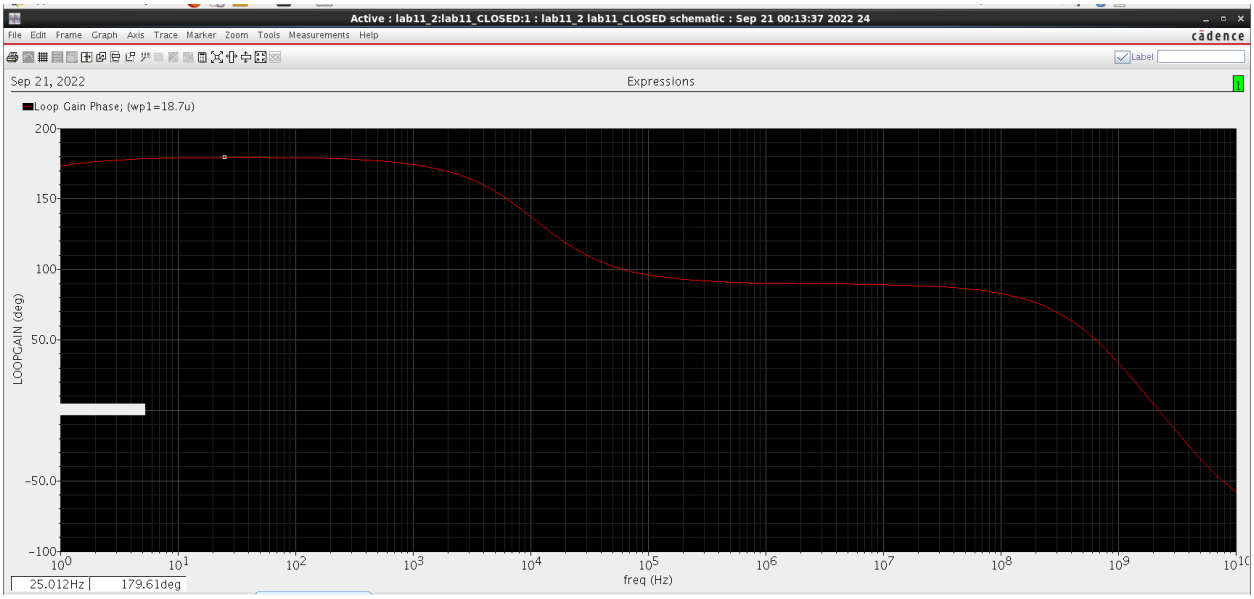

Figure 5.6

-I plotted loop gain (CM) in dB and phase of vs frequency as shown in figures 5.7 , 5.8.

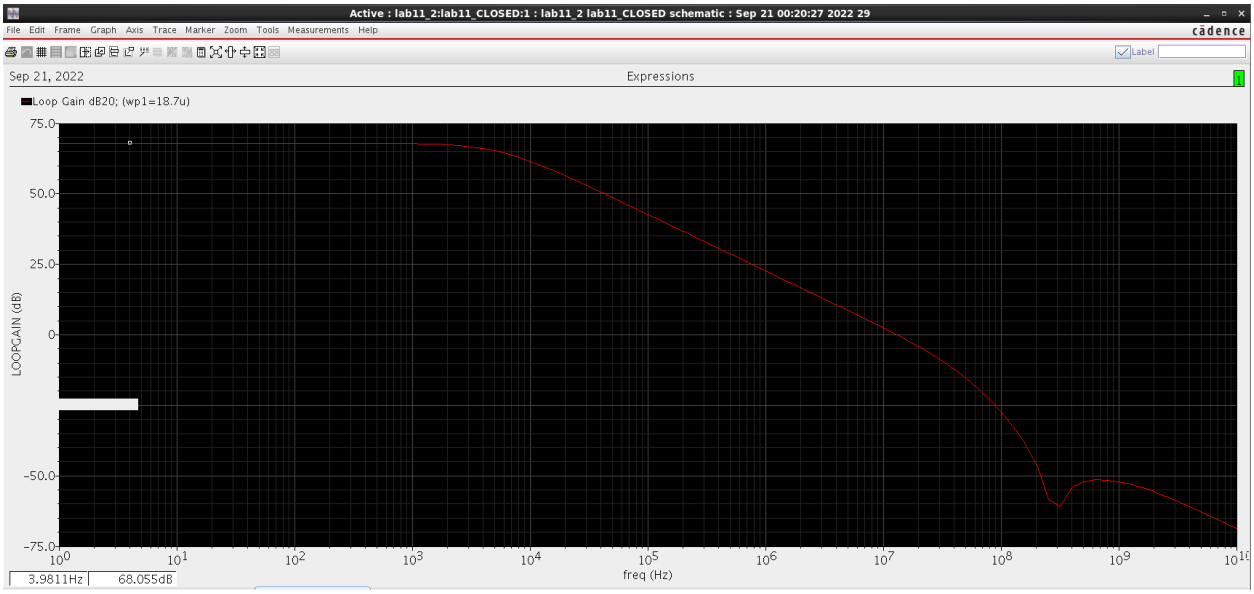

Figure 5.7

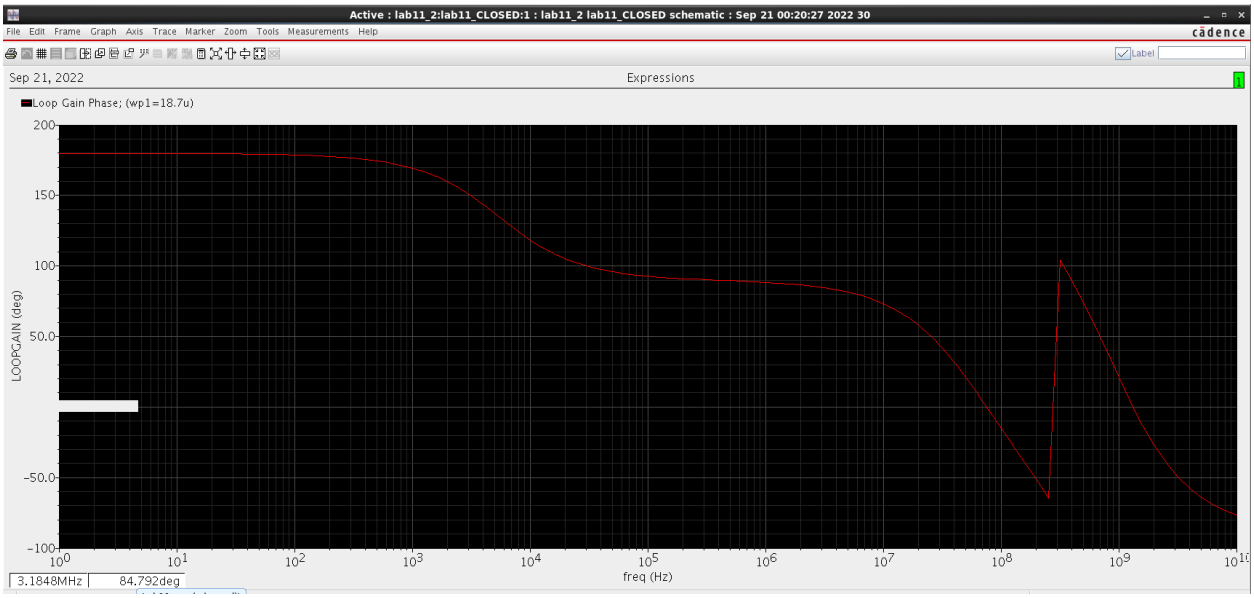

Figure 5.8

-I compared GBW and PM of diff and CM loops as shown in figures 5.9 , 5.10.

phaseMargin(Deg)=89.303472
phaseMarginFreq(Hz)=10932544

Figure 5.9(Diff)

phaseMargin(Deg)=68.3889
phaseMarginFreq(Hz)=13220364

Figure 5.10(CM)

-I found that the low PM in case of Cm loop leads to very small frequency domain peaking and time domain ringing and overshoot exists in transient response but that is not found in case of diff loop as it has a high PM = 89≈ 90 and both of them are stable as they have a good PM and GBW of the CM loop is larger than Diff loop.

-I compared DC LG and GBW of the diff loop with those obtained from open-loop simulation.

	Diff loop	Open loop
DC LG	1007=60dB	3.206k=70dB
GBW	10.9M	55.95M

-I found that as $\beta = \frac{Cf}{Cf+Cin} = \frac{1}{3}$ so, the LG = $\beta Aol = 1068 = 60.5dB$ as calculated from simulation and GBW of the open loop is larger than GBW of diff loop.

PART 6: Closed Loop Simulation (Transient Analysis)

1)Differential and CMFB loops stability (transient analysis):

-I applied a differential input pulse (initial value = 0, pulse value = 100mV, delay = 1us, period = 2us,pulse width = 1us, rise = fall = 10ns).

-I run transient analysis for 3us with 10ns max step.

-I plotted the transient signals at VINP, VINN, VOUTP, VOUTN, and VOCM as shown in figures 6.1, 6.2.

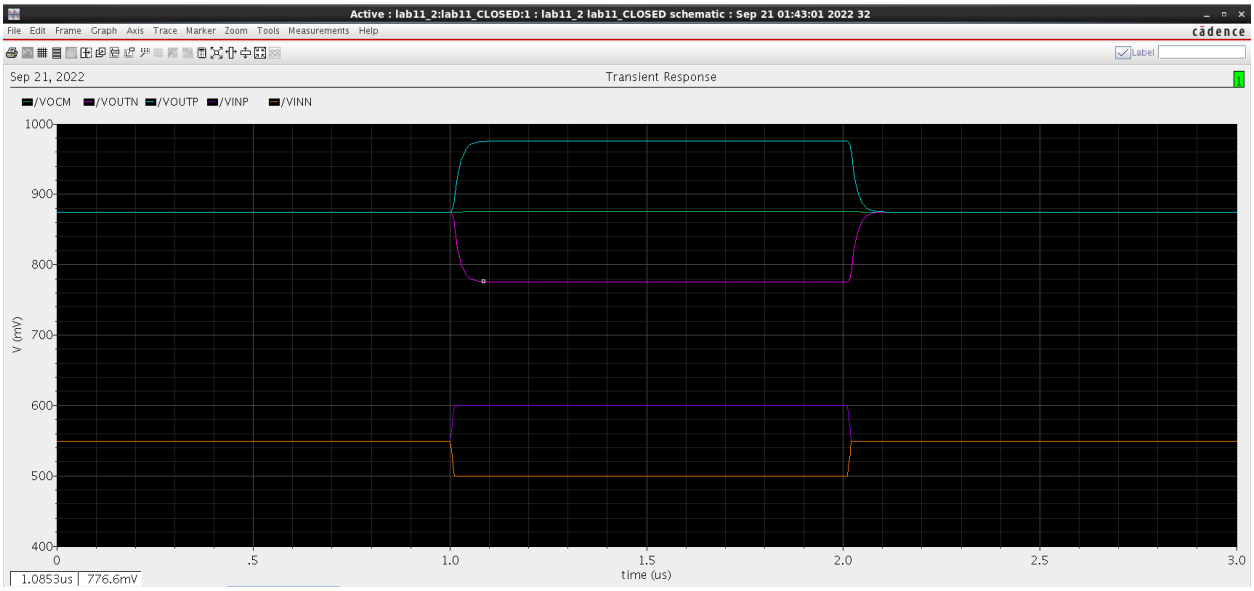

Figure 6.1

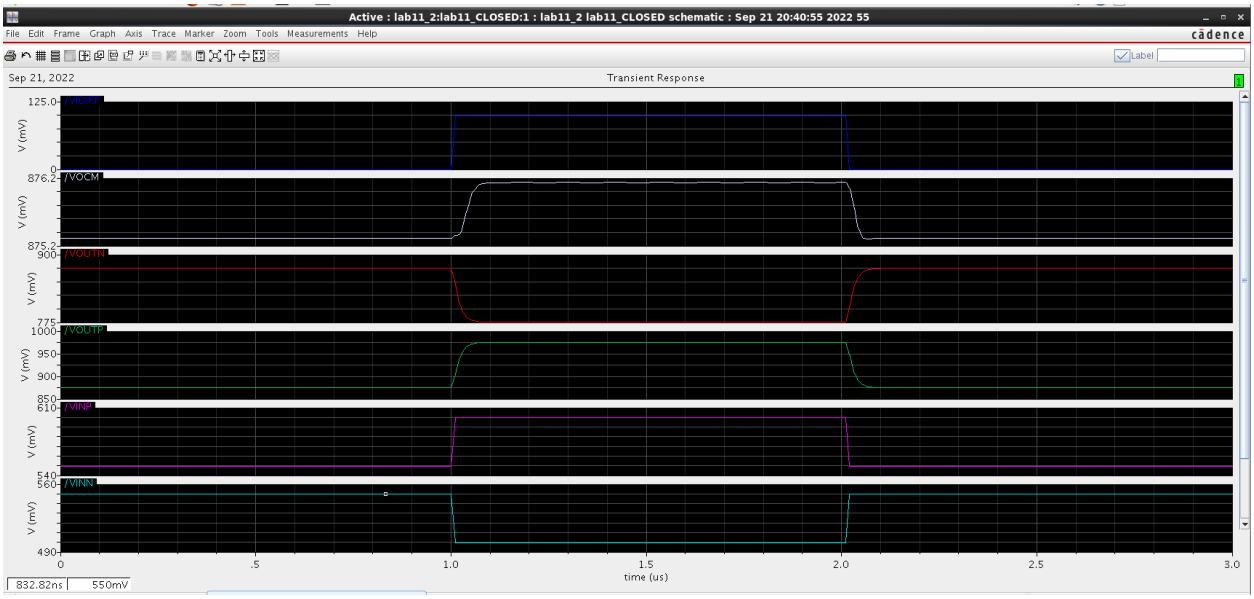

Figure 6.2

-I found that there is no differential ringing but there is a very small CM ringing and both loops are stable with adequate PM.

-I set differential input to zero and applied the same previous pulse at the balun CM input.

-I run transient analysis for 3us to test the fully differential capacitive amplifier stability.

-I plotted the transient signals at VINP, VINN, VOUTP, VOUTN, and VOCM as shown in figures 6.3, 6.4.

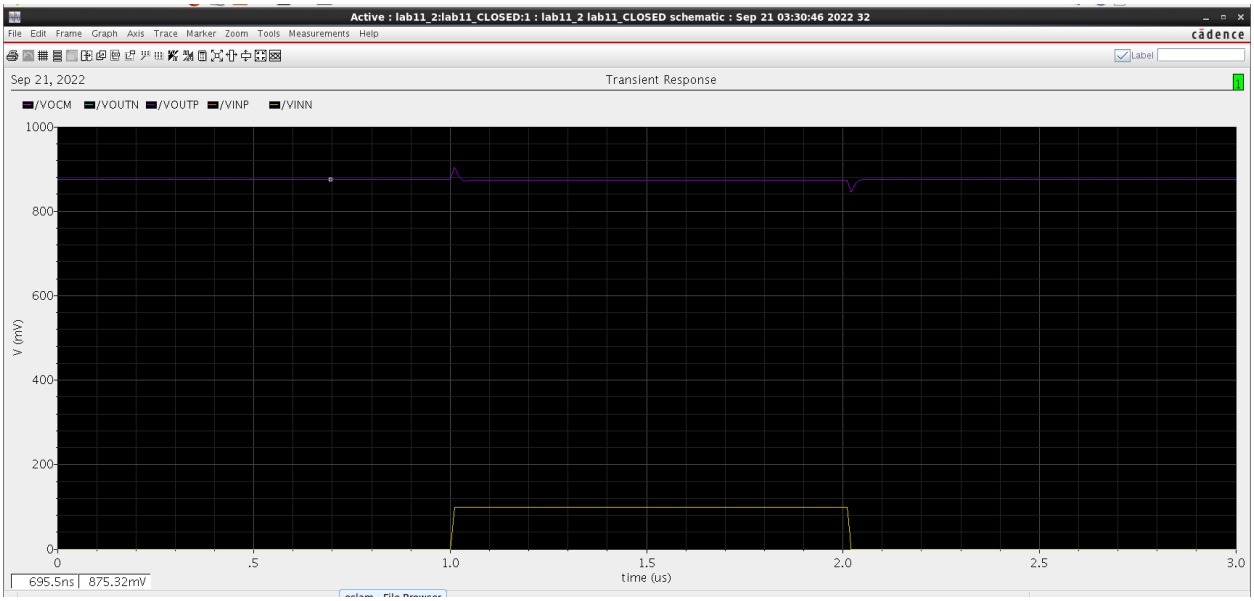

Figure 6.3

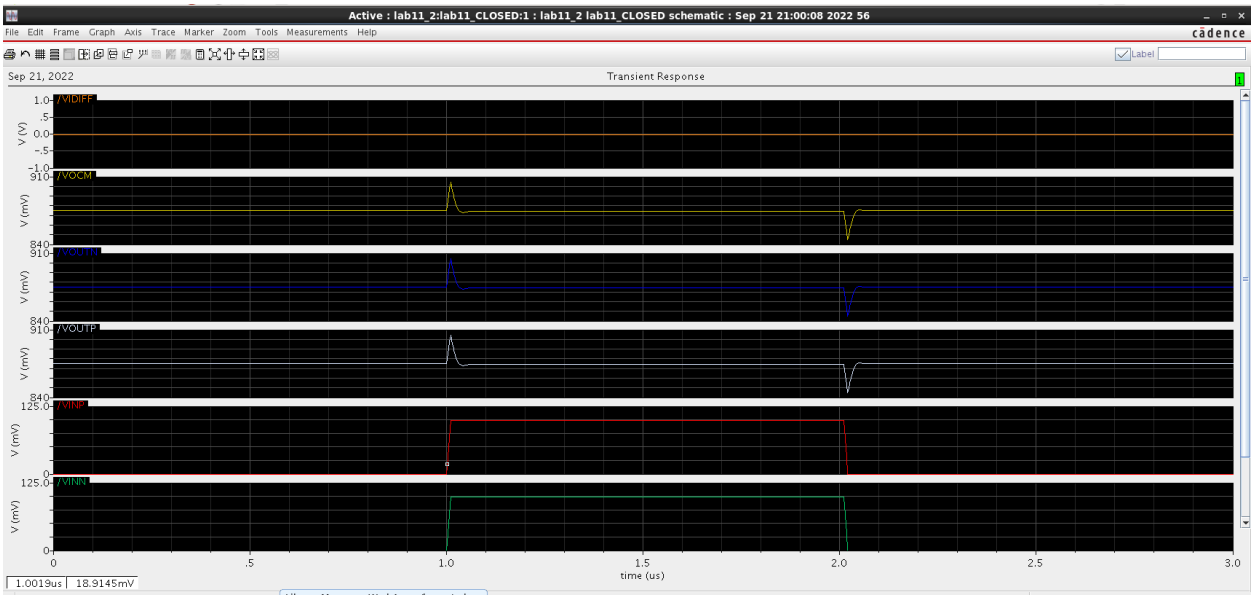

Figure 6.4

-I -I found that there is no differential ringing but there is CM ringing and both loops are stable with adequate PM.

2)Output swing:

-I applied a differential sinusoidal input with freq = 100kHz and amplitude = 150mV.

-I run transient analysis for three periods (30us) with 0.1us max time step.

-I plotted the transient signals at VINP, VINN, VOUTP, VOUTN, and VOCM as shown in figure 6.4.

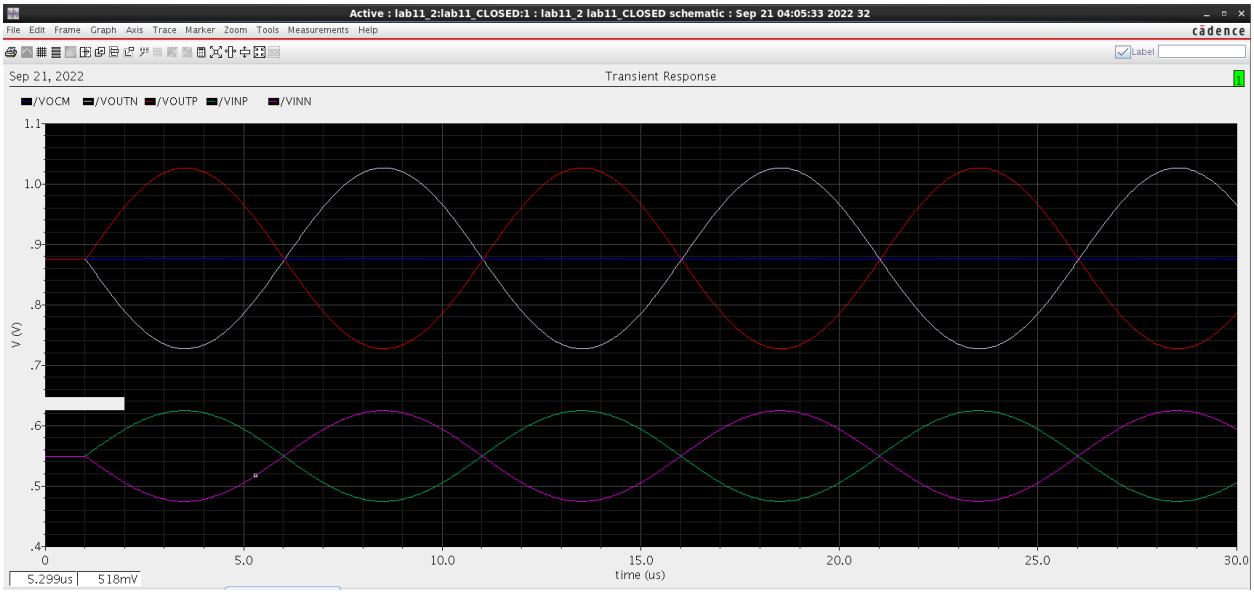

Figure 6.4

-I plotted the transient signals at VIDIFF and VODIFF as shown in figure 6.5.

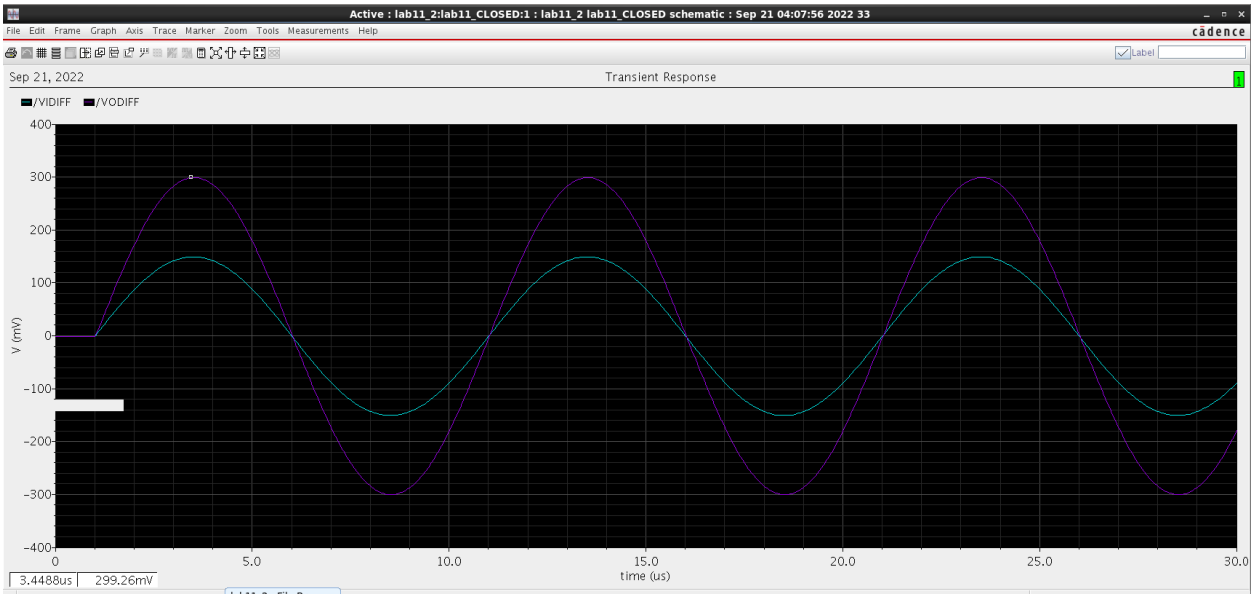

Figure 6.5

-I calculated the diff input and output peak-to-peak swings and the closed loop gain as shown in figure 6.6.

Test	Output	Nominal	Spec	Weight	Pass/Fail
lab11_2:lab11_CLOSED:1	Pkp_VODIFF	599.3m			
lab11_2:lab11_CLOSED:1	Pkp_VIDIFF	300m			
lab11_2:lab11_CLOSED:1	CL_gain	1.998			

Figure 6.6