# CS 254 - Assignment 8

## ***Rules:***

**1)** ***Any style of code is permitted.***

***2) Use the ieee.std_logic_1164 library data types. (Bit and bit vector are not permitted.)***

1) Design a traffic light controller. Assume that the traffic light for which the controller is being designed is placed at an intersection of 4 lanes and each lane has its own set of green, yellow and red lights which are controlled by the output ports green(3 downto 0), yellow(3 downto 0) and red(3 downto 0) of the controller. For any of these output lines sending a '1' on the line turns on the corresponding light and sending a '0' turns it off. As soon as the circuit is powered on all the lanes should be red except lane 1 which should be green for 30 seconds after which it should turn yellow and remain yellow for 5 seconds. After that simultaneously lane 1 turns red and lane 2 becomes green. Just like before lane 2 remains green for 30 seconds and yellow for 5 seconds before turning red at which point lane 3 becomes green. After all the lanes are completed in the same way the pattern should repeat again from lane 1.

```
entity TrafficLightController is
        port ( clk, rst : in std_logic;
        green, yellow, red: out std_logic_vector(3 downto 0));
end entity;
```

## ***Things required in Submission:***

1. All VHDL files of top-level and sub-components. (.vhd or .vhdl files)
2. Screenshot of Waveform.
3. All paperwork: State diagrams (mandatory), state minimizations, K-maps, block diagrams etc.
4. Testbench (mandatory)

### Submission rules:

1. The VHDL files of each question should be kept in a **separate folder**.
2. All the VHDL files of one question (both Top-level & sub-components) should be kept in the **same folder**.
3. The final zip file that is submitted on moodle should be named in the following format: **group_<groupnumber>.zip**. For example, the zip file for group 8 should be named group_8.zip