CS 254 - Assignment 3

Rules: *1) For all questions, only structural VHDL code is permitted.*

2)All the entities in this assignment can only be designed using 2x1 muxes.

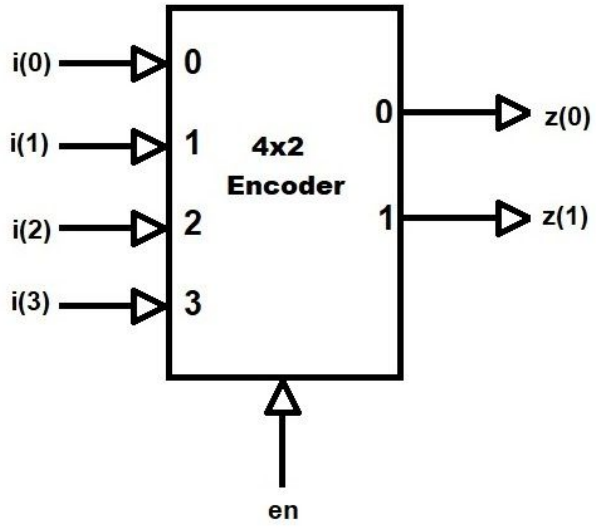
3)The 2x1 mux itself must be designed in a structural way using only 2 input gates.

3 input gates, 4 input gates, etc are not permitted.

4)Use the ieee.std_logic_1164 library data types. (Bit and bit vector are not permitted.)

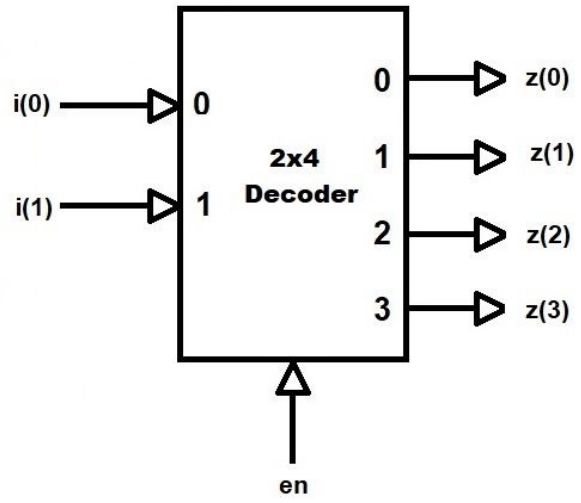
1) Design a 4x2 Encoder using only 2x1 multiplexers.

```
entity FourByTwoEncode is
        port ( i    : in std_logic_vector (3 downto 0);
        en: in std_logic;
        z : out std_logic_vector (1 downto 0));
end entity;
```



2) Design a 2x4 Decoder using only 2x1 multiplexers.

```
entity TwoByFourDecode is
        port ( i : in std_logic_vector (1 downto 0);
        en: in std_logic;
        z : out std_logic_vector (3 downto 0));
end entity;
```



3) Design a 1-bit half adder using only 2x1 multiplexers. ‘a’ and ‘b’ are the inputs and ‘sum’ and ‘carry’ are the outputs.

```
entity OnebitHalfAdd is
        port ( a, b : in std_logic;
        sum, carry: out std_logic);
end entity;
```

4) Design a 1-bit full adder using only 2x1 multiplexers and the 1-bit half adder designed in the above question. ‘a’ and ‘b’ are the inputs. ‘cin’ is the input carry. ‘sum’ and ‘carry’ are the outputs.

```
entity OnebitFullAdd is
        port ( a, b, cin : in std_logic;
        sum, carry: out std_logic);
end entity;
```

Things required in Submission:

1. All VHDL files of top-level and sub-components. (.vhd or .vhdl files)
2. Screenshot of Waveform.

Note: Test bench is not required in submission but create a test bench and use it to test your design before submission. The waveforms generated during your test should be uploaded. No other project files are required. The vhdl files of each question should be kept in a separate folder.