LAB 1 - AND, OR, NOT GATES

DLD-TEAM

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VHDL files

- andGate : Entity and Architecture for AND gate
- orGate : Entity and Architecture for OR gate
- notGate : Entity and Architecture for NOT gate
- main : Entity and Architecture for main file

Testbench files

- Testbench : For combined architecture (main)
- testbench_and : For AND gate
- testbench_or : For OR gate
- testbench_not : For NOT gate

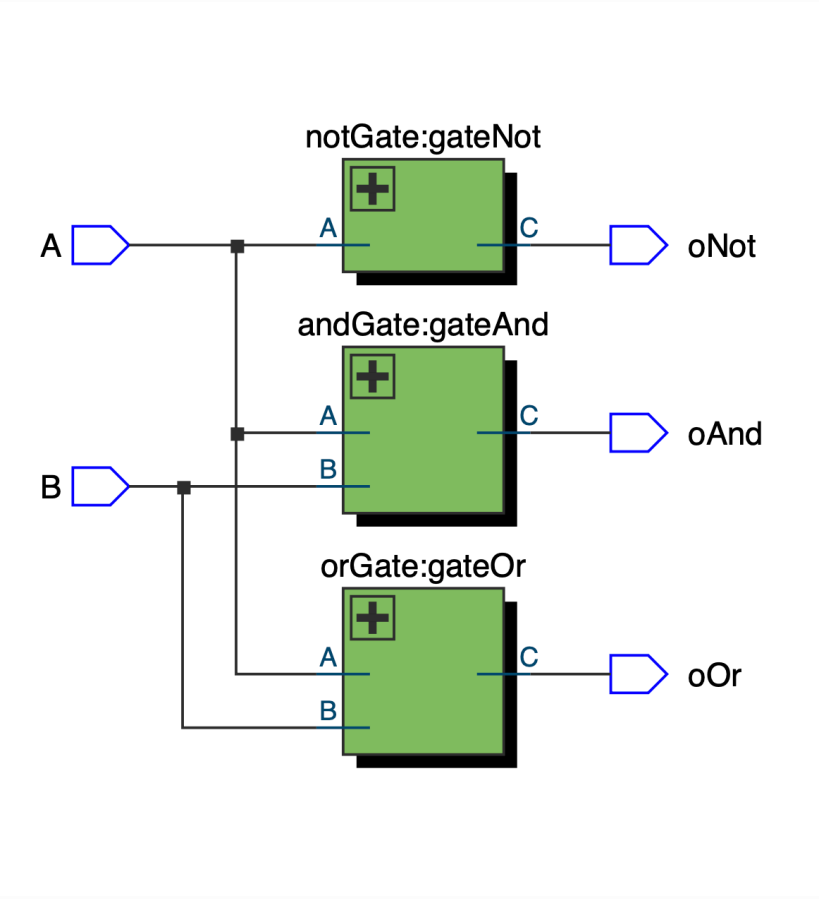
Usage and summary

We have tried to implement modular code. We first created separate entities and tested them with corresponding testbenches. After obtaining the results, with an modular idea we finally combined all chips and defined a main architecture to use all the gates in a single chip, and tested it with a corresponding testbench.

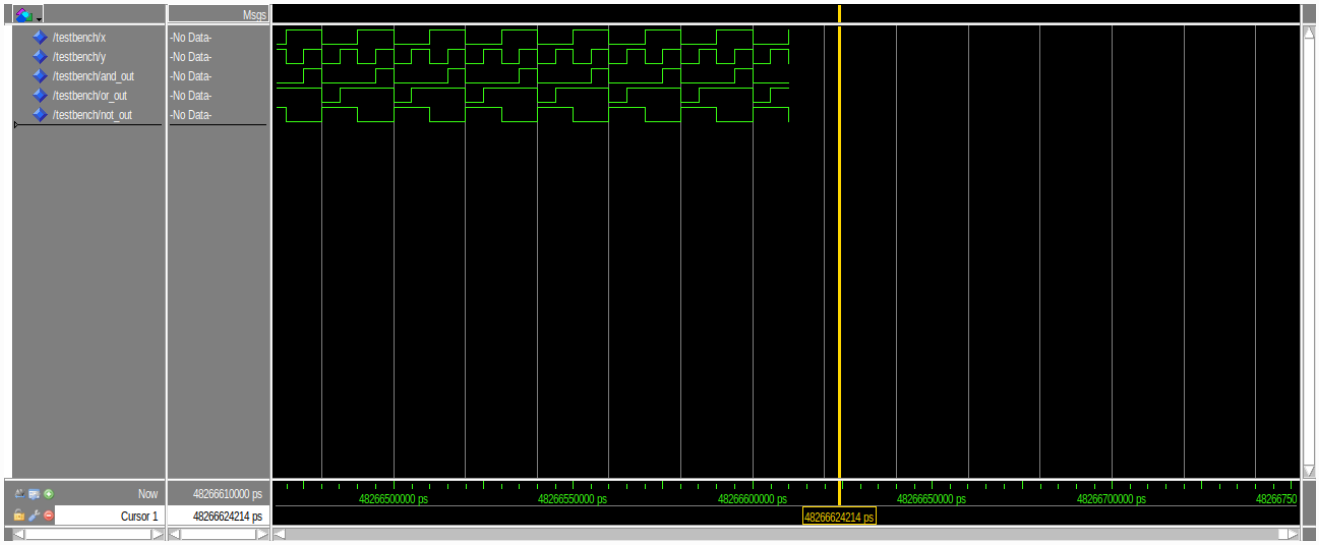
Simulation Results

Images for simulation inside the simulation folder

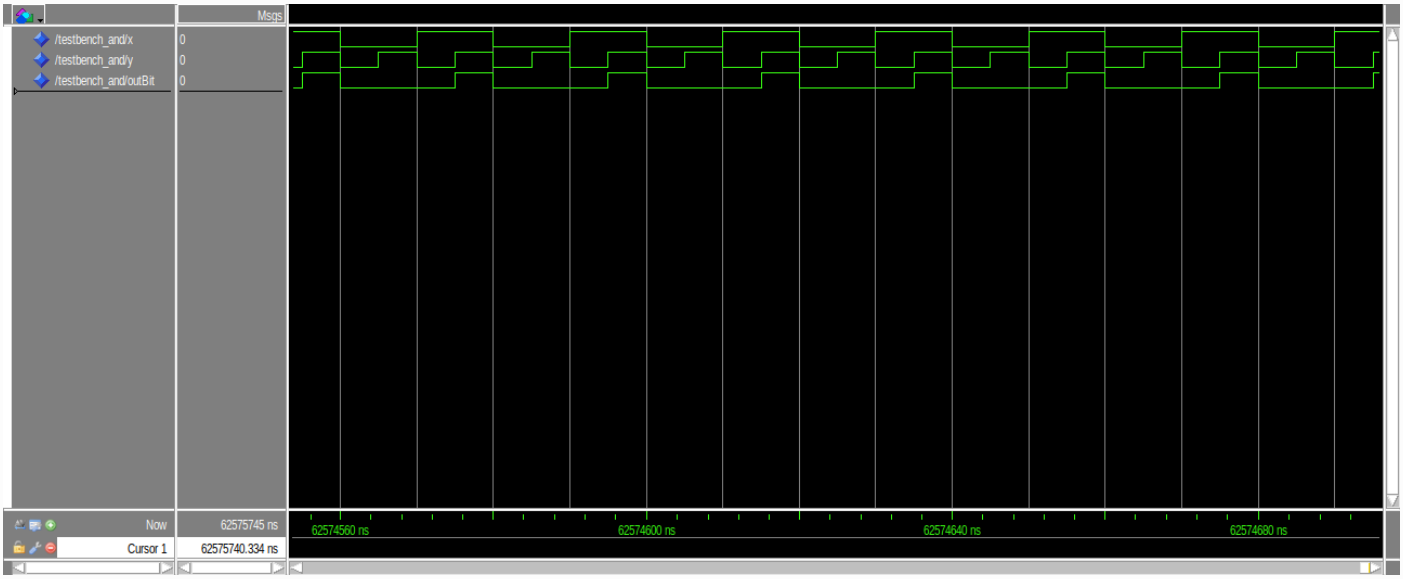
- A pdf file (main-diagram) for main architecture



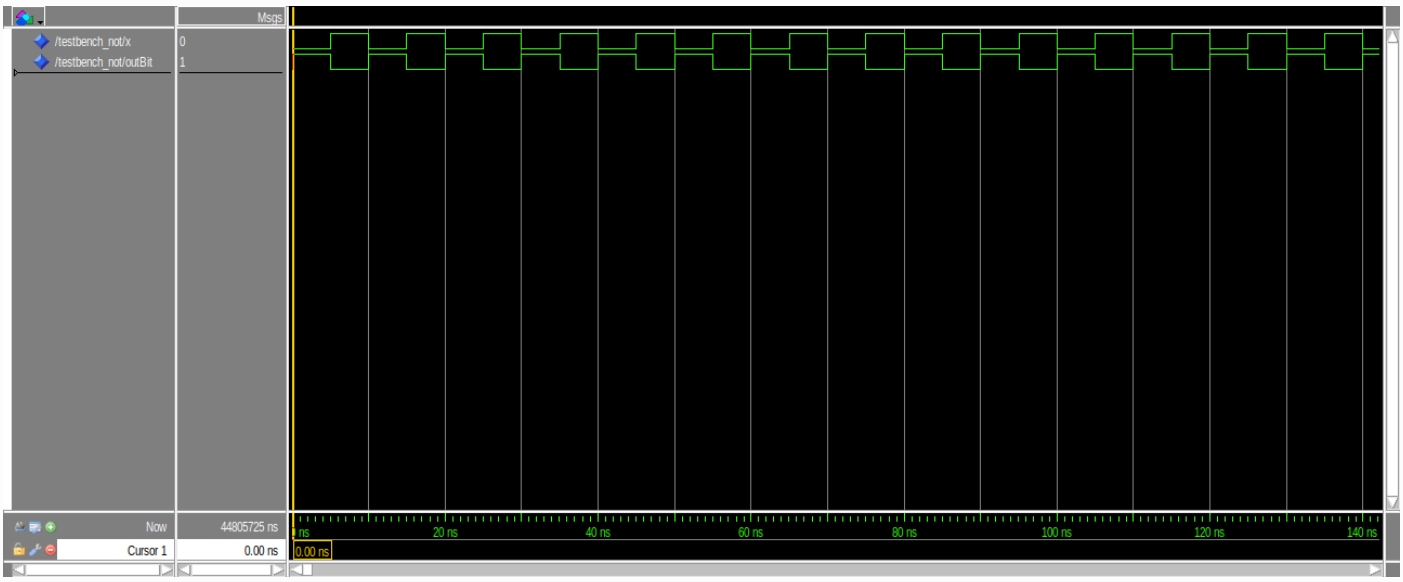
- all.bmp: Simulation for all three gates together (main)



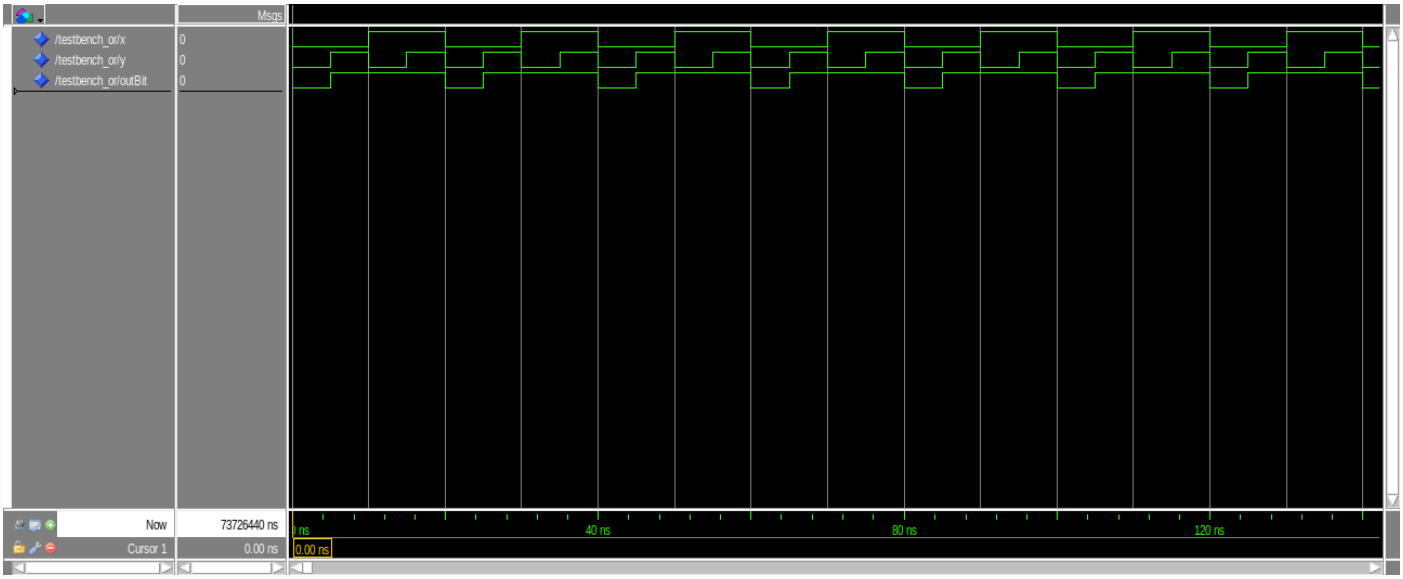
- and.bmp: Simulation for AND gate



- not.bmp: Simulation for NOT gate



- or.bmp: Simulation for OR gate


Msgs
/testbench_or/x
/testbench_or/y
/testbench_or/outBit
0
0
0
Now
73726440 ns
Cursor 1
0.00 ns
0 ns
40 ns
80 ns
120 ns
0.00 ns