Block Diagram

Block Diagram showing Testbench containing Reader and Writer, connected to Input File and Output File. Input Signal (a) and Clock (clk) feed into RL Encoder; Output Signal (z) and dvl (Data Valid Line). RL Encoder connects to Processing (Algo) via Input characters, and to Output Buffer via Extract from Buffer / Push to Buffer and Output, Counters.
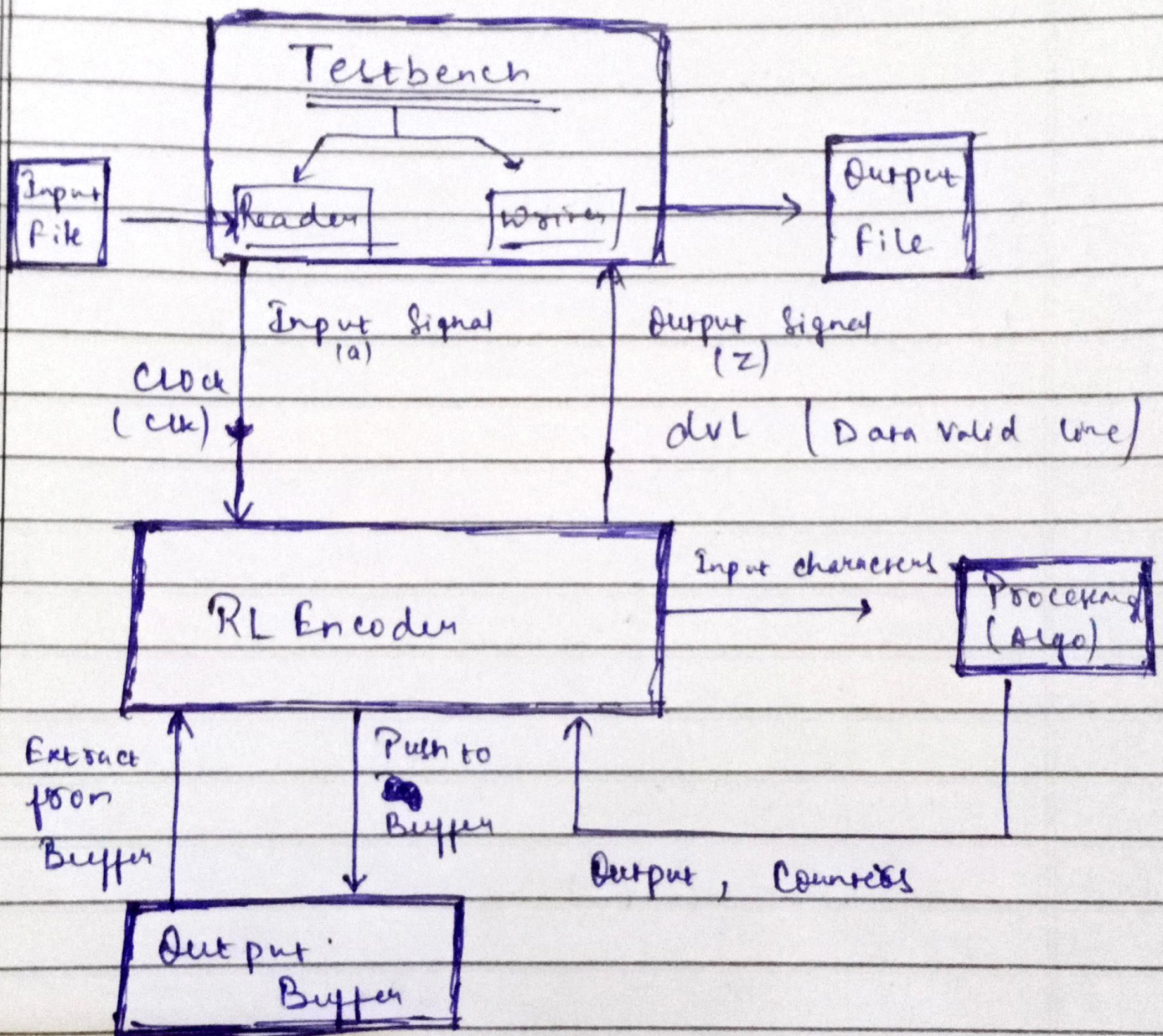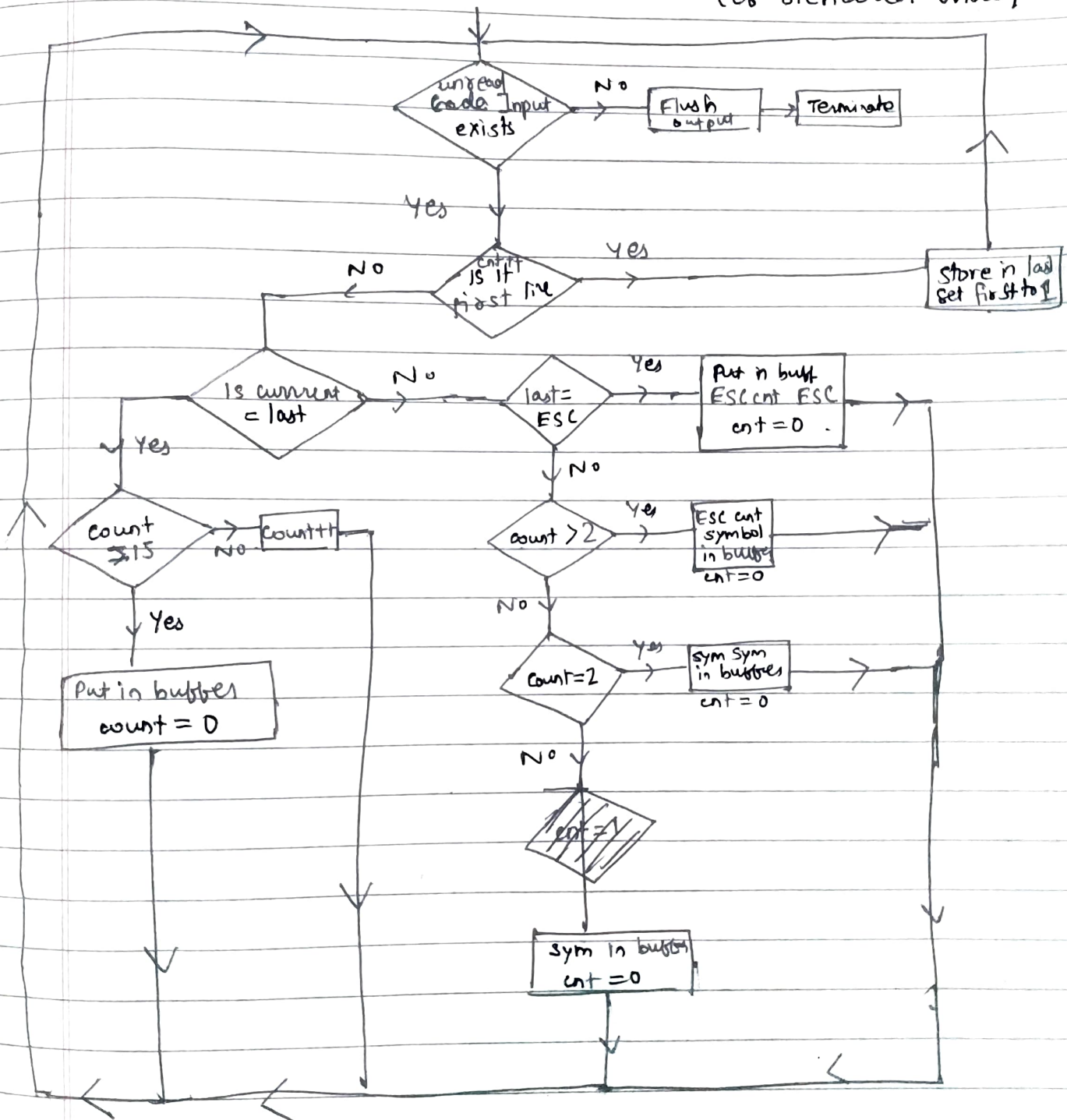
b) We have used sequential code since any type of code was allowed.
Detailed explanations of the code as is mentioned in comments.
Here is the flowchart explaing the behavious of code
(of rlencoder·vhdl)

Flowchart elements:

- unread Code Input exists → No → Flush output → Terminate
- Yes ↓
- Is it first line → Yes → Store in last, set first to 1
- No ↓
- Is current = last → No → last = ESC → Yes → Put in buff ESC cnt ESC cnt = 0
  - No ↓
  - count > 2 → Yes → ESC cnt symbol in buffer cnt = 0
    - No ↓
    - Count = 2 → Yes → sym sym in buffer cnt = 0
      - No ↓
      - cnt ≠ 1
      - sym in buffer cnt = 0
- Yes (current = last) ↓
  - count ≥ 15 → No → count++
  - Yes ↓
  - Put in buffer count = 0

NOTE - We have used `11111111` as a symbol which is sent when no input/output left while flushing.