

# **LAB MANUAL**

## **DIGITAL COMMUNICATION LAB**

### **[KEC-651]**

**DEPARTMENT OF ELECTRONICS & COMMUNICATION  
ENGINEERING**

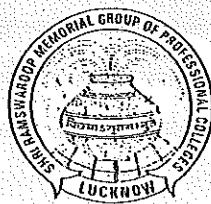


**SHRI RAMSWAROOP MEMORIAL GROUP OF  
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**AFFILIATED TO**

**DR. A. P. J. ABDUL KALAM TECHNICAL  
UNIVERSITY**

**LUCKNOW, UP**



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## OUR VISION

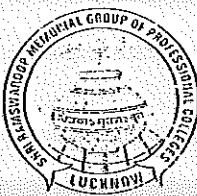
To achieve international standards in value based professional education for the benefit of society and the nation.

## OUR MISSION

- To dedicate teaching, learning, and collaborating in pursuit of frontier technologies with a spirit of innovation and excellence.
- To foster human values and ethos, compassion for ecosystem and obligation towards society and the nation.
- To provide an environment conducive to continuous learning, and all-round development of college fraternity.



Prof. (Dr.) S. R. Srivastava  
Director, SRMIMCA  
Satyamev Jayate  
Tatyagita Ganga  
Ganga Prayag



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## DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

### VISION

To create globally competitive electronics and communication professionals with strong values for the advancement of the nation.

### MISSION

M1: To provide an ambiance of excellence in teaching and learning replete with innovation, collaboration and research.

M2: To instill human values, social obligations and national responsibilities.

M3: To promote a learning ecosystem for progress and development of all in the department.

Dr. (Mrs) R.M. Jaiswal  
Professor  
Smt. Shanti Chaturvedi  
Department of Electronics & Communication Engineering



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## Program Outcomes (POs)

POs describe what the students are expected to know and would be able to do upon the graduation as a professional engineer. These are various graduate attributes that relate to the skills, knowledge, competence, and behaviour that students acquire at the end of engineering programme. The POs adopted by NBA for UG Engineering Programme are given below:

- PO-01 Engineering Knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
- PO-02 Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
- PO-03 Design/Development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
- PO-04 Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions for complex problems.
- PO-05 Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
- PO-06 The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
- PO-07 Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
- PO-08 Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
- PO-09 Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
- PO-10 Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
- PO-11 Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
- PO-12 Lifelong learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Prof. (col.) H.K. Jaiswal

Director General

Shri Ramswaroop Memorial Group of  
Professional Colleges, Lucknow



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## DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

### PROGRAMME SPECIFIC OUTCOMES (PSOs)

- PSO1: Able to apply fundamental concepts of electronics to design and develop electronic systems.
- PSO2: Proficient in usage of popular and specialized software for the development of quality electronic systems.

### PROGRAMME EDUCATIONAL OBJECTIVES (PEOs)

- PEO1: To be able to identify and apply domain specific knowledge to provide solutions to real world problems.
- PEO2: To become an ethical professional who is aware of synergy between development and environment for the betterment of society.
- PEO3: To be willing to learn and adapt the ever evolving technology through higher education.
- PEO4: To be a team player who has respect and consideration for all team members.

Prof. (Dr.) A. M. J. Singh  
Creator General

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## **SHRI RAMSWAROOP MEMORIAL GROUP OF PROFESSIONAL COLLEGES**

### **B. TECH. (EC) VI SEM. (2020-21)** **Digital Communication Lab (KEC-651)**

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#### **Course Outcomes (CO)**

**At the end of this course, the student will be able to:**

- CO1** : To formulate basic concepts of pulse shaping in digital communication.
- CO2** : To identify different line coding techniques and demonstrate the concepts.
- CO3** : To design equipment related to digital modulation and demodulation schemes.
- CO4** : To analyze the performance of various digital communication systems and evaluate the key parameters.
- CO5** : To conceptualize error detection & correction using different coding schemes in digital communication.

## **EXPERIMENT NO:-1**

**OBJECT:** -To study generation of Unipolar RZ & NRZ Line Coding.

**APPARATUS REQUIRED:**

S.No.	Instrument Required	Specification	Quantity
01	Training kit	ST-2106 Scientech	1
02	CRO	20 MHz Scientech	1
03	Connecting Probes		

**THEORY:** -

**UNIPOLAR LINE CODING:** -

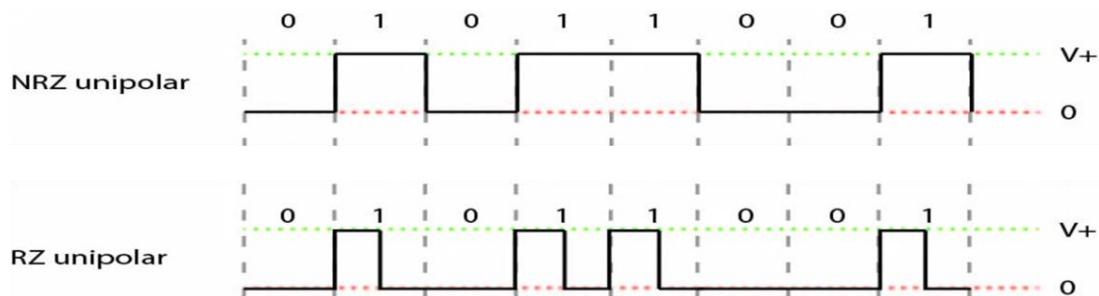
Line coding is the process of converting digital data to digital signals. In Unipolar line coding all the signal levels are either above or below the axis. It has only one voltage level other than zero. The symbols 0&1 in digital system can represented in various formats with different levels and wave forms. The selection of particular format for common pulse depends on the systems band width, system's ability to pass DC level information, error checking facility, case of clock regeneration & synchronization at receiver, complexity & cost etc.

**NON RETURN TO ZERO (LEVEL) NRZ:** -

It is the simplest form of data representation. The NRZ waveform simply goes low for one bit time to represent a data 0& high for one bit time to represent a data 1. It is unipolar line coding scheme in which positive voltage defines bit 1 and the zero voltage defines bit 0. Signal does not return to zero at the middle of the bit thus it is called NRZ.

**RETURN TO ZERO (LEVEL) RZ:** -

Return-to-zero (RZ or RTZ) describes a line code used in telecommunications signals in which the signal drops (returns) to zero between each pulse. That "zero" condition is typically halfway between the significant condition representing a 1 bit and the other significant condition representing a 0 bit. RZ uses pulses at the start of the clock cycle to indicate a 1 value.



**Fig.(1.1)**

**PROCEDURE:-**

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1. Connect the ground, clock, data nodes of 8 bit variable data generator (ST2111) to clock, data input & ground nodes of data formatting circuit.
2. Connect the CRO on the output node of unipolar NRZ available at data formatting circuit & trace out the waveform.
3. Connect the CRO on the output node of unipolar RZ available at data formatting circuit & trace out the waveform.

### **RESULT:-**

Waveform of the unipolar NRZ& RZ format has been observed on CRO & traced out.

### **PRECAUTIONS:-**

1. Don't make loose connection.
2. Check the connection before switch ON the power supply.
3. Check the all-switch fault carefully.

### **RELATED QUESTIONS: -**

**Q.1** What is meant by Line coding?

**Q.2** What is unipolar line coding?

**Q.3** What do you mean by RZ and NRZ linecoding?

**Q.4** Convert 1010 (binary data) in to digital waveform using unipolar RZ& NRZ line coding.

**Q.5** What are advantages and disadvantages of unipolar line coding?

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## **EXPERIMENT NO:-2**

**OBJECT**:-To study generation of Polar RZ & NRZ Line Coding.

**APPARATUS REQUIRED:**

S.No.	Instrument Required	Specification	Quantity
01	Training kit	ST-2106 Scientech	1
02	CRO	20 MHz Scientech	1
03	Connecting Probes		

**THEORY:** -

**POLAR LINE CODING:** -

Line coding is the process of converting digital data to digital signals. In Polar line coding the voltages are on the both sides of the axis. which means it will have both positive and negative values for voltages or amplitude, it is quite like NRZ scheme but, here we have NRZ-L (i.e., NRZ-Level) and NRZ-I (i.e., NRZInvert). It has two voltage level other than zero. The symbols 0&1 in digital system can represented in various formats with different levels and wave forms. The selection of particular format for common pulse depends on the systems band width, system's ability to pass DC level information, error checking facility, case of clock regeneration & synchronization at receiver, complexity & cost etc.

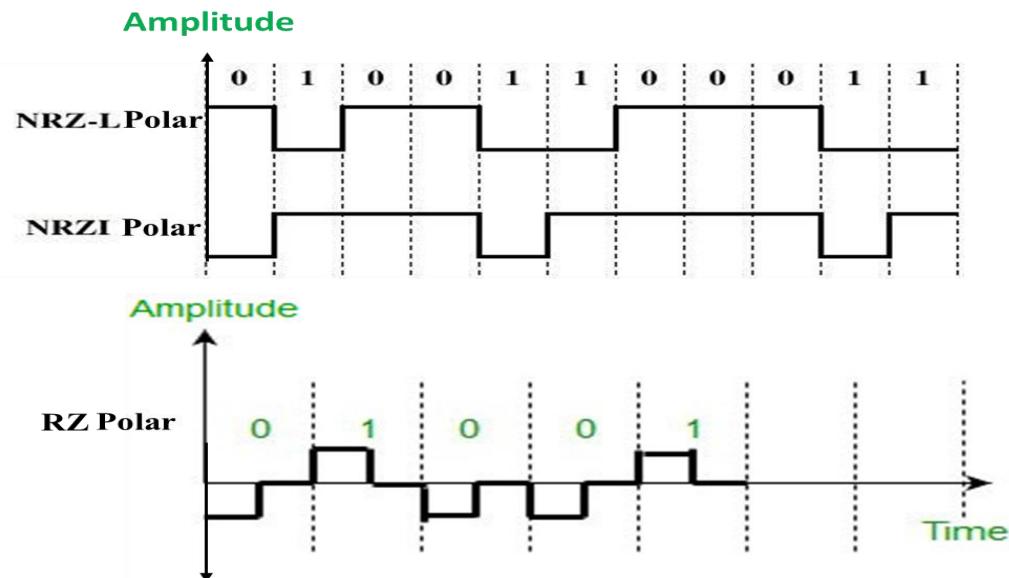
**NRZ-L AND NRZ-I –**

These are somewhat similar to unipolar NRZ scheme but here we use two levels of amplitude (voltages). For **NRZ-L(NRZ-Level)**, the level of the voltage determines the value of the bit, typically binary 1 maps to logic-level high, and binary 0 maps to logic-level low, and for **NRZ-I(NRZ-Invert)**, two-level signal has a transition at a boundary if the next bit that we are going to transmit is a logical 1, and does not have a transition if the next bit that we are going to transmit is a logical 0.

**RETURN TO ZERO RZ:** -

One solution to NRZ problem is the RZ scheme, which uses three values positive, negative, and zero. In this scheme signal goes to 0 in the middle of each bit. The logic we are using here to represent data is that for bit 1 half of the signal is represented by +V and half by zero voltage and for bit 0 half of the signal is represented by -V and half by zero voltage.

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**Fig.2.1****PROCEDURE: -**

1. Connect the ground, clock, data nodes of 8-bit variable data generator (ST2111) to clock, data input & ground nodes of data formatting circuit.
2. Connect the CRO on the output node of Unipolar NRZ-L, NRZ-I &RZ available at data formatting circuit & trace out the waveform.

**RESULT: -**

Waveform of the Unipolar NRZ-L, NRZ-I &RZ format have been observed on CRO & traced out.

**PRECAUTIONS: -**

1. Don't make loose connection.
2. Check the connection before switch ON the power supply.
3. Check the all-switch fault carefully.

**RELATED QUESTIONS:-**

- Q.1 What is meant by Line coding?
- Q.2 What is polar line coding?
- Q.3 What do you mean by RZ and NRZ linecoding?
- Q.4 Convert 1010 (binary data) in to digital waveform using polar RZ& NRZ line coding.
- Q.5 What are advantages and disadvantages of polar line coding?

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## EXPERIMENT NO:-3

**OBJECT:**-To study generation of Bipolar RZ & NRZ Line Coding.

**APPARATUS REQUIRED:**

S.No.	Instrument Required	Specification	Quantity
<b>01</b>	Training kit	ST-2106 Scientech	1
<b>02</b>	CRO	20 MHz Scientech	1
<b>03</b>	Connecting Probes		

**THEORY:** -

**BIPOLAR LINE CODING:** -

In this scheme there are three voltage levels positive, negative, and zero. The voltage level for one data element is at zero, while the voltage level for the other element alternates between positive and negative. Bipolar encoding, binary zero ('0') is represented by 0 voltage whereas binary one ('1') is represented by alternating positive and negative voltages. The Bipolar coding technique uses different types of pulses based on which it is known as NRZ (Non-Return to Zero) or RZ (Return to Zero).

**NOT RETURN TO ZERO (NRZ):** -

Uses three levels of signal level (+A, 0, -A) and has "Alternate Mark Inversion" (AMI). Bipolar NRZ coding uses zero voltage to represent binary zero and +ve pulse and -ve pulse to represent alternating binary ones during entire bit period. Hence pulse duration and symbol bit duration are equal in NRZ type.

**RETURN TO ZERO (RZ):** -

Uses three levels of signal level (+A, 0, -A) has "Alternate Mark Inversion" (AMI). There is a half-width +ve output pulse if the input is a '1'; or a half-width -ve output pulse if the input is a '0'. There is a return-to-zero for the second half of each bit period.

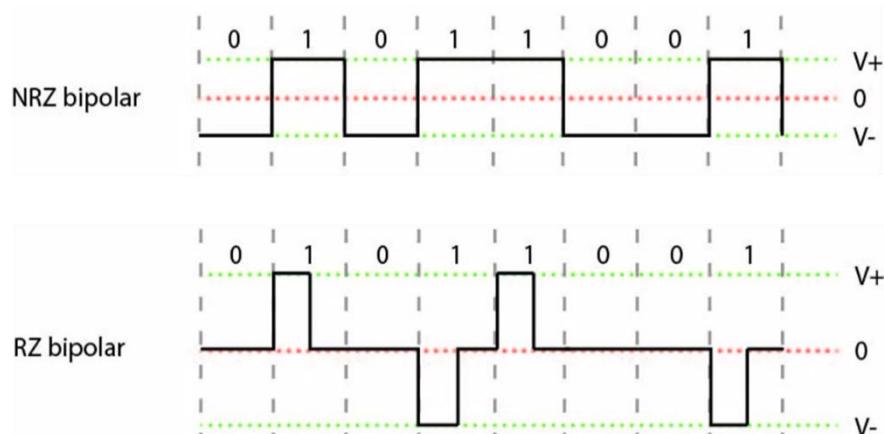


Fig.3.1

**PROCEDURE: -**

1. Connect the ground, clock, data nodes of 8-bit variable data generator (ST2111) to clock, data input & ground nodes of data formatting circuit.
2. Connect the CRO on the output node of Bipolar NRZ & RZ available at data formatting circuit & trace out the waveform.

**RESULT: -**

Waveform of the Bipolar NRZ & RZ format have been observed on CRO & traced out.

**PRECAUTIONS: -**

1. Don't make loose connection.
2. Check the connection before switch ON the power supply.
3. Check the all-switch fault carefully.

**RELATED QUESTIONS: -**

**Q.1** What is meant by Line coding?

**Q.2** What is bipolar line coding?

**Q.3** What do you mean by RZ and NRZ linecoding?

**Q.4** Convert 1010 (binary data) in to digital waveform using unipolar RZ& NRZ line coding.

**Q.5** What are advantages and disadvantages of polar line coding?

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## EXPERIMENT NO:-4

**OBJECT:** - Implementation and analysis of Binary Amplitude shift keying BASK modulation and demodulation

**APPARATUS REQUIRED:** -

S. No.	Apparatus name	Specification	Quantity
01	Transmitter kit	ST-2106 Scientech	1
02	Receiver kit	ST-2107 Scientech	1
03	8bit variable data generator	ST-2111 Scientech	1
04	CRO	20MHz Scientech	1

**THEORY:** -

To transmit the digital data from one place to another, we have to choose the transmission medium. It is not possible to send the digital data directly over the antenna because the antenna of practical size works on very high frequencies much higher than our data transmission rate. To be able to transmit the data over antenna, we have to MODULATE the carrier signal phase frequencies or amplitude etc. which is varied in accordance with the digital data. At the receiver we separate the signal from digital information by the process of “DEMODULATION”. Modulation also allows different data streams to be transmitted over same channel.

This process is called as MULTPLEXING & result in a considerable saving of available bandwidth. Some of the basic digital modulation techniques are ASK PSK & FSK.

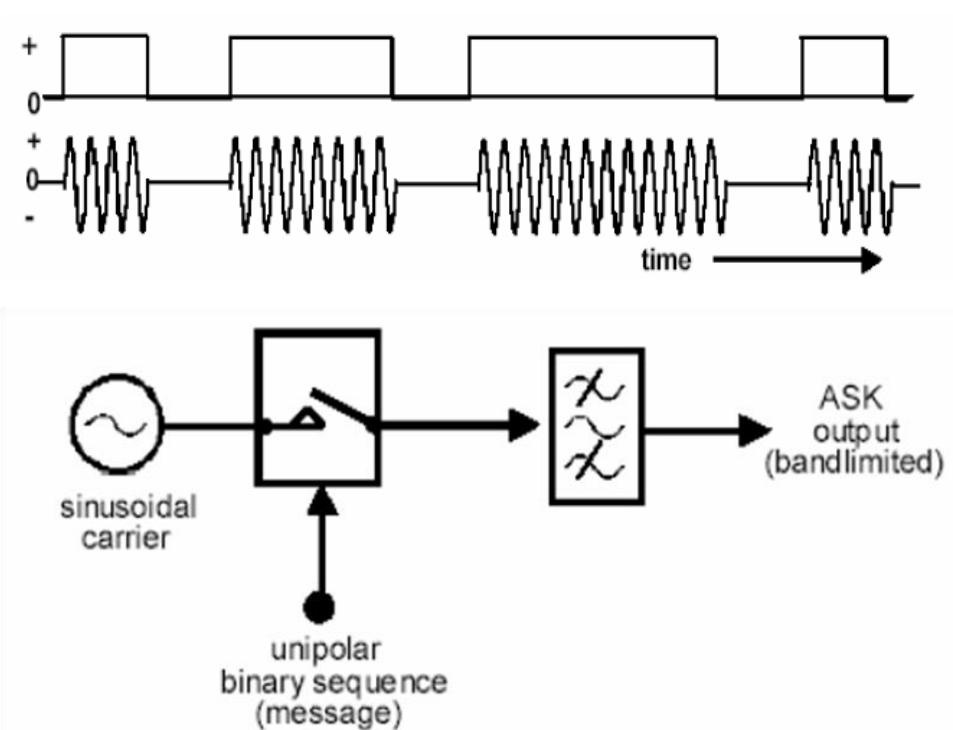
**BASK (BINARY AMPLITUDE SHIFT KEYING):** -The simplest method of modulating a carrier with a data stream is to change the amplitude of the carrier wave every time the data changes. This modulation technique is known as “AMPLITUDE SHIFT KEYING”. The simplest way of achieving amplitude shift keying is by switching on the carrier whenever the data bit is 1 & switching off whenever the data bit is ‘0’ This technique is known as ON-OFF KEYING. Thus

DATA = 1 CARRIER TRANSMITTED.

DATA = 0 CARRIER SUPPRESSED.

The BASK wave form is generated by balanced modulator circuit which is also known as a linear multiplier. In order to generate ASK wave form we apply the digital data stream and modulation input as a input to the linear multiplier. The method of demodulate the ASK wave form is to rectify it pass it through the filter & square up the resulting wave form, the output is the original data stream. Amplitude shift keying is less efficient because the noise inherent in the transmission channel can deteriorate the signal so much that the amplitude changes in the modulated carrier wave due to noise addition. This may lead to the incorrect decoding at the receiver. Hence **THIS TECHNIQUE IS NOT WIDELY USED IN PRACTICAL** application & it is however used in diverse areas and old emergency radio transmissions and fiber-optic communication.

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**Fig. 4.1****PROCEDURE:-**

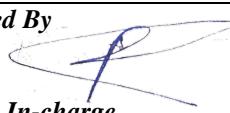
1. Connect the ground, clock, data nodes of 8 bit variable data generator (ST-2111) to clock, data input & ground nodes of data formatting circuit.
2. Connect the output node of NRZ (L) available at node 5 to modulation I/P node of carrier modulation circuit available at node 27.
3. Connect the node16 available at carrier generator circuit to node 26 available at carrier generator circuit to node 26 available at carrier modulation circuit.
4. Do proper adjustments via carrier offset, gain and modulation offset nodes.
5. Connect the output node of carrier modulation circuit available at node 28 to CRO & trace out the ASK waveform.
6. For Demodulation, connect the output of carrier modulation circuit available at node 28 to the ASK demodulator available at node 21.
7. Connect the output node 22 of ASK demodulator to the input of LPF available at node 27.
8. Connect the CRO at LPF output available at node 28 &trace out the demodulated ASK wave form.

**RESULT:-**

The study modulation &demodulation is completed.

**PRECAUTIONS: -**

1. Analyze the kit carefully.
2. Observe the wave form carefully.

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3. Do all the connection at right position.

**RELATED QUESTIONS: -**

- Q.1** What is modulation and demodulation?
- Q.2** What is digital modulation and state various techniques?
- Q.3** What do you mean by BPSK?
- Q.4** What is multiplexing?
- Q.5** Explain the need of modulation and demodulation.

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## **EXPERIMENT NO:-5**

**OBJECT:-** Implementation and analysis of Binary Frequency shift keying (BFSK) modulation and demodulation.

**APPARATUS REQUIRED:** -

S.No.	Apparatus name	Specification	Quantity
<b>01</b>	Transmitter kit	ST-2106 Scientech	1
<b>02</b>	Receiver kit	ST-2107 Scientech	1
<b>03</b>	8 bit variable data generator	ST-2111 Scientech	1
<b>04</b>	CRO	20MHz Scientech	1

**THEORY:** -

In frequency shift keying the carrier frequency is shifted in steps i.e. from one frequency to one particular value of data & another corresponding to another value of digital data. The higher frequency is used to represent a data '1' & lower frequency a data '0' thus,

DATA = 1: Higher frequency

DATA = 0: Low frequency

On a closer look at the BFSK wave, it can be represented as the sum of BASK wave forms.

**BFSK MODULATION:-**

Let us now apply the binary data stream to 1st BASK modulator using the high frequency carrier. Let us now invert the original data stream.

Original      0110001011

Inverted      1001110100

Now apply the inverted data stream to the 2<sup>nd</sup> BASK modulator using a lower frequency carrier. The result is the original data '0' filled with lower frequency carrier & 1 is filled with higher frequency carrier.

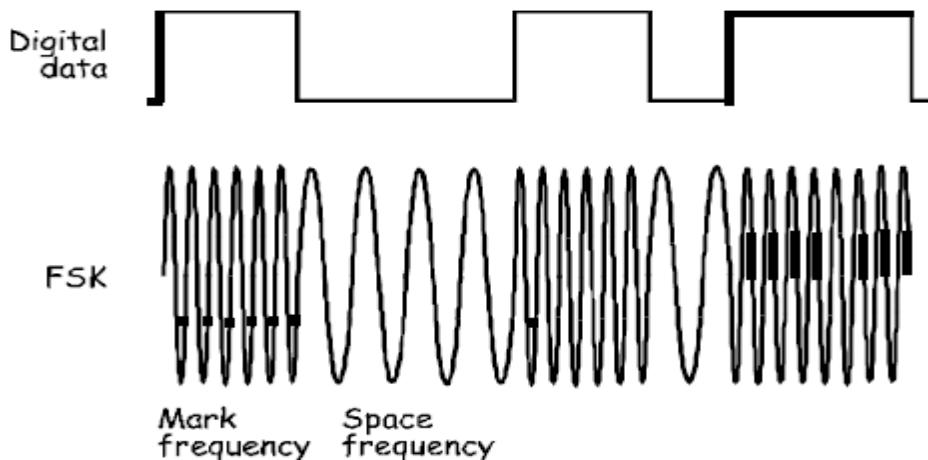
Finally, we will sum the two ASK waveform, to get the BFSK wave.

**FSK DEMODULATION:-**

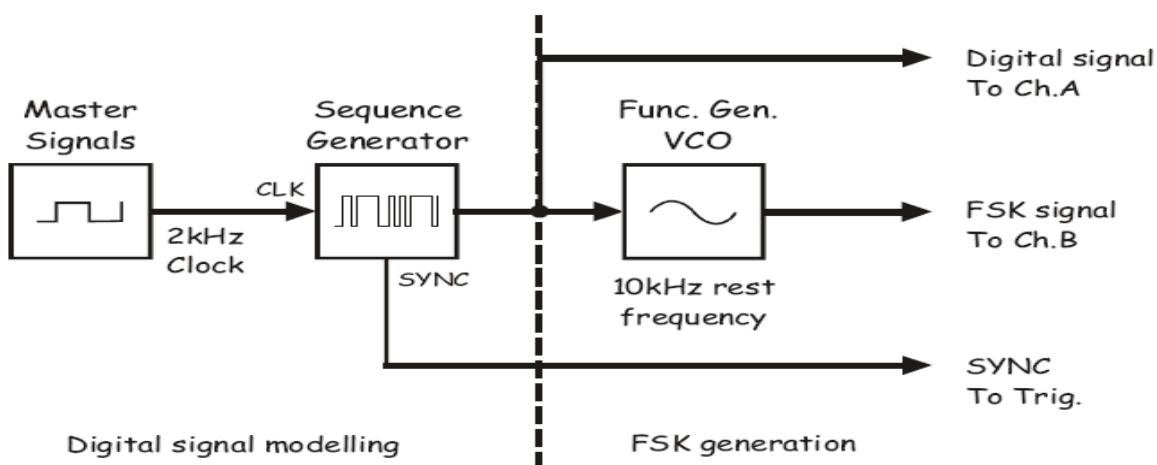
The demodulation of FSK is done by using a phase locked loop which tries to 'lock' to the input frequency. It is achieved by generating corresponding output voltage to be fed to the voltage-controlled oscillator. If any frequency deviation at its input is encountered, the PLL follows the frequency changes and generates proportional output voltage. The output of PLL contains carrier components. Therefore, the signal is passed through the LPF to remove them. The resulting wave is to be rounded off to be used for digital data processing. Also, the amplitude level may be very low due to channel attenuation. Since the amplitude change in FSK wave form does not matter. Thus it is a modulation technique which is very reliable even in noisy and fading channels. But

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there is always a price to be paid to gain that advantage. The price in this case is widening of the required bandwidth. The bandwidth increase depends upon the two-carrier frequency used and the digital data rate. **The bandwidth required is at least double than in the case of BASK modulation.** This means that lesser number of communication channels for a given band of frequencies.



**Fig 5.1BFSK modulation**



**Fig 5.2BFSK generator**

### **PROCEDURE:-**

1. Connect the ground, clock, data nodes of 8 bit variable data generator (ST-2111) to clock, data input & ground nodes of data formatting circuit.
2. Connect the output node of NRZ (L) available at node 5 to modulation I/P node of carrier modulation circuit available at node 27.
3. Connect the node 16 available at carrier generator circuit to node 26 available at carrier modulation circuit.
4. Do proper adjustments via carrier offset, gain and modulation offset nodes.
5. Connect the 960 KHz carrier frequency available at node 17 to node 29.

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6. Connect the node 27 to input data inverter available at node 32.
7. Connect the output node of data inverter available at node 33 to the modulation input available at node 30.
8. Connect the output node 28 & 31 to the input A & B of summing amplifier available at node 34 & 35 respectively.
9. Connect the output summing amplifier available at node 36 to CRO & trace out the BFSK waveform.
10. For Demodulation, connect the output of summing amplifier available at node 36 to the input of FSK demodulator available at node 16.
11. Connect the output of BFSK demodulator available at node 17 to the input of LPF available at node 23.
12. Connect the CRO to the output of LPF available at node 24 & trace out the BFSK demodulated wave form.

### **RESULT:-**

The study of BFSK modulation and demodulation is completed.

### **PRECAUTION:-**

1. Connect the circuit carefully.
2. Observe the wave forms carefully.

### **RELATED QUESTIONS:-**

- Q.1** What is modulation and demodulation?
- Q.2** What is digital modulation and state various techniques?
- Q.3** What do you mean by BFSK?
- Q.4** What is multiplexing?
- Q.5** Explain the need of modulation and demodulation.

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## **EXPERIMENT NO:-6**

**OBJECT:**Implementation and analysis of BPSK modulation and demodulation.

**APPARATUS REQUIRED:**

S.No.	Apparatus name	Specification	Quantity
<b>01</b>	Transmitter kit	ST-2106 Scientech	1
<b>02</b>	Receiver kit	ST-2107 Scientech	1
<b>03</b>	Variable data generator	ST-2111 Scientech	1
<b>04</b>	CRO	20MHz Scientech	1

**THEORY:**

Binary Phase Shift Keying (BPSK) is digital transmission scheme where the binary data is transmitted using out of phase signals. During logic ‘0’ a preset number of cycles of a sinusoidal carrier signal is transmitted and during logic ‘1’ the same number of cycles of the carrier signal is transmitted but with  $180^{\circ}$  phase shift.

**MODULATOR:**

A simple BPSK modulator circuit using an NPN-PNP transistor pair, and an Op-amp is shown in figure. The transistors work as switches and the Op amp works as inverting/noninverting amplifier. The carrier signal is fed to the collectors and the message signal is fed to the bases of the two transistors simultaneously. The emitters of the transistors are grounded. When the message signal is at logic ‘1’ (+5V), the NPN transistor is ON and works as a closed switch. The PNP transistor is OFF and works as an open switch. The Op-amp now works as a non-inverting amplifier with the carrier signal fed to its non-inverting input. The carrier signal reaches the output without any phase shift. When the message signal is at logic ‘0’ (-5V), the NPN transistor is OFF and the PNP transistor ON. The Op amp works as an inverting amplifier with the carrier signal fed to its inverting pin. The carrier signal now reaches the output with  $180^{\circ}$  phase shift. Thus, the carrier signal switches its phase as the message signal switches between ‘0’ and ‘1’. The resulting output is BPSK modulated.

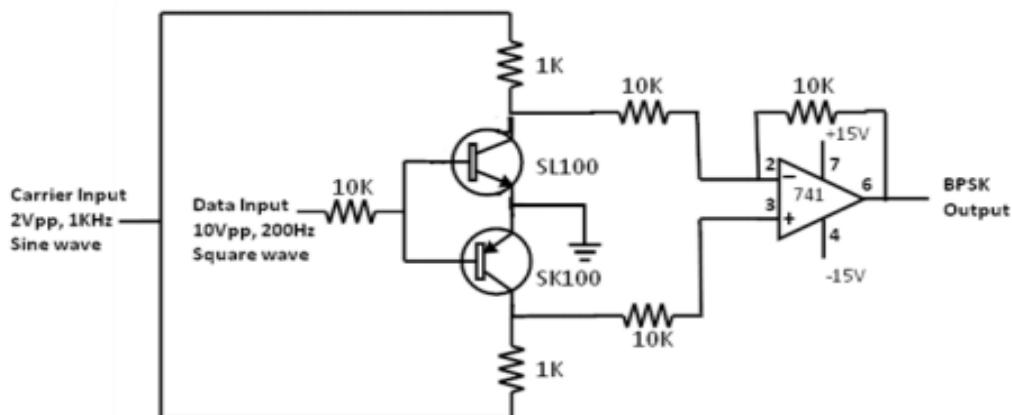
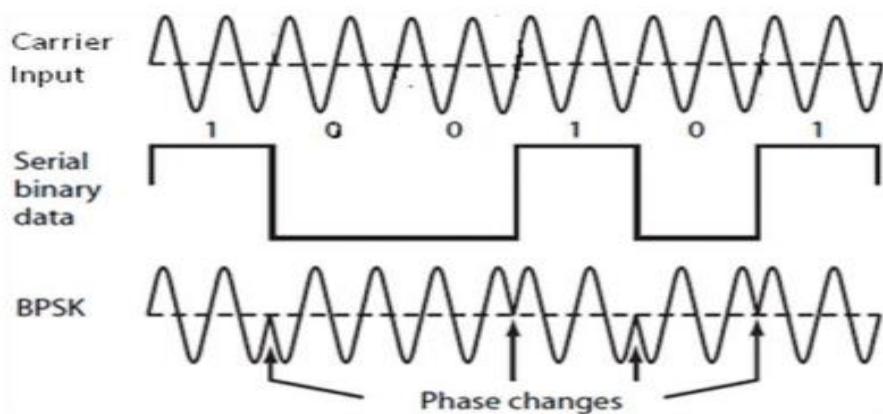
**DEMODULATOR:**

The BPSK demodulator circuit shown in figure consists of an Op-Amp difference amplifier, a rectifier, an envelope detector and a comparator. The difference amplifier which is fed with the unmodulated carrier signal at the non-inverting input and the BPSK modulated signal at the inverting input passes only the phase shifted signal to the output. The in phase signals get subtracted completely. The envelope detector removes the carrier content and recovers the data information. The comparator inverts and level limits the signal to regain the correct logic level.

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**PROCEDURE:**

1. Test all the components and probes.
2. Set up the circuits on the bread board as shown in figure.
3. Feed 2Vpp, 1KHz sine wave as carrier input and 10Vpp, 200Hz square wave signal as the message input.
4. Observe the BPSK output on CRO and plot the waveforms.
5. Feed this BPSK modulated signal to the inverting input of the demodulator. Also feed the unmodulated carrier signal (2Vpp, 1KHz) to the non-inverting input.
6. Observe waveforms on CRO. Adjust the potentiometer to obtain the correct output (if needed).
7. Plot the waveforms.

**CIRCUIT DIAGRAM:****BPSK Modulator****WAVEFORM:**

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**RESULT:-**

BPSK modulator and demodulator circuits were set up and the waveforms were plotted.

**PRECAUTION:-**

1. Connect the circuit carefully.
2. Observe the wave forms carefully.

**RELATED QUESTIONS:-**

- Q.1** What is the phase difference between the two transmitted signals through BPSK scheme?
- Q.2** Express the BPSK signal mathematically.
- Q.3** State the Euclidean distance for BPSK.
- Q.4** What is advantage and disadvantage of BPSK receiver?
- Q.5** Which type of receiver is used for BPSK detection?

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## **EXPERIMENT NO:-7**

**OBJECT:** Implementation and analysis of QPSK modulation and demodulation

**APPARATUS REQUIRED:**

S.No.	Apparatus name	Specification	Quantity
01	Transmitter kit	ST-2106 Scientech	1
02	Receiver kit	ST-2107 Scientech	1
03	8 bit variable data generator	ST-2111 Scientech	1
04	CRO	20MHz Scientech	1

**THEORY:**

QPSK is also known as quaternary PSK, quadri phase PSK, 4-PSK, or 4-QAM. It is a phase modulation technique that transmits two bits in four modulation states. Phase of the carrier takes on one of four equally spaced values such as  $\pi/4$ ,  $3\pi/4$ ,  $5\pi/4$  and  $7\pi/4$ .

$$S_i(t) = \sqrt{2E/T} \cos \{2 \pi f_{ct} t + (2i - 1) \pi/4\}, \quad 0 \leq t \leq T_b \\ = 0 \quad \text{elsewhere}$$

Where  $i = 1, 2, 3, 4$ , &  $E = \text{Tx signal energy per symbol}$ ,  $T = \text{symbol duration}$ .

Each of the possible value of phase corresponds to a pair of bits called dibits. Thus, the gray encoded set of digits: 10, 00, 01, 11

$$S_i(t) = \sqrt{2E/T} \cos [(2i - 1)\pi/4] \cos (2\pi f_{ct} t) - \sqrt{2E/T} \sin [(2i - 1)\pi/4] \sin (2\pi f_{ct} t), \quad 0 \leq t \leq T_b \\ = 0, \quad \text{elsewhere}$$

There are two orthonormal basis functions.

$$c_1(t) = \sqrt{2/T} \cos 2\pi f_{ct} t, \quad 0 \leq t \leq T_b \\ c_2(t) = \sqrt{2/T} \sin 2\pi f_{ct} t, \quad 0 \leq t \leq T_b$$

There are four message points

Input debits	Phase of QPSK signal	Co-ordinates of message signals	
		S1	S2
10	$\pi/4$	$\sqrt{E}/2$	$-\sqrt{E}/2$
00	$3\pi/4$	$-\sqrt{E}/2$	$-\sqrt{E}/2$
01	$5\pi/4$	$-\sqrt{E}/2$	$+\sqrt{E}/2$

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11	$7\pi/4$	$+\sqrt{E}/2$	$+\sqrt{E}/2$
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The I/p binary sequence  $b(t)$  is represented in polar form with symbols 1 & 0 represented as  $+\sqrt{E}/2$  and  $-\sqrt{E}/2$ . This binary wave is demultiplexed into two separate binary waves consisting of odd & even numbered I/P bits denoted by  $b_1(t)$  &  $b_2(t)$ .  $b_1(t)$  &  $b_2(t)$  are used to modulate a pair of quadrature carrier. The result is two PSK waves. These two binary PSK waves are added to produce the desired QPSK signal

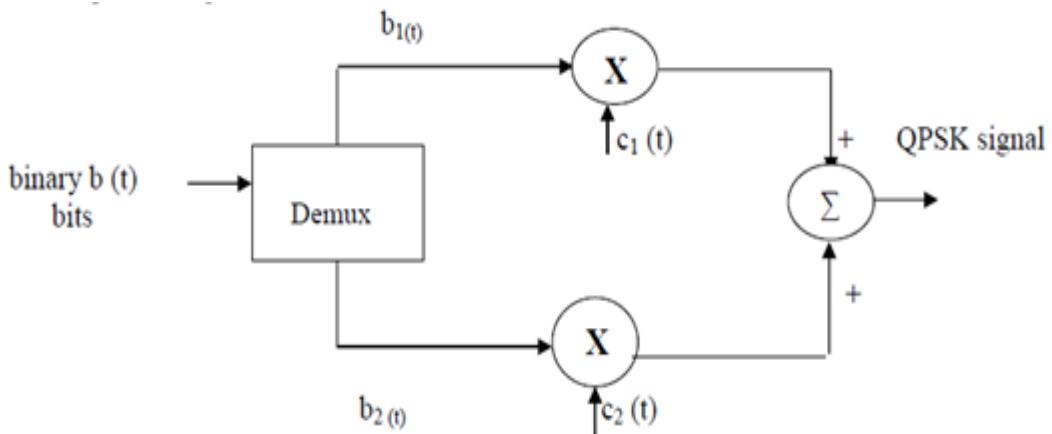


Figure. 7.1: Block diagram of QPSK Transmitter

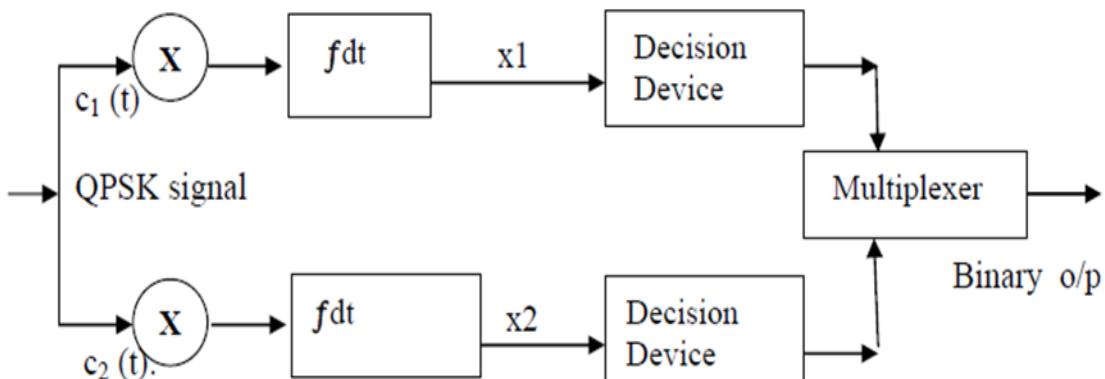


Figure 7.2: Block diagram of QPSK Receiver

QPSK receiver consists of a pair of correlators with common I/P & supplied with locally generated signal  $c_1(t)$  &  $c_2(t)$ . The correlator output,  $x_1$ , &  $x_2$  are each compared with a threshold of zero volt. If  $x_1 > 0$ , decision is made in favour of symbol '1' for upper channel and if

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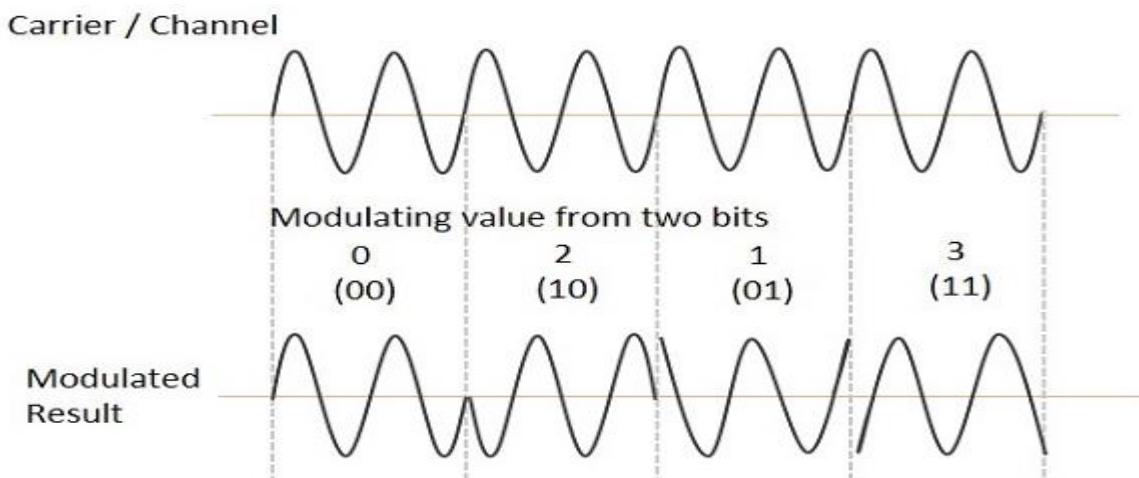
$x_1 > 0$ , decision is made in favour of symbol 0. Parallelly if  $x_2 > 0$ , decision is made in favour of symbol 1 for lower channel & if  $x_2 < 0$ , decision is made in favour of symbol 0. These two channels are combined in a multiplexer to get the original binary output.

## **PROCEDURE:**

1. Test all the components and probes.
2. Set up the circuits on the kit.
3. Feed 2Vpp, 1KHz sine wave as carrier input and 10Vpp, 200Hz square wave signal as the message input.
4. Observe the QPSK output on CRO and plot the waveforms.
5. Feed this QPSK modulated signal to the inverting input of the demodulator. Also feed the unmodulated carrier signal (2Vpp, 1KHz) to the non-inverting input.
6. Observe waveforms on CRO. Adjust the potentiometer to obtain the correct output (if needed).
7. Plot the waveforms.

## **WAVEFORM:**

The QPSK waveform for two-bits input is as follows, which shows the modulated result for different instances of binary inputs.



## **RELATED QUESTIONS:-**

- Q.1** Write down the QPSK signal mathematically.
- Q.2** What is the phase difference between the adjacent messages in QPSK ?
- Q.3** What is the phase difference between the adjacent messages in QPSK ?
- Q.4** Discuss the application of QPSK technique.
- Q.5** What are the advantages of QPSK system ?

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## **EXPERIMENT NO:-8**

**OBJECT:** - To Simulate differential phase shift keying technique using MATLAB software and also observe its performance.

**APPARTUS USED:** - PC

**THEORY:-**

DPSK involves 2 basic operations at the transmitter, differential encoding of the i/p binary wave and phase shift keying, hence the name DPSK. In the differential encoding at the transmitter input, starts with an arbitrary first bit serving as reference and thereafter the sequence is generated using  $b(t) - 1'$  previous value of differentially encoded digit  $d(t)$  i/p binary digit at time  $k T_b$ . Assuming reference bit added to  $b(t)$  is  $a'1'$ .  $B(k)$  is thus generated and used to phase shift key a carrier with phase angles 0 and  $180^\circ$ .

### **BER -Bit Error Rate**

In digital transmission, the number of bit errors is the number of received bits of a data stream over a communication channel that has been altered due to noise, interference, distortion or bit synchronization errors. The bit error rate or bit error ratio (BER) is the number of bit errors divided by the total number of transferred bits during a studied time interval. BER is a unitless performance measure, often expressed as a percentage. In a communication system, the receiver side BER may be affected by transmission channel noise, interference, distortion, bit synchronization problems, attenuation, wireless multipath fading, etc. The BER may be analyzed using stochastic computer simulations. If a simple transmission channel model and data source model is assumed, the BER may also be calculated using Binary symmetric channel (used in analysis of decoding error probability in case of non bursty bit errors on the transmission channel) and Additive white gaussian noise (AWGN) channel without fading.

Algorithm

\* To send '0' and '1' following  
Consideration is adopted.

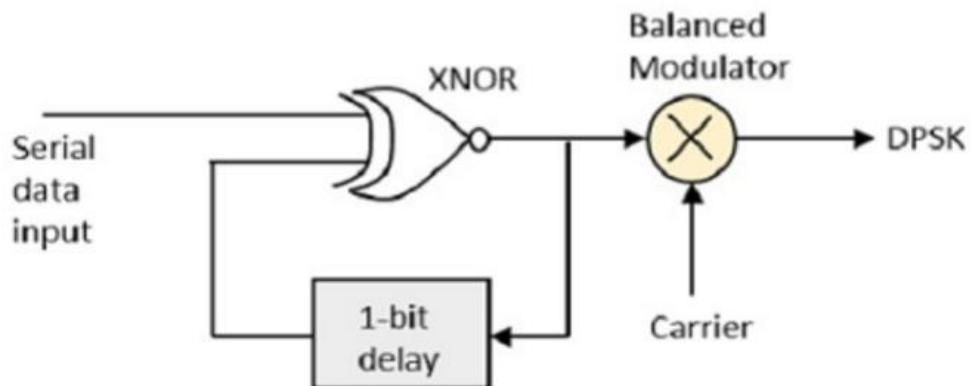
Initialization commands

1. Generate the input data randomly
  2. Implement differential encoding
  3. Do BPSK modulation
  4. Add AWGN noise
  5. Calculate the no of bits in error
  6. Plot the BER graph
- ‘1’- no phase change  
‘0’- phase change of  $180^\circ$   
or  
‘1’ – phase change of  $180^\circ$   
‘0’ – no phase change

# Let  $d(t) = 1 \ 1 \ 0 \ 1 \ 0 \ 1 \ 1 \ 1$

Phase = 0 0  $180^\circ$  0  $180^\circ$  0 0 0 -- '1' no change

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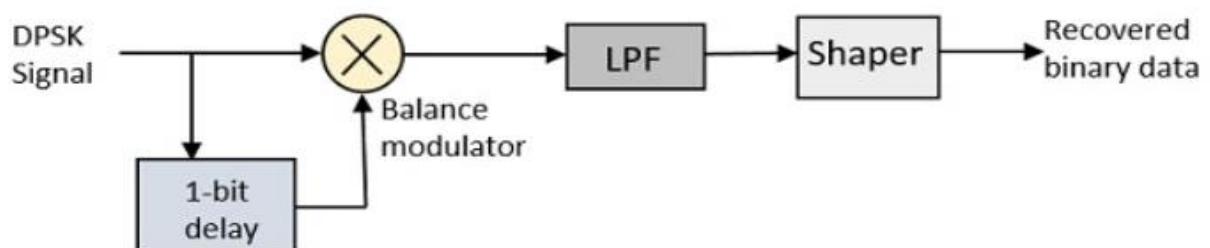
**TRANSMITTER CIRCUIT: -**

DPSK Modulator

$$d(t) = \begin{matrix} 1 & 1 & 0 & 1 & 1 & 0 & 1 & 0 & 1 & 0 & 1 \end{matrix}$$

$$b(t) = \begin{matrix} 1 & 1 & 1 & 0 & 0 & 0 & 1 & 1 & 0 & 0 & 1 & 1 \end{matrix}$$

(Let)

**RECEIVER CIRCUIT:-**

DPSK Demodulator

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**PROGRAM :-**

```

N = 10^4 % number of bits or symbols
rand('state',100); % initializing the rand() function
randn('state',200);% initializing the randn() function
ip = rand(1,N)>0.5;% generating 0,1 with equal probability
ipD = mod(filter([1 -1],1,ip),2); % %differential encoding y[n]=y[n-1]+x[n]
s = 2*ipD-1; % BPSK modulation 0 -> -1; 1 -> 0
n = 1/sqrt(2)*[randn(1,N) + j*randn(1,N)]; % white gaussian noise, 0dB variance
Eb_N0_dB = [-3:10]; % multiple Eb/N0 values
for ii = 1:length(Eb_N0_dB)
    y = s + 10^(-Eb_N0_dB(ii)/20)*n; % additive white gaussian noise
    ipDHat_coh = real(y) > 0; % coherent demodulation
    ipHat_coh = mod(filter([1 -1],1,ipDHat_coh),2); %differential decoding
    nErr_dbpsk_coh(ii) = size(find([ip - ipHat_coh]),2); % counting the number of errors
end
simBer_dbpsk_coh = nErr_dbpsk_coh/N;
theoryBer_dbpsk_coh = erfc(sqrt(10.^((Eb_N0_dB/10))).*(1 - .5*erfc(sqrt(10.^((Eb_N0_dB/10)))));
close all
figure
semilogy(Eb_N0_dB,theoryBer_dbpsk_coh,'b.-');
hold on
semilogy(Eb_N0_dB,simBer_dbpsk_coh,'mx-');
axis([-2 10 10^-6 0.5])
grid on
legend('theory', 'simulation');
xlabel('Eb/No, dB')
ylabel('Bit Error Rate')
title('Bit error probability curve for coherent demodulation of DBPSK')

```

**RESULT:-**

1. Simulation of DPSK is done.
2. Performance is observed by measuring the BER characteristics. Characteristics are similar to theoretical result.

**RELATED QUESTIONS:-**

- Q.1** What is the DPSK?  
**Q.2** Write down the advantages of DPSK.  
**Q.3** Discuss the disadvantages of DPSK.  
**Q.4** Which method is commonly used in modulation and demodulation of DPSK?  
**Q.5** Write down the application of DPSK.

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## EXPERIMENT NO:-9

**OBJECT:** Implementation and analysis of Delta modulation and demodulation.

### APPARATUS USED:

SNO	APPARATUS NAME	SPECIFICATION	QUANTITY
01	Training kit	ST-2105 Scientech	1
02	CRO	20MHz Scientech	1
03	Connecting Probes		2

### THEORY:

Delta modulation is a system of digital modulation scheme in which the difference between the sample value at sampling time K and sampling value at previous sampling time (K-1) is encoded into just a single bit. One way in which delta modulator and demodulator is assembled is as shown

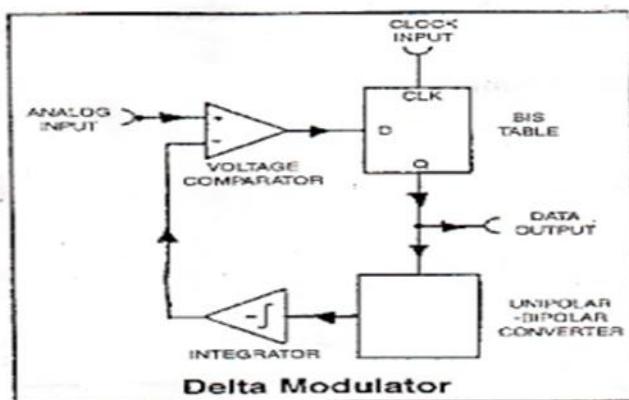


Fig.1

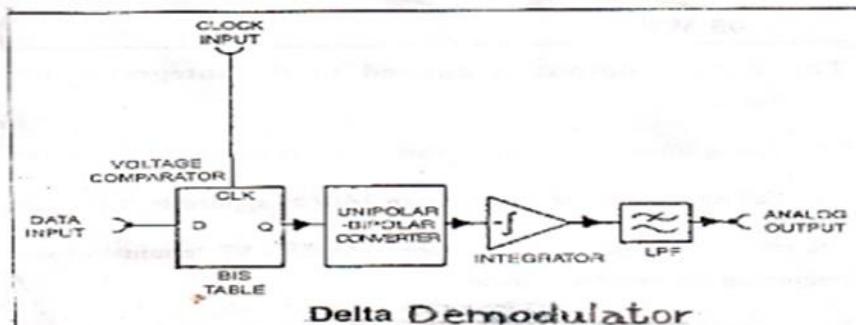


Fig.2

es is as shown

The baseband signal  $m(t)$  and its quantized approximation  $m'(t)$  are applied as inputs to a comparator. A comparator simply makes a comparison between inputs. If signal amplitude has increased, then modulator's output is at logic level 1. If the signal amplitude has decreased, the modulator output is at logic level 0. Thus the output from the modulator is a series of 0's and 1's to indicate rise and fall of the waveform since the previous value. The comparator output is then latched into a D flip-flop which is clocked by the transmitter clock. Thus the output of the flip-flop is a latched 1 or 0 synchronous with the transmitter clock edge. The binary sequence is transmitted to receive and is also fed to the unipolar to bipolar converter. This block converts logic 0 to voltage level of +4V and 1 to voltage level of -4V. The bipolar output is applied to the integrator whose output is :

- a) Rising linear ramp signal when -4V is applied to it
- b) Falling linear ramp signal when +4V is applied to it.

The integrator output is then connected to the -ve terminal of voltage comparator.

#### Procedure:

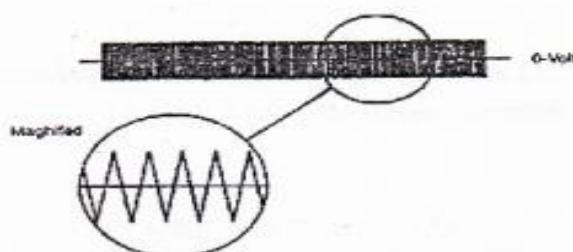
1. Make connections as per diagram.
2. Ensure that the clock frequency selector block switches A & B are in A=0 and B=0 position.
3. Now turn On the kit and see that LED glows.
4. In order to ensure for the correct operation of the system, we first connect 0 volts to the +ve input of the comparator. Now observe the output of the integrator 1 (i.e. tp 17) and the output of transmitter's level changer (i.e. tp 15). When the positive and negative output levels of the level changer will be equal the output will be a triangular waveform as shown in fig3 (Case A). When the negative level is greater than positive level, the integrator's output level will be as shown in fig3 (Case B). And when the positive output level is greater, then the integrator's output will be as shown in fig3 (Case C). The levels can be adjusted by turning the potentiometer from one extreme to another.
5. Adjust the transmitter's level changer preset until the output of integrator is a triangular wave centered at 0 volts. The peak to peak amplitude of the wave should be 0.5 volts (approx.), this amplitude is known as the integrator Step Size.
6. Now observe the output of the transmitter's bistable circuit (i.e. tp 14). It is now a stream of alternate '1' and '0'. This is the output of a delta modulator and the Delta modulator is now said to be balanced for correct operation.
7. Now examine the output of integrator at the receiver (i.e. tp 47). It should be a triangular wave with step size equal to that of integrator in transmitter and ideally centered around 0 volts.
8. Now observe the output of low pass filter. It will be a DC level centered around 0 volts. This is the output of Delta demodulator and it is balanced for correct operation.
9. Now disconnect the 0 volts from the +ve input of the comparator and reconnect it to 250 Hz signal of the function generator block. Now observe the output of voltage comparator (tp 9), integrator (tp 17). Also observe the delta modulated output at the output of bistable circuit. It has been encoded into stream of '0' and '1'.
10. Also observe the output of low pass filter in the receiver (tp 51), which is the output of demodulator.

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in figure given below

11. Now disconnect 250 Hz from the +ve input of comparator and reconnect it to 500 Hz , 1 KHz, and 2 KHz outputs in turn. Now note the frequency of the analog signal increases, so the low pass filter's output becomes more distorted and reduced in amplitude. This effect is known as 'Slope Overloading'.

**Observations:**



**Case A : Bipolar output – Positive level = Negative level**



**Case B : Bipolar output – Positive level < Negative level**



**Case C : Bipolar output – Positive level > Negative level**

**Result:** The Delta modulation / demodulation and Slope Overloading effect has been studied.

**Precautions:**

1. The connections should be made properly and tightly.
2. Check all the connections before switching ON the kit.

**RELATED QUESTIONS:-**

- Q.1** In predictive coding, differentiate between DM and ADM.
- Q.2** In predictive coding, differentiate between DPCM and ADPCM.
- Q.3** What are slope overload distortion and granular noise distortion in DM coding?
- Q.4** Explain how ADM coding solves the above errors.
- Q.5** What is the difference between DM and DPCM?

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## **EXPERIMENT NO:-10**

**OBJECT:** To study encoding and decoding of Linear Block Codes

**APPARATUS REQUIRED:**

SNO	APPARATUS NAME	SPECIFICATION	QUANTITY
01	Training kit	ST-2121A & 2121B Scientech	1
02	Banana Cable	2 mm	1
03	Regulated Power Supply		

**THEORY:**

**Error Detection and Correction:** Error detection is the ability to detect the presence of errors caused by noise or other impairments during transmission from the transmitter to the receiver. Error correction is the additional ability to reconstruct the original, error-free data. There are two basic ways to design the channel code and protocol for an error correcting system.

**LINEAR BLOCK CODES:**

Linear block codes are conceptually simple codes that are basically an extension of single-bit parity check codes for error detection. A single-bit parity check code is one of the most common forms of detecting transmission errors. This code uses one extra bit in a block of  $n$  data bits to indicate whether the number of 1s in a block is odd or even. Thus, if a single error occurs, either the parity bit is corrupted or the number of detected 1s in the information bit sequence will be different from the number used to compute the parity bit: in either case the parity bit will not correspond to the number of detected 1s in the information bit sequence, so the single error is detected. Linear block codes extend this notion by using a larger number of parity bits to either detect more than one error or correct for one or more errors. Unfortunately, linear block codes, along with convolutional codes, trade their error detection or correction capability for either bandwidth expansion or a lower data rate, as will be discussed in more detail below. We will restrict our attention to binary codes, where both the original information and the corresponding code consist of bits taking a value of either 0 or 1.

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## ENCODING

Each linear block code can be described by:

$$\mathbf{c} = \mathbf{u} \cdot \mathbf{G} \quad (1)$$

$$(2)$$

where  $\mathbf{u}$  is the uncoded information word with  $k$  bits,  $\mathbf{c}$  is the corresponding code word for the information word  $\mathbf{u}$  with  $n$  bits and  $\mathbf{G}$  is the  $n \times k$  generator matrix of the block code.

With the information word  $\mathbf{u} = (u_0 \ u_1 \ u_2)$ , the matrix multiplication equals (here an example generator matrix is taken):

$$\mathbf{c} = \mathbf{u} \cdot \mathbf{G} \quad (3)$$

$$\mathbf{c} = (u_0 \ u_1 \ u_2) \cdot \begin{pmatrix} 1 & 1 & 0 & 1 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 & 0 & 1 & 1 \\ 1 & 1 & 1 & 0 & 1 & 0 & 0 \end{pmatrix} \quad (4)$$

$$= u_0 \cdot \underbrace{\begin{pmatrix} 1 & 1 & 0 & 1 & 0 & 0 & 1 \end{pmatrix}}_{\text{1st row of } \mathbf{G}} + \quad (5)$$

$$u_1 \cdot \underbrace{\begin{pmatrix} 1 & 0 & 1 & 0 & 0 & 1 & 1 \end{pmatrix}}_{\text{2nd row of } \mathbf{G}} + \quad (6)$$

$$u_2 \cdot \underbrace{\begin{pmatrix} 1 & 1 & 1 & 0 & 1 & 0 & 0 \end{pmatrix}}_{\text{3rd row of } \mathbf{G}} . \quad (7)$$

Note that summation and multiplication is done in the binary domain ( $0 + 0 = 0$ ,  $0 + 1 = 1$ ,  $1 + 1 = 0$ ). The complete code is given by all linear combinations of the rows of  $\mathbf{G}$ . A clear scheme how to get all linear combinations is given next:

$$k \left\{ \overbrace{\begin{pmatrix} 1 & 1 & 0 & 1 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 & 0 & 1 & 1 \\ 1 & 1 & 1 & 0 & 1 & 0 & 0 \end{pmatrix}}^n \right\} = \mathbf{G}$$

$\mathbf{u}_0 = (0 \ 0 \ 0)$	$(0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0)$	$= \mathbf{c}_0$	$w_H(c_i)$
$\mathbf{u}_1 = (0 \ 0 \ 1)$	$(1 \ 1 \ 1 \ 0 \ 1 \ 0 \ 0)$	$= \mathbf{c}_1$	4
$\mathbf{u}_2 = (0 \ 1 \ 0)$	$(1 \ 0 \ 1 \ 0 \ 0 \ 1 \ 1)$	$= \mathbf{c}_2$	4
$\mathbf{u}_3 = (0 \ 1 \ 1)$	$(0 \ 1 \ 0 \ 0 \ 1 \ 1 \ 1)$	$= \mathbf{c}_3$	4
$\mathbf{u}_4 = (1 \ 0 \ 0)$	$(1 \ 1 \ 0 \ 1 \ 0 \ 0 \ 1)$	$= \mathbf{c}_4$	4
$\mathbf{u}_5 = (1 \ 0 \ 1)$	$(0 \ 0 \ 1 \ 1 \ 1 \ 0 \ 1)$	$= \mathbf{c}_5$	4
$\mathbf{u}_6 = (1 \ 1 \ 0)$	$(0 \ 1 \ 1 \ 1 \ 0 \ 1 \ 0)$	$= \mathbf{c}_6$	4
$\mathbf{u}_7 = (1 \ 1 \ 1)$	$(1 \ 0 \ 0 \ 1 \ 1 \ 1 \ 0)$	$= \mathbf{c}_7$	4

The minimum distance  $d_{\min}$  of the code is the minimum number of digits in which two code words are different. It is shown in the lecture that the minimum distance equals the minimum weight of the code words:

$$\begin{aligned} d_{\min} &= \min \{w_H(\mathbf{c}_i) \mid \mathbf{c}_i \neq \mathbf{0}\} \\ &= 4 . \end{aligned}$$

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## DECODING:-

The decoding process is done in the following steps:

Step 1: Calculate the syndrome  $\mathbf{s}$  by evaluating  $\mathbf{s} = \mathbf{y} \cdot \mathbf{H}'^T$ .

Step 2: Check  $\mathbf{s}$  (Case distinction)

if  $\mathbf{s} = 0 \implies$  accept the received word (perhaps more than  $t_e = 3$  errors)

if  $\mathbf{s} \neq 0 \implies$  search in table

- a)  $\mathbf{s}$  included in the table  $\implies$  determine error vector  $\mathbf{e}$
- b)  $\mathbf{s}$  not included in the table  $\implies$  more than  $t = 1$  errors  
 $\implies$  not correctable

Step 3: Correct the error by calculation of  $\mathbf{y}_{corr} = \mathbf{y} + \mathbf{e}$ .

Consider the following example with the parity check matrix:

$$\mathbf{H}'^T = \begin{pmatrix} 1 & 1 & 1 & 0 \\ 0 & 1 & 1 & 1 \\ 1 & 1 & 0 & 1 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{pmatrix}. \quad (9)$$

$$\mathbf{y}_a = (0 \ 0 \ 0 \ 1 \ 1 \ 0 \ 1) \quad (1 \ 1 \ 0 \ 1) = \mathbf{s}_a$$

The according error vector is obtained from the syndrome table.

$$\mathbf{s}_a = (1 \ 1 \ 0 \ 1) \implies \mathbf{e}_a = (0 \ 0 \ 1 \ 0 \ 0 \ 0 \ 0)$$

The corrected vector becomes therefore

$$\mathbf{y}_{a,corr} = \mathbf{y}_a + \mathbf{e}_a = (0 \ 0 \ 1 \ 1 \ 1 \ 0 \ 1).$$

## **RESULTS:**

The understanding of modulation and demodulation schemes for linear block code developed.

## RELATED QUESTIONS:-

**Q.1** What is the definition of a linear block code?

**Q.2** If we want to be able to detect two-bit errors, what should be the minimum Hamming distance?

**Q.3** In a codeword, we add two redundant bits to each 8-bit data word. Find the number of  
(a) Valid codeword (b) Invalid codeword

**Q.4** What is the minimum distance in linear block codes?

**Q.5** What is the Hamming distance for each of the following codewords?

- (a) (10000, 00000)    (b) (10101, 10000)    (c) (00000, 11111)    (d) (00000, 00000)

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