# National Institute Of Technology Goa

# Assignment Of VLSI Circuit Design

TOPIC: NMOS INVERTER

**Submitted To:**

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**Aim**: *The aim of this experiment is NMOS Inverter analysis, salient feature transfer characteristics, delay and power dissipation computation*

**Tools Used**: Cadence Software

## INTRODUCITON

An NMOS inverter consists of an NMOS transistor and a resistor connected in series between the supply voltage VDD and the ground. The output is taken at the junction of the transistor and the resistor. The operation of the NMOS inverter is based on the switching characteristics of the NMOS transistor. When the input voltage $Vin$ is low, the NMOS transistor is off, and the output voltage $Vout$ is high (near $V$dd ). Conversely, when $Vin$ is high, the NMOS transistor is on, and $Vout$ is low.

## PRINCIPLE OF OPERATION OF NMOS INVERTER

The logic symbol and truth table of ideal inverter is shown in figure given below. Here A is the input and B is the inverted output represented by their node voltages. Using positive logic, the Boolean value of logic 1 is represented by Vdd and logic 0 is represented by 0. Vth is the inverter threshold voltage, which is Vdd /2, where Vdd is the output voltage.

The output is switched from 0 to Vdd when input is less than Vth. So, for 0<Vin<Vth output is equal to logic 0 input and Vth<Vin< Vdd is equal to logic 1 input for inverter.

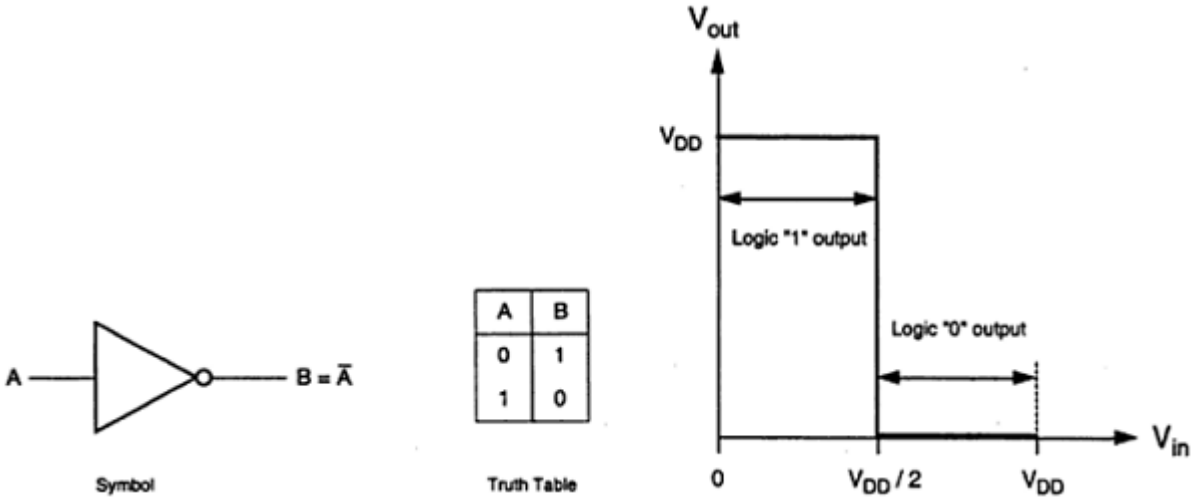


Fig: Logic symbol , Truth table and output for Ideal Inverter
Src: electronics.com

The generalized circuit structure of an NMOS inverter is shown in the figure below.

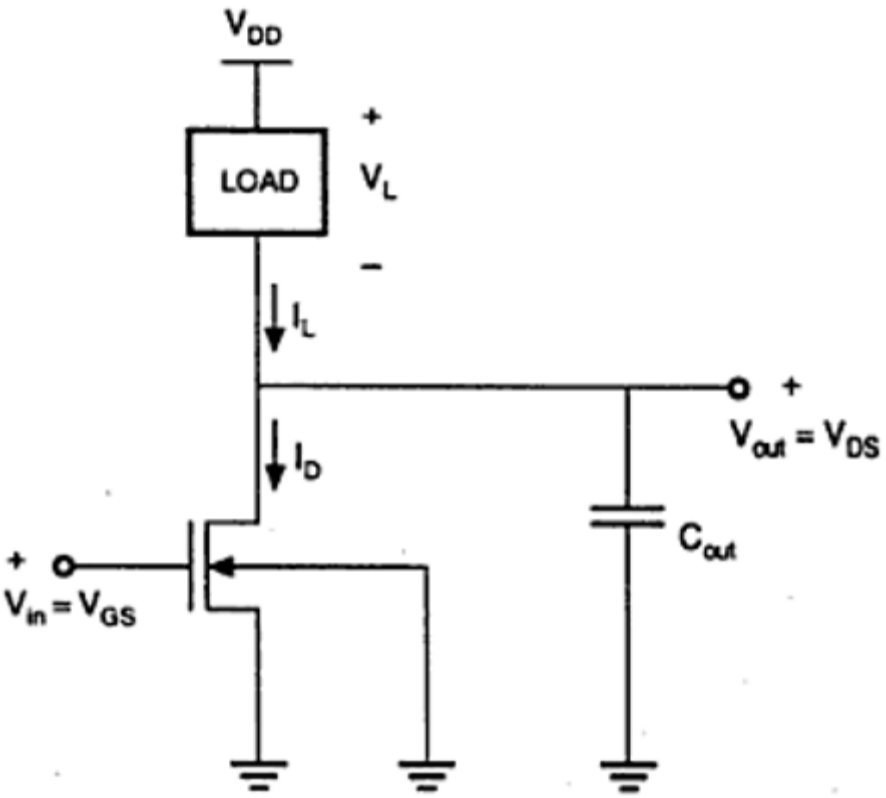


Fig: circuit diagram Nmos Inverter
Src: electronics.com

From the given figure, we can see that the input voltage of inverter is equal to the gate to source voltage of nMOS transistor and output voltage of inverter is equal to drain to source voltage of nMOS transistor. The source to substrate voltage of nMOS is also called driver for transistor which is grounded; so $V_{SS} = 0$. The output node is connected with a lumped capacitance used for $V_{TC}$.

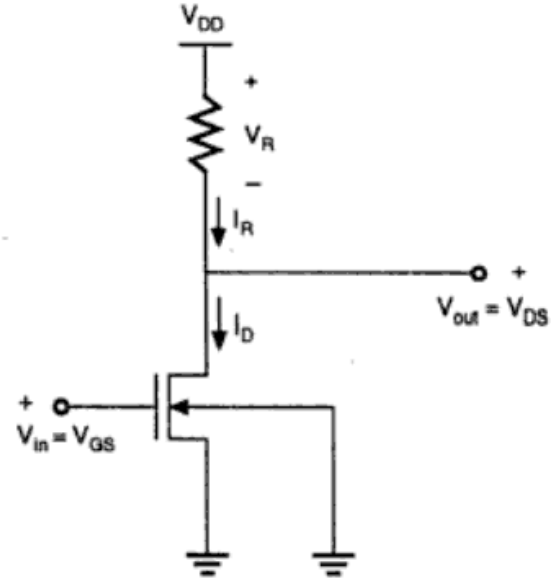


Fig :Resistive Load Inverter

## CIRCUIT OPERATION

When the input of the driver transistor is less than threshold voltage VTH ($V_{in} < V_{TH}$), driver transistor is in the cut – off region and does not conduct any current. So, the voltage drop across the load resistor is ZERO and output voltage is equal to the VDD. Now, when the input voltage increases further, driver transistor will start conducting the non-zero current and nMOS goes in saturation region.

Mathematically,

$$I_D = Kn^2[V_{GS} - V_{TO}]^2$$

Increasing the input voltage further, driver transistor will enter into the linear region and output of the driver transistor decreases.

$$I_D = 2(K_n/2)^2[V_{GS} - V_{TO}]V_{DS} - V_{DS}^2$$

## CALCULATIONS

**1. Transfer Characteristics:**

The output voltage $Vout$ of an NMOS inverter is given by

$$V_{out} = V_{DD} - I_D R_L$$

where:

- VDD is the supply voltage.
- ID is the drain current.
- RL is the load resistor.

The drain current IDI_DID in the NMOS transistor operates in different regions:

- **Cutoff Region:** $V_{in} < V_{th} \quad I_D = 0$

- **Linear Region:** $V_{in} > V_{th}\ and\ V_{DS} < V_{in} - V_{th}$

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{in} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

- **Saturation Region:**

$$V_{in} > V_{th} \quad and V_{DS} \geq V_{in} - V_{th}$$
$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{in} - V_{th})^2$$

**2. Power Dissipation:**

In this analysis, we focus on dynamic power dissipation, which occurs during the switching process, and is given by

$$P_d = \frac{1}{2} C_L V_{DD}^2 f$$

$$P_d = \frac{1}{2} C_L V_{DD}^2 f = \frac{1}{2} \times 10pF \times (1.8V)^2 \times 387.7MHz = 1.25\text{m}W$$

Where:

- $C_L is the load capacitance.$
- $V_{DD} is the supply voltage.$
- $f \text{ is the switching frequency.}$

**3.Propagation Delay:**

Propagation delay $t$p is the time taken for the output voltage to reach 50% of its final value after the input voltage has reached 50% of its final value. This delay is an important parameter in determining the speed of digital circuits.

$$t_p = (t_{pLH} + t_{pHL})/2$$

Where:

- tpLH is the low-to-high propagation delay (rise time).
- tpHL is the high-to-low propagation delay (fall time).

➢ **For $\boldsymbol{R_L} = 1\text{K}\boldsymbol{\Omega}$ $\boldsymbol{and}$ $\boldsymbol{C_L} = \boldsymbol{1pF}$**

- $t_{pLH} = 0.3465ns$
- $t_{pHL} = 0.1803ns$
- $t_p = 0.2484ns$

➢ **For $\boldsymbol{R_L} = 2\text{K}\boldsymbol{\Omega}$ $\boldsymbol{and}$ $\boldsymbol{C_L} = \boldsymbol{1pF}$**

- $t_{pLH} = 0.3665ns$
- $t_{pHL} = 0.1503ns$
- $t_p = 0.2584ns$

1. **NMOS Inverter:**

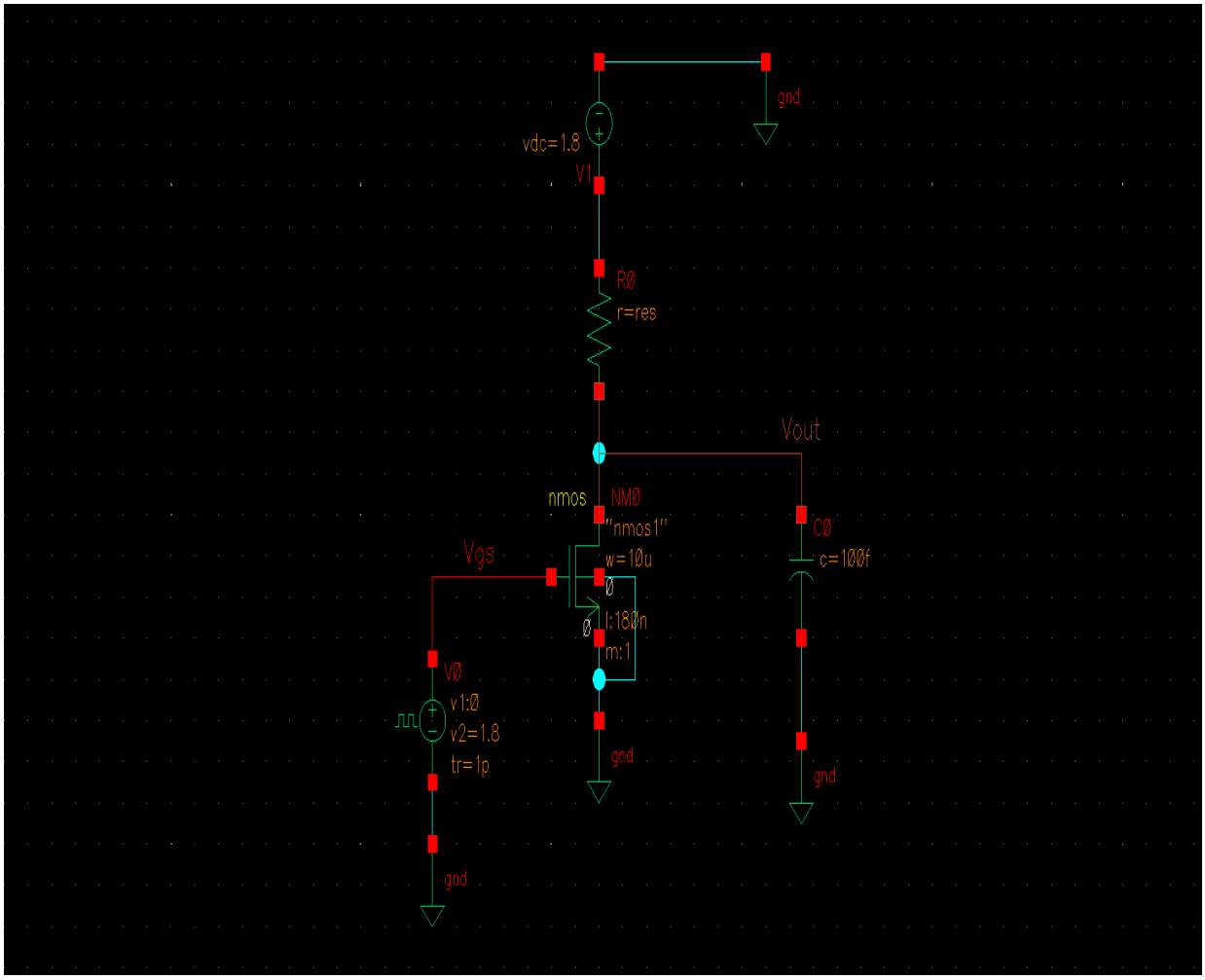


Fig: Circuit Diagram NMOS Inverter

## ❖ Transfer Characteristics

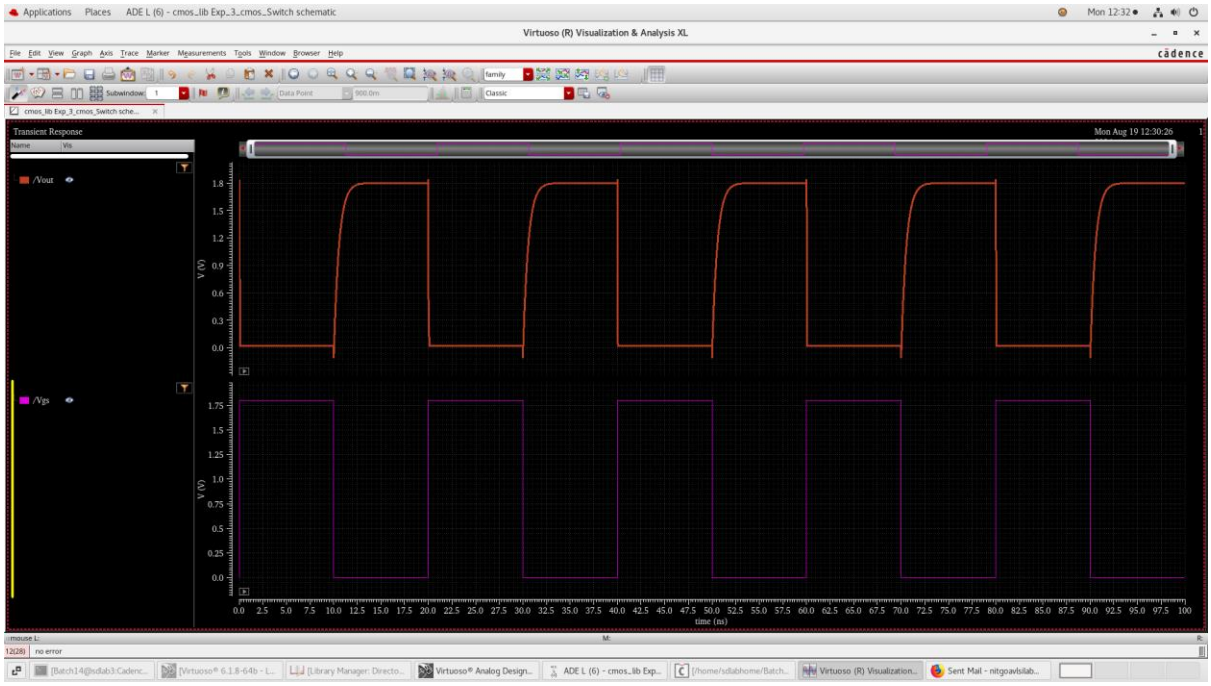


Fig: Output Characteristics for NMOS

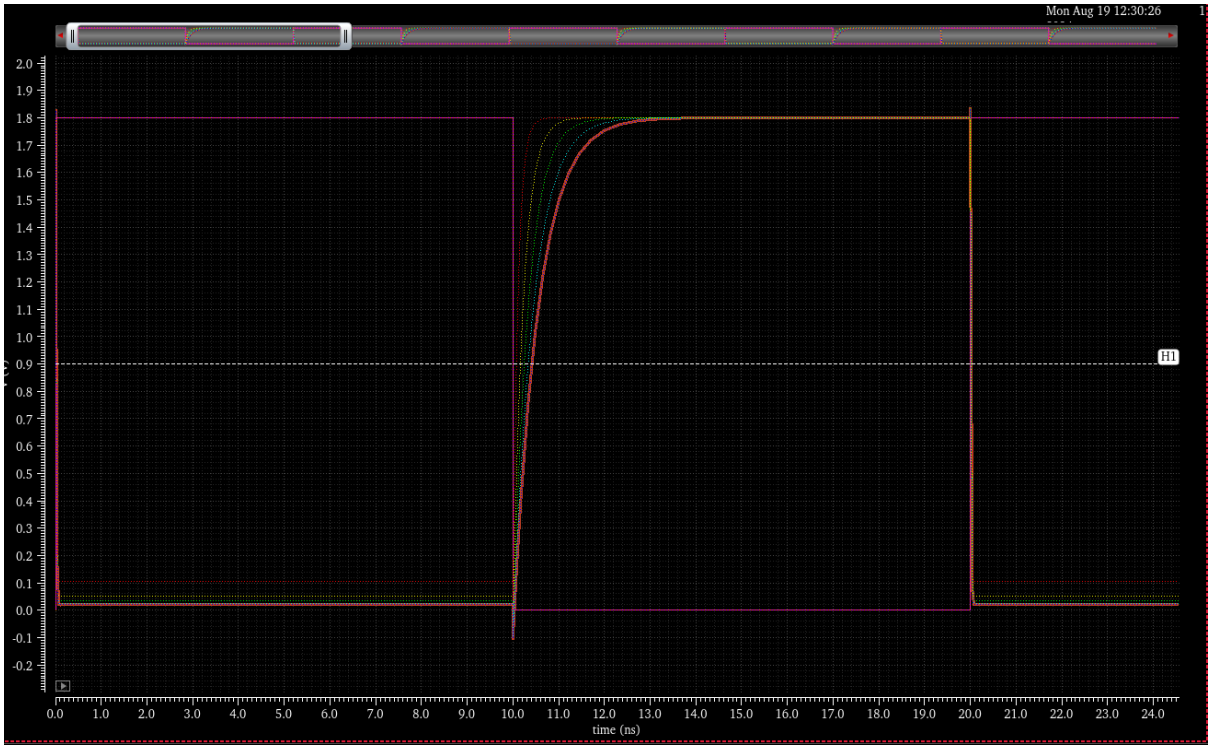


Fig: Parametric analysis for different values of resistances (NMOS)

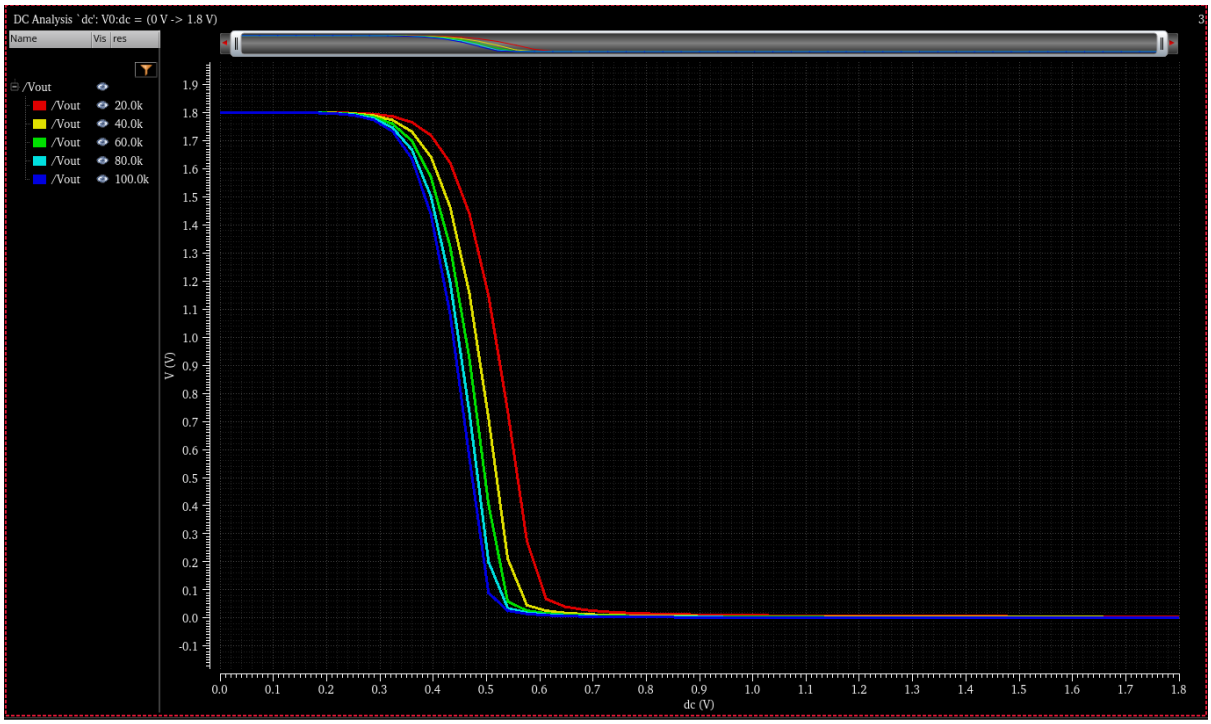


Fig: Parametric analysis for different values of vgs (NMOS)

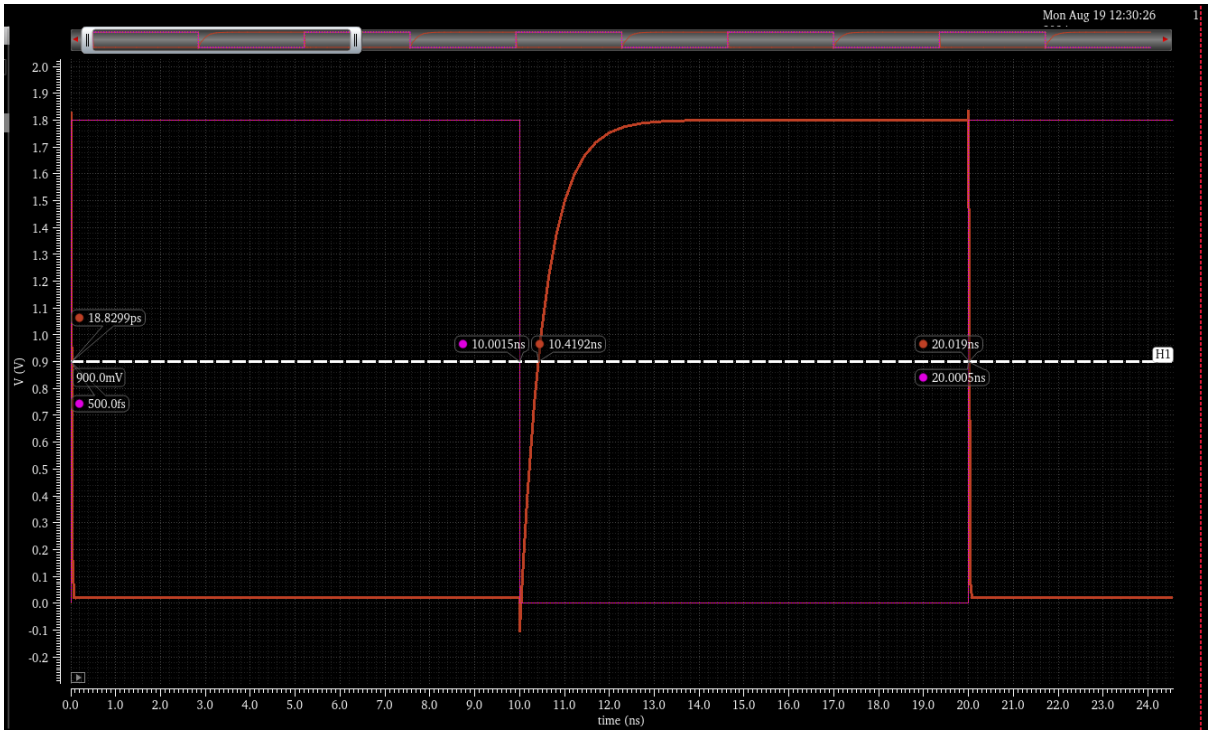


Fig: Calculation of Propagation Delay (NMOS)

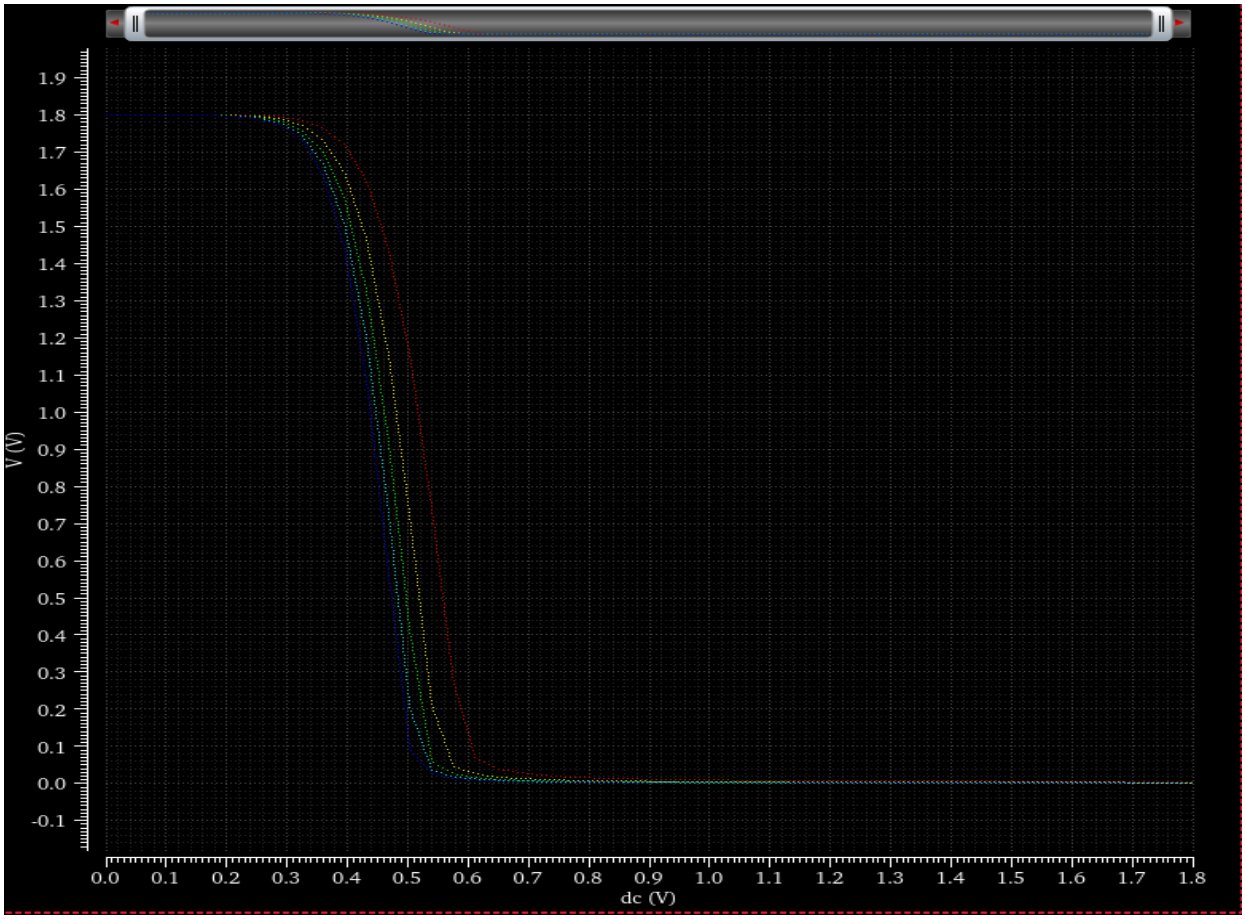


Fig: Parametric analysis for different values of vgs (NMOS)

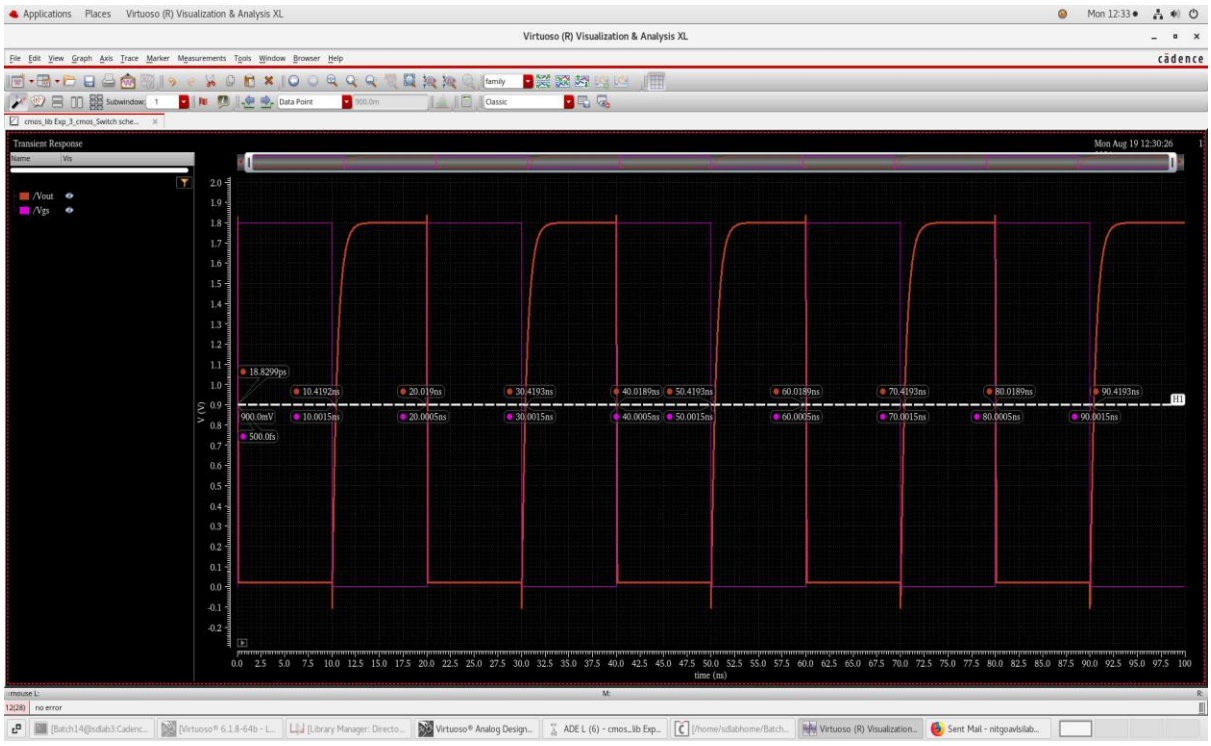


Fig: Propagation Delay for at different Time Instance (NMOS)

## PROCEDURE

**1.Setup in Cadence:**

- Open Cadence Virtuoso and create a new schematic for the NMOS Inverter circuits.
- Add an NMOS transistor and a DC voltage source for VGS and VDS.
- Repeat the setup for the PMOS transistor with appropriate polarity for the voltage sources.
- Connect the measurement probes to record the drain current Id and the gate voltage Vgs or Vsg.

**2.Circuit configuration:**

- Set VDD to 1.8V.
- Use a resistor value RL of 1 kΩ.
- Sweep the input voltage Vin from 0V to 1.8V.
- Simulate the circuit to obtain the transfer characteristics.

**3.Simulation:**

- Perform a DC sweep of Vin to observe the output voltage Vout.
- Analyze the power dissipation during the switching process.
- Measure the propagation delay by applying a step input and observing the output response.

## OBSERVATIONS

- Transfer **Characteristics:**

  - The simulation results show that the NMOS inverter behaves as expected, with the output voltage Vout transitioning from high (close to VDD) to low (close to 0V) as the input voltage Vin increases and crosses the threshold voltage Vth=0.4V.
  - The transition region, where the output changes state, is sharp, indicating good switching behavior of the inverter. The output remains at VDD when Vin<Vth and drops to nearly 0V when Vin>Vth .

- Power **Dissipation:**

  - **Power Dissipation:** The dynamic power dissipation, calculated to be approximately 1.25mW, is higher during switching operations due to the charging and discharging of the load capacitance CL. This highlights the importance of minimizing the switching frequency and load capacitance to reduce dynamic power consumption.

- Propagation **Delay:**

- The propagation delay tp for the NMOS inverter was calculated to be approximately 0.257ns. This delay is influenced by the load resistance RL and capacitance CL, as well as the supply voltage VDD and the threshold voltage Vth.
- The relatively low propagation delay indicates that the NMOS inverter can switch states quickly, making it suitable for high-speed digital applications.

- Load **Dependence:**

  - The performance of the NMOS inverter, particularly the power dissipation and propagation delay, is heavily dependent on the load capacitance CL. A higher load capacitance increases the dynamic power dissipation and propagation delay, while a lower load capacitance improves the speed but may affect the noise margin.
  - The resistor RL value also plays a crucial role in determining the output voltage levels and the overall inverter performance. A higher RL increases the output voltage swing but also increases the propagation delay.

- Effect **of Threshold Voltage (Vth):**

  - The threshold voltage Vth is a critical parameter in determining the switching point of the NMOS inverter. A lower Vth would cause the inverter to switch at a lower input voltage, while a higher Vth would require a higher input voltage for the transition.
  - The observed transfer characteristics align with the theoretical expectations, confirming that the NMOS transistor operates correctly within the designed threshold voltage limits.

- Supply **Voltage (VDD) Influence:**

  - The supply voltage VDD directly affects the output voltage levels and the power dissipation of the inverter. In this experiment, VDD=1.8V was used, which provided a sufficient voltage swing for clear logic levels.
  - Any variation in VDD would proportionally affect the output voltage, power dissipation, and propagation delay, demonstrating the need for a stable supply voltage in digital circuits.

## RESULT

- **Transfer Characteristics:** The transfer curve obtained from the simulation shows the expected inverter behavior, with the output switching from high to low as the input voltage crosses the threshold voltage.

- **Power Dissipation:** The total power dissipation of the NMOS inverter is calculated to be approximately 1.25mW.

- **Propagation Delay:** The propagation delay is calculated to be approximately 0.257ns.

## CONCLUSION

The NMOS inverter was successfully simulated using Cadence software, and its transfer characteristics were analyzed. The power dissipation and propagation delay were calculated, demonstrating the effectiveness of the NMOS inverter in switching applications. The results obtained from the simulation closely match the theoretical calculations, validating the design and performance of the NMOS inverter.

## REFERENCES

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