4 BIT Vedic Multiplier

VLSI Lab-EC403

Under the supervison of

Dr .Vasantha MH

Presented by

SAHIL YADAV **[20ECE1039]**

RAUSHAN KUMAR **[20ECE1042]**

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

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AIM

- The main aim of this project is to design and simulation of Low power, High Performance Full adder and half adder circuit and measure different parameters 4-bit multiplier and Low-Power¸ High Performance a) 4 bit Vedic Multiplier and 4 bit multiplier using Cadence tool
- Considering their advantages and disadvantage these are compares on the basis of area, speed and delay

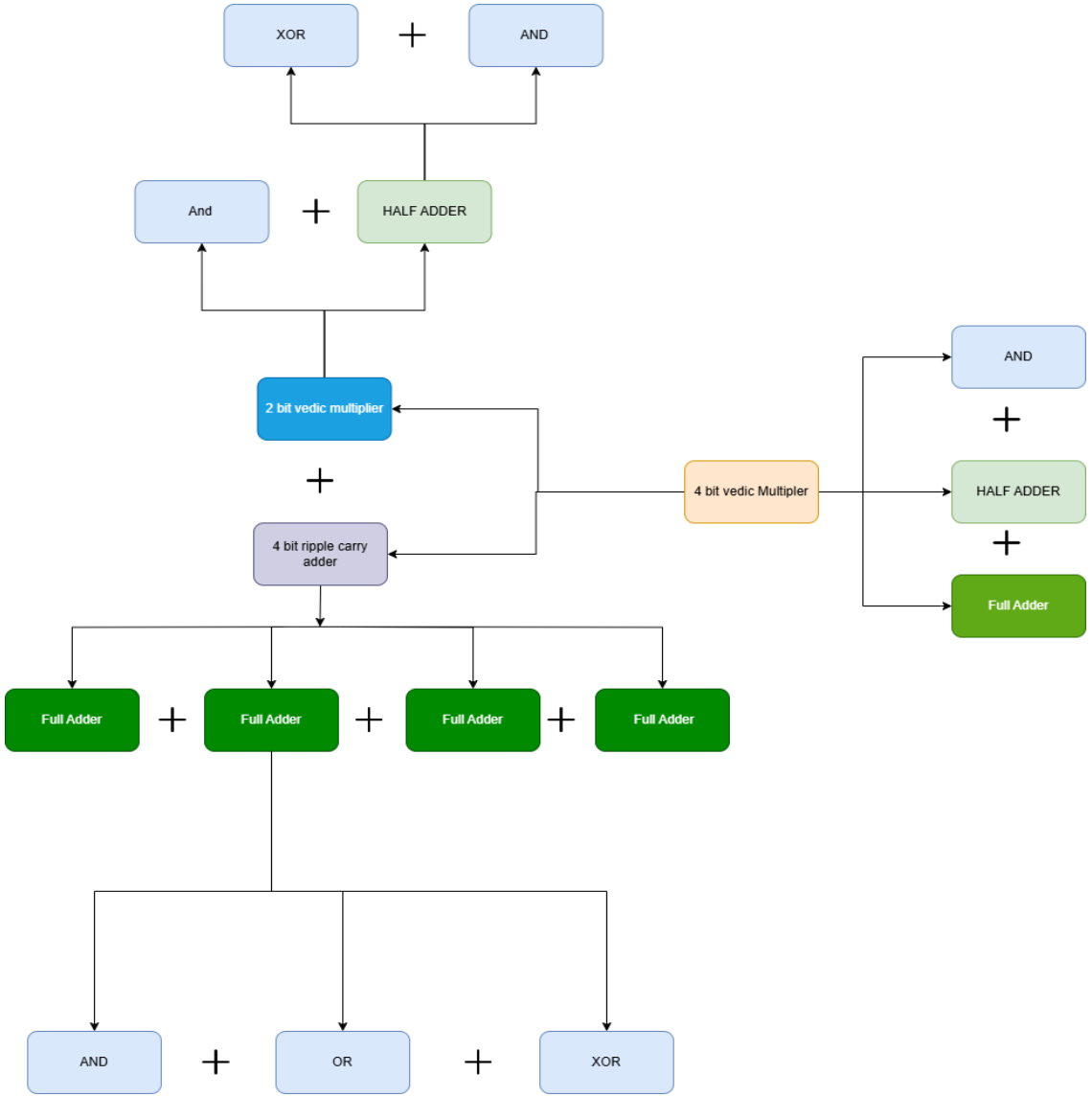
What is an Multiplier ?

- Multiplication is a mathematical operation that at its simplest is an abbreviated process of adding an integer a specified of times.
- Carries out arithmetic and logic operations on the Operands in computer .

What is Propagation Delay ?

- The average of time taken for output to change from low level to high level and high level to low level.
- $Tp = (TpHL + TpLH) / 2$

Our Approach ..?



Inverter:

$$Y=A'$$

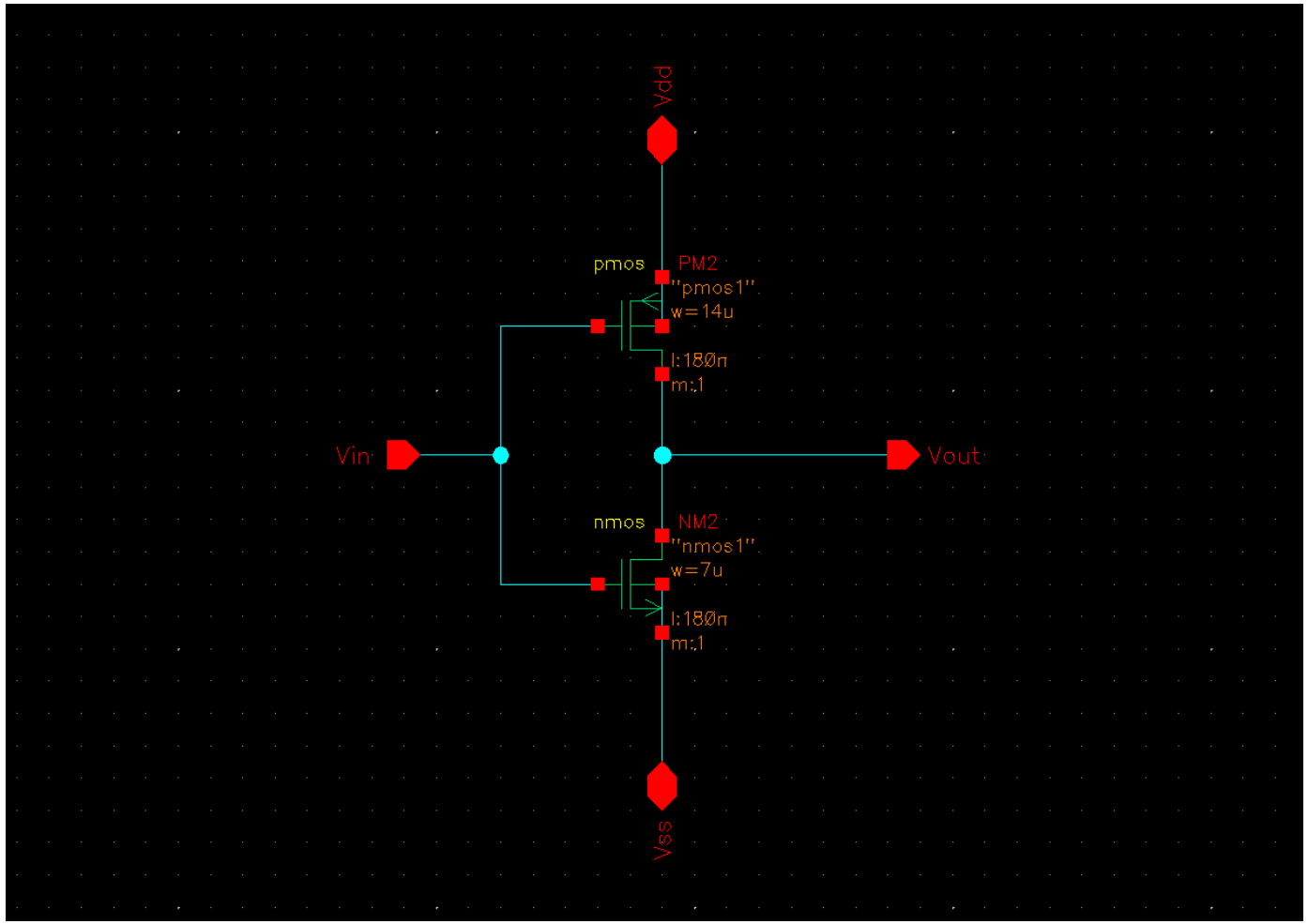


Fig-1 : Schematic of Inverter

A	Y
0	1
1	0

Delay :

$Ton=0.04ns$

$Toff=0.03ns$

$T=\frac{Ton+Toff}{2}$

$T=0.03ns$

Transistors:

2 mosfets

NAND: Y=(A.B)’

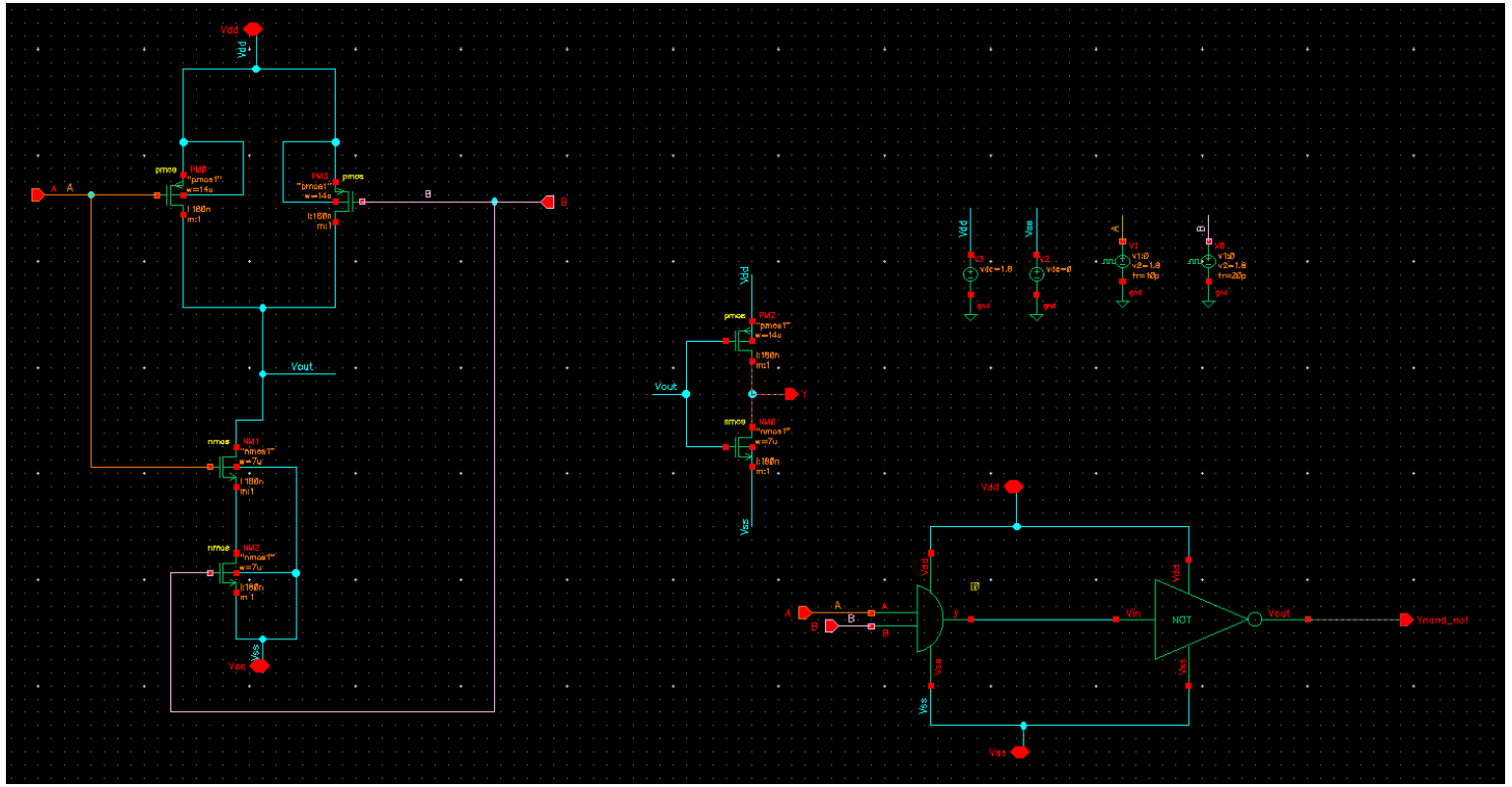


Fig-2 : Schematic of NAND

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

Delay :

$Ton = 0.06ns$

$Toff = 0.02ns$

$$T = \frac{Ton + Toff}{2}$$

$T = 0.04ns$

Transistors:

4 mosfets

AND:

$Y=A.B$

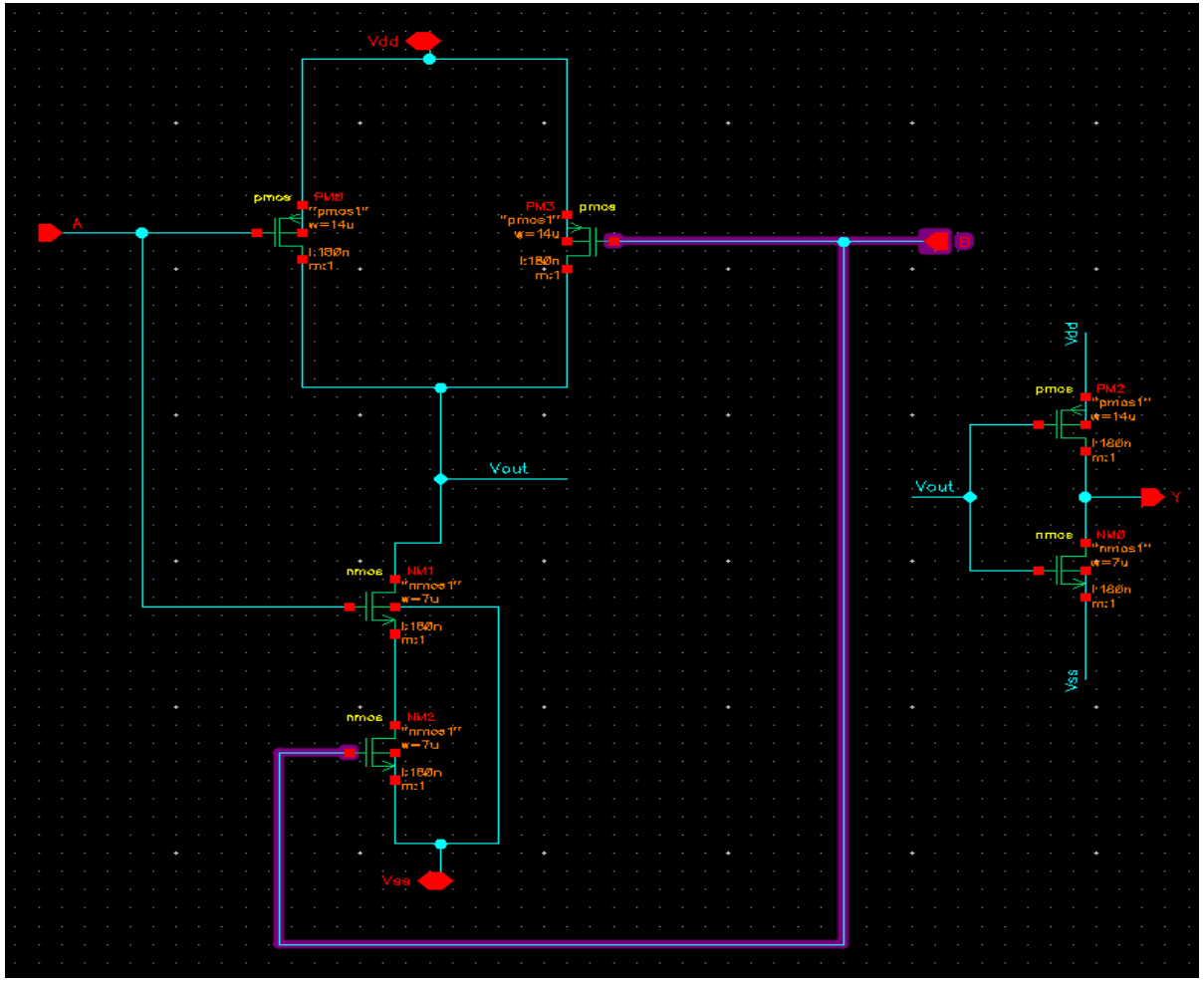


Fig-4 : Schematic of AND

A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

Delay :

$Ton=0.25ns$

$Toff=0.19ns$

$T=\frac{Ton+Toff}{2}$

$T=0.22ns$

Transistors:

6 mosfets

NOR:

$$Y=(A+B)'$$

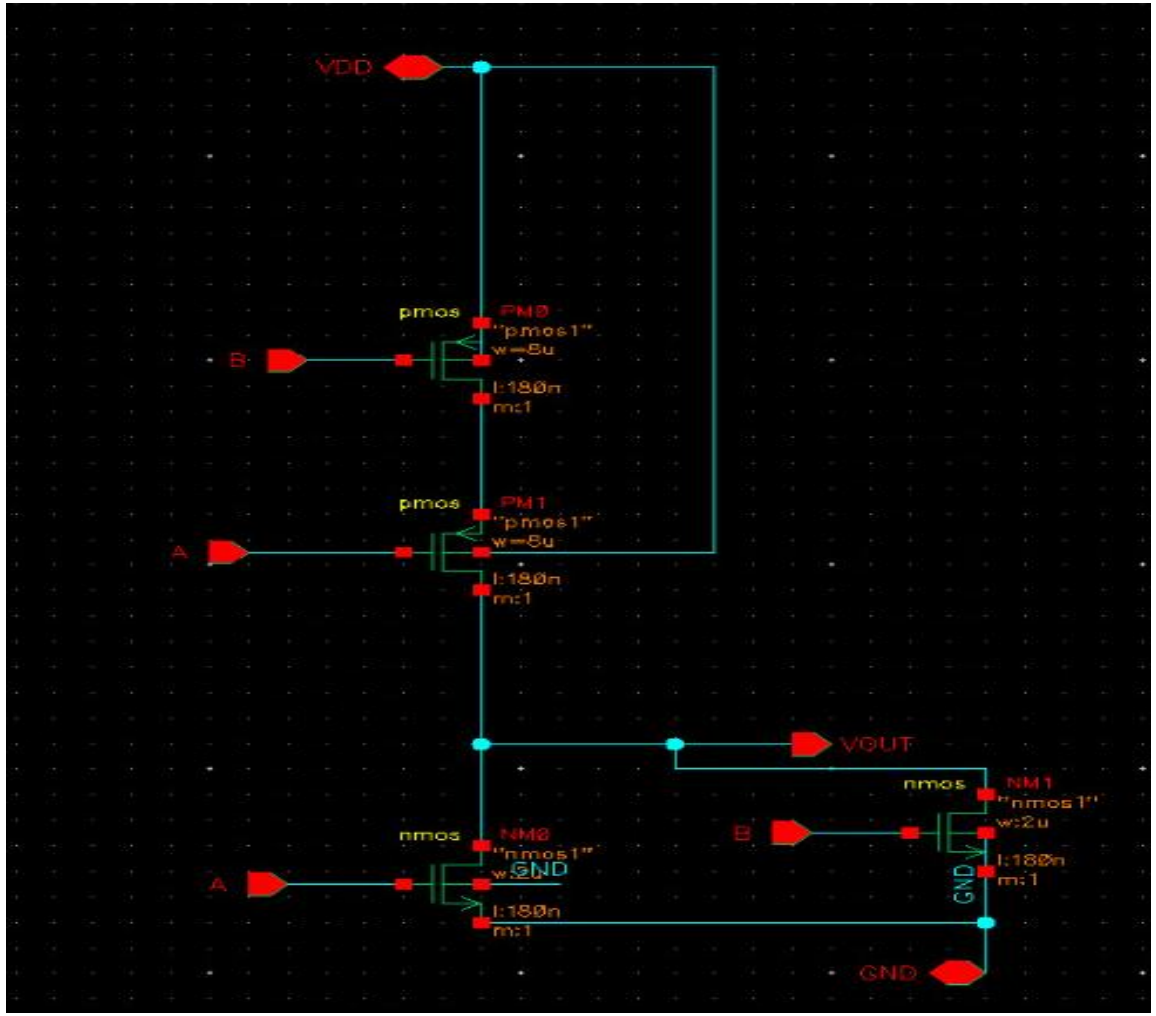


Fig-3 : Schematic of NOR

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

Delay :

$Ton=0.060ns$

$Toff=0.067ns$

$T=\frac{Ton+Toff}{2}$

$T=0.0635ns$

Transistors:

4 mosfets

OR:

$$Y=A+B$$

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

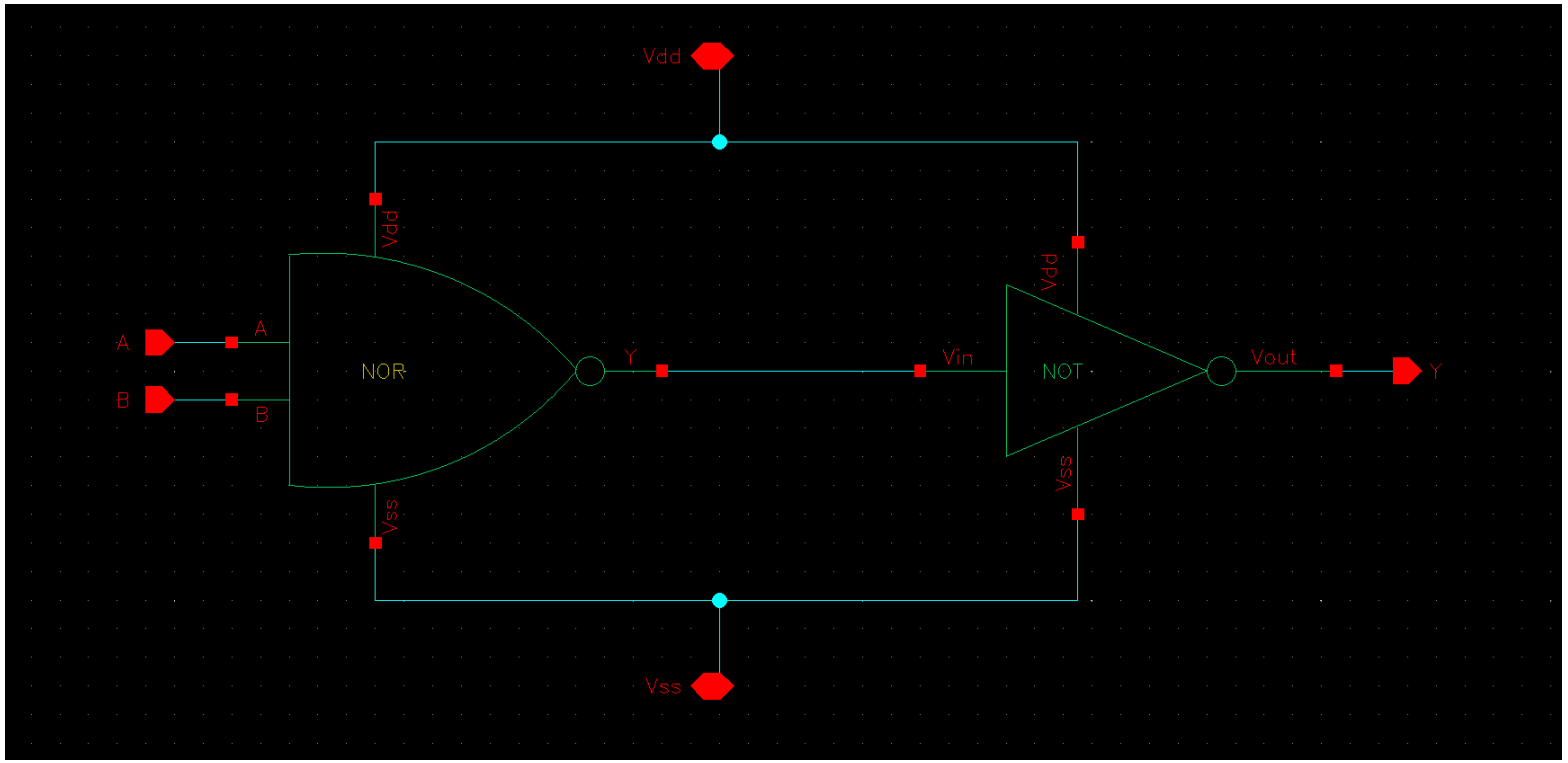


Fig-5 : Schematic of OR

Delay :

$Ton=0.3ns$

$Toff=0.25ns$

$T=\frac{Ton+Toff}{2}$

$T=0.27ns$

Transistors:

6 mosfets

XOR:

$$Y=A'B + AB'$$

A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

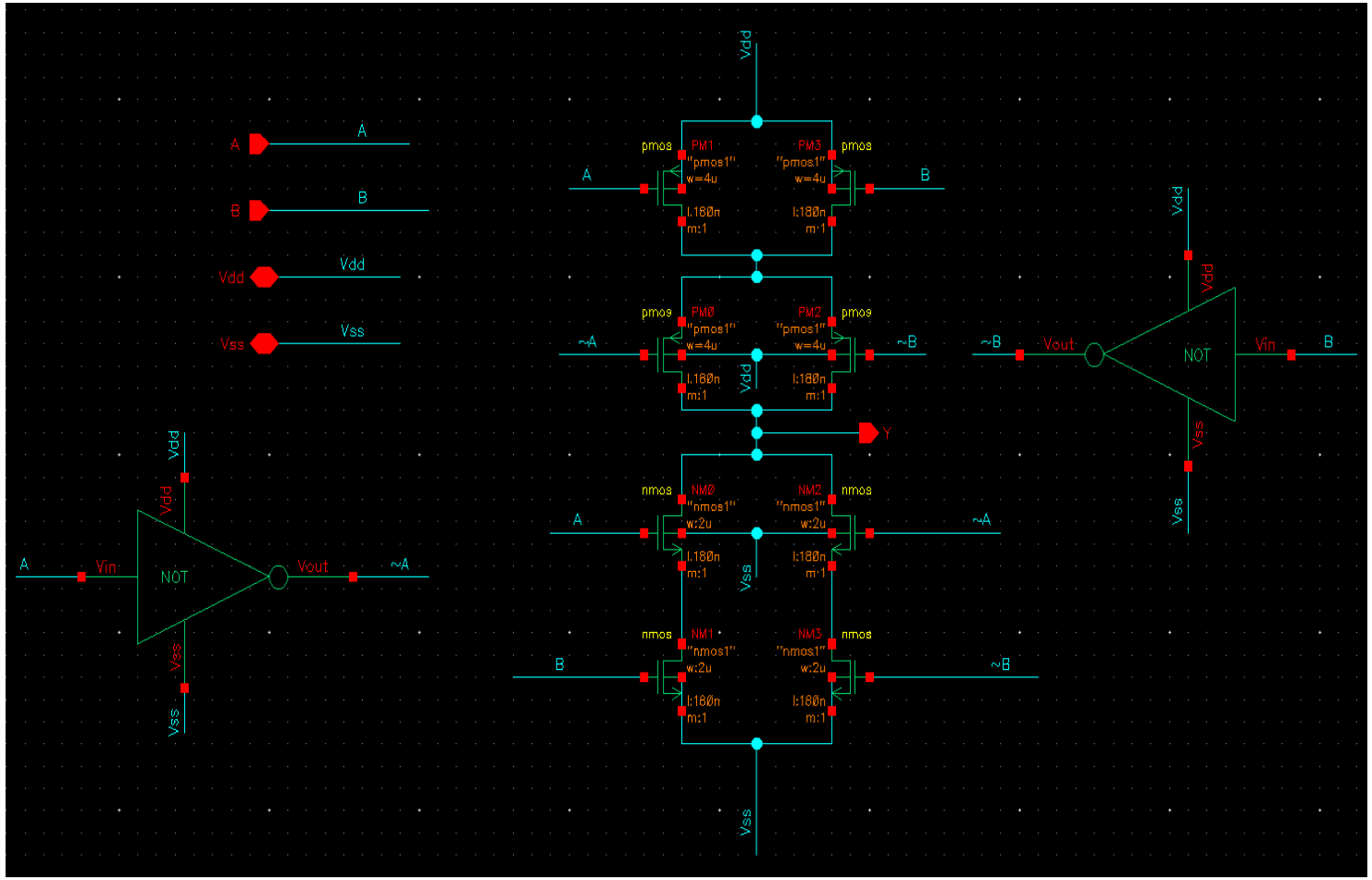


Fig-6 : Schematic of XOR

Delay :

$Ton=0.14ns$

$Toff=0.09ns$

$$T=\frac{Ton+Toff}{2}$$

$T=0.11ns$

Transistors:

12 *mosfets*

Half-Adder

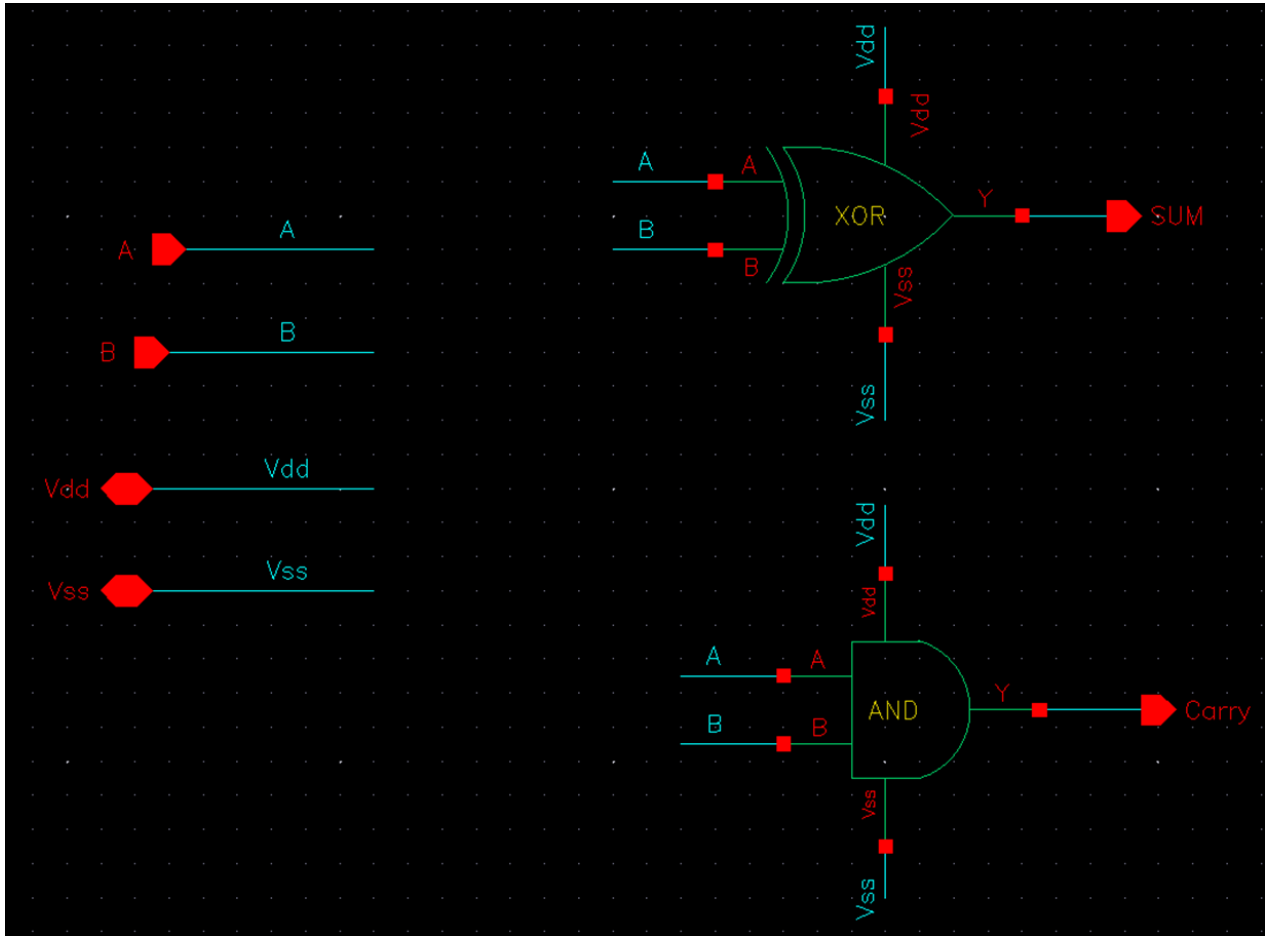


Fig-9 : Schematic of Half Adder

$$Sum = A \oplus B$$

$$Carry = A * B$$

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Transistors:

20 mosfets

Output For Half- Adder:

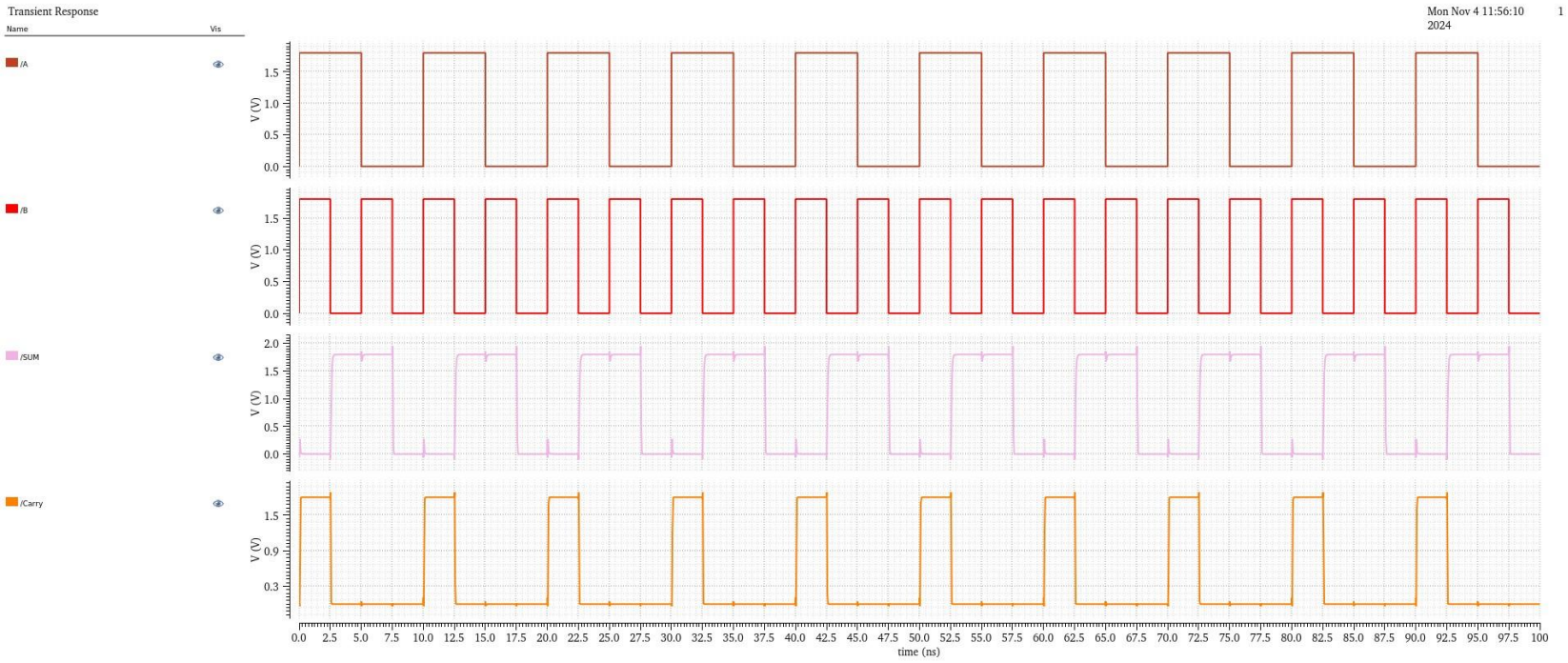


Fig-10 : Output of Half-Adder

Delay :

Sum:

$Ton=0.179ns$

$Toff=0.07ns$

$T=\frac{Ton+Toff}{2}$

$T=0.35ns$

Carry:

$Ton=0.07ns$

$Toff=0.06ns$

$T=\frac{Ton+Toff}{2}$

$T=0.065ns$

Full Adder

$S = A \oplus B \oplus Cin;$

$Cout = (A*B) + (Cin*(A \oplus B)).$

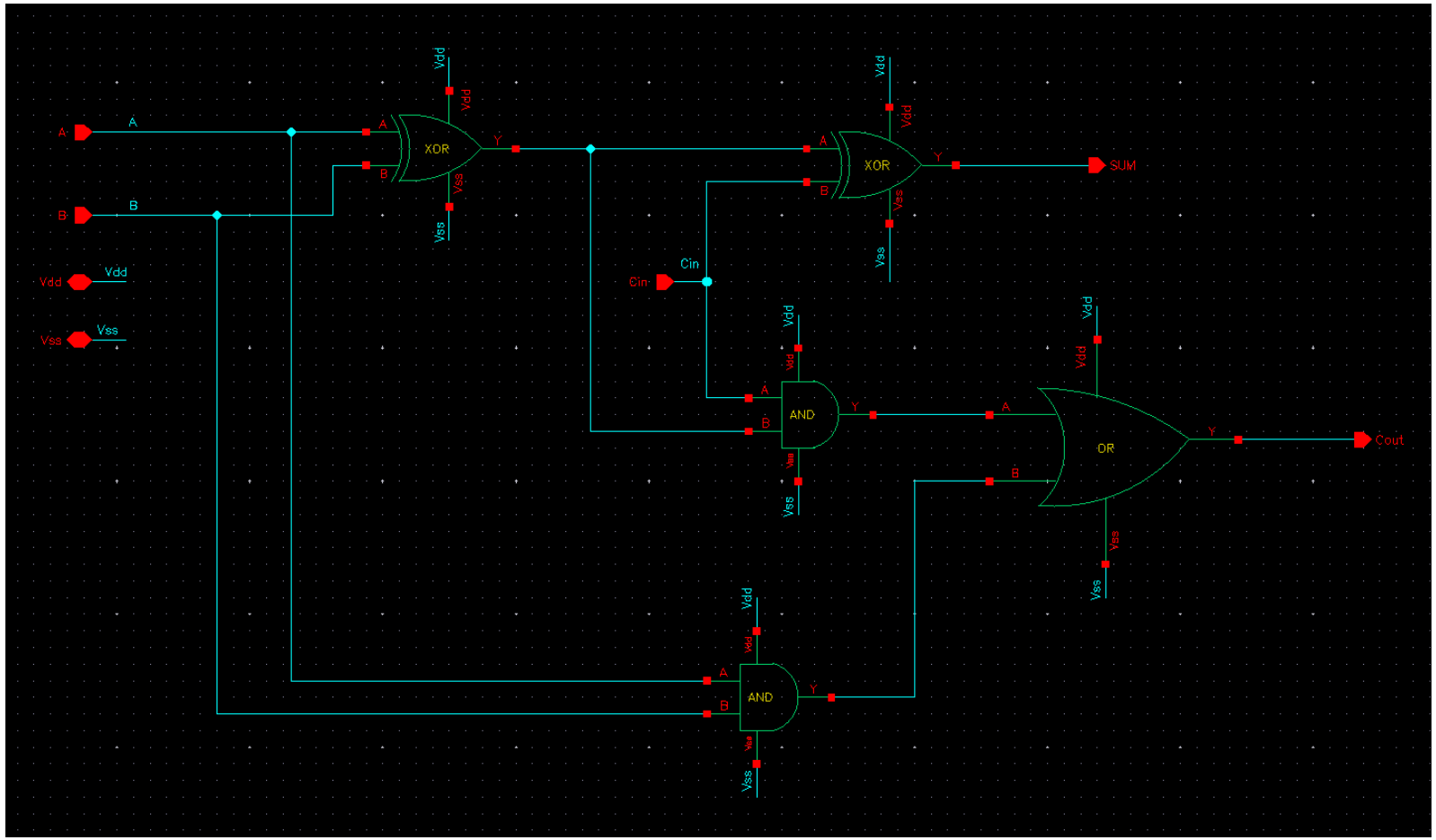


Fig-11 : Schematic of Full Adder

A	B	C	S	C0
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Transistors:

48 *mosfets*

Output For Full Adder:

Fig-12 : Output of Full Adder

Delay :

Sum:

$Ton=0.75ns$

$Toff=0.6ns$

$T=\frac{Ton+Toff}{2}$

$T=0.65ns$

Carry:

$Ton=0.15ns$

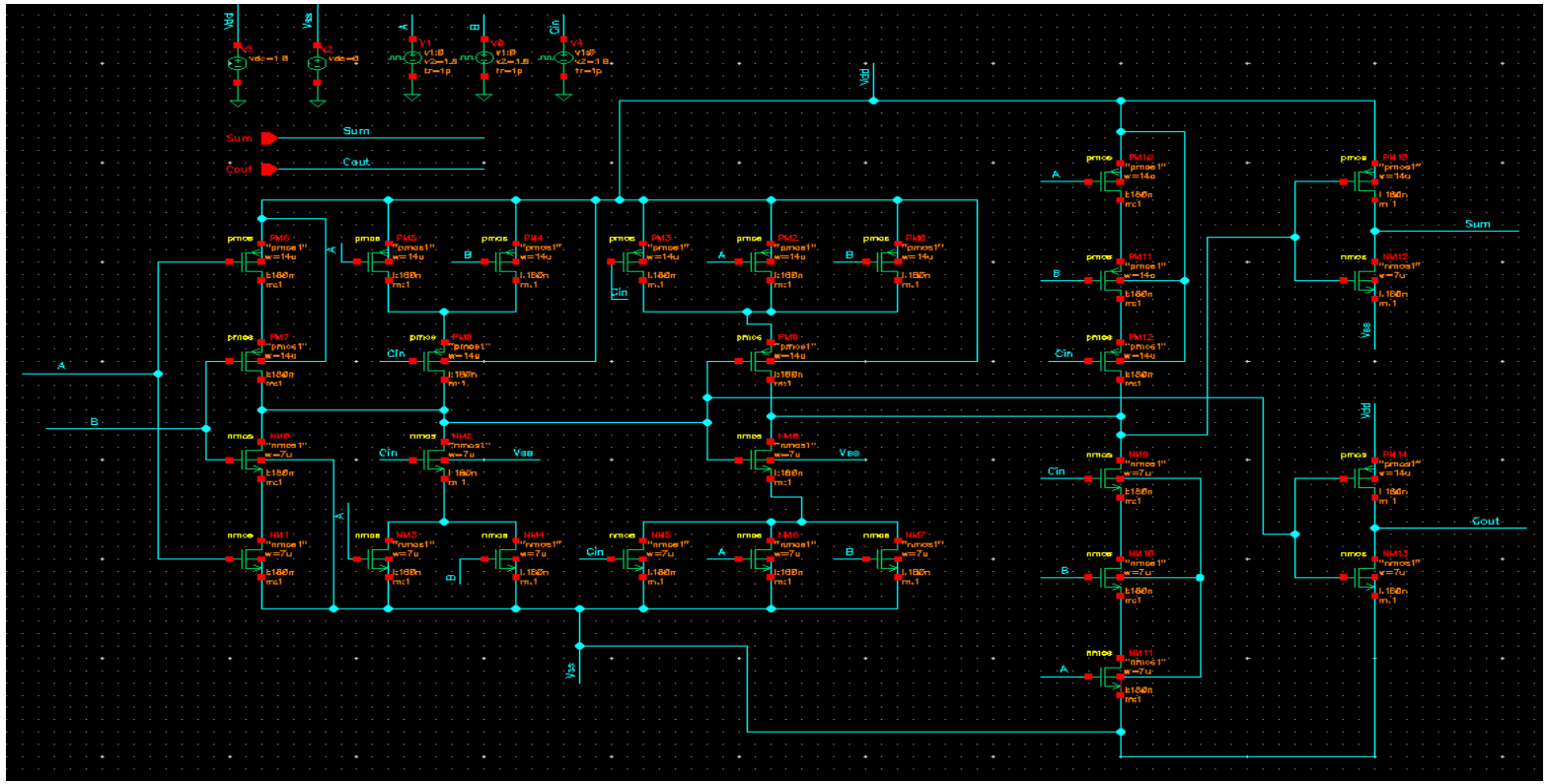
$Toff=0.2ns$

$T=\frac{Ton+Toff}{2}$

$T=0.17ns$

Full Adder Using Gates

S = A ⊕B⊕Cin;
Cout = (A*B) + (Cin*(A⊕B)).



A	B	C	S	C0
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Fig-11 : Schematic of Full Adder

Transistors:

28 mosfets

Output For Full Adder Using Gates:

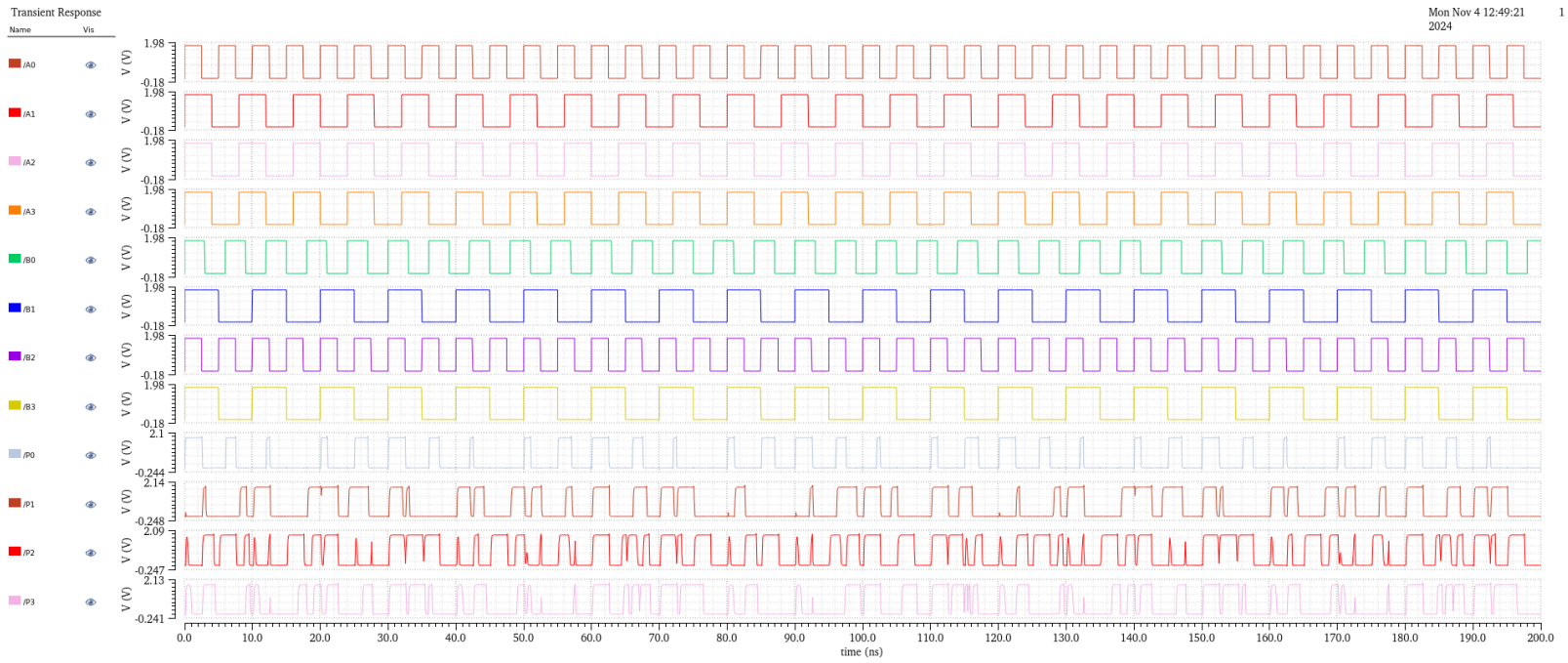


Fig-12 : Output of Full Adder

Delay :

Sum:

$Ton=0.208ns$

$Toff=0.477ns$

$T=\frac{Ton+Toff}{2}$

$T=0.3425ns$

Carry:

$Ton=0.075ns$

$Toff=0.0069ns$

$T=\frac{Ton+Toff}{2}$

$T=0.072ns$

4 Bit Multiplication Algorithm

```
                                  b7   b6   b5   b4   b3   b2   b1   b0
                                  a7   a6   a5   a4   a3   a2   a1   a0
-------------------------------------------------------------------------
                             a0b7 a0b6 a0b5 a0b4 a0b3 a0b2 a0b1 a0b0
                        a1b7 a1b6 a1b5 a1b4 a1b3 a1b2 a1b1 a1bo
                   a2b7 a2b6 a2b5 a2b4 a2b3 a2b2 a2b1 a2b0 c0
              a3b7 a3b6 a3b5  a3b4 a3b3 a3b2 a3b1 a3b0 c1
         A4b7 a4b6 a4b5 a4b4 a4b3 a4b2 a4b1 a4b0 c2
    a5b7 a5b6 a5b5 a5b4 a5b3 a5b2 a5b1 a5b0 c3
a6b7 a6b6 a6b5 a6b4 a6b3 a6b2 a6b1 a6b0  c4
a7b7 a7b6 a7b5 a7b4 a7b3 a7b2 a7b1 a7b0 c5
c14  c13  c12  c11  c10  c9   c8   c7   c6
-------------------------------------------------------------------------
S15  S14  S13  S12  S11  S10  S9   S8   S7   S6   S5   S4   S3   S2   S1   S0
```

4 Bit Normal Multiplier:

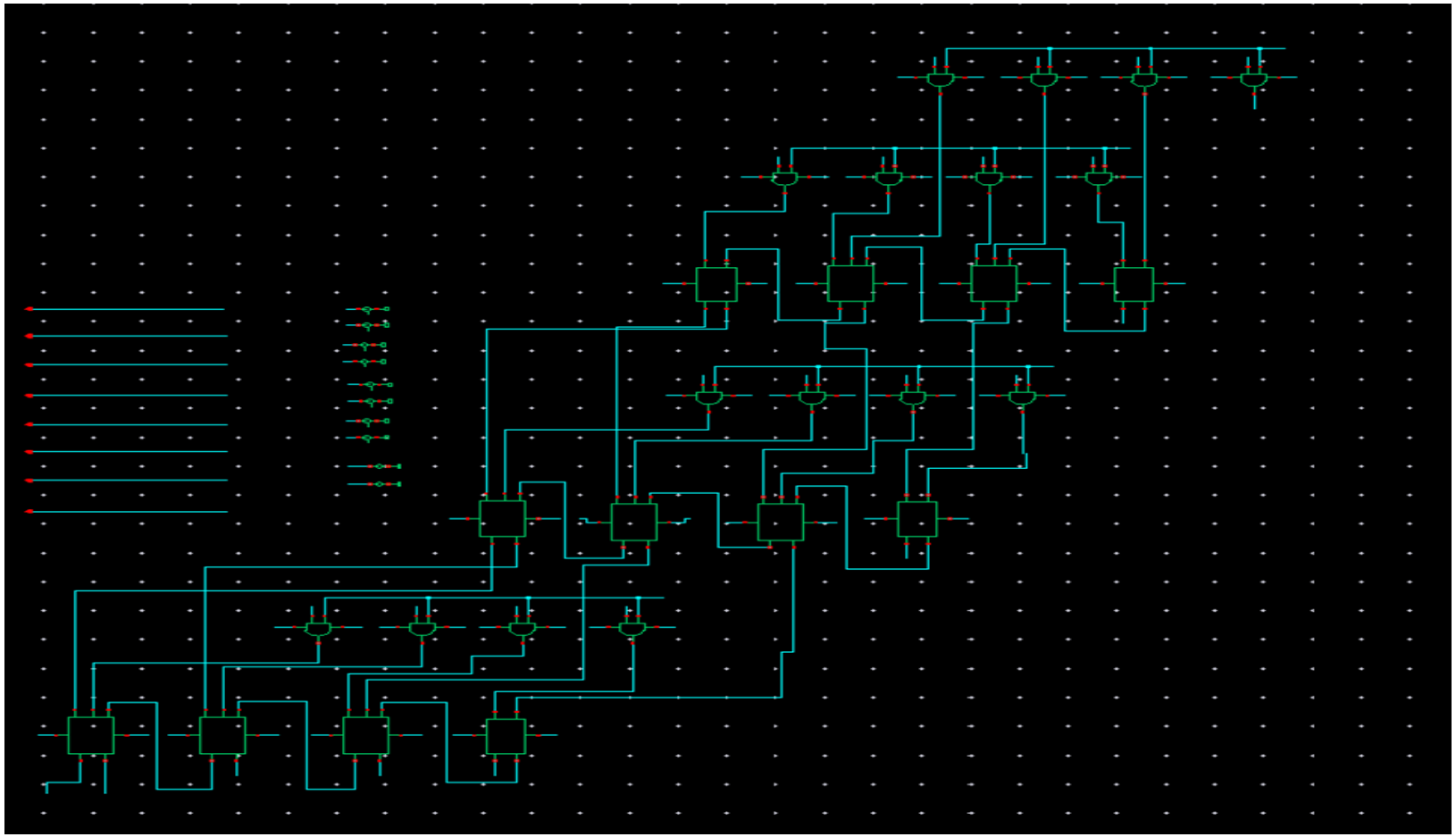


Fig-6 : 4 Bit Normal Multiplier

Delay :

$Ton=0.14ns$

$Toff=0.09ns$

$T=\frac{Ton+Toff}{2}$

$T=0.11ns$

Transistors:

400 *mosfets*

Output For 4 Bit Multiplier :

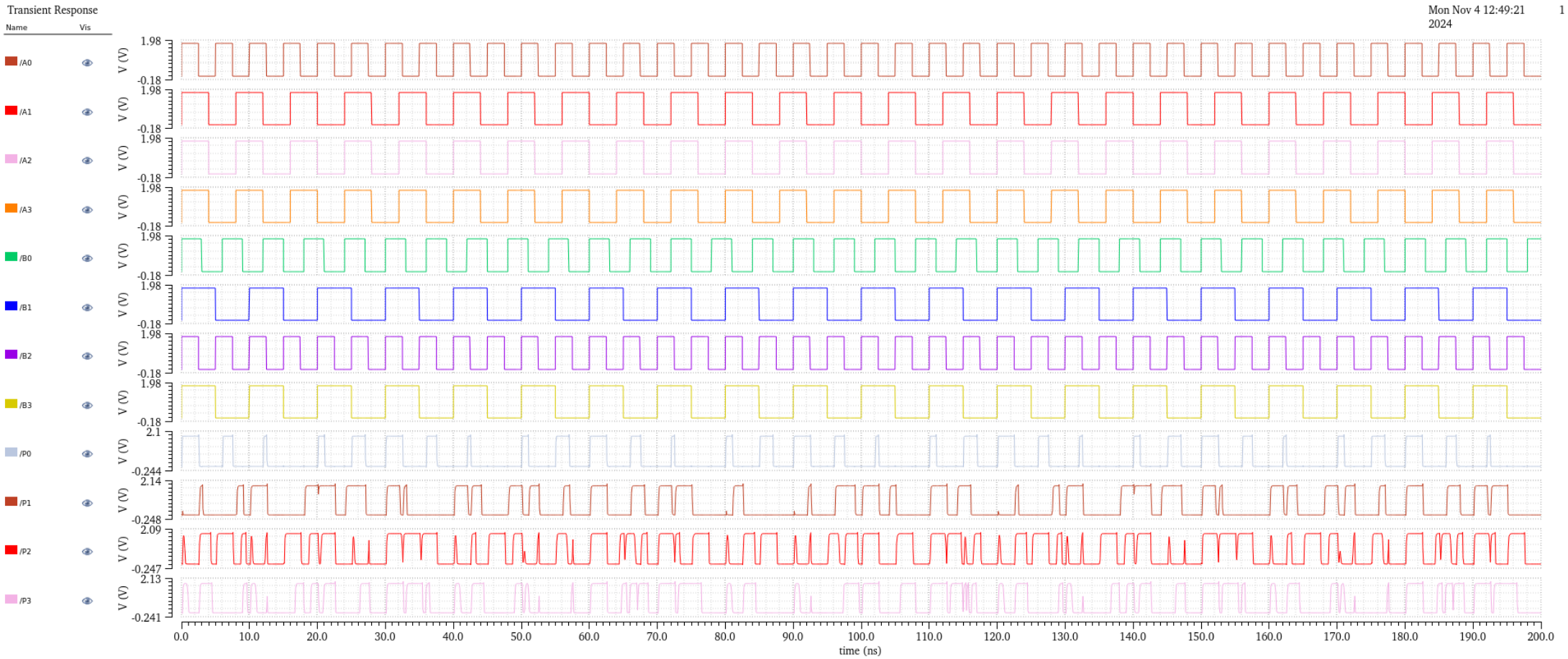


Fig- 37: Output of 4 Bit Multiplier

4 Bit Vedic Multiplication Algorithm

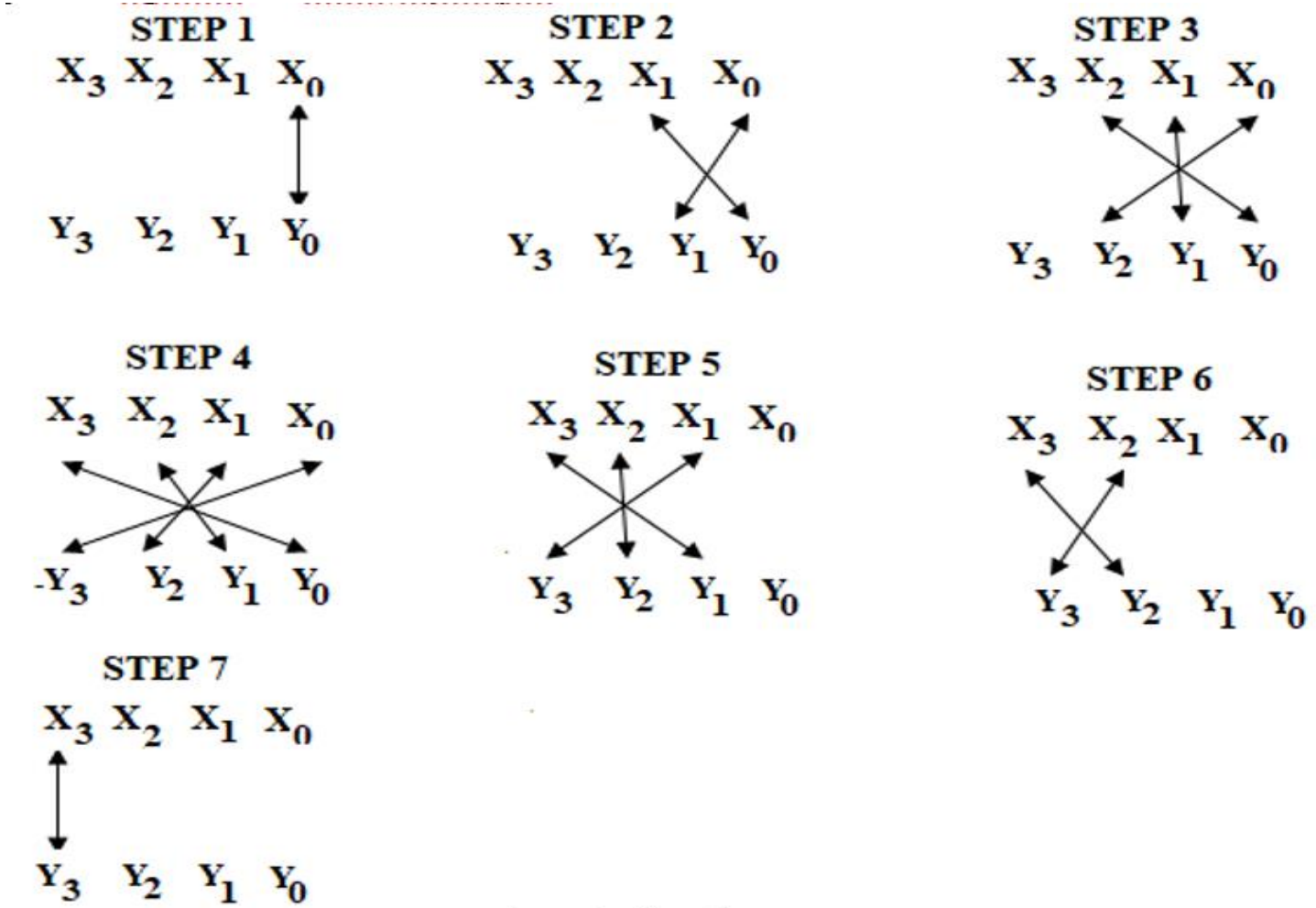


Fig2: Algorithm of UT sutra

4 Bit Vedic Using Gates:

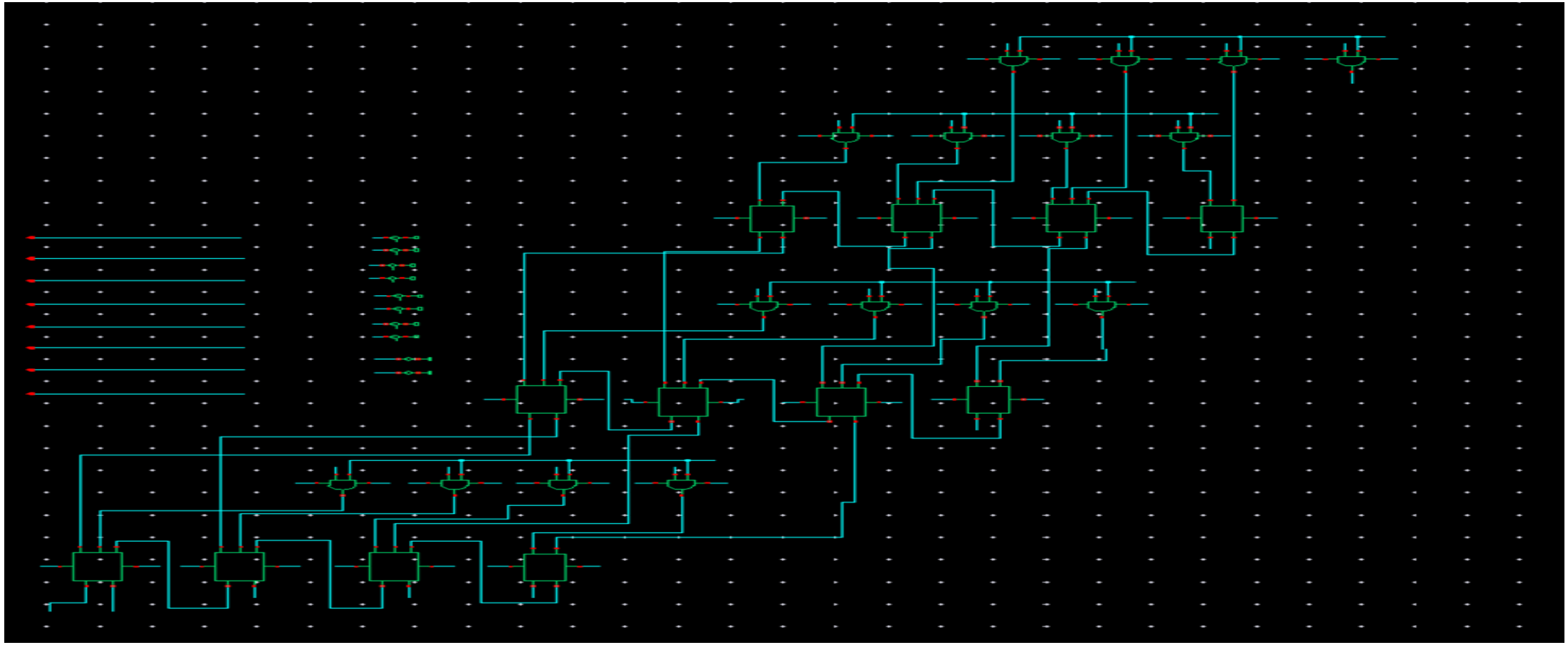


Fig-6 : 2 Bit Vedic Multiplier

Output For 4 Bit Vedic Using Gates:

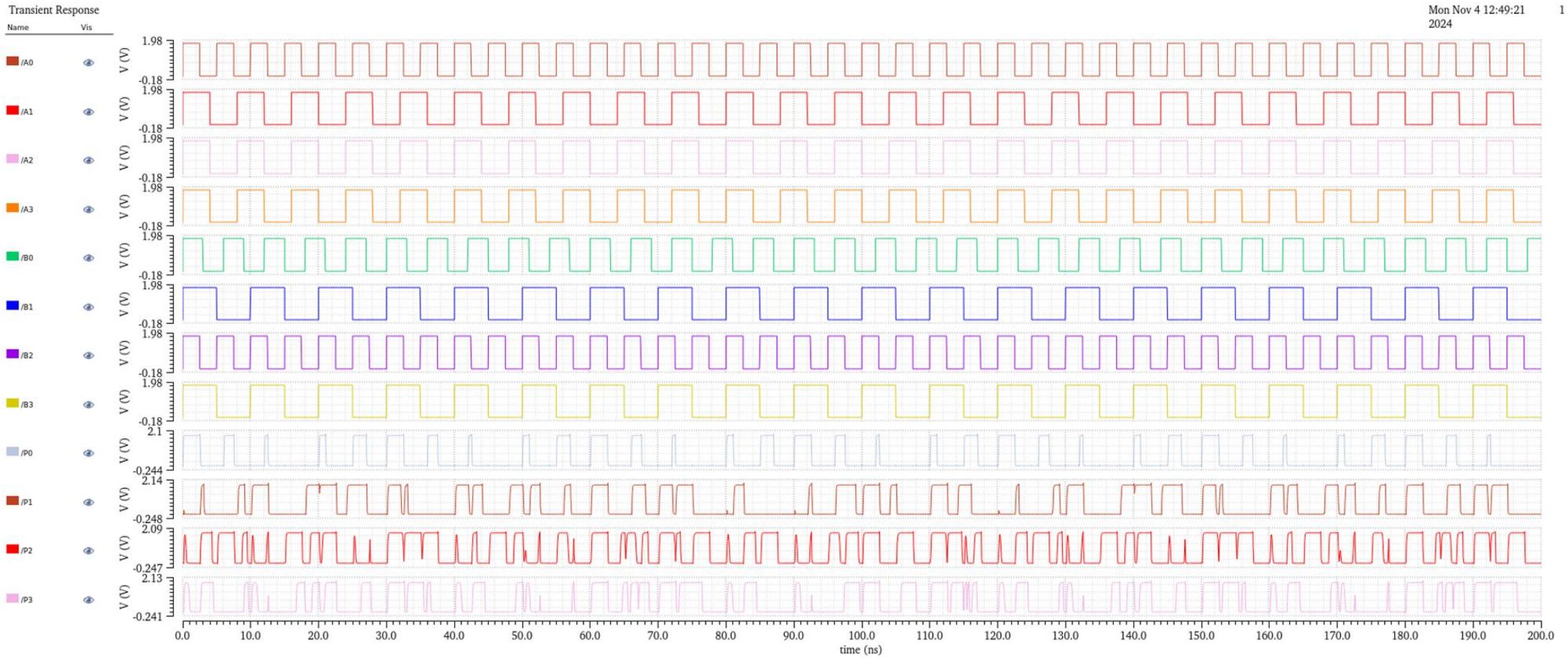
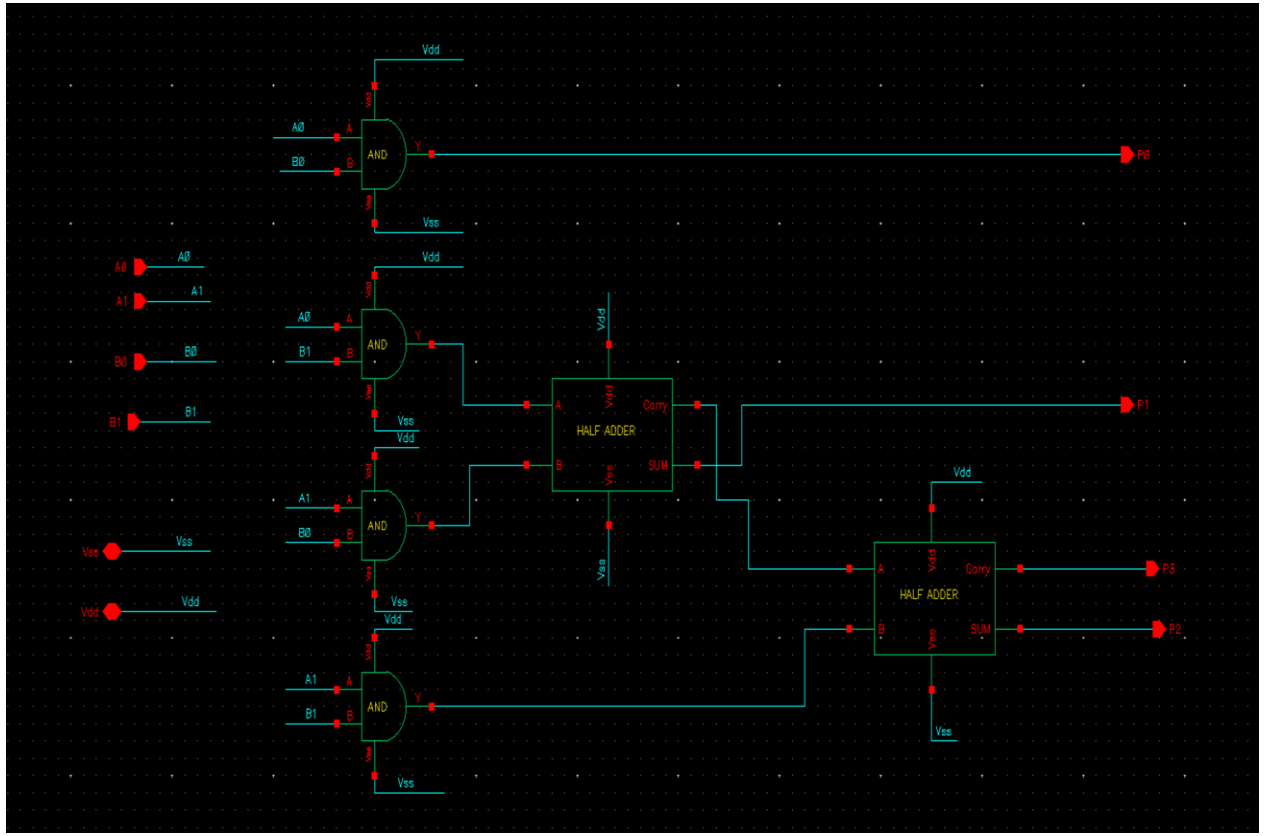


Fig- 37: Output of 8 Bit Multiplier

2 Bit Vedic Multiplier:



Delay :

$Ton = 0.0344ns$

$Toff = 0.107ns$

$T = \frac{Ton + Toff}{2}$

$T = 0.55ns$

Transistors:

64 *mosfets*

Fig-6 : 2 Bit Vedic Multiplier

Output For 2 Bit Vedic Multiplier :

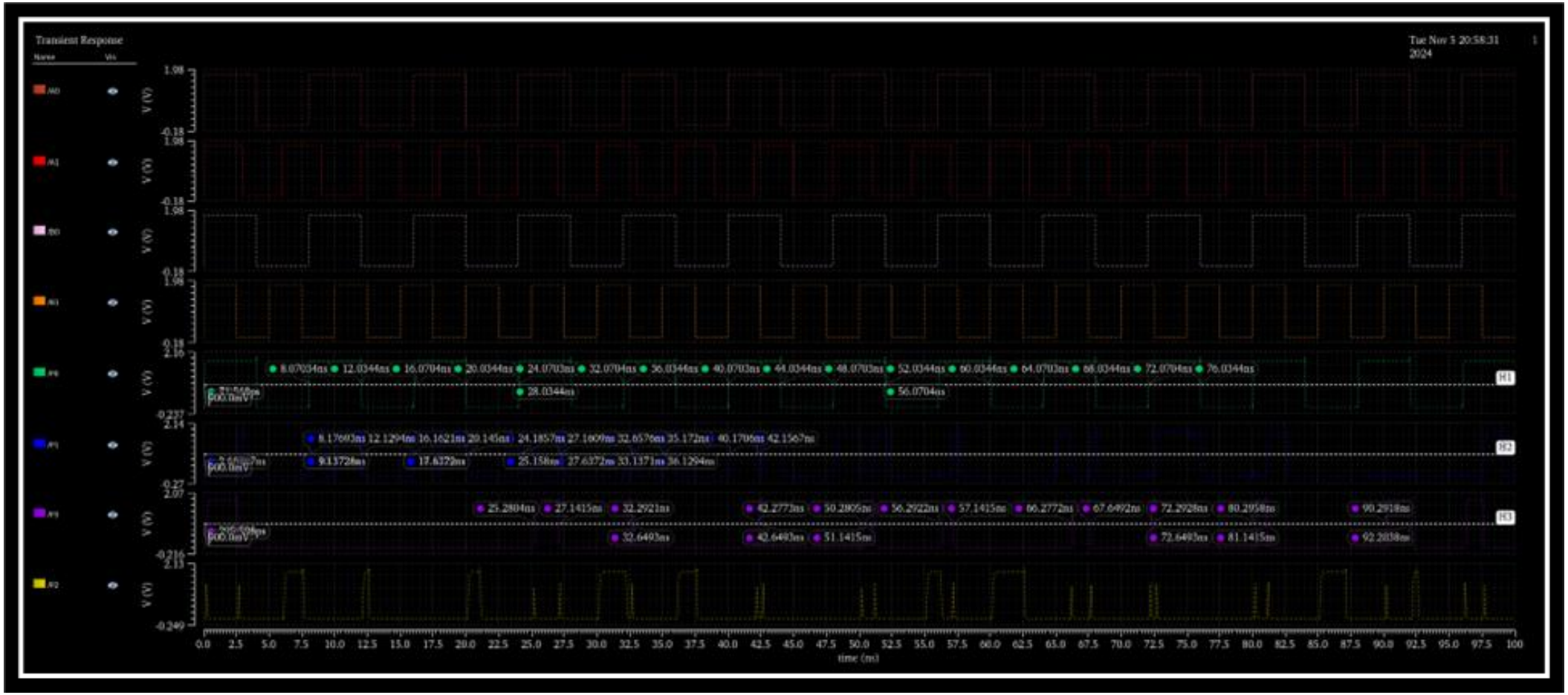


Fig- 37: Output of 2 Bit Multiplier

4 Bit RC Adder

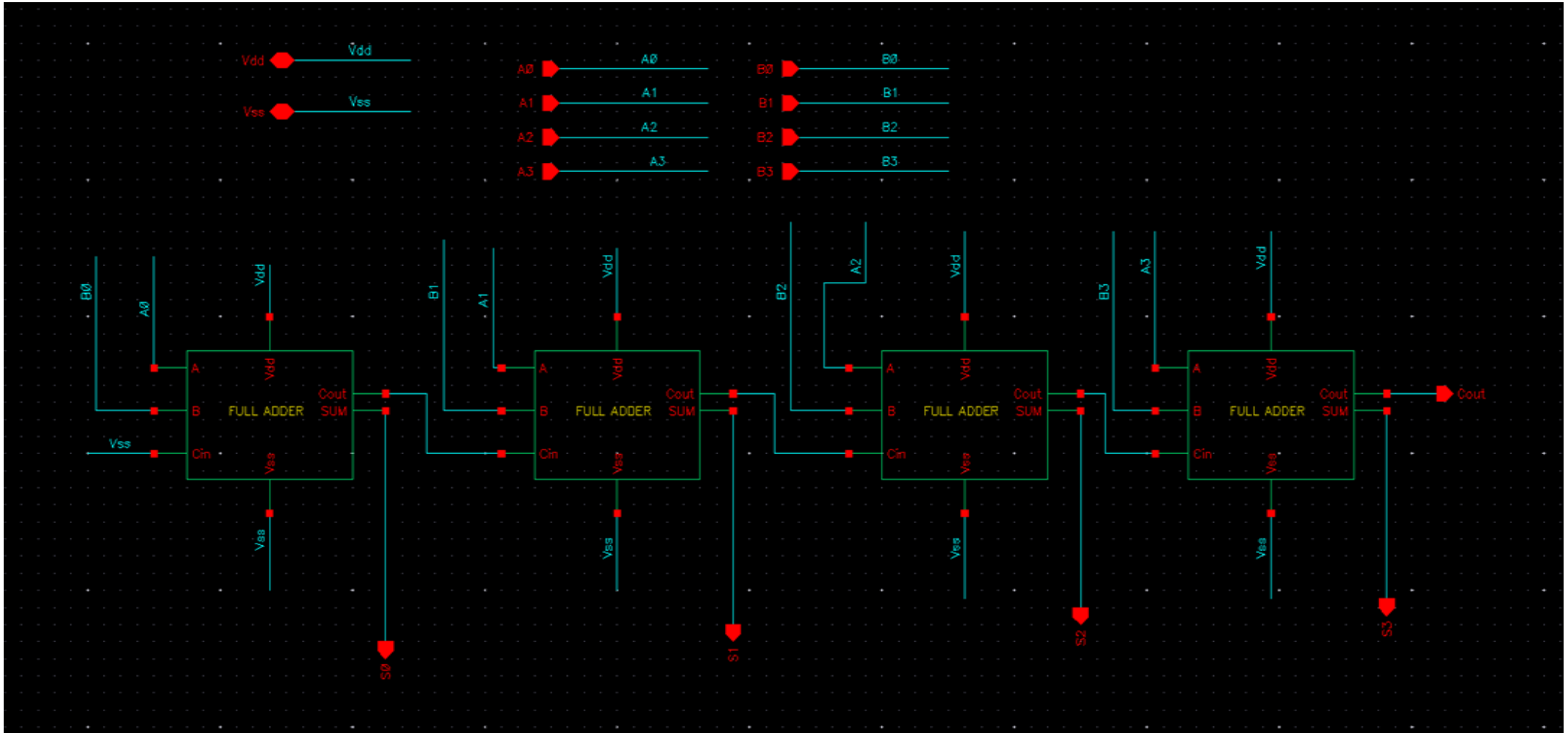
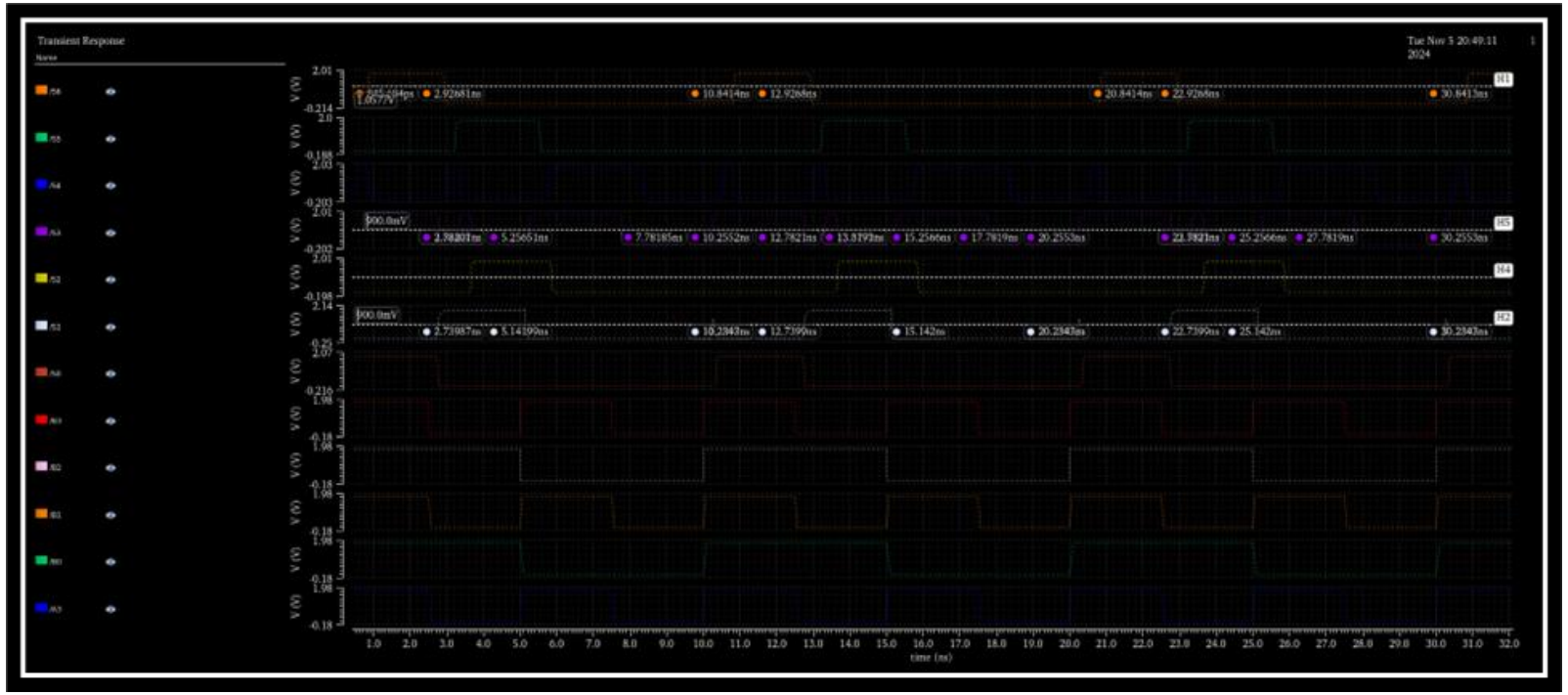


Fig-15 : Schematic of Adder

Output For 4 Bit RC Adder :



Delay :

$Ton = 1.02ns$

$Toff = 0.5ns$

$T = \frac{Ton + Toff}{2}$

$T = 0.75ns$

Transistors:

112 *mosfets*

Fig-16 : Output of 4 Bit Adder

4 Bit Vedic Multiplier Using RCA

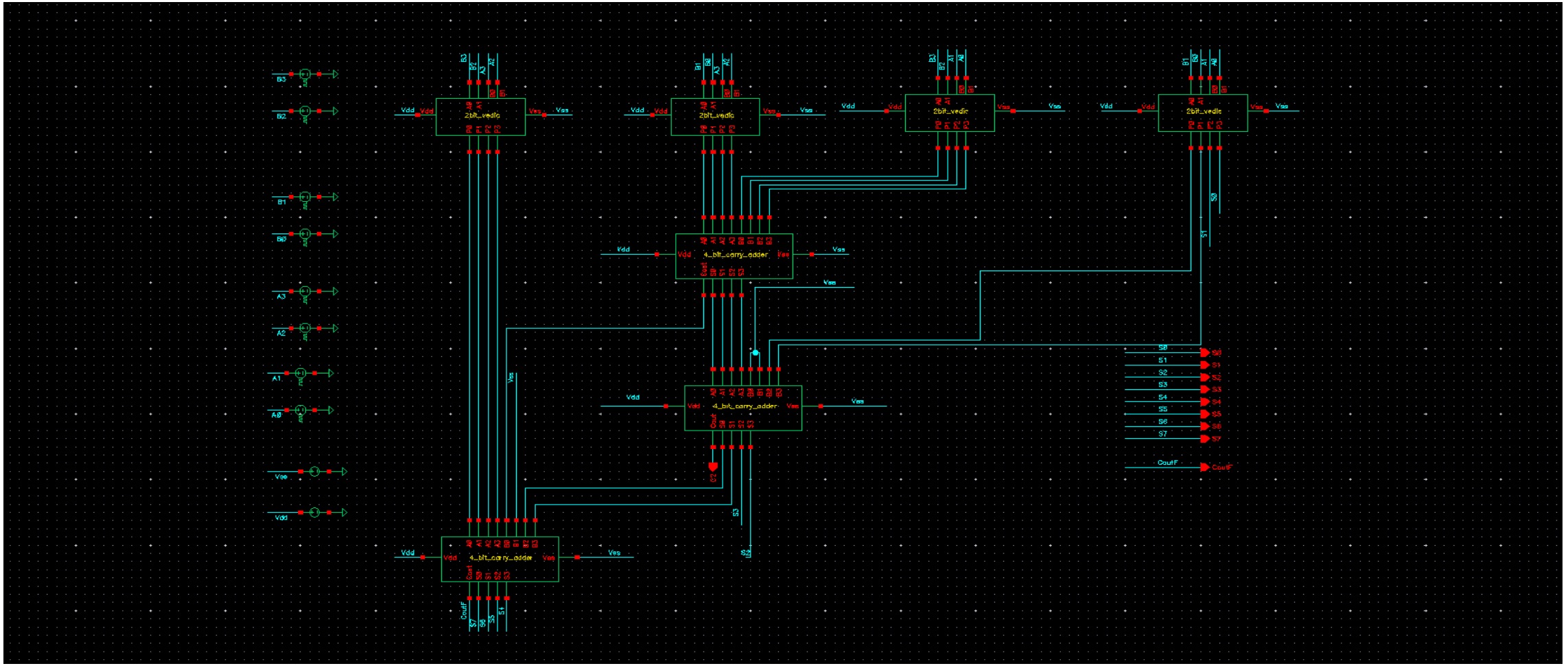
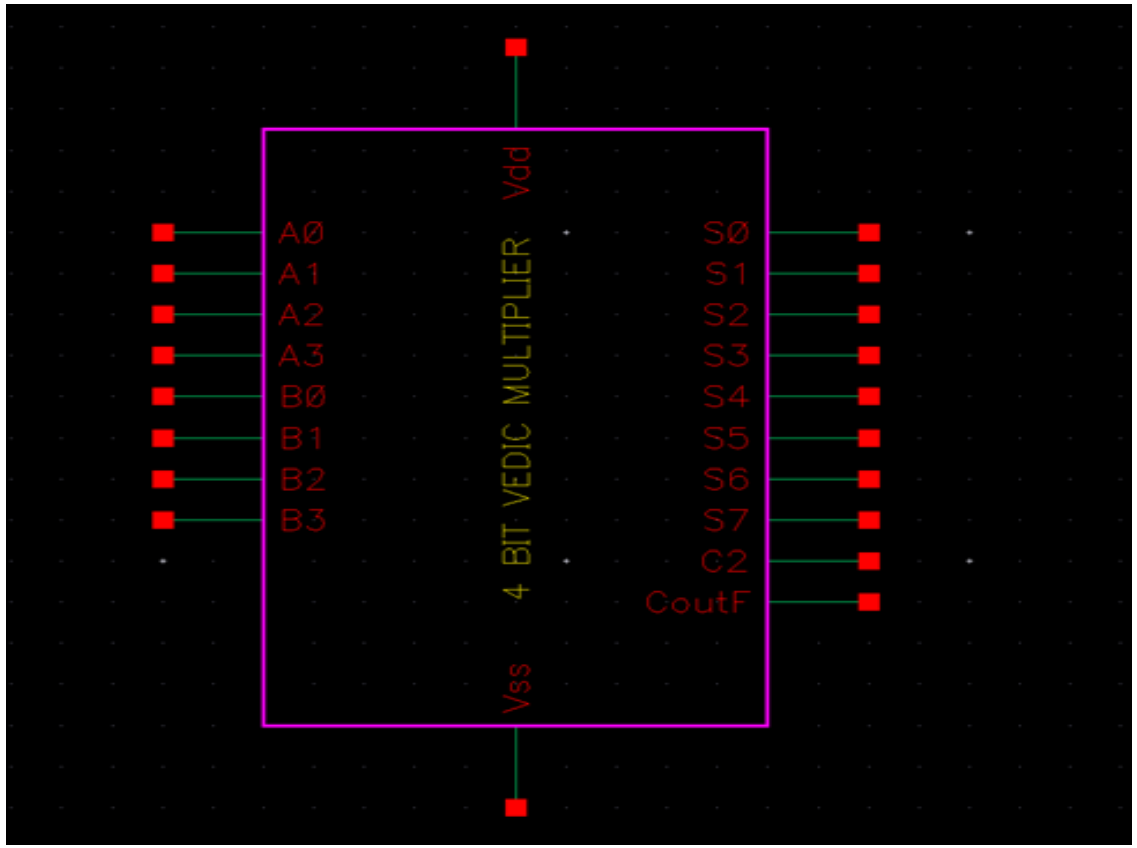


Fig-36 : Schematic of Multiplication

4 Bit Vedic Multiplier:



Delay :

$Ton=1.02ns$

$Toff=0.82ns$

$T=\frac{Ton+Toff}{2}$

$T=0.92ns$

Transistors:

592 mosfets

Fig-6 : Symbol of 4 Bit Vedic Multiplier

Output For 4 Bit Vedic Using RCA Part1 :

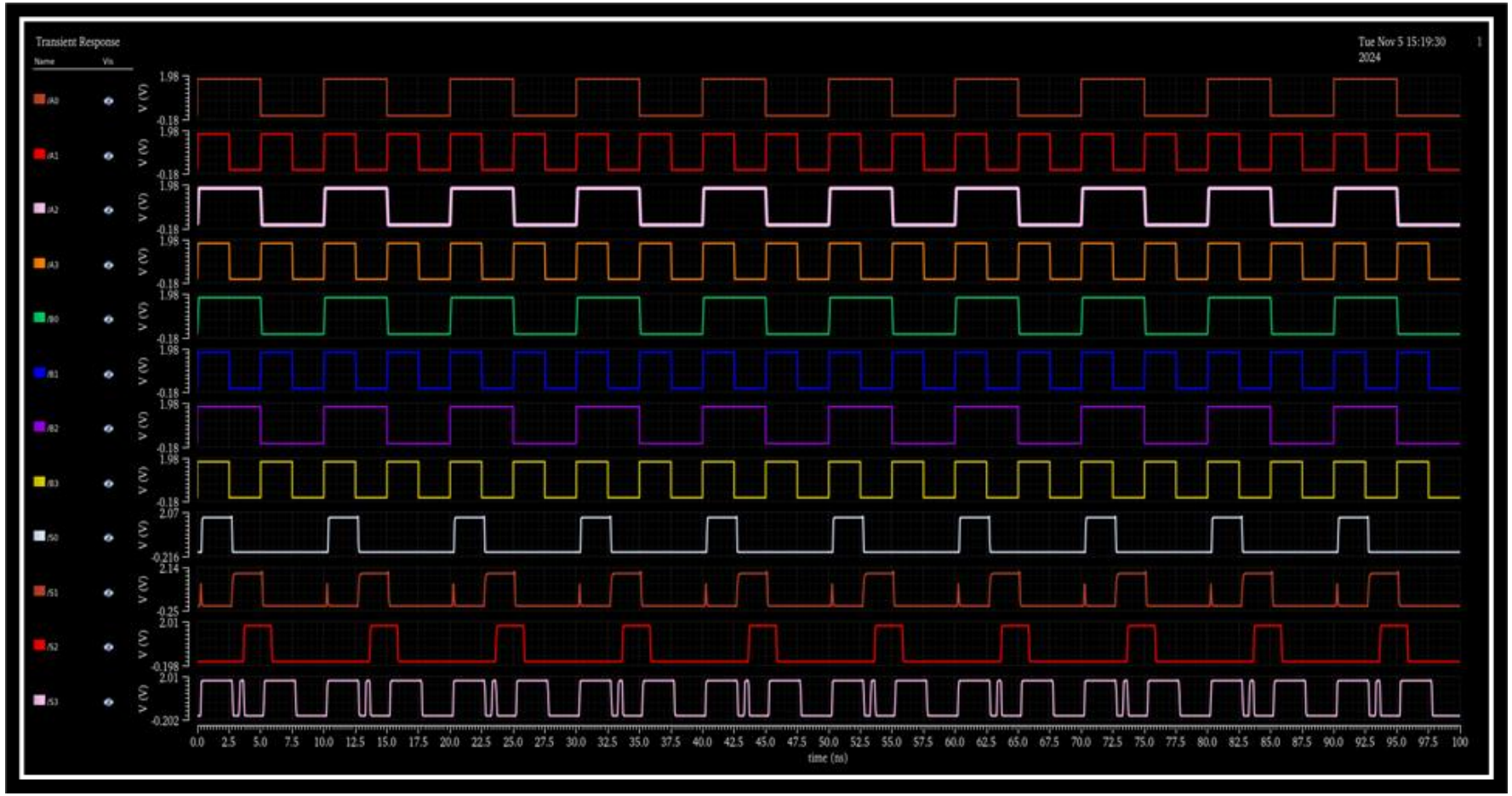


Fig- 37: Output of 8 Bit Multiplier

Output For 4 Bit Vedic Using RCA Part2 :

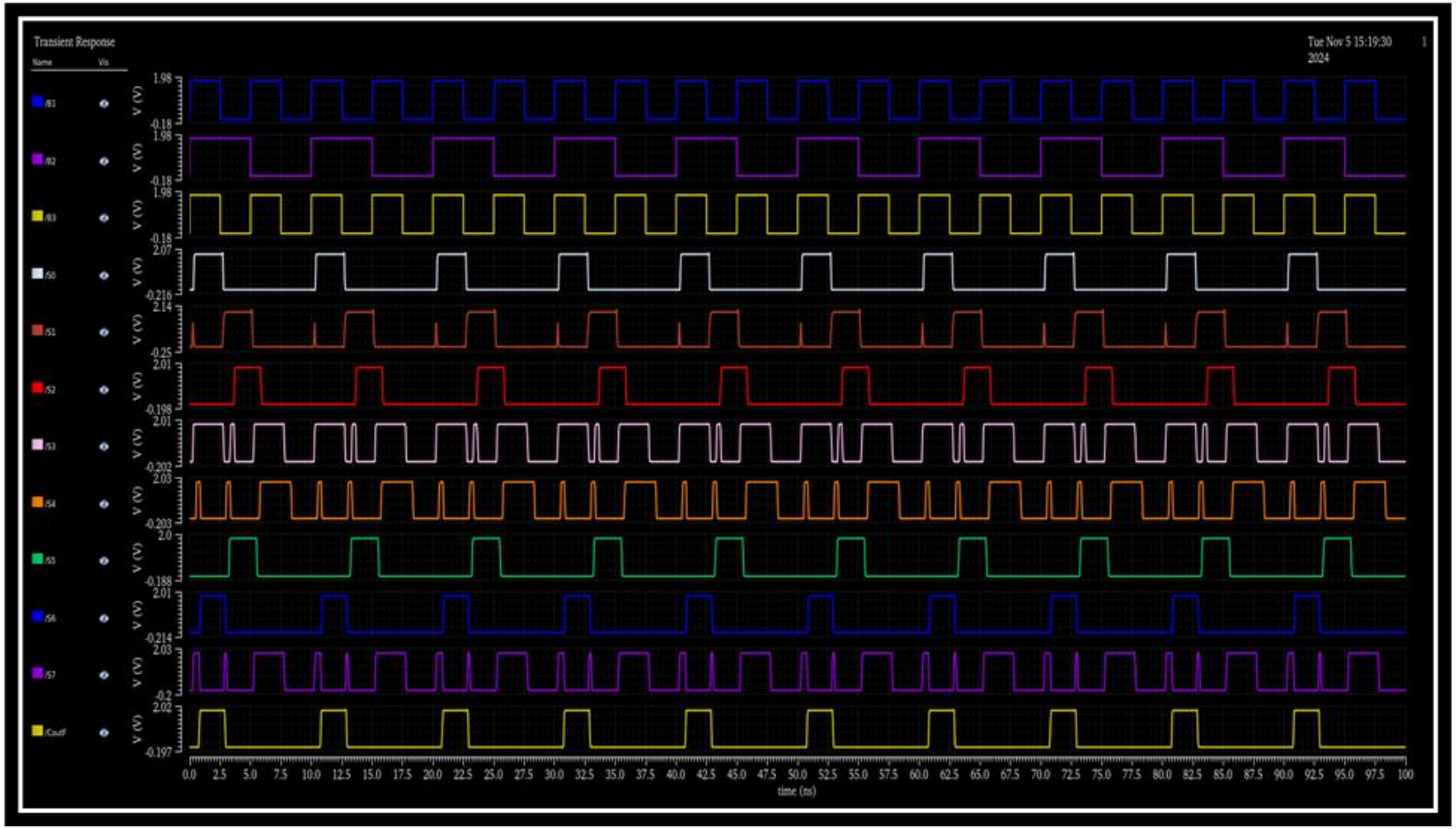
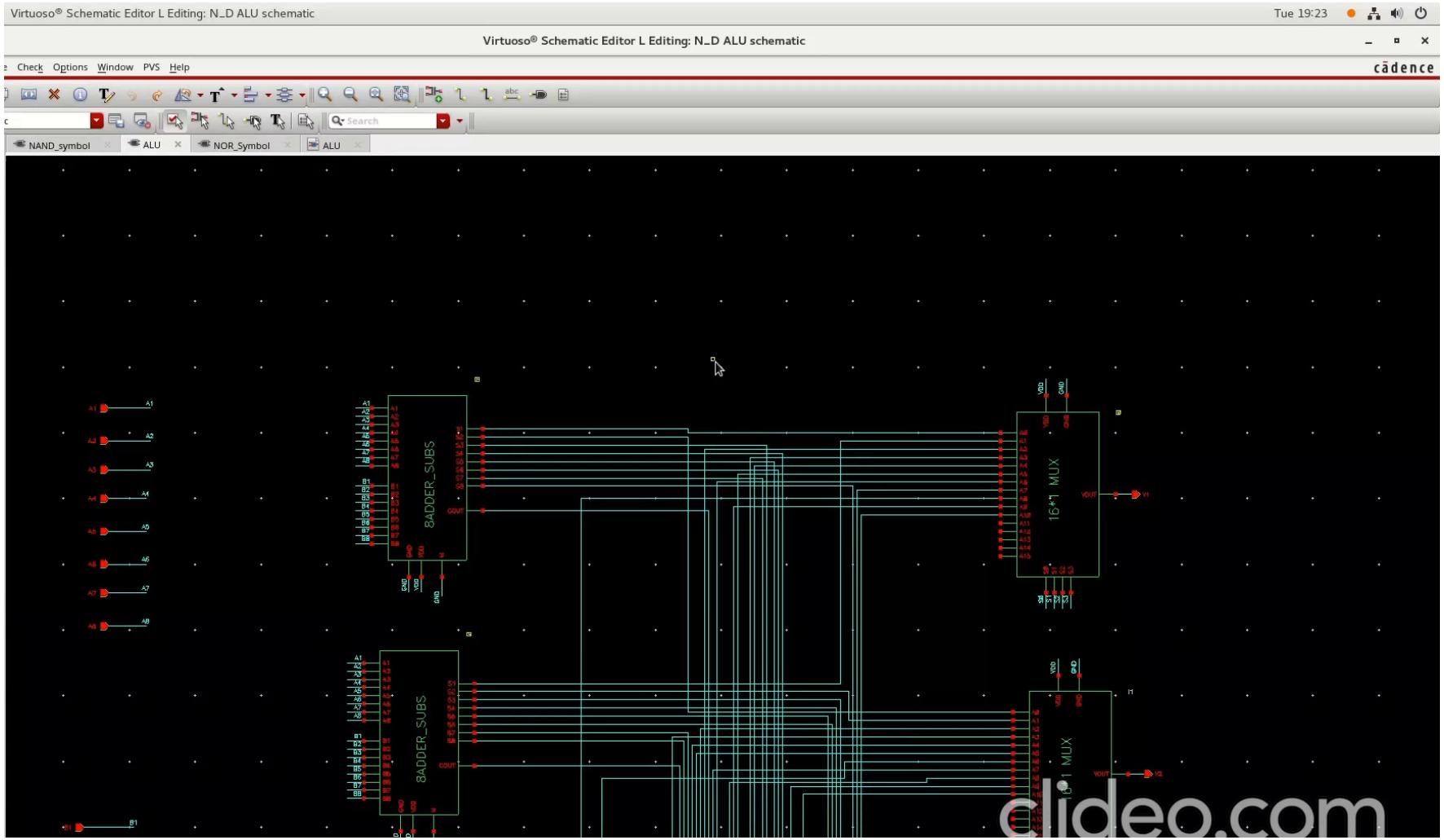


Fig- 37: Output of 8 Bit Multiplier

4 Bit Vedic Multiplier Demo Video :



COMPARISON

Parameter	Delay (ns)	Power (µW)	PDP (pJ)
Inverter	0.03	13.3	0.399
NAND Gate	0.24	18.72	4.492
AND Gate	0.22	28.32	6.23
OR Gate	0.27	32.18	8.688
XOR Gate	0.11	42.53	4.67
Half Adder	0.35	84.82	29.6
Full Adder	0.65	220.41	143.19
2-bit vedic Multiplier	0.5	140.58	70.25
4 -bit VedicType 1	1.43	1429	2043.47
4 -bit Vedic Type 2	0.92	1138	1046.96

APPLICATIONS

- It is used in DSP applications
- It is used for filters and Fourier Transform
- It is also used in ALU
- Embedded Systems
- Communications system in QAM , OFDM
- Machine Learning Matrix Multiplication
- Control System Controller design

Thank You….!