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4 BIT VEDIC MULTIPLICATION USING THRESHOLD LOGIC MEMRISTIVE CMOS TECHNOLOGY

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Abstract - The fourth circuit element is memristors, that are mostly used in brain-like circuits and also in computing systems. Brain-like circuits has an advantage of fault tolerance and generalization ability of logic gates. The major problem that arises in the progress of implementing brainlike circuits in VLSI is the scalability of networks and limitation of solving large Boolean functions. In this paper, a 4 bit Vedic multiplier using memristor threshold logic circuit was designed. The proposed memristive cmos circuit is a combination of memristive circuits and cmos circuit, which provide the lower chip area, lower total harmonic distortion, and controllable leakage power. For the designing and simulation of the proposed system Ltspice IV tool was used.

Keywords - Area-efficient, Low power, CSLA, Binary to excess one converter, Multiplexer.

I. INTRODUCTION

Brain-inspired circuits can provide an opportunity to put into effect computing architectures taking advantage of fault tolerance and generalization capacity of logic gates. There has been several attempts to functionally and electrically mimic the neuron activity and its networks. But, predominant project that deters the development in VLSI implementations of brain like logic gates is the scalability of the networks and its sensible limitations in fixing large variable Boolean functions. One possibility is to apply the threshold logic gates in designing conventional computational blocks, while other option is to develop a completely trainable architecture that does not strictly bind itself to conventional computing topologies. In this brief, were strict the notion of the brain mimicking to develop generalized memristive threshold logic (MTL) cell in application to designing conventional computing blocks[6]. Nonetheless, this topic is one of the forefront challenges in development of on-chip brain computing, and would require us to investigate not just new circuit design logic, but also new devices and systems. Threshold logic is the primary logic of human brain that inspires from the neuronal firing and training mechanisms. The progress in threshold logic circuit[2] are often limited to implementation of logic gates with a few number of input variables; this leads to limited progress being made in the development of practical computing circuit topologies.

II. MEMRISTIVE THRESHOLD LOGIC CELL

Memristor like switching devices [3] unlike many other electronic devices has an interesting appeal in on-chip brain computing, as it offers switching state through its bi-level resistance values. Furthermore, these resistors are mapped to the binary memory space and offer the advantage of low on-chip area and low leakage currents. We explore this aspect of memristor, and extend over our previous work [4] in designing Vedic additions and multiplications for efficient Arithmetic Logic Unit design. The resulting circuits can be used in combination with conventional CMOS circuits to develop threshold logic processor designs. In contrast to previous work on resistive threshold logic [4], the cell has the input potential divider circuit modified by removing the pull-down resistor to form an input voltage averaging circuit and the threshold circuit modified with the combined use of operational amplifier (op-amp) and CMOS inverter[6]. In particular, by removing the pull-down resistor from [4], an important improvement over lower power dissipation is achieved in cell. The threshold unit consisting of a combination of an op-amp [5] and a CMOS inverter that allows for fault tolerance in terms of logical output signal stability. The generalization of the cell to work as different logic gates is achieved with the ability of the cell to utilize a wider range of threshold value.

III. VEDIC MULTIPLIER

Vedic multiplier is used to solve a wide range of mathematical problems. Using regular mathematical steps, solving problems sometimes are complex and time consuming. But using Vedic Mathematics General Techniques (applicable to all sets of given data) and Specific Techniques (applicable to specific sets of given data), numerical calculations can be done very fast. The use of Vedic mathematics provides reduced calculations and reduced delay in conventional mathematic problems. This is because the Vedic mathematics is based on the principles on which algorithms are implemented as human minds interpret.

Urdhva – Tiryagbhyam Sutra

Urdhva – tiryagbhyam is the general formula applicable to all cases of multiplication and also in the division of a large number by another large number. As the multiplication operation in UT sutra is computed parallel the delay in output is significantly reduced. Initially the UT sutra was used for decimal numbers only. However it can also be used for binary numbers[8]. The multiplication is done in vertically and crosswise method so it literally means "Vertically and crosswise technology". The partial products and their sums are calculated independently and the multiplier which is independent of the processor clock. The delay generated is only due to the carry occurrence from the partial products that is to be added in each next step's partial product.

Multiplication of two 2 digit numbers 11 * 13

The right hand most digit of the multiplicand, the first number (11) i.e.,1 is multiplied by the right hand most digit of the multiplier, the second number (13)i.e., 3. The product 1 X 3 = 3 forms the right hand most part of the answer. Now, diagonally multiply the first digit of the multiplicand (11) i.e., 1 and second digit of the multiplier (13)i.e., 1 (answer 1 X 1=1); then multiply the second digit of the multiplicand i.e.,1 and first digit of the multiplier i.e., 3(answer 1 X 3 = 3); add these two i.e.,1 + 3 = 4. It gives the next, i.e., second digit of the answer. Hence second digit of the answer is 4. Now, multiply the second digit of the multiplicand i.e., 1 and second digit of the multiplier i.e.,1 vertically, i.e., 1 X 1 = 1. It gives the left hand most part of the answer. Thus the answer is 143.

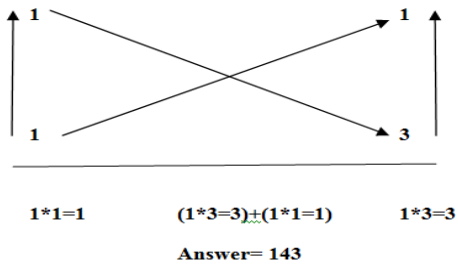

Figure 1: multiplication of 11 * 13

IV. PROPOSED MULTIPLIER ARCHITECTURE

The proposed system for 2x2and 4x4 bit Vedic multiplier are shown in the below sections. Here, "Urdhva-Tiryagbhyam" (Vertically and Crosswise) sutra is used for the multiplication of two binary numbers.

2X2 BITS VEDIC MULTIPLIER

The 2 X 2 bit vedic multiplication is done by using vertically and crosswise technique. As the multiplication operation in UT sutra is computed parallel, the delay in output is significantly reduced. It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. The Multiplier based on this sutra has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other conventional multipliers[7].The method is explained for two, 2 bit numbers A and B where A = a1a0 and B = b1b0 as shown in Figure 2.

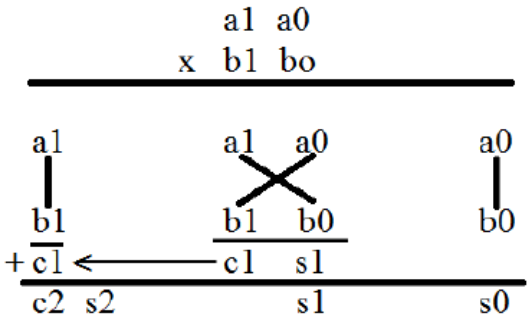

Figure 2: 2 x 2 bit multiplication

Firstly, the Least Significant Bits are multiplied which gives the Least Significant Bit (LSB) of the final product (vertical). Then, the LSB of the multiplicand is multiplied with the next higher bit of the multiplier and added with, the product of LSB of multiplier and next higher bit of the multiplicand (crosswise). The sum gives second bit of the final product and the carry is added with the partial product obtained by multiplying the most significant bits to give the sum and carry. The sum is the third corresponding bit and carry becomes the fourth bit of the final product. The output sum is taken as s0,c1s1 and c2s2.

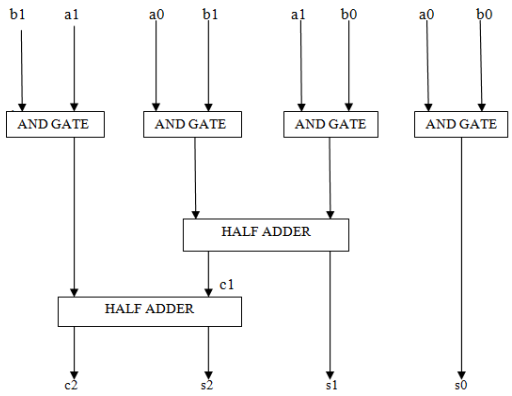

Figure 3: block diagram of 2 bit vedic

For implementing 2 bit vedic multiplier it requires four AND gates & two half Adders which is shown in figure 3. Based on the algorithm of 2 bit vedic multiplier, memristive threshold logic 2 bit vedic multiplier is designed. The circuit of 2 bit memristive vedic multiplier is implemented by using Lt spice IV

tool and is shown in Figure 4. From the circuit shown in Fig 4 we can get four output as S0,S1,S2,S3 with corresponding to the inputs A0,B0,A1,B1.

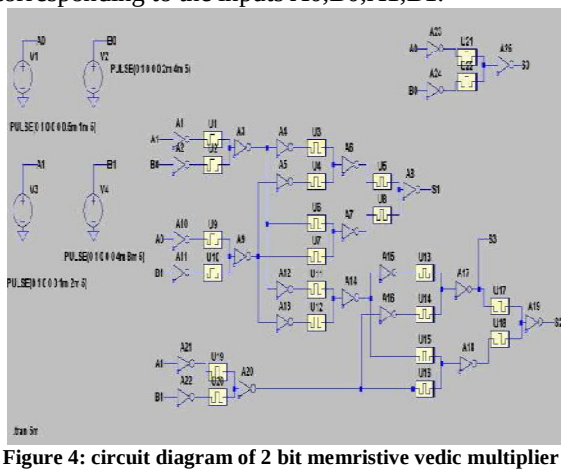

Figure 4: circuit diagram of 2 bit memristive vedic multiplier in Ltspice tool

V. 4X4 BIT VEDIC MULTIPLICATIONS

Proposed system was 4 bit vedic multiplier using memristor technology. The basic operation of the 4 bit Vedic multiplier using vertically and crosswise method is given in the Figure 5.

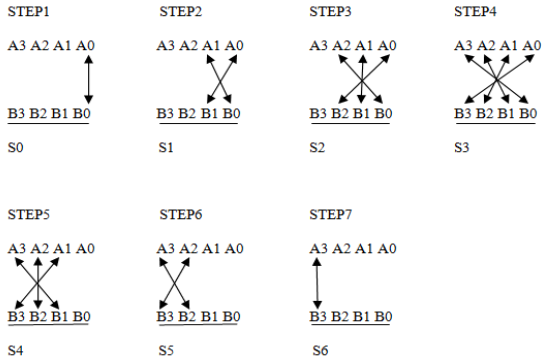

Figure 5: 4 bit vedic multiplication

MEMRISTIVE THRESHOLD 4 BIT VEDIC MULTIPLIER

The 4x4 bit Vedic multiplier is implemented using four 2x2 bit Vedic multiplier blocks is shown in Figure 6. The two 4 bit numbers, say A= A3 A2 A1 A0 and B= B3 B2 B1 B0. The output line for the multiplication result is – S7 S6 S5 S4 S3 S2 S1 S0. Using the fundamental of Vedic multiplication, we are taking two bit at a time and using 2 bit multiplier block**.**

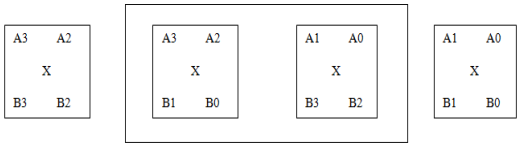

Figure 6: Structure for 4x4 bit Multiplication

last 2x2 multiplier inputs are “A1 A0” and “B1 B0”. The first block is 2x2 bit multiplier with inputs “A3 A2” and “B3 B2”. The middle one shows two, 2x2 bit multiplier with inputs “A3A2” & “B1B0” and “A1A0” & “B3B2”. So the final result of multiplication, which is of 8 bit, “S7S6S5S4S3S2 S1S0”. Each block is made up of 2x2 bit Vedic multiplier. Last 2x2 bit multiplier inputs are A1A0 and B1B0(Vertically). The first block is 2x2 bit multiplier with inputs A3A2 and B3B2(Vertically). The middle two 2x2 bit multipliers with inputs A3A2 & B1B0 and A1A0 &B3B2(Crosswise). So the final result is of 8 bit, S7 S6 S5 S4 S3 S2 S1 S0. To get final product S7S6S5S4S3S2S1S0 four, 2-bit Vedic multiplier and three 4-bit Ripple Carry (RC) Adders are required which is shown in the Figure 7. In this proposal, the first 4-bit RC Adder is used to add two 4-bit operands obtained from cross multiplication of the two middle 2x2 bit multiplier modules. The second 4-bit RC Adder is used to add two 4-bit operands, i.e. concatenated 4-bit (“00” & most significant two output bits of right hand most of 2x2 multiplier module as shown in Figure 7) and one 4-bit operand we get as the output sum of first RC Adder. Its carry “ca1” is forwarded to third RC Adder. Now the third 4-bit RC Adder is used to add two 4-bit operands, i.e. concatenated 4 -bit (carry ca1, “0” & most significant two output sum bits of 2nd RC Adder as shown in Figure 7) and one 4-bit operand we get as the output sum of left hand most of 2x2 multiplier module. The proposed Vedic multiplier can be used to reduce delay.

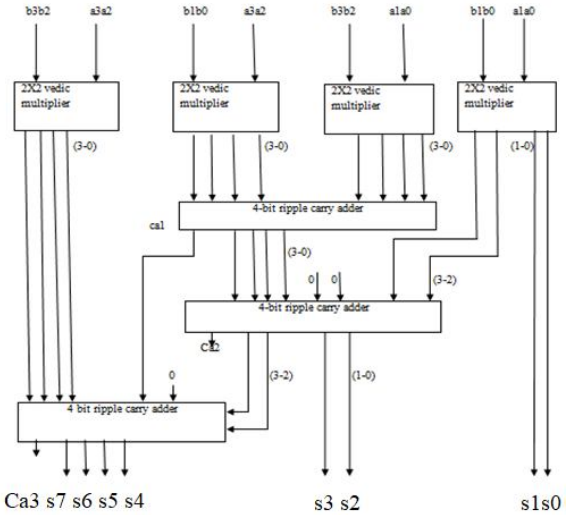

Figure 7: Block Diagram of 4x4 bit VM

4-BIT RIPPLE CARRY ADDER

Threshold logic memristive 4 bit vedic multiplier is consist of four 2 bit vedic multipliers and three 4 bit ripple carry adders. Ripple carry adder is the combination of four full adder circuits. The proposed system that uses 4 bit ripple carry for the addition of the output bits from the 2 bit vedic multipliers. Ripple carry adders create a logical circuit using multiple full

adders to add N-bit numbers. Each full adder inputs a Cin, which is the Cout of the previous adder. The ripple-carry adder allows fast design time; however, the ripple-carry adder is relatively slow, since each full adder must wait for the carry bit to be calculated from the previous full adder. Sum out S0 and carry out Co0 of the Full Adder 1 is valid only after the propagation delay of Full Adder 1. In the same way, Sum out S3 of the Full Adder 4 is valid only after the joint propagation delays of Full Adder 1 to Full Adder 4. In simple words, the final result of the ripple carry adder is valid only after the joint propagation delays of all full adder circuits inside it. The circuit diagram of full adder using memristor is shown in the Figure 8.

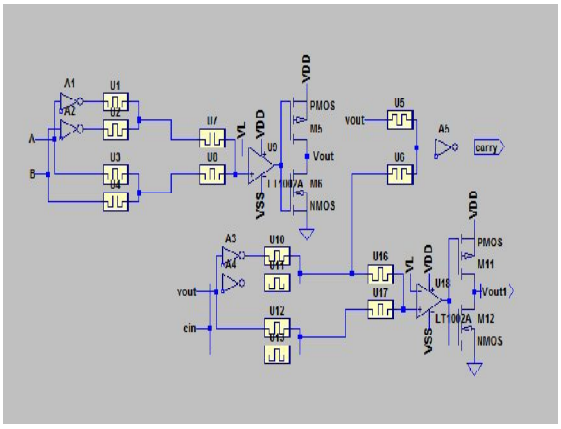

Figure 8: Memristor full adder circuit

This circuit has cmos inverter and operational amplifier. Which work as an insulator, that is it insulates the input and the output from larger power variations. In two input circuit the requirement of operational amplifier and cmos inverter is not necessary, but here we are using for the better output.

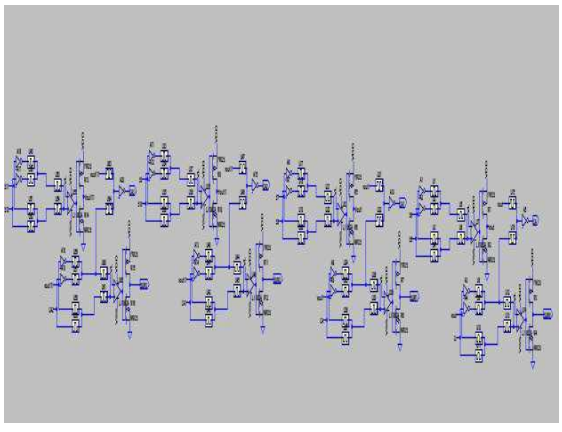

Figure 9: Ripple Carry Adder

4 bit ripple carry adder is shown in figure 9, which is the combination of four full adder circuits. The figure 10 shows the circuit diagram of 4 bit memristive Vedic multiplier. By using the memristor as a circuit element we can reduce the area of the overall system because the memristors are of small size.

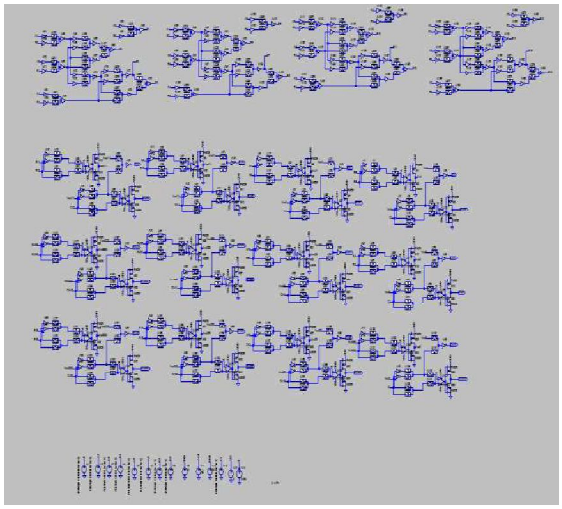

Figure10: 4 bit Memristive Vedic multiplier

VI. SIMULATIONS AND EXPERIMENTAL RESULTS

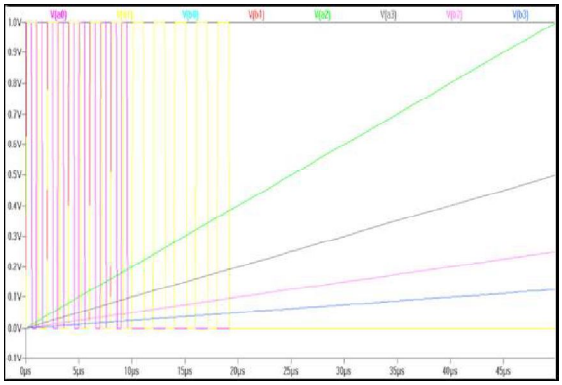

Figure 11: Inputs of 4 bit Vedic multiplier

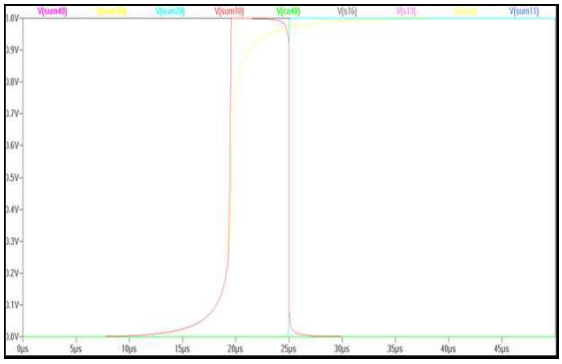

Figure 12:Outputs of 4 bit vedic multiplier

The inputs that are given to the system are pulse signal with the cycles of 5 and 10 and it does not has any time delay which is given in the input. The inputs are a0, a1, a2, a3, b0, b1, b2, b3. The operation designed by the LTspice IV tool has advantage like it is very fast operation, that is by giving the input in 'ms' rage, the output can be obtained in 'µs' range and is shown in Figure 12. The inputs for the 4 bit

memristive threshold logic Vedic multiplier are shown in Figure 11.

CONCLUSIONS

In the proposed system the Memristive Threshold Logic circuit was constructed and simulated successfully for the 4 bit Vedic Multiplier, which can be widely used in the modern microprocessors. The advantages of the system are smaller area and faster operation. The proposed memristor threshold logic circuits are extremely useful for the computing microprocessors due to their fault tolerance and logic generalization capability. The power dissipation and leakage power are the main problem which is due to the op-amp part of the circuit, and can be improved in future by the developing low power high-speed op-amps.

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