National Institute Of Technology Goa

Assignment Of VLSI Circuit Design

TOPIC: CMOS INVERTER

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Aim: *The aim of this experiment is CMOS inverter transfer curve, transient response, power and delay calculation, transfer curve variation with W and VDD variation using Cadence simulation software*

Tools Used: Cadence Software

INTRODUCITON

Complementary Metal-Oxide-Semiconductor (CMOS) technology forms the foundation of modern digital circuits due to its high noise immunity and low static power consumption. The CMOS inverter, composed of a PMOS and an NMOS transistor, is a basic building block of digital logic gates. This report explores the characteristics of a CMOS inverter, focusing on its transfer curve, transient response, power dissipation, and delay calculations. Additionally, the variation of the transfer curve with changes in the width-to-length ratio (W/L) of the transistors and supply voltage (VDD) is analyzed using simulations.

Each transistor consists of a stack of a conducting gate, an insulating layer of silicon dioxide and a semiconductor substrate (body or bulk). Here PMOS and NMOS are connected with gates and drain shorted to each other. Side view is shown in figure 5.1.

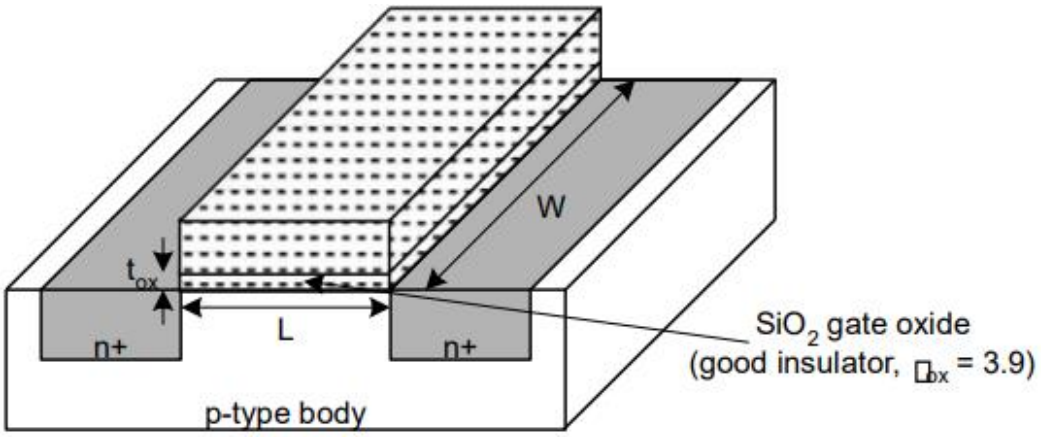


Fig 5.1: Basic MOS Transistor

The CMOS inverter is a basic building block for digital circuit design. As Figure 5.2 shows, the inverter performs the logic operation of A to Abar. When the input to the inverter is connected to ground, the output is pulled to VDD through the PMOS device M2 (and Ml shuts off). When the input terminal is connected to VDD, the output is pulled to ground through the NMOS device Ml (and M2 shuts off). The CMOS inverter has several important characteristics that are addressed in this lab: for example, its output Voltages wings from VDD to ground unlike other logic families that never quite reach the supply levels. Also, the static power dissipation of the CMOS inverter is practically zero, the inverter can be sized to give equal sourcing and sinking capabilities, and the logic Switching threshold can be set by changing the size of the device.

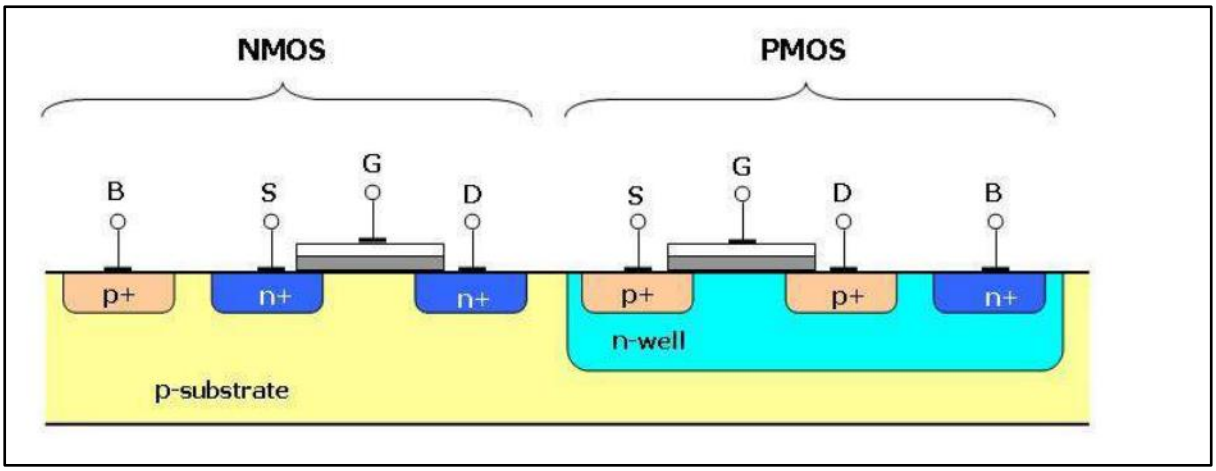


Fig 5.2 Side view of CMOS Inverter

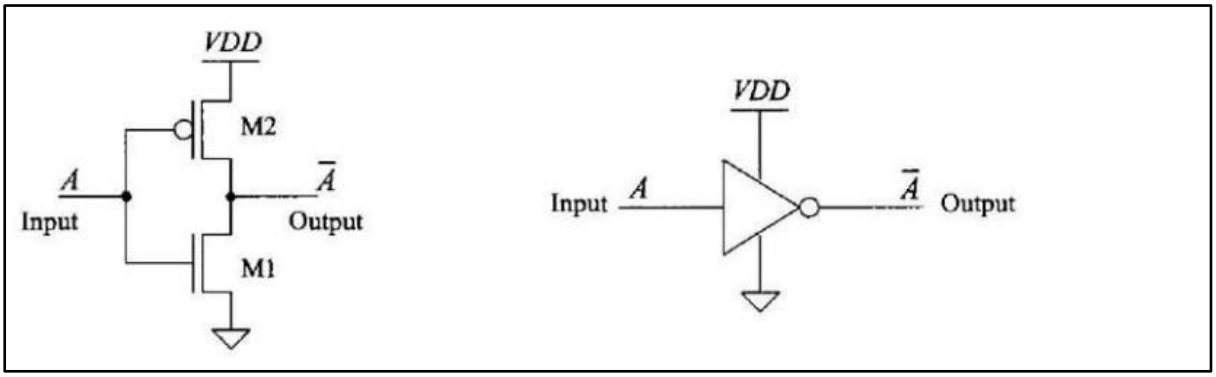


Fig 5.3 CMOS Inverter, schematic and logic symbol

As the inverter shown in Figure 5.3 and the associated transfer characteristic plot. In Region1of the transfer characteristics, the input voltage is sufficiently low (typically less than the threshold voltage of Ml), so that Ml is off and M2 is on (V_{sa} »V_{THP}). As Vin is increased, both M2 and Ml turn on (region2). Increasing Vin further causes M2 to turnoff and Ml to fully turn on, as shown in region3

THEORY

The CMOS inverter operates by complementarily switching between the NMOS and PMOS transistors:

- **When the input is low (0V):** The NMOS is off, and the PMOS is on, pulling the output to VDD.
- **When the input is high (VDD):** The NMOS is on, and the PMOS is off, pulling the output to ground (0V).

Transfer Curve

The transfer characteristic of the CMOS inverter is a plot of the output voltage Vout versus the input voltage Vin. It demonstrates how the output transitions from high to low as the input crosses the threshold voltage (Vth) of the transistors. The switching point, where

$$Vin = Vout, is\ typically\ at\ VDD/2.$$

Transient Response

The transient response of the inverter refers to the time-dependent behavior of the output signal when a time-varying input is applied. The key parameters are the propagation delay tp and the rise/fall times, which measure how quickly the output responds to changes in the input.

Power Dissipation

Power dissipation in a CMOS inverter includes both dynamic and static components. The dynamic power is the dominant factor and is given by:

$$P_{dynamic}=1/2\ \ C_L\ \ V^2_{DD}\ f$$

Where:

- CL is the load capacitance
- VDD is the supply voltage
- f is the switching frequency

Static power dissipation is minimal due to the near-zero current when both transistors are off.

Delay Calculation

Propagation delay tp is the average of the time taken for the output to transition from low-to-high (t_{pLH}) and high-to-low (t_{pHL}):

$$t_p = \frac{t_{pLH} + t_{pHL}}{2}$$

This delay is crucial for determining the speed of digital circuits.

PRINCIPLE OF OPERATION

The CMOS inverter functions by leveraging the complementary switching of NMOS and PMOS transistors. When the input voltage Vin is low, the NMOS transistor is in the cutoff region (off), and the PMOS transistor is in saturation (on), causing the output to be pulled to VDD. Conversely, when Vin is high, the NMOS transistor is in saturation (on), and the PMOS is in cutoff (off), pulling the output to ground. The inverter's high gain and sharp transition make it ideal for digital switching applications. Figure 5.4 shows characteristics of ideal inverter

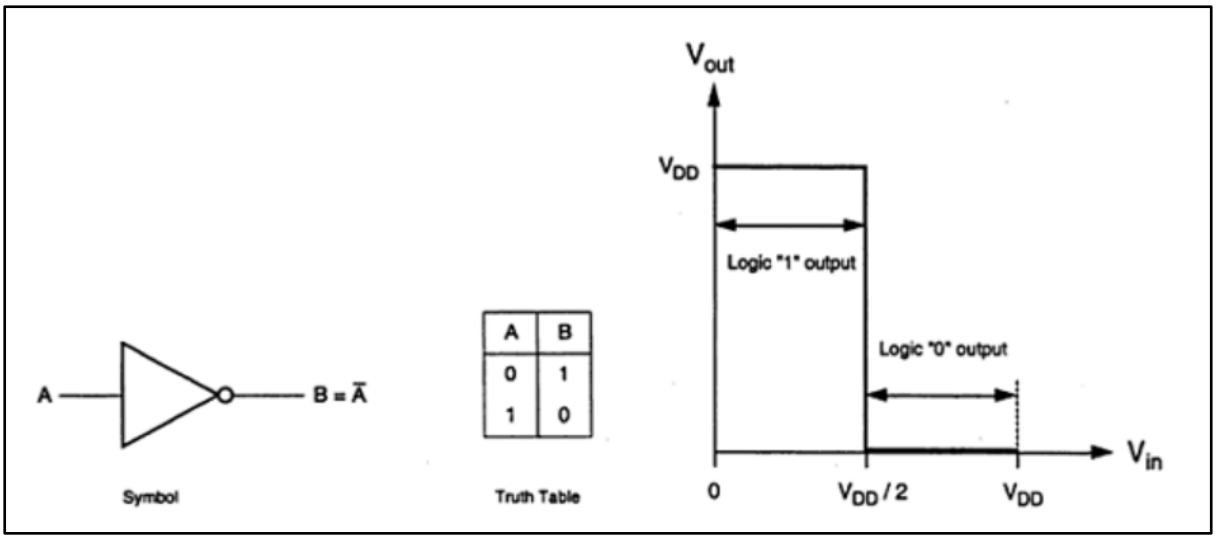


Fig 5.4: Ideal Inverter Characteristic and truth table

CIRCUIT DESIGN

1. **CMOS INVERTER:**

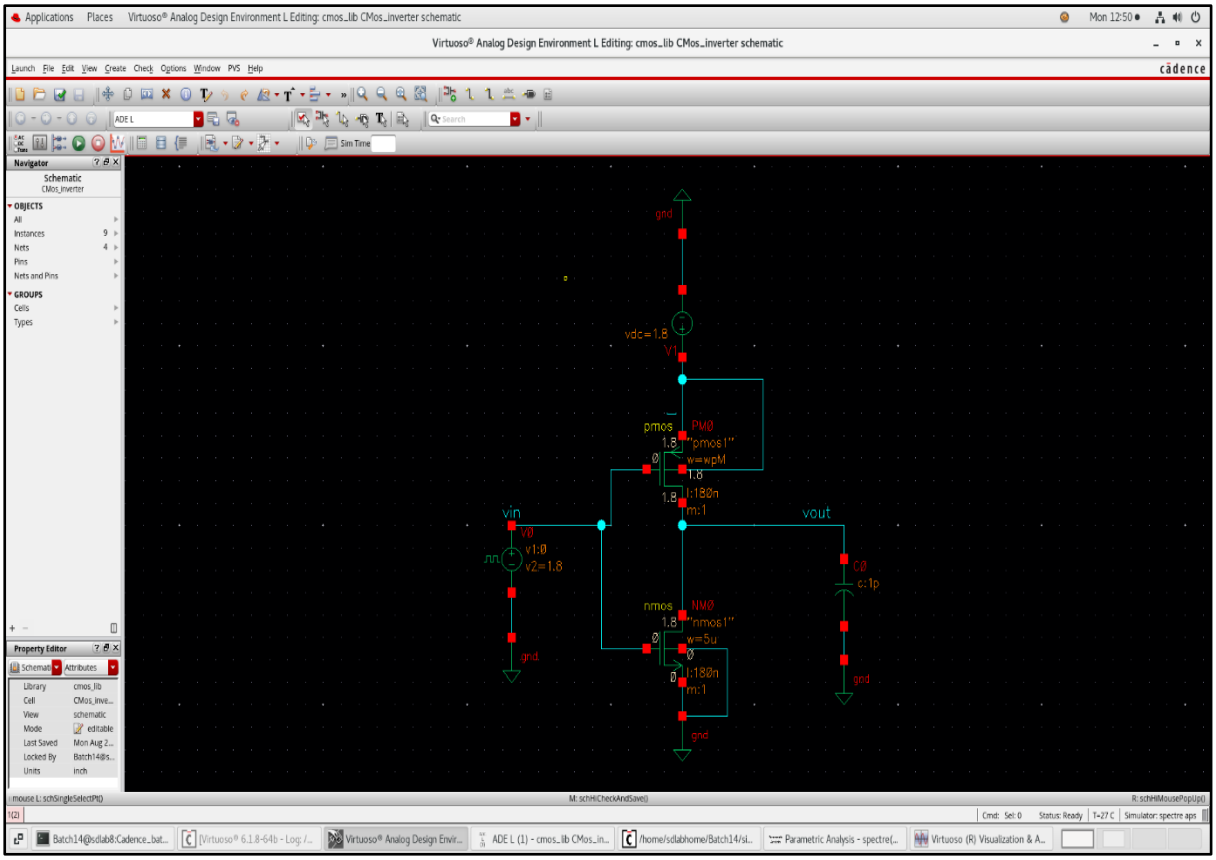


Fig: Circuit Diagram CMOS

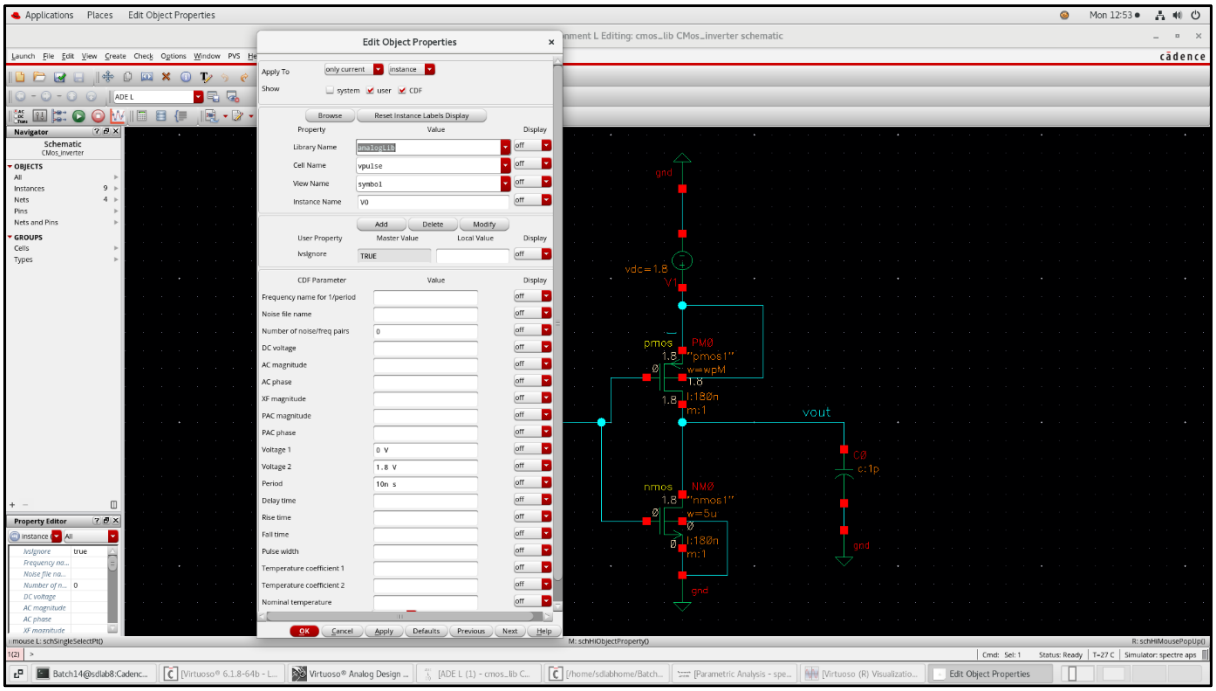


Fig: Input properties

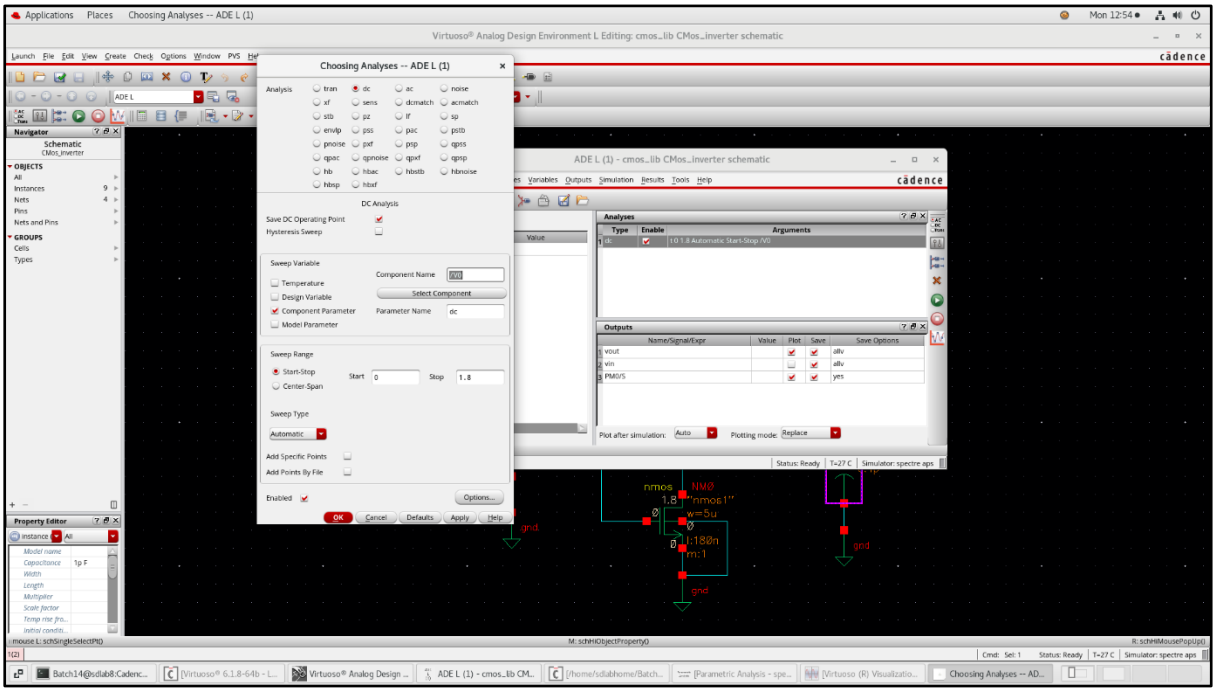


Fig: Analysis Details

Fig: Transfer characteristics

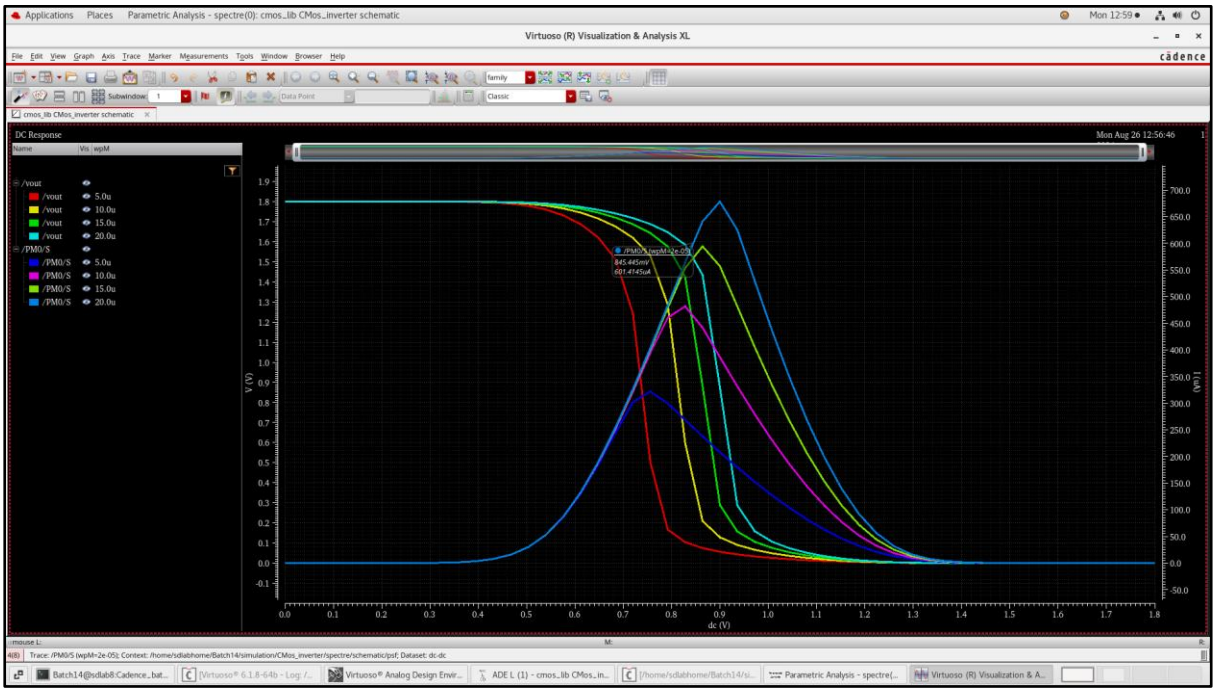


Fig: parametric analysis Transfer characteristics

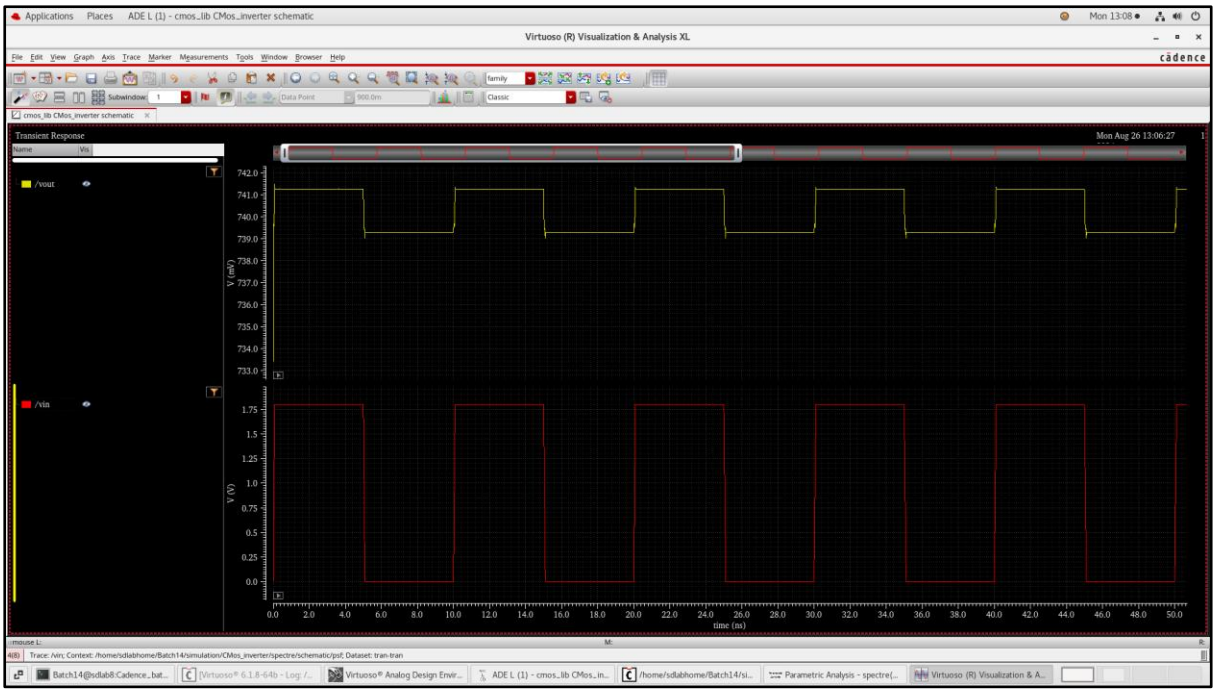


Fig : Input and output

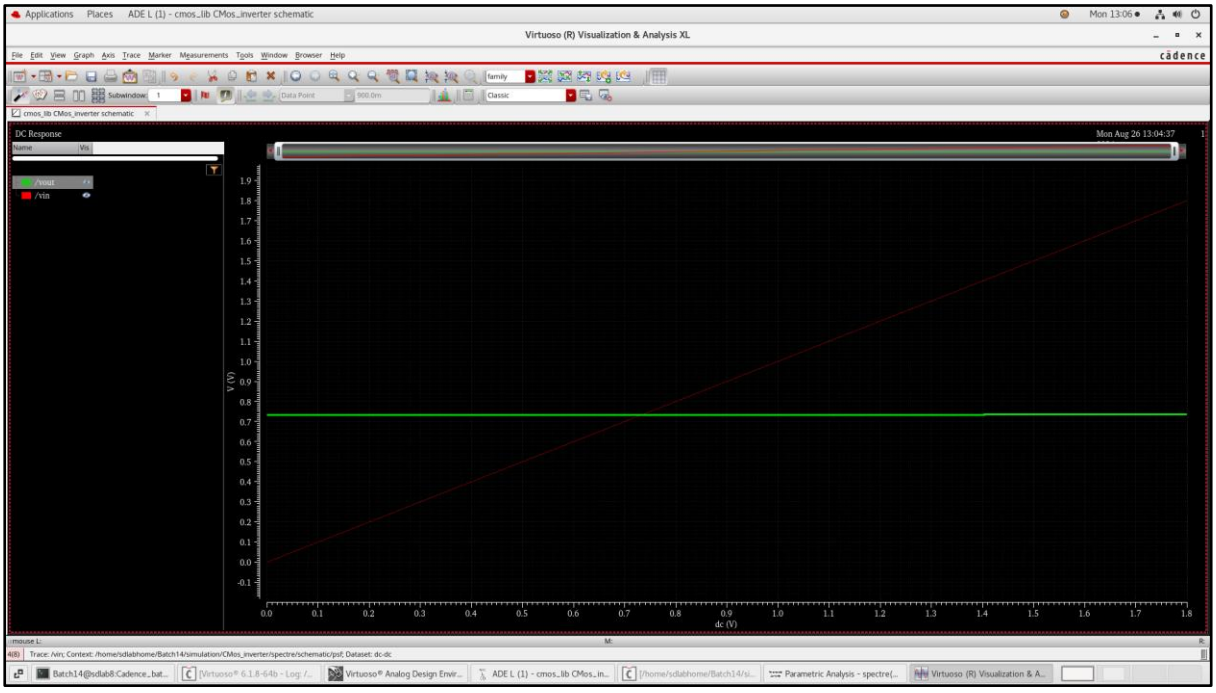
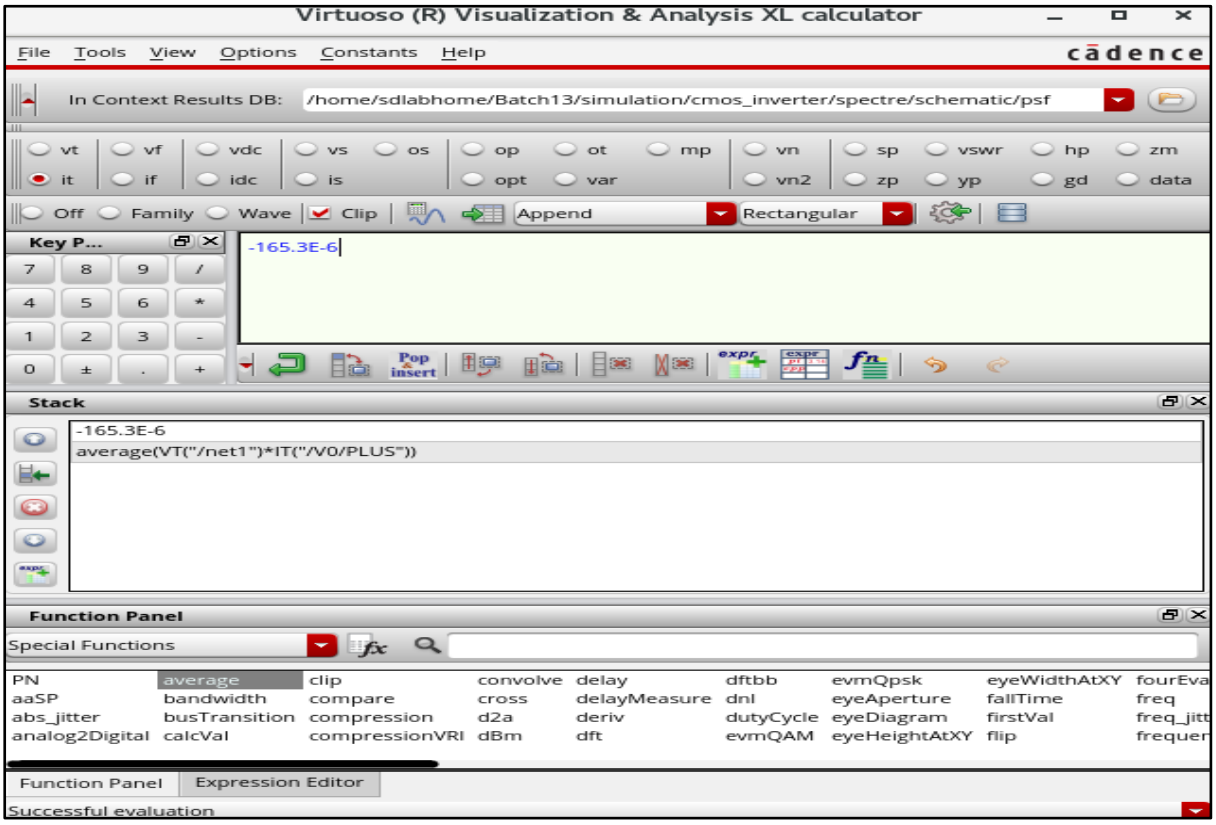


Fig: PMOS and NMOS are interchanged

POWER AND DELAY CALCULATIONS

- Power calculation using cadence calculator



- Propagation Delay

Fig: Propagation delay

Calculation of Propagation Delay

1. Propagation delay for the rising edge (t_{pLH})

This measures the time difference **between** the input signal reaching 50% (marked by the small red circle) and the output signal reaching 50% (marked by the yellow circle).

- Input 50% $t_{in\_rising} = 5.0005$ ns
- Output 50%: tout_rising = 5.30044 ns

The propagation delay for the rising edge is:

$$tpLH = t_{out\_rising} - t_{in\_rising} = 5.30044 \text{ ns} - 5.0005 \text{ ns} = 0.29994 \text{ ns}$$

2. Propagation delay for the falling edge (t_{pHL})

This measures the time difference between the input signal falling to 50% and the output signal falling to 50%.

- Input 50%: $t_{in\_falling} = 10.0005$ ns
- Output 50%: $t_{out\_falling} = 10.33145$ ns

The propagation delay for the falling edge is:

$$t_{pHL} = t_{out\_falling} - t_{in\_falling} = 10.33145 \text{ ns} - 10.0005 \text{ ns} = 0.33095 \text{ ns}$$

3. Average Propagation Delay t_p

The overall propagation delay is the average of t_{pLH}:

$$t_p = \frac{t_{pLH} + t_{pHL}}{2} = \frac{0.29994 \text{ ns} + 0.33095 \text{ ns}}{2} = 0.31545 \text{ ns}$$

Result

- **Rising Edge Delay (t_{pLH}):** 0.29994 ns
- **Falling Edge Delay (t_{pHL}):** 0.33095 ns
- **Average Propagation Delay (t_p):** 0.31545 ns

PROCEDURE

1. **Schematic Creation:** Design the CMOS inverter circuit with PMOS and NMOS transistors connected in a complementary configuration. Set VDD=1.8V and load capacitance CL=10pF.
2. **Transfer Curve Analysis:**
    - Sweep the input voltage Vin from 0V to VDD .
    - Plot the output voltage Vout as a function of Vin to generate the transfer characteristic curve.
3. **Transient Response Analysis:**
    - Apply a square wave input signal with a frequency of 500 MHz.
    - Observe the output signal and measure the rise time, fall time, and propagation delays t_{pLH} and t_{pHL}.
4. **Power Dissipation Calculation:**
    - Calculate the dynamic power dissipation using the load capacitance, supply voltage, and switching frequency.
5. **Variation Analysis:**
    - Vary the width-to-length ratio (W/L) of the transistors and observe the effect on the transfer curve.
    - Repeat the transfer curve analysis for different values of VDD.
6. **Record Observations:** Note the behavior of the CMOS inverter under different conditions.

OBSERVATIONS

Transfer Curve:

- The CMOS inverter exhibits a sharp transition in the output voltage around the threshold voltage Vth, with the midpoint approximately at VDD/2.
- Increasing the W/L ratio results in a steeper transfer curve, indicating faster switching.

Transient Response:

- The propagation delay tp was measured to be approximately 0.3147 ns.
- The rise and fall times were symmetrical, indicating balanced pull-up and pull-down strengths.

Power Dissipation:

- The dynamic power dissipation was calculated to be 163.1 uW.

Transfer Curve Variation:

- Increasing VDD shifts the transfer curve to the right and increases the switching threshold.
- Decreasing the W/L ratio causes a slower transition in the transfer curve.

RESULT

Transfer Curve: The CMOS inverter displayed a sharp inversion around the midpoint of VDD, with the steepness of the curve varying based on W/L and VDD.

Transient Response: The inverter demonstrated low propagation delay and balanced rise/fall times, making it suitable for high-speed operations.

Power Dissipation: The dynamic power dissipation was measured to be 8.1 mW, which is within the expected range for the given capacitance and frequency.

CONCLUSION

The CMOS inverter is a highly efficient component in digital circuits, providing a clear and sharp transition between logic levels. The analysis revealed that both the propagation delay and power dissipation are sensitive to changes in the transistor dimensions and supply voltage. By optimizing the W/L ratio and VDD, the performance of the CMOS inverter can be tailored to meet specific requirements, such as low power consumption or high-speed operation. The simulations using Cadence software provided valuable insights into the inverter's behavior, confirming theoretical expectations and allowing for further optimization in practical designs.

REFERENCES

1. Jan M. Rabaey, "Digital Integrated Circuits- A Design Perspective", Prentice Hall, Second Edition, 2005
2. Sung –Mo Kang & Yusuf Leblebici, "CMOS Digital Integrated Circuits- Analysis & Designing", MGH, Third Ed., 2003
3. John P Uyemura, "Introduction to VLSI Circuits and Systems", Wiley India, 2006
4. S K Gandhi, "VLSI Fabrication Principle", John Wiley