National Institute Of Technology Goa

Assignment Of VLSI Circuit Design

TOPIC: DESIGN OF 2 INPUT NAND GATE WITH MINIMUM POWER DELAY

Submitted To:

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Aim: The aim of this experiment is *Design of 2 Input NAND Gate with minimum power delay product and obtain its characteristics* and analysis using Cadence simulation software

Tools Used: Cadence Software

INTRODUCTION

In the design of digital circuits, optimizing power dissipation and speed is critical, especially for battery-powered applications. One commonly used logic gate is the two-input NAND gate, which is essential for various digital functions. Traditional complementary CMOS logic may occupy more area than necessary and could operate at insufficient speeds. This drives the need for alternative design strategies that prioritize lower power consumption while maintaining performance.

Power density often increases with technology scaling, making power dissipation a significant concern for circuit designers. To address these challenges, engineers aim to minimize the power-delay product (PDP), a key metric that reflects the efficiency of a circuit by balancing its power consumption and operational speed. A lower PDP indicates a more optimized design.

This report focuses on the design of a two-input NAND gate that minimizes the power-delay product while analysing its electrical characteristics. Various design methodologies will be explored, including complementary CMOS logic, pseudo nMOS logic, and dynamic CMOS logic. Through this analysis, we will evaluate the performance of the NAND gate in terms of power efficiency and speed, contributing to the development of more effective low-power digital circuits.

THEORY

NAND gate is one of the basic logic gates to perform the digital operation on the input signals. It is the combination of AND Gate followed by NOT gate i.e. it is the opposite operation of AND gate where the Logic NAND gate is complementary of AND gate.

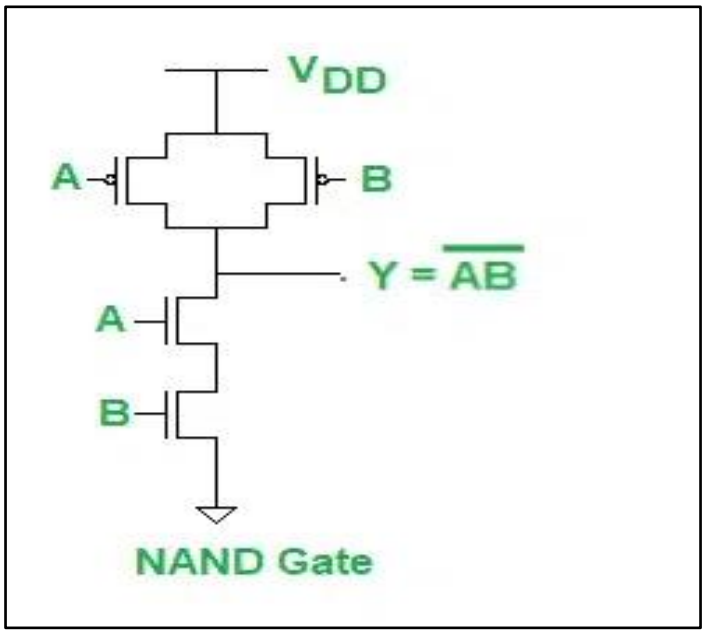


Fig: schematic of NAND gate

Image Src: https://geeksforgeeks.com/

Fig shows CMOS NAND Gate. It consists of two P-channel MOSFETs, Q1 and Q2, connected in parallel and two N-channel MOSFETs, Q3 and Q4 connected in series. P-channel MOSFET is ON when its gate voltage is negative with respect to its source whereas N-channel MOSFET is ON when its gate voltage is positive with respect to its source

When both inputs are low. Here, the gates of both P-channel MOSFETs are negative with respect to their sources, since the sources are connected to +VDD. Thus, Q1 and Q2 are both ON. Since the gate to source voltages of Q3 and Q4 (N-channel MOSFETs) are both 0V, those MOSFETs are OFF. The output is therefore connected to +VDD (HIGH) through Q1 and Q2 and is disconnected from ground.

The characterization of NMOS and PMOS devices is critical in integrated circuit design, as it

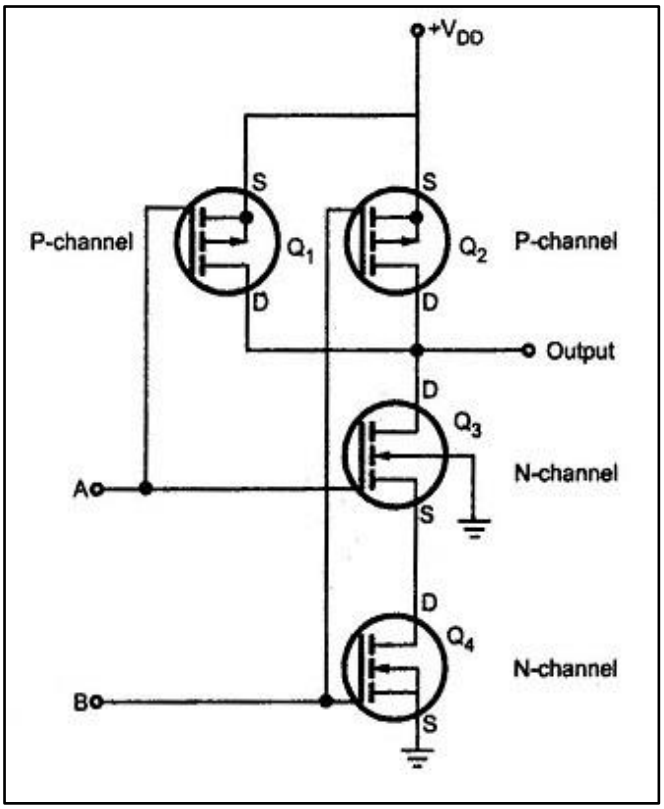


Fig: schematic of NAND gate

Image Src: https://geeksforgeeks.com/

When A = 0 and B = +VDD. In this case, Q1 is on because VGS1 = −VDD and Q4 is ON because VGS4 = +VDD. MOSFETs Q2 and Q3 are off because their gate-to-source voltages are 0 V. Since Q1 is ON and Q3 is OFF, the output is connected to +VDD and it is disconnected from ground. When A = $+V_{DD}$ and B = 0V, the situation is similar to the output is connected to $+V_{DD}$ through Q_2 and it is disconnected from ground because Q_4 is OFF. Finally, when both inputs are high (A = B = +VDD), MOSFETs Q1 and Q2 are both OFF and Q3 and Q4 are both ON. Thus, the output is connected to the ground through Q3 and Q4 and it is disconnected from +VDD.

A	B	Q1	Q2	Q3	Q4	O/P
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	1
1	0	OFF	ON	ON	OFF	1
1	1	OFF	OFF	ON	ON	0

Table: Truth table for NAND gate

The design of a two-input NAND gate that minimizes the power-delay product while analysing its electrical characteristics. Various design methodologies will be explored, including complementary CMOS logic, pseudo nMOS logic, and dynamic CMOS logic. Through this analysis, we will evaluate the performance of the NAND gate in terms of power efficiency and speed, contributing to the development of more effective low-power digital circuits.

CALCULATION

Given the power dissipation and delay values:

- Power $P = 93\,\mu J/s = 93 \times 10 - 6\ J/s$
- Delay $tp = 2.2ns \quad = 2.2 \times 10 - 9\ s$

We calculate the **Power Delay Product (PDP)** as:

$$PDP = P \times t_p$$
$$= (93 \times 10 - 6J/s) \times (2.2 \times 10 - 9\,s)$$
$$= (93 \times 10^{-6}) \times (2.2 \times 10^{-9})$$
$$= 204.6 \times 10 - 15\,J$$

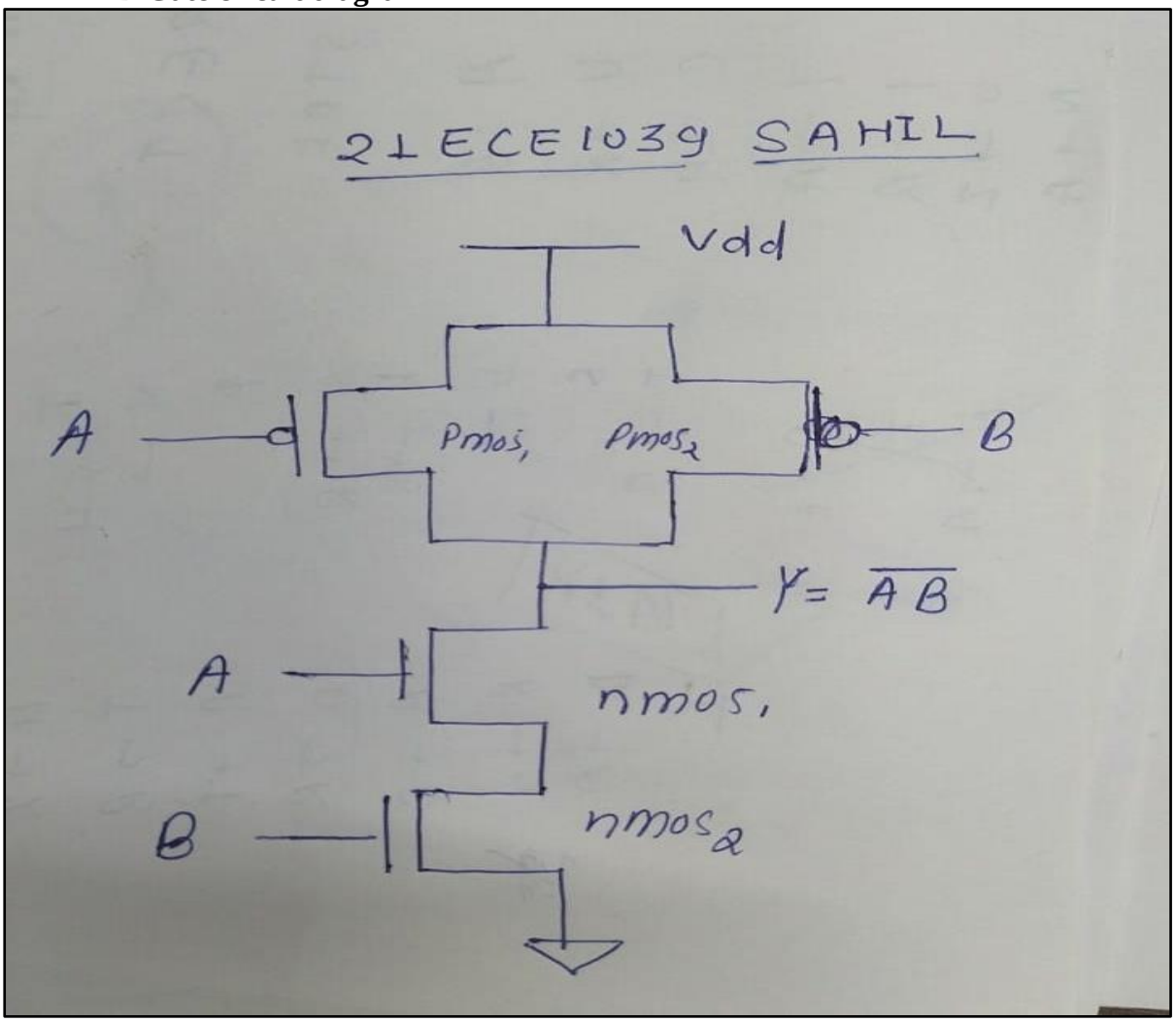
Thus, the **Power Delay Product** is **204.6 femtojoules**.

Transistor Width (Wp/Wn)	VDD (V)	Delay (ns)	Power (µW)	PDP (fJ)
1.5 / 1.0	1.8	2	80	160
2.0 / 1.0	1.8	2.2	93	204.6
2.5 / 1.5	1.8	2.6	85	221
3.0 / 1.5	1.8	2.9	100	290
3.5 / 2.0	1.8	3.1	110	341

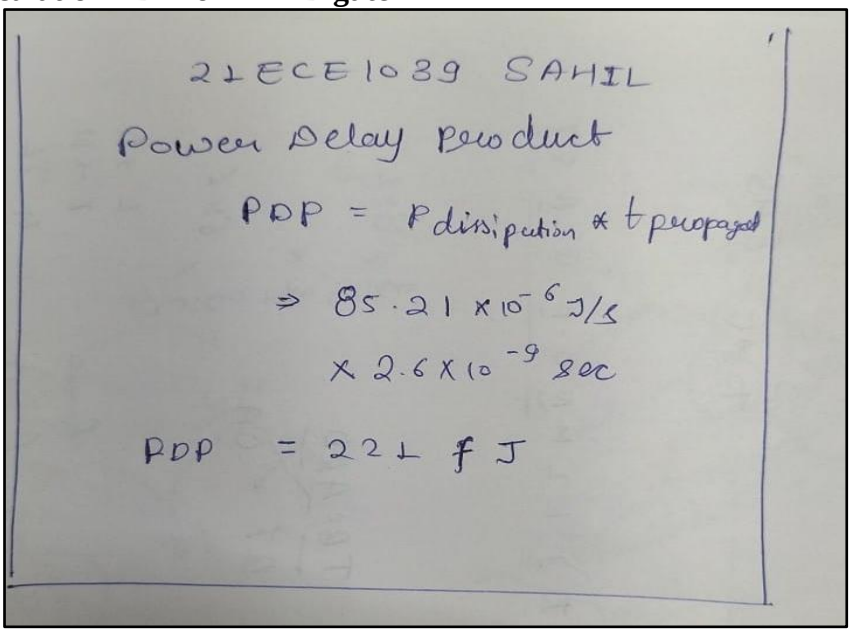
Table : power delay product calculation for different values of Wp/Wn

GRAPHS AND HAND CALCULATIONS

❖ **NAND Gate circuit diagram**



❖ **Hand calculation PDP for NAND gate**



❖ **NAND Gate circuit in cadence:**

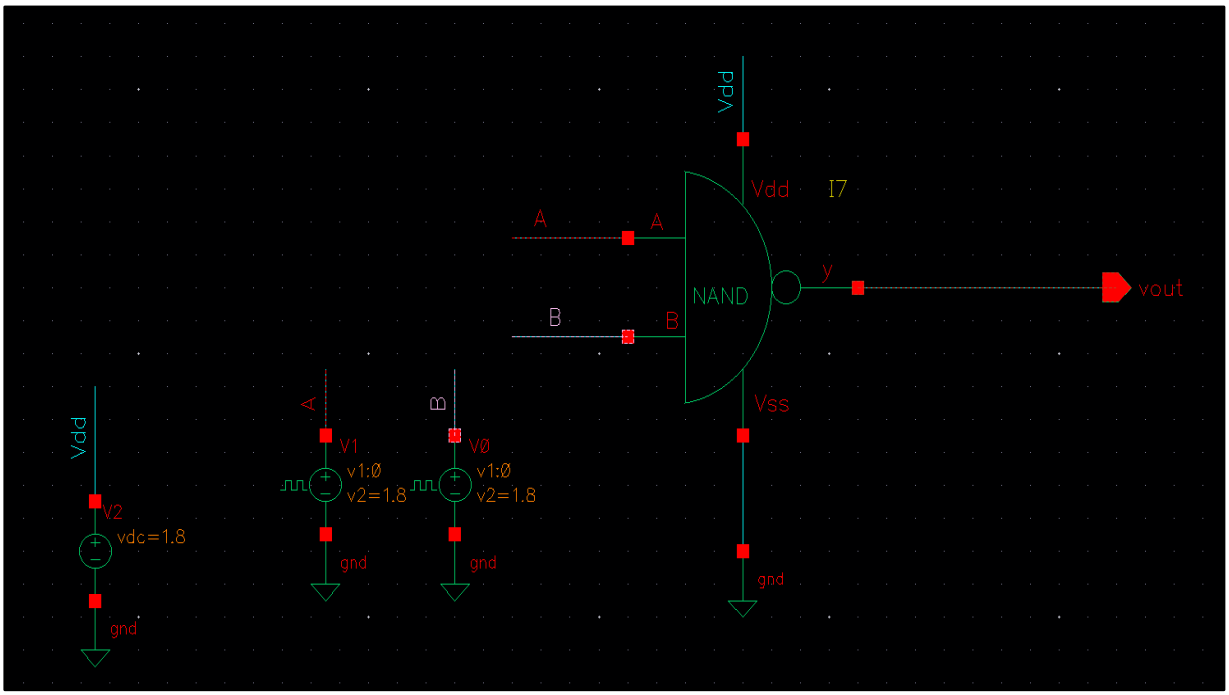
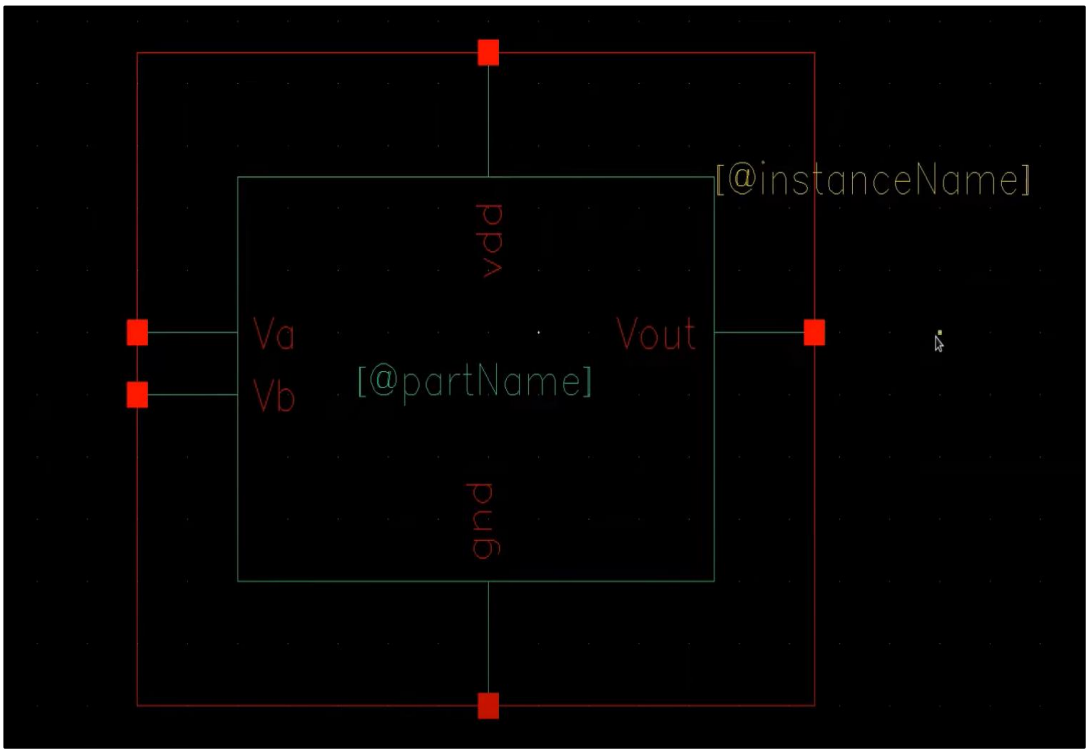


Fig: Circuit Diagram NMOS

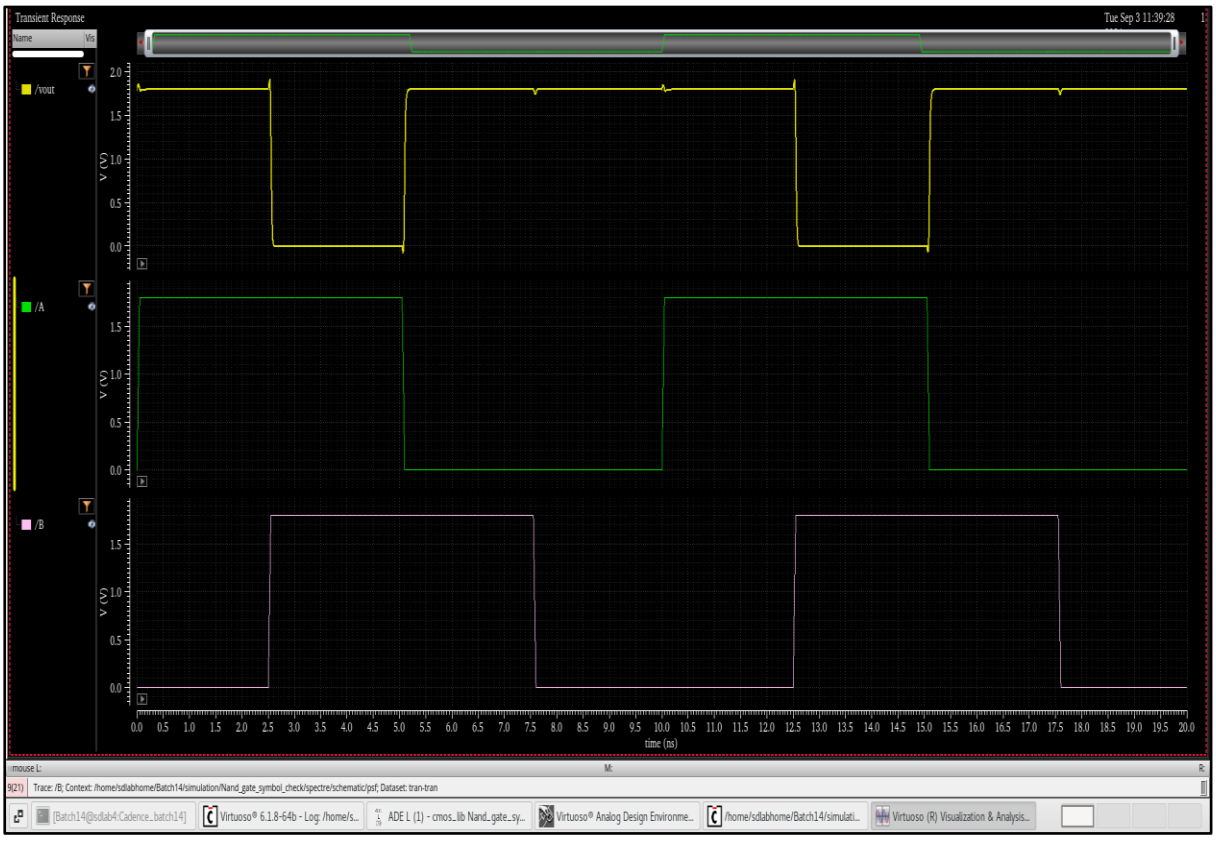
Here we have,

- Voltage source (V1) = 0 -1.8 V
- Width of Transistor(W)=2 µm
- Length of Transistor(L)=180nm (W:L=1:180)
- Gate Voltage , Vgate=1.8V
- Drain Voltage , Vd=0V
- Substrate Voltage , Vsub=0V

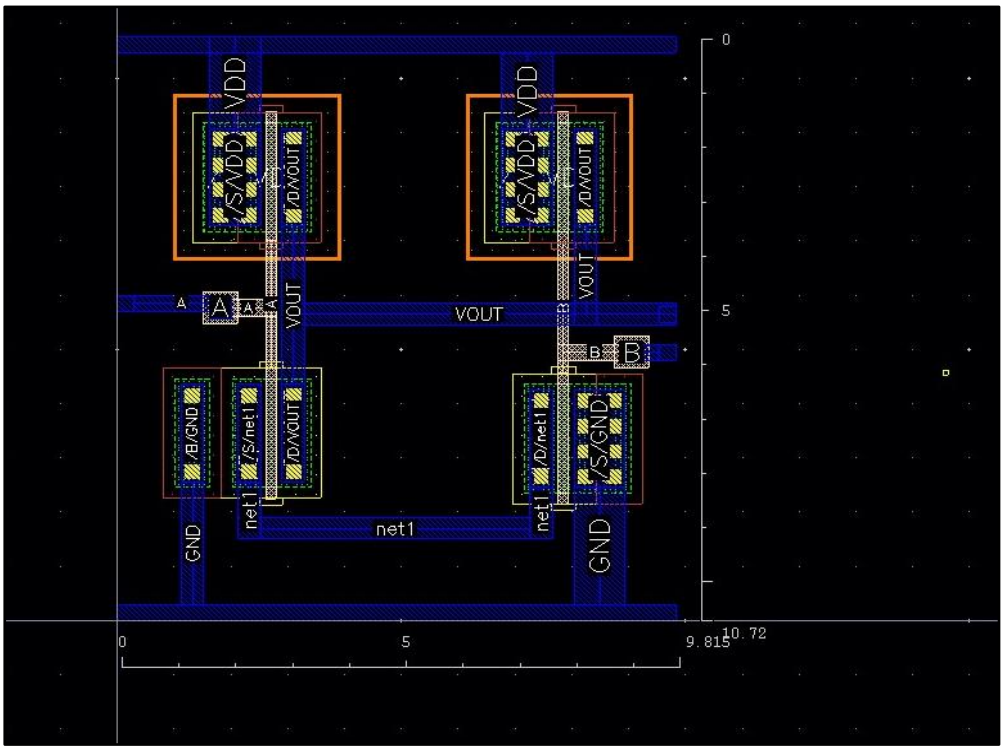
❖ **NAND Gate symbol creation cadence:**



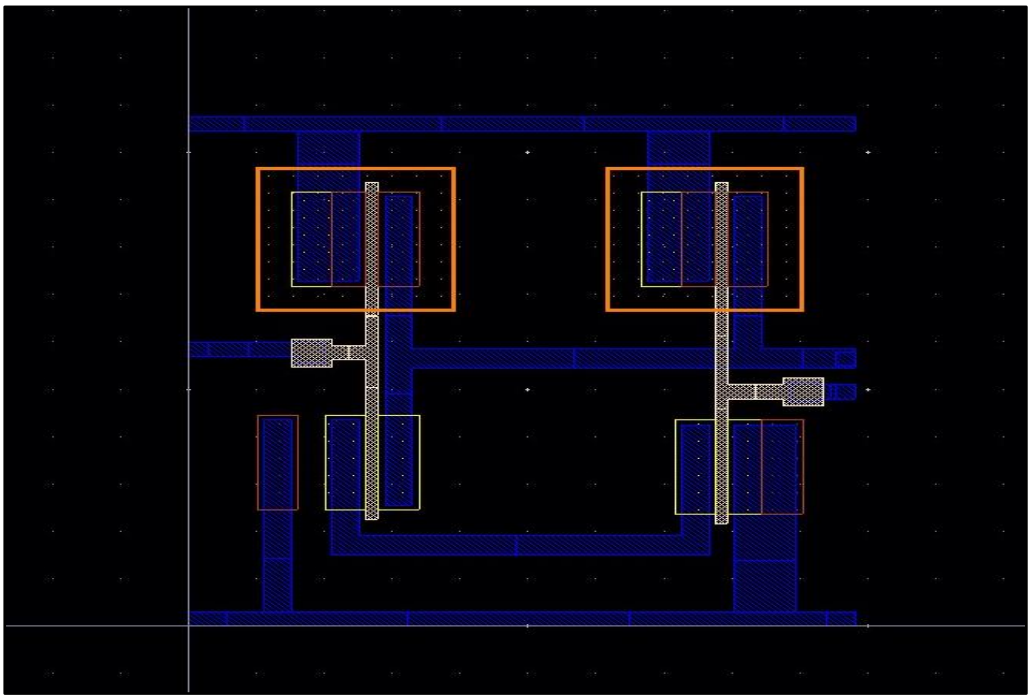
❖ **Transfer Characteristics**



❖ **Layout of NAND gate**



❖ **Extract of cmos Nand Gate**



PROCEDURE

1) Set Vgs to a constant value above the threshold voltage (e.g., 1.8V for NMOS and -1.5V for PMOS).
2) Sweep Vds from 0V to the supply voltage for NMOS (or from 0V to the negative supply voltage for PMOS).
3) Run the simulation and plot Ids versus Vds to obtain the output characteristics.
4) Design the 2-input NAND gate in simulation software such as Cadence, SPICE, or any other CMOS circuit design tool.
5) Run DC analysis to obtain the transfer curve by sweeping the input voltages.
6) Run transient analysis to measure the propagation delay (tPLH and tPHL) for rising and falling transitions.
7) Run power analysis to measure dynamic and static power consumption during the gate's operation.
8) Optimize transistor widths (Wn and Wp) and supply voltage (VDD) to minimize the PDP.
9) Vary the operating conditions (VDD, transistor sizes) and observe the impact on power, delay, and transfer characteristics.

OBSERVATIONS

Effect of Transistor Width Ratio (Wp/Wn) on Delay:

- As the width ratio (Wp/Wn) increases, the **propagation delay** of the circuit increases. This is because increasing the width of the PMOS transistor relative to NMOS adds capacitance to the circuit, which slows down the switching speed.
- For instance, when Wp/Wn changes from **1.5/1.0** to **3.5/2.0**, the delay increases from **2.0 ns** to **3.1 ns**.

Effect on Power Dissipation:

- Power dissipation varies with the width ratio but doesn't increase in a strictly linear fashion. Larger PMOS transistors consume more power, but the exact impact also depends on the load capacitance and switching characteristics.
- The power increases from **80 µW** to **110 µW** as the ratio changes from **1.5/1.0** to **3.5/2.0**.

Power-Delay Product (PDP) Analysis:

- The **PDP** provides a combined measure of the energy efficiency and performance of the circuit. Lower PDP values are more desirable, indicating better performance with lower power consumption.
- The smallest **PDP** value is **160 fJ** for the ratio Wp/Wn=1.5/1.0 ,while the highest is **341 fJ** for Wp/Wn=3.5/2.0. As the width ratio increases, the **PDP** also increases, indicating that larger width ratios are less efficient.

RESULT

Based on the table, the optimal transistor width ratio for this NAND gate design, in terms of minimizing the **power-delay product (PDP)**, is $W_p/W_n = 1.5/1.0$ with a **PDP** of **160 fJ**.

- This design offers a **balance** between speed (lower delay of **2.0 ns**) and power consumption (lower power of **80 µW**).
- Increasing the width ratio improves the drive strength of PMOS, but this also increases delay and power dissipation, leading to a **higher PDP**, as seen with the $\boldsymbol{W_p/W_n = 3.5/2.0}$ **,** which has the highest **PDP** of **341 fJ**

CONCLUSION

The schematic provides an accurate representation of the logical functionality of the NAND gate. It serves as a crucial tool for conceptualizing and understanding the circuit's behavior without delving into the intricacies of the physical layout. The layout plays a pivotal role in determining the performance of the NAND gate. Through simulation, it becomes apparent that optimizing the physical arrangement of transistors can significantly impact parameters such as propagation delay, power consumption, and overall efficiency. The layout simulation allows for a more realistic assessment of parasitic elements, including capacitance and resistance, which may not be as apparent in the schematic. Understanding and mitigating these parasitic effects are critical for achieving accurate performance predictions.

REFERENCES

1. Jan M. Rabaey, “Digital Integrated Circuits- A Design Perspective”, Prentice Hall, Second Edition, 2005
2. Sung –Mo Kang & Yusuf Leblebici, “CMOS Digital Integrated Circuits- Analysis & Designing”, MGH, Third Ed., 2003
3. John P Uyemura, “Introduction to VLSI Circuits and Systems”, Wiley India, 2006
4. S K Gandhi, “VLSI Fabrication Principle”, John Wiley