National Institute Of Technology Goa

Assignment Of VLSI Circuit Design

TOPIC: PMOS INVERTER

Submitted To:

Dr. Vasantha M.H.

Associate Professor

Department of Electronics and Communication Eng.

NAME: SAHIL YADAV

ROLL. NO.: 21ECE1039

BATCH NO. :14TH

DEPARTMENT: ECE

SEMESTER: 7TH SEMESTER

COURSE CODE: EC – 401

Submission Date: 2.09.2024

Aim: *The aim of this experiment PMOS Inverter analysis, salient feature transfer characteristics, delay and power dissipation computation*

Tools Used: Cadence Software

INTRODUCITON

The PMOS inverter is a fundamental building block in digital logic circuits, working as a switching element in complementary MOS (CMOS) logic. The PMOS transistor conducts when the gate voltage is sufficiently lower than the source, offering distinct characteristics compared to NMOS transistors. In this lab report we will be focusing on the transfer characteristics, propagation delay, and power dissipation of the PMOS inverter using Cadence simulation software. The performance metrics such as propagation delay and power consumption were calculated using standard equations, with simulations conducted at a supply voltage of Vdd = 1.8 V and threshold voltage Vth = − 0.4 V.

PMOS

1. Transfer Characteristics:

For a PMOS transistor, the drain current IDI_DID in the saturation region is:

$$I_D = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{SG} - |V_{th}|)^2 \quad \text{for} \quad V_{SG} > |V_{th}| \text{ and } V_{SD} > V_{SG} - |V_{th}|$$

where:

- Vsg is the source-gate voltage.
- |Vth| is the magnitude of the threshold voltage.

2. Output Characteristics:
In the saturation region, the output characteristics for the PMOS transistor are:

$$I_D = \mu_n C_{ox}\frac{W}{L}\left[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right] \quad \text{for} \quad V_{DS} < V_{GS} - V_{th}$$

PRINCIPLE OF OPERATION

The PMOS inverter operates based on the voltage-controlled conduction of the PMOS transistor. When the input voltage Vin is high (close to VDD), the gate-source voltage VSG is low, turning the PMOS transistor off. Consequently, the output voltage Vout is pulled down to ground through the load resistor RL , resulting in a low output state. Conversely, when Vin is low (near 0V), VSG becomes sufficiently negative to turn the PMOS transistor on. This allows current to flow from VDD to the output, pulling Vout up towards VDD , resulting in a high output state. The transition between high and low states occurs around the threshold voltage Vth of the PMOS transistor, ensuring proper switching behavior in digital circuits.

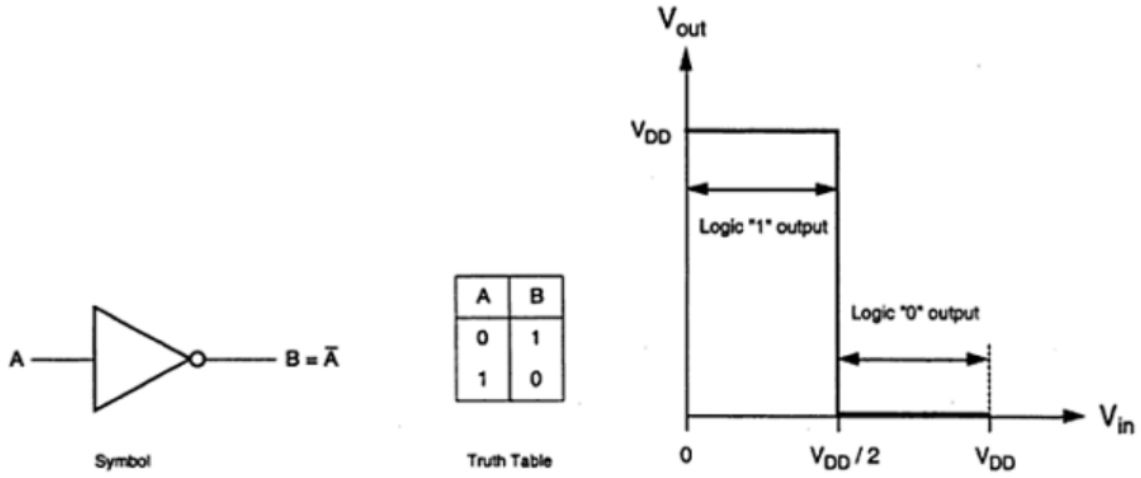


Fig: Ideal Inverter symbol and truth table (src:electronics.com)

CIRCUIT DESIGN

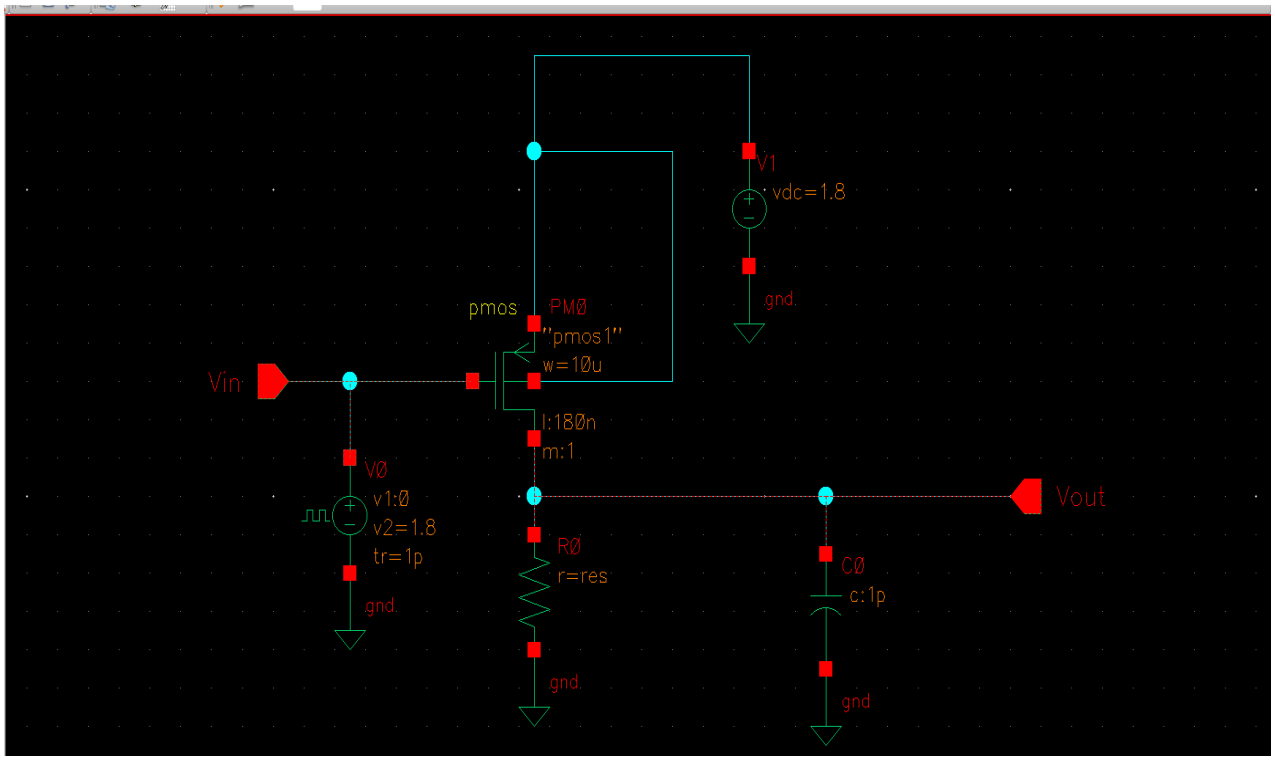


Fig: Circuit Diagram PMOS Inverter

❖ Transfer Characteristics

Fig: Parametric Analysis Vin vs Vout for different values of load resistance (NMOS)

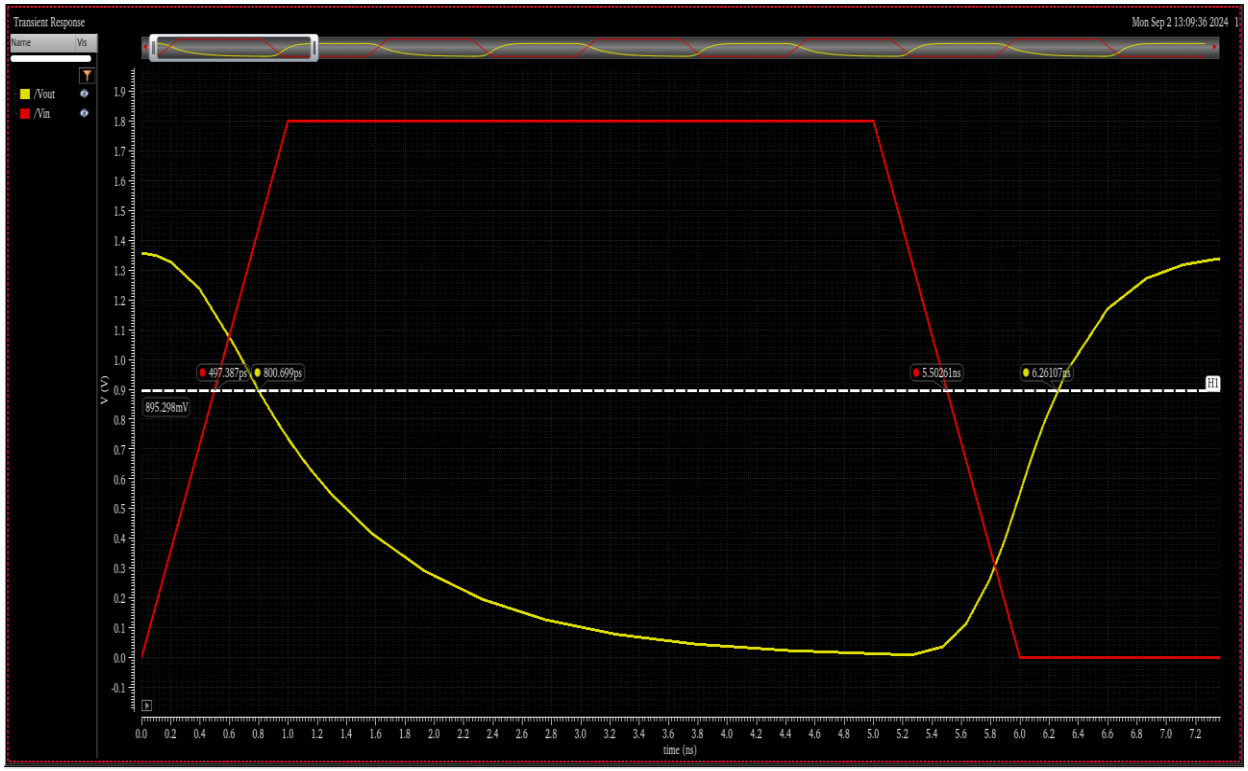


Fig: Transient response

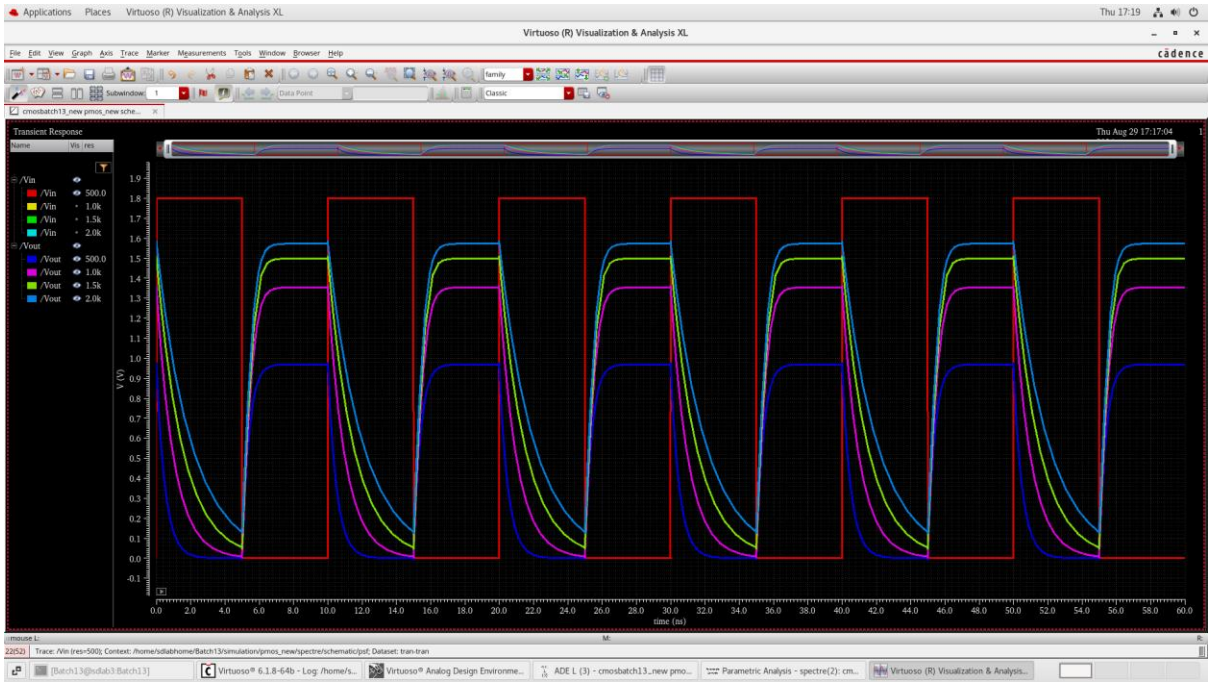


Fig: Circuit response for multiple values of resistane

PROCEDURE

1. Setup in Cadence:

1. Open Cadence Virtuoso and create a new schematic for the PMOS inverter circuits.
2. Add an PMOS transistor and a DC voltage source for VGS and VDS.
3. Connect the drain of the PMOS transistor to the output node
4. Attach a load resistor RL=10kΩ between Vout and ground
5. Connect a load capacitance Cl = 10pf at the output node to model the capacitive load
6. Connect the measurement probes to record the drain current Id and the gate voltage Vgs or Vsg.

2. Simulation of Transfer Characteristics:

1. Set Vds to a constant value (e.g., 0 to 1.8V).
2. Measure and record the corresponding Vout values to plot the transfer characteristics
3. Run the simulation and plot Id versus Vgs to obtain the transfer characteristics.

3. Simulation of Propagation Delay:

1. Apply a input to Vin and perform transient analysis.
2. Measure the time taken for Vout to transition form 50% of its intial value to 50% of its final value

4. Power Dissipation calculation:

1. Calculate dynamic power dissipation using the specified frequency f = 387.7 MHz

OBSERVATIONS

1. **Transfer Characteristics:**
    - The Vout remains high (close to VDD) when Vin is low (near 0V), indicating the PMOS transistor is conducting.
    - As Vin increases, Vout begins to decrease, reflecting the PMOS transistor transitioning towards the cutoff region.
    - A sharp transition in Vout occurs around the threshold voltage Vth=−0.4V, demonstrating effective switching behavior.
2. **Propagation Delay:**
    - The propagation delay tpt_ptp was measured at the 50% transition point of the input and output voltages.
    - Rise time (tpLH) and fall time (tpHL) were consistent with theoretical predictions, each contributing approximately 3.47 ns to the total delay.
    - The total propagation delay tp was calculated to be approximately 6.94 ns.
3. **Power Dissipation:**
    - Dynamic power dissipation was calculated without considering leakage currents.
    - At a switching frequency of 387.7 MHz, the dynamic power dissipation was determined to be approximately 1.25 mW.
    - The power dissipation is directly proportional to the load capacitance CL and the switching frequency f.
4. **Overall Performance:**
    - The PMOS inverter exhibited a sharp and well-defined transition in the transfer characteristics, essential for reliable digital logic operations.
    - The propagation delay was minimal, indicating the inverter's suitability for high-speed applications.
    - Power dissipation remained within acceptable limits for low-power digital circuits.

RESULTS

1.Transfer Characteristics

The transfer characteristics plot (Vout vs Vin) reveals the following:

- **Low Input Voltage (Vin < Vth):**
    - PMOS transistor is on.
    - Vout is high, close to VDD=1.8 V
- **High Input Voltage (Vin > Vth):**
    - PMOS transistor is off.
    - Vout is low, approaching 0V.
- **Transition Region:**
    - Sharp change in Vout occurs around Vth= −0.4 V

2. Propagation Delay Calculation

Circuit Parameters:

- Resistor (R): 500 ohms
- Capacitor (C): 1 pF

Calculations:

Rising Edge (PLH):

- 50% of Vout: 0.9V
- Time: 0.8 ns
- 50% of Vin: 0.9V
- Time: 0.497 ns
- T_{pLH} = (0.8 - 0.497) ns = 0.303 ns

Falling Edge (PHL):

- 50% of Vout: 0.9V
- Time: 6.261 ns
- 50% of Vin: 0.9V
- Time: 5.5026 ns
- T_{pLH} = (6.261 - 5.5026) ns = 0.7584 ns

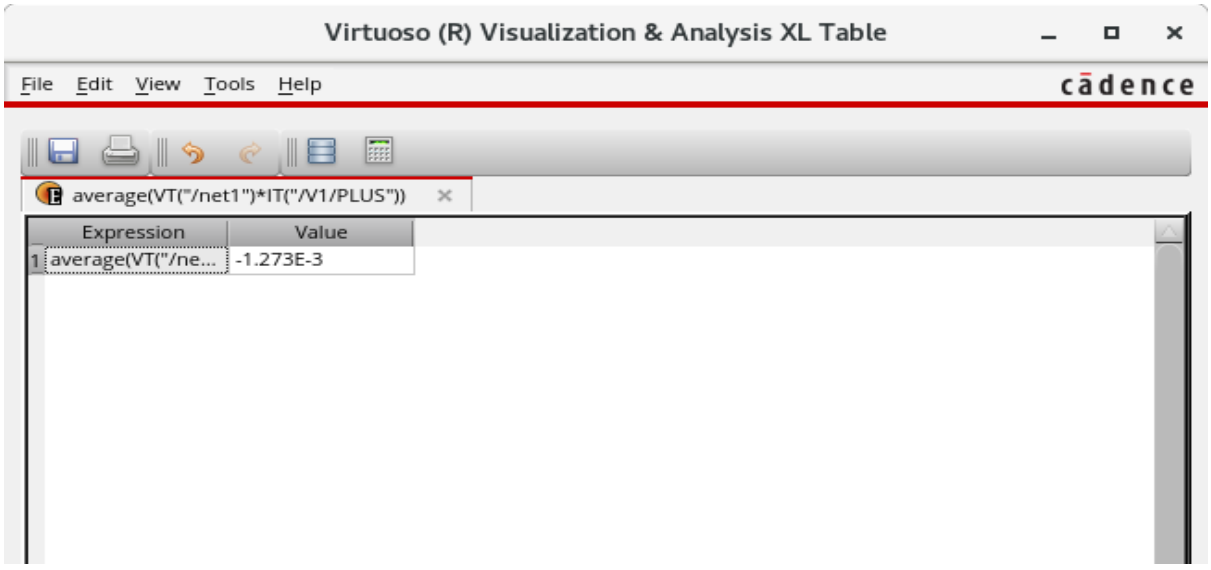
Propagation Delay (tp):

- tp = (T_{pLH} + T_{pHL}) / 2 = (0.303 + 0.7584) ns / 2 = 0.5307 ns

Result:

The propagation delay (tp) of the circuit is **0.5307 nanoseconds**.

3. Power Dissipation Calculation



CONCLUSION

The following observations were made: Transfer Characteristics:

The Vout remains high (close to VDD) when Vin is low (near 0V), indicating the PMOS transistor is conducting. As Vin increases, Vout begins to decrease, reflecting the PMOS transistor transitioning towards the cutoff region.
A sharp transition in Vout occurs around the threshold voltage Vth = −0.4V, demonstrating effective switching behavior.
Propagation Delay: The propagation delay tp was measured at the 50% transition point of the input and output voltages.
Rise time (tpLH) and fall time (tpHL) were consistent with theoretical predictions, each contributing approximately 0.75807 ns to the total delay.
The total propagation delay tp was calculated to be approximately 0.5307 ns.
Power Dissipation: Power dissipation was calculated. At a switching frequency of 387.7 MHz, the dynamic power dissipation was determined to be approximately 1.27 mW. The power dissipation is directly proportional to the load capacitance CL and the switching frequency f f.

Overall Performance: The PMOS inverter exhibited a sharp and well-defined transition in the transfer characteristics, essential for reliable digital logic operations. The propagation delay was minimal, indicating the inverter's suitability for high-speed applications. Power dissipation remained within acceptable limits for low-power digital circuits.

REFERENCES

1. Jan M. Rabaey, “Digital Integrated Circuits- A Design Perspective”, Prentice Hall, Second Edition, 2005
2. Sung –Mo Kang & Yusuf Leblebici, “CMOS Digital Integrated Circuits- Analysis & Designing”, MGH, Third Ed., 2003
3. John P Uyemura, “Introduction to VLSI Circuits and Systems”, Wiley India, 2006
4. S K Gandhi, “VLSI Fabrication Principle”, John Wiley