

DIGITAL COMMUNICATIONS

LABORATORY MANUAL

**B.TECH
(III YEAR – I SEM)
(2021-22)**

Department of Electronics & Communication Engineering



**MALLA REDDY COLLEGE
OF ENGINEERING & TECHNOLOGY**

(Autonomous Institution – UGC, Govt. of India)

Recognized under 2(f) and 12 (B) of UGC ACT 1956

Affiliated to JNTUH, Hyderabad, Approved by AICTE - Accredited by NBA & NAAC – ‘A’ Grade - ISO 9001:2015 Certified
Maisammaguda, Dhulapally (Post Via. Kompally), Secunderabad – 500100, Telangana State, India

VISION

To evolve into a center of excellence in Engineering Technology through creative and innovative practices in teaching-learning, promoting academic achievement & research excellence to produce internationally accepted competitive and world class professionals.

MISSION

To provide high quality academic programmes, training activities, research facilities and opportunities supported by continuous industry institute interaction aimed at employability, entrepreneurship, leadership and research aptitude among students.

QUALITY POLICY

- ❖ Impart up-to-date knowledge to the students in Electronics & Communication area to make them quality engineers.
- ❖ Make the students experience the applications on quality equipment and tools.
- ❖ Provide systems, resources and training opportunities to achieve continuous improvement.
- ❖ Maintain global standards in education, training and services.

PROGRAMME EDUCATIONAL OBJECTIVES

PEO1: PROFESSIONALISM & CITIZENSHIP

To create and sustain a community of learning in which students acquire knowledge and learn to apply it professionally with due consideration for ethical, ecological and economic issues.

PEO2: TECHNICAL ACCOMPLISHMENTS

To provide knowledge based services to satisfy the needs of society and the industry by providing hands on experience in various technologies in core field.

PEO3: INVENTION, INNOVATION AND CREATIVITY

To make the students to design, experiment, analyze, interpret in the core field with the help of other multi disciplinary concepts wherever applicable.

PEO4: PROFESSIONAL DEVELOPMENT

To educate the students to disseminate research findings with good soft skills and become a successful entrepreneur.

PEO5: HUMAN RESOURCE DEVELOPMENT

To graduate the students in building national capabilities in technology, education and research.

CODE OF CONDUCT FOR THE LABORATORIES

1. All students must observe the Dress Code while in the laboratory.
2. Sandals or open-toed shoes are NOT allowed.
3. Foods, drinks and smoking are NOT allowed.
4. All bags must be left at the indicated place.
5. The lab timetable must be strictly followed.
6. Be PUNCTUAL for your laboratory session.
7. Program must be executed within the given time.
8. Noise must be kept to a minimum.
9. Workspace must be kept clean and tidy at all time.
10. Handle the systems and interfacing kits with care.
11. All students are liable for any damage to the accessories due to their own negligence.
12. All interfacing kits connecting cables must be RETURNED if you taken from the lab supervisor.
13. Students are strictly PROHIBITED from taking out any items from the laboratory.
14. Students are NOT allowed to work alone in the laboratory without the Lab Supervisor
15. USB Ports have been disabled if you want to use USB drive consult lab supervisor.
16. Report immediately to the Lab Supervisor if any malfunction of the accessories, is there.

Before leaving the lab

- Place the chairs properly.
- Turn off the system properly
- Turn off the monitor.
- Please check the laboratory notice board regularly for updates.

CONTENTS

S.NO	NAME OF THE EXPERIMENT	PAGE NO
1.	Time Division Multiplexing	1
2.	Pulse Code Modulation & Demodulation	5
3.	Differential Pulse Code Modulation & Demodulation	8
4.	Delta Modulation	13
5.	Amplitude Shift Keying	17
6.	Frequency Shift Keying	23
7.	Phase Shift Keying	29
8.	Differential Phase Shift Keying	34
9.	Quadrature Phase Shift Keying	41
10.	Digital Companding (A-Law & μ -Law)	46
11.	Linear Block Code- Encoder and Decoder	50
12.	Binary Cyclic Code- Encoder and Decoder	53

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DEPT.OF ECE – DC LAB MANUAL

EXPERIMENT NO-1

TIME DIVISION MULTIPLEXING & DEMULTIPLEXING

Aim:

Study of 4 Channel Analog Multiplexing and De multiplexing Techniques.

Apparatus:

1. Time division multiplexing & demultiplexing trainer kit.
2. CRO (30 mhz)
- 3.Patch chords.

Theory:

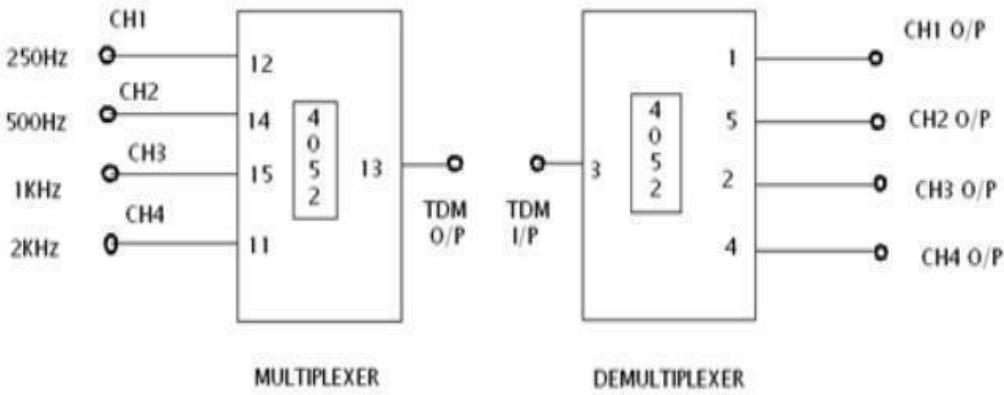
The TDM is used for transmitting several analog message signals over a Communication channel by dividing the time frame into slots, one slot for each message signal. The four input signals, all band limited by the input filters are sequentially sampled, the output of which is a PAM waveform containing samples of the input signals periodically interlaced in time. The samples from adjacent input message channels are separated by T_s/M , where M is the number of input channels. A set of M pulses consisting of one sample from each of the input M-input channels is called a frame.

At the receiver the samples from individual channels are separated by carefully synchronizing and are critical part TDM. The samples from each channel are filtered to reproduce the original message signal. There are two levels of synchronization. Frame synchronization is necessary to establish when each group of samples begins and word synchronization is necessary to properly separate the samples within each frame.

Besides the space diversity & frequency diversity there is a method of sending multiple analog signals on a channel using “TIME DIVISION MULTIPLEXING & DEMULTIPLEXING” Technique.

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CIRCUIT DIAGRAM:



Procedure:

Multiplexing:

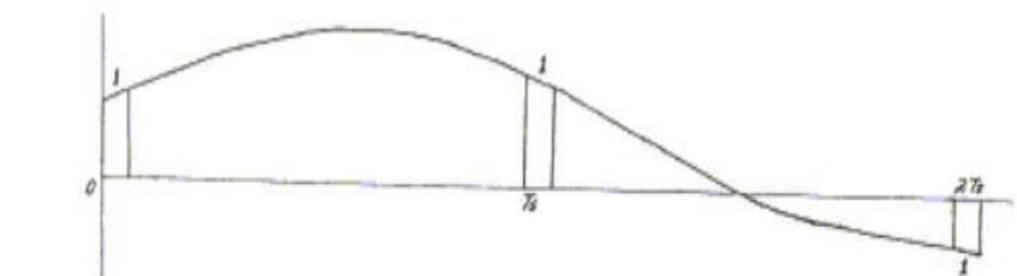
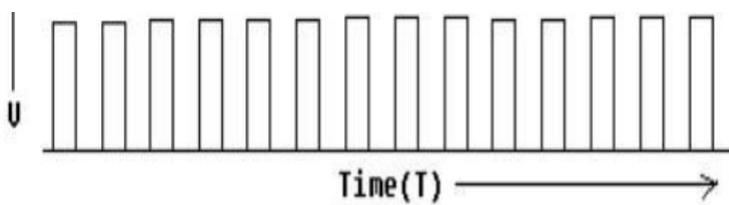
1. Connect the circuit as shown in diagram.
2. Switch ON the power supply.
3. Set the amplitude of each modulating signal as 5v peak-peak.
4. Monitor the outputs at test points 5,6,7,8. these are natural sampling PAM outputs.
5. Observe the outputs varying the duty cycle pot(P5). The PAM outputs will vary with 10% to 50% duty cycle.
6. Try varying the amplitude of modulating signal corresponding each channel by using amplitude pots P1,P2,P3,P4. Observe the effect on all outputs.
7. Observe the TDM output at pin no.13 (at TP9) OF 4052. all the multiplexer channel are observed during the full period of the clock(1/32 KHz).

Demultiplexing & Low Pass Filter:

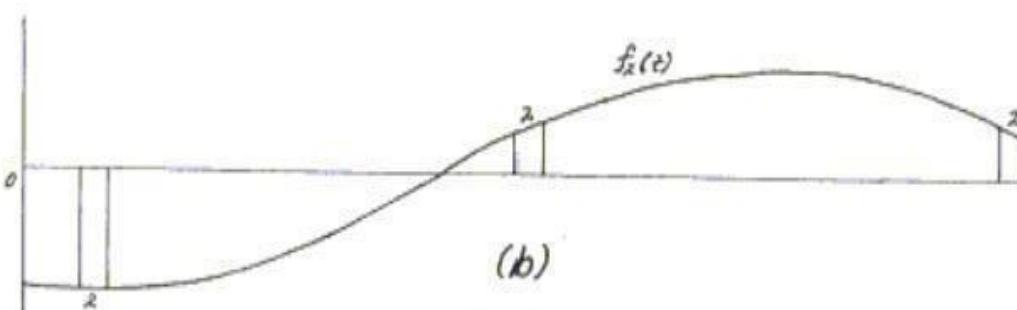
1. Connect the circuit as shown in diagram 2.
2. Observe the demultiplexed outputs at test points 13,14,15,16 respectively.
3. Observe by varying the duty cycle pot P5 and see the effect on the outputs.
4. Observe the low pass filter outputs for each channel at test points 17,18,19,20 and at sockets channels CH1,CH2,CH3,CH4. These signals are true replica of the inputs. These signals have lower amplitude.

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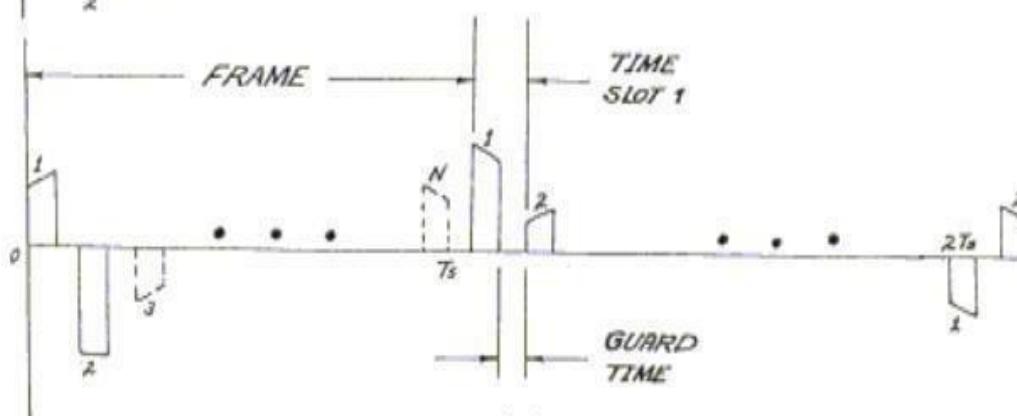
Expected Waveforms:



(a)



(b)



(c)

fig (2) TDM output should be natural sampling

Fig (a) message1 (b) message 2 and

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Result:

Questions:

1. Draw the TDM signal with 2 signals being multiplexed over the channel?
2. Define guard time & frame time?
3. Explain block schematic of TDM?
4. How TDM differ from FDM?
5. What type of filter is used at receiver end in TDM system?
6. What are the applications of TDM?
7. If 2 signal band limited to 3 kHz, 5KHz & are to be time division multiplexed. What is the maximum permissible interval between 2 successive samples.?
8. Is the bandwidth requirement for TDM & FDM will be same?
9. Is TDM system is relatively immune to interference with in channels (inter channel cross talk) as compared to FDM?
10. Is the FDM susceptible to harmonic distortion compared to TDM?
11. In what aspects, TDM is superior to FDM?

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EXPERIMENT NO-2

PULSE CODE MODULATION & DEMODULATION

Aim: To convert an analog signal into a pulse digital signal using PCM system and to convert the digital signal into analog signal using PCM demodulation system.

Apparatus:

1. PCM transmitter trainer.
2. PCM receiver trainer.
3. CRO and connecting wires.

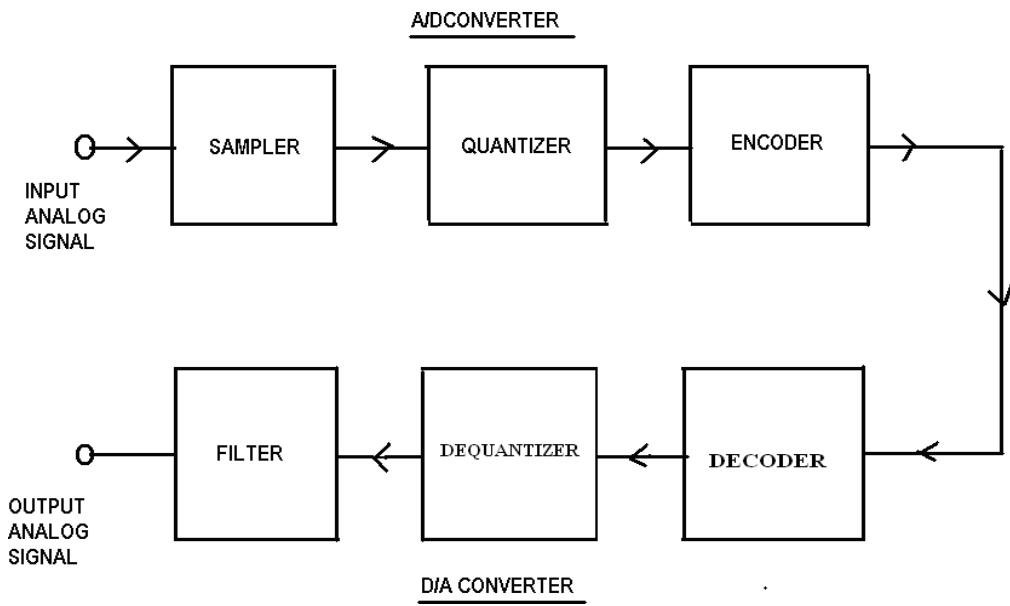
Theory:

In the PCM communication system, the input analog signal is sampled and these samples are subjected to the operation of quantization. The quantized samples are applied to an encoder. The encoder responds to each such a sample by generation unique and identifiable binary pulse. The combination of quantize and encoder is called analog to digital converter. It accepts analog signal and replaces it with a successive code symbol, each symbol consists of a train of pulses in which the each pulse represents a digit in arithmetic system.

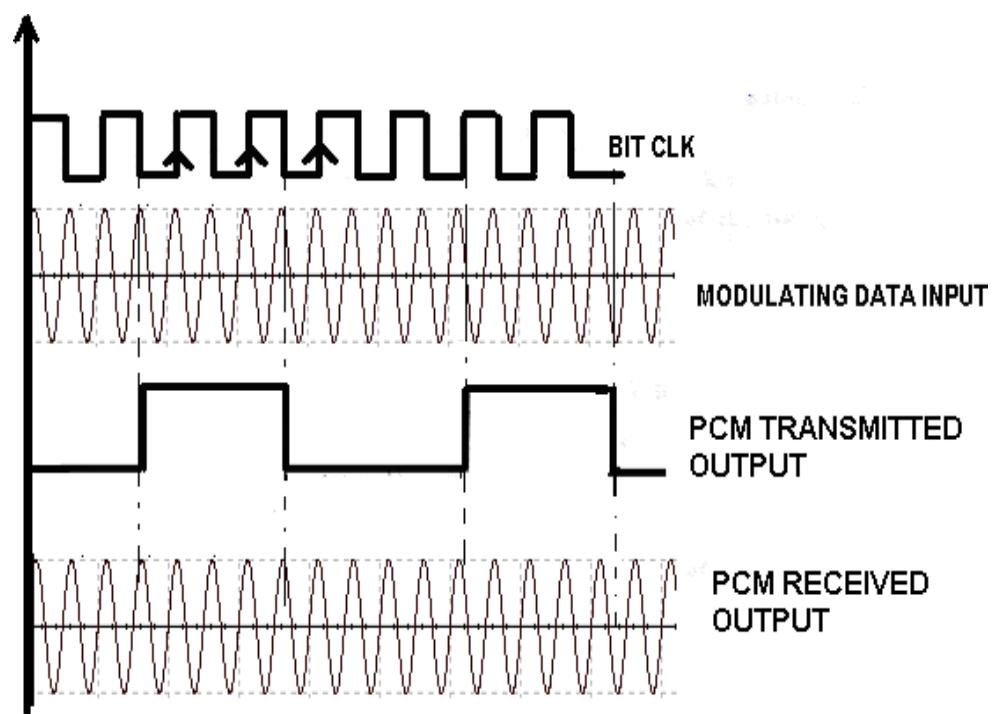
When this digitally encoded signal arrives at the receiver, the first operation to be performed is separation of noise which has been added during transmission along the channel. It is possible because of quantization of the signal for each pulse interval; it has to determine which of many possible values has been received.

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Block Diagram:



Output Waveform:



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Procedure:

1. The two inputs of function generator are connected to channel -0 and channel-1 simultaneously that is DC₁ output to channel -0 and DC₂ to channel-1.
2. With the help of oscillator DC₁ output is adjusted to 0 volts.
3. Transmitter and receiver are connected by the synchronization of clock pulses and by connecting ground transmitter to ground receiver.
4. The transmitter is connected to the input of receiver to go the original signal at the receiver output.
5. After connection is made the inputs channel 1 and channel 0 are noted. The sampled output of bit channels are taken by connecting DC₁ output to channel 0 and DC₂ output to channel-1.
6. The phase shift of a channel can be obtained by comparing the input and output of channels at the transmitter block.
7. Thus the output of transmitter can be noted down and input of receiver is similar to that.
8. The receiver output signals are noted down at channel 0 and channel 1 of the receiver block.

Result:

Questions:

1. What is the expression for transmission bandwidth in a PCM system?
2. What is the expression for quantization noise /error in PCM system?
3. What are the applications of PCM?
4. What are the advantages of the PCM?
5. What are the disadvantages of PCM?

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EXPERIMENT NO-3

DIFFERENTIAL PULSE CODE MODULATION

Aim:

To study the differential pulse code modulation and demodulation by sending variable frequency sine wave and variable DC signal outputs.

Apparatus:

1. DPCM Trainer kit
2. Patch cards
3. CRO- (0-20MHz)
4. AC Adapter ($\pm 8V$)
5. CRO Probes.

Theory:

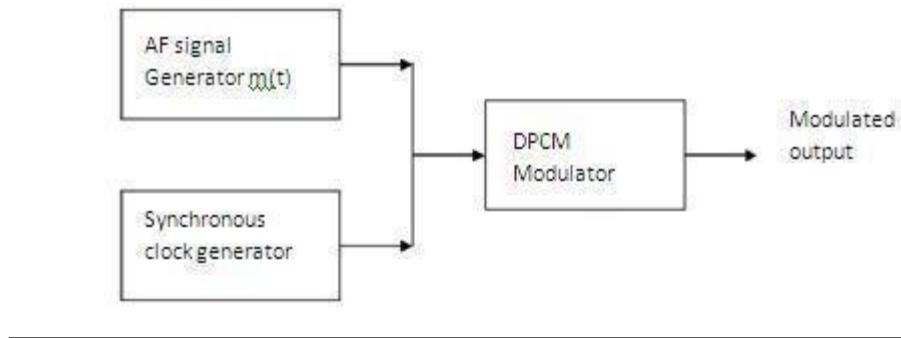
In Differential Pulse Code Modulation (DPCM), instead of quantizing each sample, the difference between the two successive samples is quantized, encode, and transmitted as in the PCM. This particularly useful in the Voice communication, because in this case two successive samples do not differ much in amplitude.

Thus, the difference signal is much less in amplitude than the actual sample and, hence, less number of quantization levels is needed. Therefore, the number of bits per code is reduced, resulting in a reduced bit rate. Thus, the band width required in this case is less than the one required in PCM.

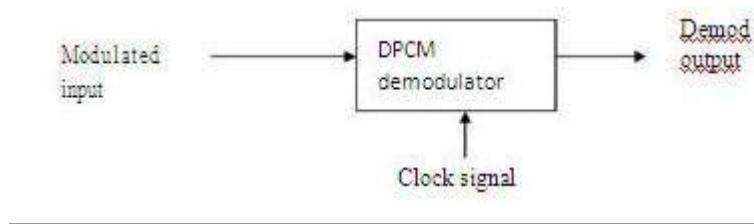
The disadvantage of DPCM is that the modulator and demodulator circuits are more complicated than those in PCM.

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DPCM MODULATOR

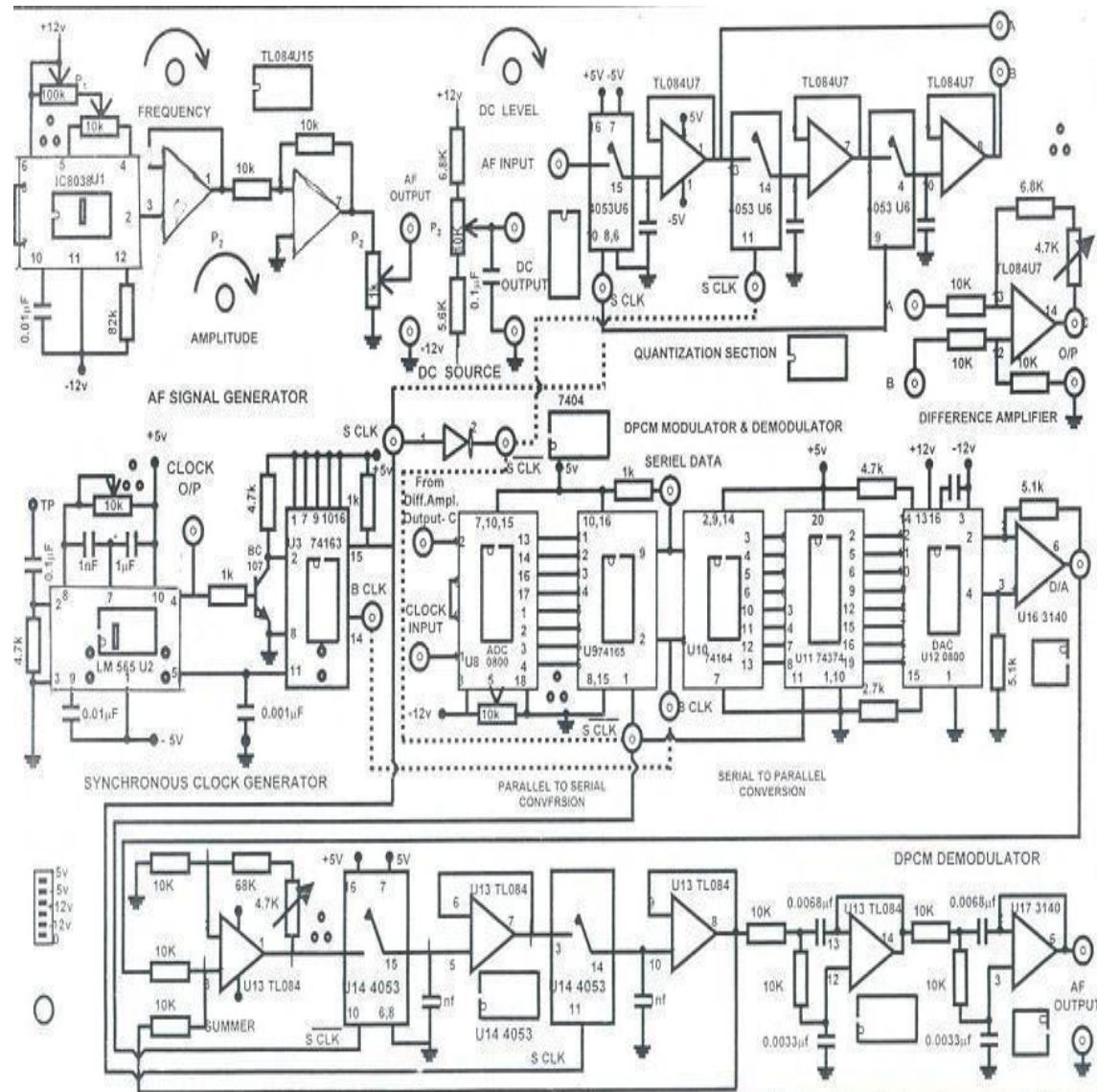


DPCM DEMODULATOR



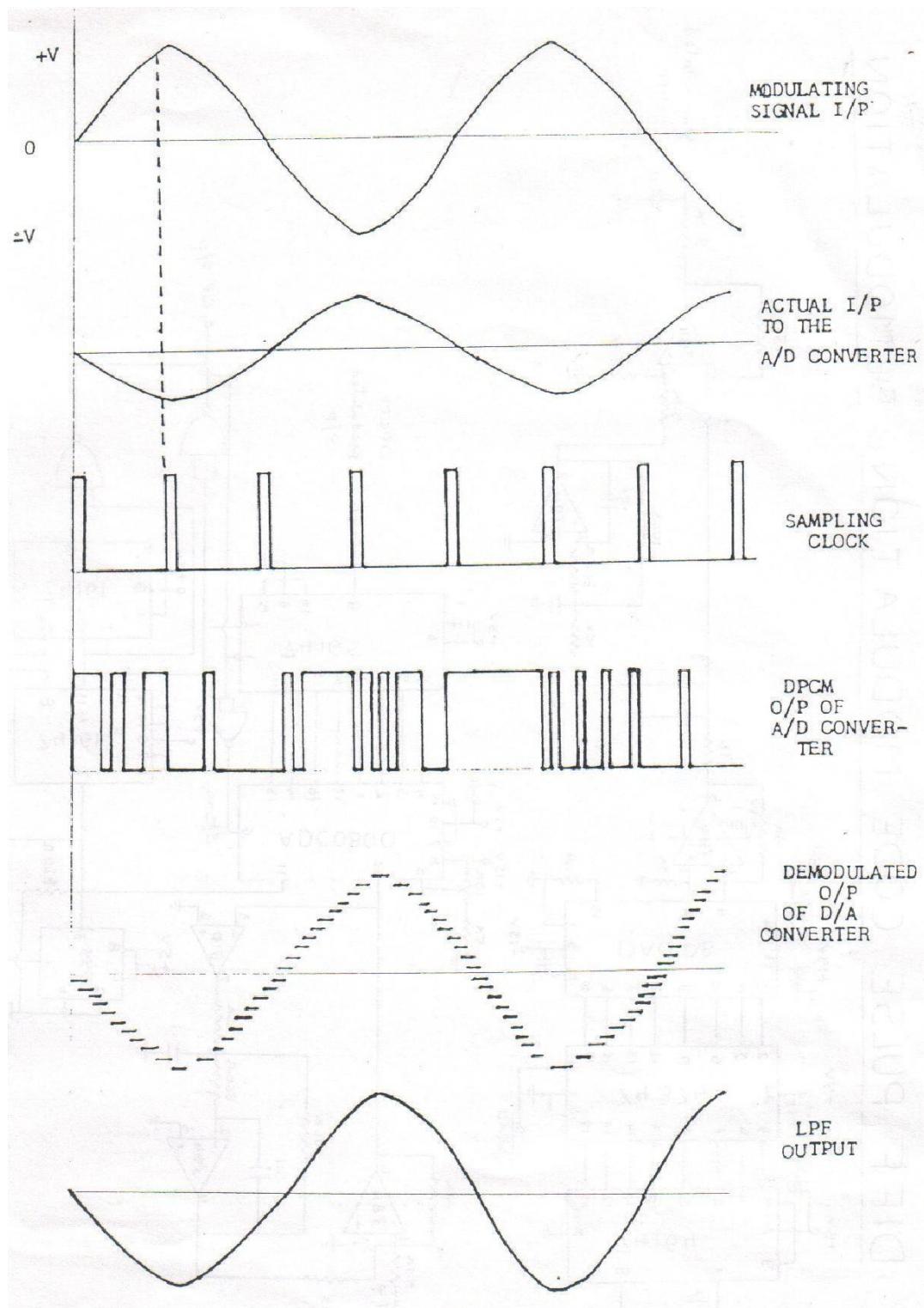
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Circuit Diagram:



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Model Waveforms:



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Procedure:

1. Switch on the Kit.
2. Apply the variable DC signal to the input terminals of DPCM modulator.
3. Observe the sampling signal output on CRO
4. Observe the output of DPCM on the second channel of CRO
5. By adjusting the DC voltage potentiometer we can get the DPCM output from 0000 0000 to 1111 1111.
6. Now, disconnect the DC voltage and apply AF oscillator output to the input of the DPCM modulator
7. observe the output of conditioning amplifier (differential output) and DPCM outputs in synchronization with the sampling signal.
8. During demodulation, connect DPCM output to the input of demodulation and observe the output of Demodulator

Observations:

1. Amplitude of AF signal = -----
2. Frequency of AF signal = -----
3. Amplitude of Synchronous clock signal = -----
4. Frequency of Synchronous clock signal = -----
5. Amplitude of DPCM Modulated signal = -----
6. Frequency of DPCM Modulated signal = -----
7. Amplitude of demodulated output = -----
8. Frequency of demodulated output = -----

Result:

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EXPERIMENT NO-4

DELTA MODULATION & DEMODULATION

Aim:

To study the Delta modulation process by comparing the present signal with the previous signal of the given modulating signal.

Apparatus:

1. Delta Modulation trainer
2. CRO
3. Connecting wires.

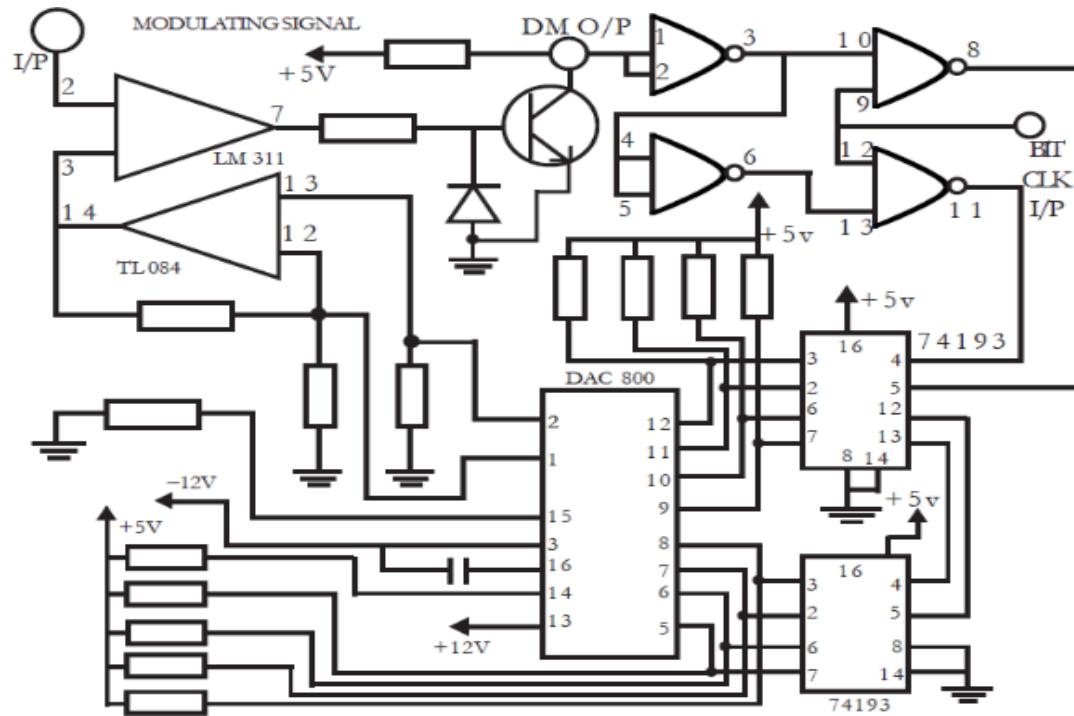
Theory:

DM uses a single bit PCM code to achieve digital transmission of analog signal. With conventional PCM each code is binary representation of both sign and magnitude of a particular sample. With DM, rather than transmitting a coded representation of a sample a single bit is transmitted, which indicates whether the sample is smaller or larger than the previous sample. The algorithm for a delta modulation system is a simple one. If the current sample is smaller than the previous sample then logic 0 is transmitted or logic 1 is transmitted if the current sample is larger than the previous sample. The input analog is sampled and converted to a PAM signal followed by comparing it with the output of the DAC. The output of the DAC is equal to the regenerated magnitude of the previous sample which was stored in the up/down counter as a binary number. The up/down counter is incremented or decremented whether the previous sample is larger or smaller than the current sample. The up/down counter is clocked at a rate equal to the sample rate. So, the up/down counter is updated after each comparison.

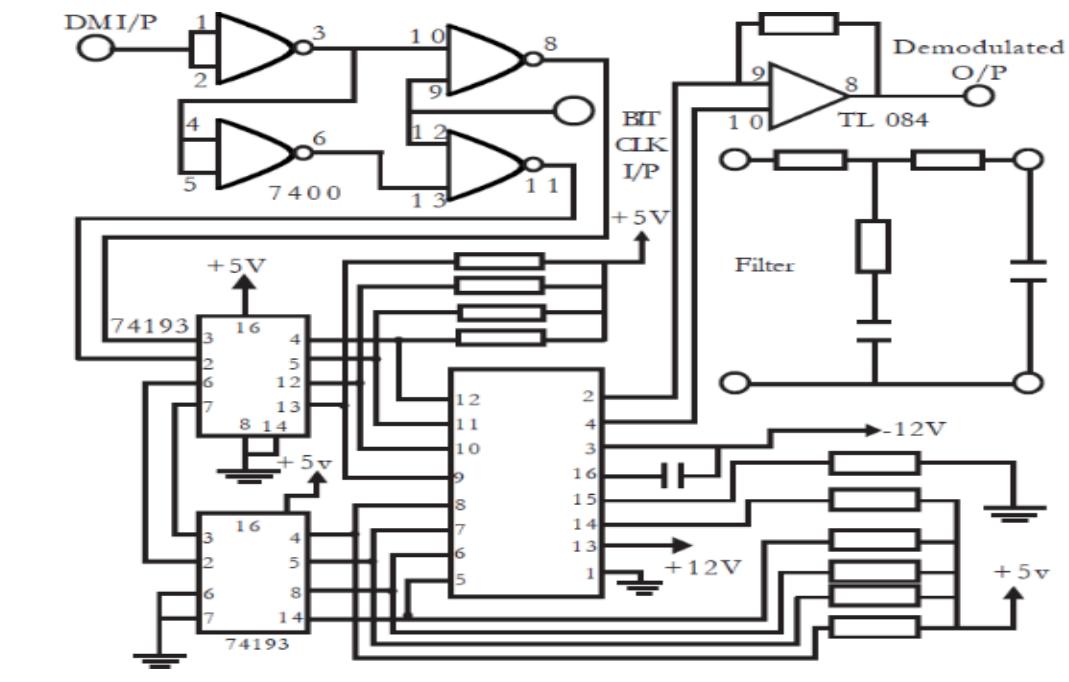
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Circuit Diagram:-

Modulator:-



Demodulator:-

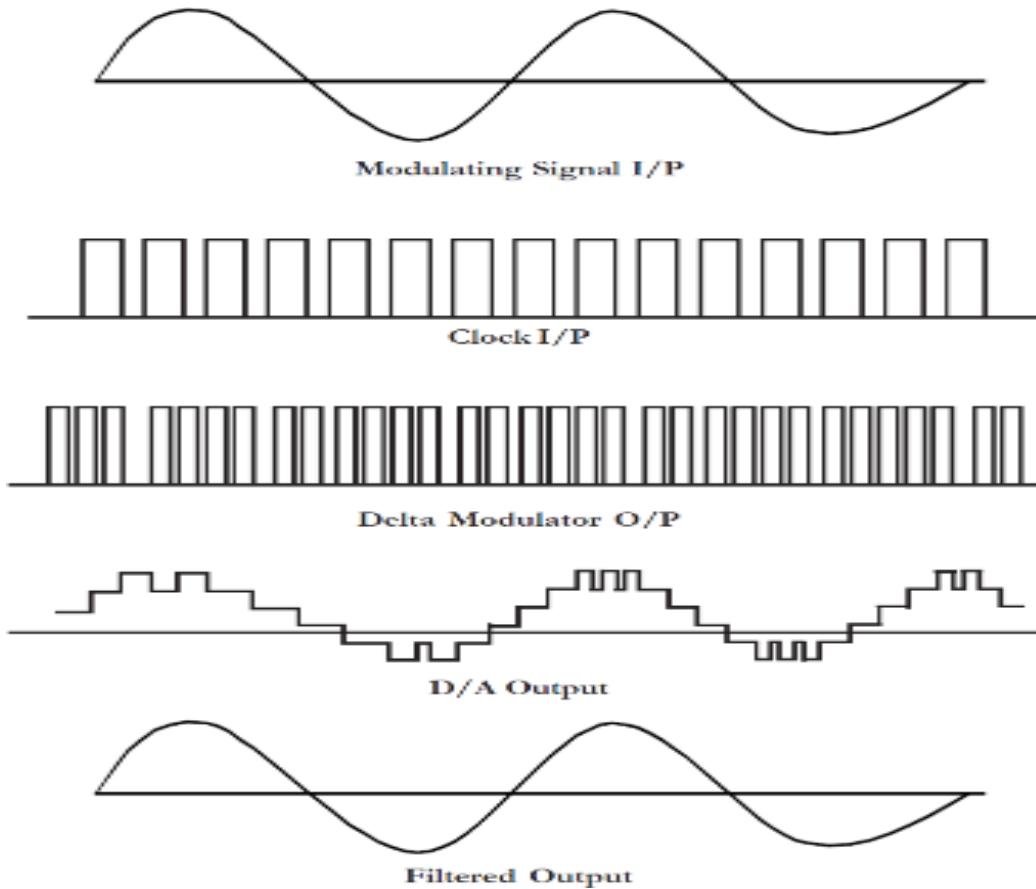


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Procedure:

1. Switch on the experimental board
2. Connect the clock signal of Bit clock generator to the bit clock input of Delta modulator circuit.
3. Connect modulating signal of the modulating signal generator to the modulating signal input of the Delta modulator.
4. Observe the modulating signal on Channel 1 of CRO
5. Observe the Delta modulator output on channel 2 of CRO
6. Connect the DM o/p of modulator to the DM I/P of Demodulator circuit.
7. Connect the clock signal to the Bit clock I/P of Demodulator circuit.
8. Observe the demodulated o/p on channel 2 of CRO.
9. Connect the demodulated o/p to the filter input of demodulator circuit.
10. Observe the demodulated o/p with filter on CRO.

Expected Waveforms:



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Result:

Questions:

- 1.What is Delta Modulation?
- 2.Differentiate DM and ADM.
- 3.What are the drawbacks of DM and what is the remedy?
- 4.How DM differ from PCM?
- 5.What is slope overload distortion?

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EXPERIMENT NO-5

ASK MODULATION AND DEMODULATION

Aim:

To study the process of ASK modulation& demodulation and study various data formatting modulation and demodulation techniques.

Apparatus:

1. ASK MODULATION & DEMODULATION Trainer kit.
2. CRO 30MHz Dual Channel.
3. Patch Chords.

Theory:

Modulation also allows different data streams to be transmitted over the same channel. This process is called as ‘Multiplexing’ & result in a considerable saving in bandwidth no of channels to be used. Also it increases the channel efficiency.

The variation of particular parameter variation of the carrier wave give rise to various modulation techniques. Some of the basic modulation techniques are described as under.

ASK:-

In this modulation involves the variation of the amplitude of the carrier waves in accordance with the data stream. The simplest method of modulating a carrier with a data stream is to change the amplitude of the carrier wave every time the data changes. This modulation technique is known as amplitude shift keying.

The simplest way of achieving amplitude shift keying is ‘ON’ the carrier whenever the data bit is ‘HIGH’ & switching ‘OFF’ when the data bit is low i.e. the transmitter outputs the carrier for HIGH & totally suppresses the carrier for low. This technique is known as ON-OFF keying Fig. illustrates the amplitude shift keying for the given data stream.

Thus,

DATA = HIGH CARRIER TRANSMITTED

DATA = LOW CARRIER SUPPRESSED

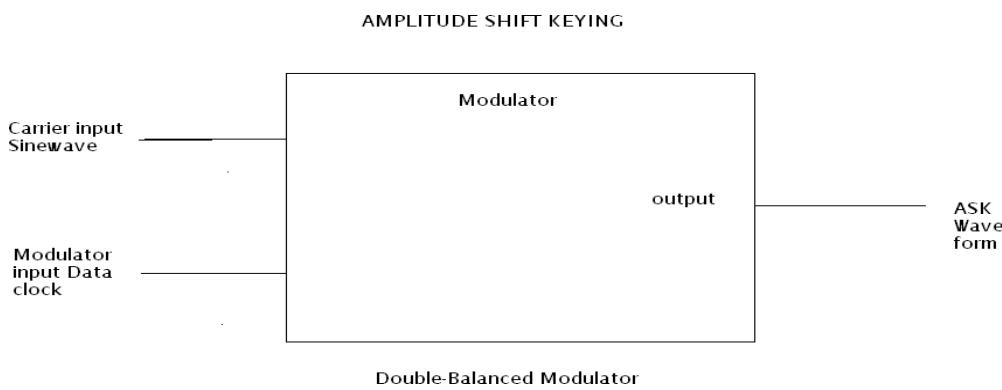
The ASK waveform is generated by a balanced modulator circuit, also known as a linear multiplier, As the name suggests, the device multiplies the instantaneous signal at its two inputs, the output voltage being product of the two input voltages at any instance of time. One of the input is a/c coupled ‘carrier’ wave of high frequency. Generally the carrier wave is a sinewave since any other waveform would increase the bandwidth imparting any advantages requirement without improving or to it. The

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other i/p which is the information signal to be transmitted, is D.C. coupled. It is known as modulating signal.

In order to generate ASK waveform it is necessary to apply a sine wave at carrier input & the digital stream at modulation input. The double balanced modulator is shown in fig.

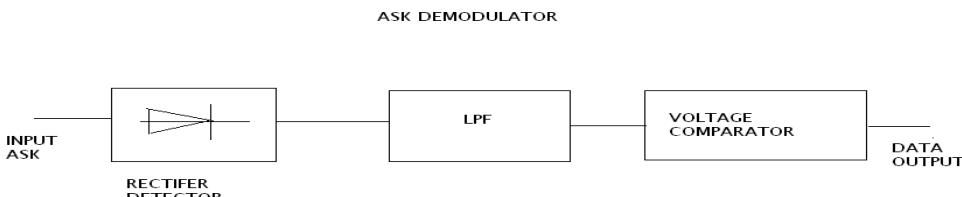
Block Diagram:



The data stream applied is unipolar i.e. 0Volt at logic LOW & +4.5Volts at logic HIGH. The output of balanced modulator is a sinewave, unchanged in phase when a data bit ‘HIGH’ is applied to it. In this case the carrier is multiplied with a positive constant voltage when the data bit LOW is applied, the carrier is multiplied by 0 Volts, giving rise to 0Volt signal at modulator’s o/p.

The ASK modulation results in a great simplicity at the receiver. The method to demodulate the ASK waveform is to rectify it, pass it through the filter & ‘square up’ the resulting waveform. The o/p is the original digital data stream. Fig. shows the functional blocks required in order to demodulate the ASK waveform at receiver.

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Circuit Description:-

Carrier Generation:-

The function of the carrier is to generate a stable sine wave signal at the rest frequency, when no modulation is applied. It must be able to linearly change frequency when fully modulated, with no measurable change in amplitude.

Sine wave is generated by using the colpitts Oscillator. 500KHz and 1MHz frequencies are selected.

Modulation Generation:-

The square wave generated by 555 and is given to 74121. the o/p of this multivibrator is used as a clock i/p to a decade counter 7490. Which generates the modulating data outputs D1,D2, D3,D4.

Modulator:-

The ASK215 Modulator is based on U2(LM 1496). It is configured as a linear multiplier. At any movement of time the o/p of this U2(PIN 12) is proportional to the instantaneous product of the CARRIER INPUT and MODULATION INPUT signals which serves as two inputs to this U2. The CARRIER INPUT can be monitored at TP7 & The MODULATION INPUT can be monitored at TP8.

The o/p voltage from U2 can be adjusted in amplitude by potentiometer P3(5K). it is now fed to the OP-AMP U3, LF 356 at its non-inverting terminal(pin 3). The op-amp configured as a simple non inverting amplifier with the gain of 2.47. the o/p(pin 6 is a/c coupled by capacitor C18 to appear at the o/p of OUTPUT socket.

DC bias can be added to both CARRIER INPUT signal & MODULATION INPUT signals by varying the pots P1&P2 respectively. This action takes place prior

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to signal multiplication. The DC bias from both the signals can be removed by careful setting of the two potentiometers.

Demodulation:-

The ASK demodulator comprises of

- 1) op-amp ICU6A configured as a unity gain, non inverting buffer, and
- 2) A simple half wave rectifier circuit, consisting diode D1 and resistor R72.

The incoming ASK signal can be monitored at TP12. the signal at TP12 is then buffered by ICU6A & then rectified by half wave rectified CKT comprising of Diode D5 & resistor R72. This removes the negative half cycle of the wave form. The output of rectifier is available at OUTPUT socket of the demodulator & can be monitored at TP13. example waveforms are as shown in the timing diagram in Fig.

Low Pass Filters:-

The low pass filter block consists of two fourth-order butter worth low pass filter circuit. The filter is identical & i.e. is described in the section to follow.

The input signal to this block is first buffered by the op-amp ICU6B. The op-amp is simply configured as a noninvert in, unity-gain buffer. The buffer output(TP15) is then fed into data squaring circuit. The final o/p's of the filter can be monitored at TP15.

Data Squaring Circuits:-

The data squaring circuit ‘square up’ the input signal. It does this with the help of voltage comparator. The function of comparator circuit is identical & hence only one is described. The input is connected to the non-inverting(+ve) input(pin 5) of the voltage comparator ICU4A whose inverting (-ve) input(pin 4) is connected to a voltage divider network of resistors R61, R60 & variable Resistor P4 through resistor R59. the input impedance of the comparator circuit is set to 100k by resistor R58. A hysteresis of 0.3V is set by resistor R59& R57. the slider voltage of can be adjusted from 2.2V to +2.2V.

The output of the comparator is 0V when the input at inverting terminal is more positive then the input at non inverting terminal.

Procedure:

Modulation:

1. Connect the sinewave 500KHz from the carrier generator TP1 to the carrier input of the modulator TP7.

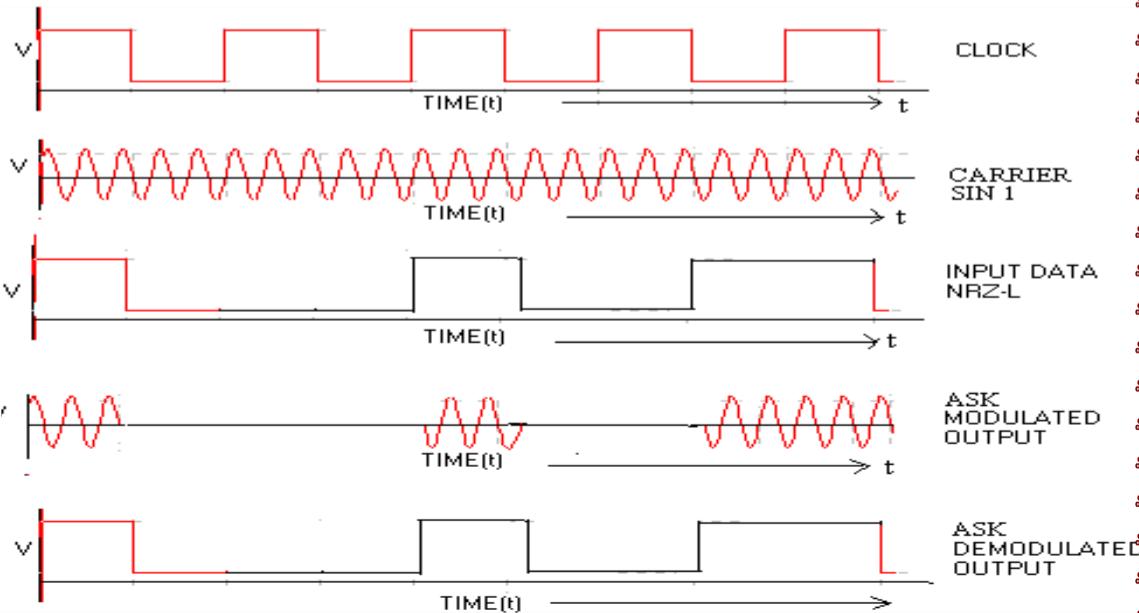
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2. And also connect data clock D1 i.e., modulation signal TP3 to the modulation input TP8.
3. Switch ON the power supply.
4. Observe the output at TP9.
5. By varying the gain pot P3 observe the ASK output at TP10.
6. Adjusting the carrier offset and modulation offset we can observe the ASK output.
7. By changing the carrier signal 1MHz and different data clocks D2,D3,D4 observe the output.

Demodulation:

1. Connect ASK output TP10 to the rectifier input TP12 and observe the waveform.
2. Now connect rectifier output TP13 to the low pass filter input TP14 and observe the output at TP15.
3. CONNECT LPF output TP15 to the data squaring circuit input TP16 and observe the demodulation output waveform at TP17.
4. By changing the different data clocks and observe the demodulation output.

Expected Waveforms:



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Result:

Questions:

- 1.If the bit rate of an ASK signal is 1200bps,what is the baud rate?
- 2.Is ASK highly susceptible?
3. What are the characteristics of transmission medium which effect speed of transmission in ASK?
4. Find the minimum band width for an ASK signal transmitting at 2000bps.The transmission made is half duplex?
5. If B.W is 5000Hz for an ASK signal, what are the baud rate?
6. What is the advantage of ON-OFF keying () in ASK?
7. Given the bandwidth of 10KHz(1Hz to 1KHz), Find the band width for upper side & lower side band of carrier in full duplex ASK?
8. For the above problem, what are the carrier frequencies in upper & lower side bands?

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EXPERIMENT NO-6

FREQUENCY SHIFT KEYING

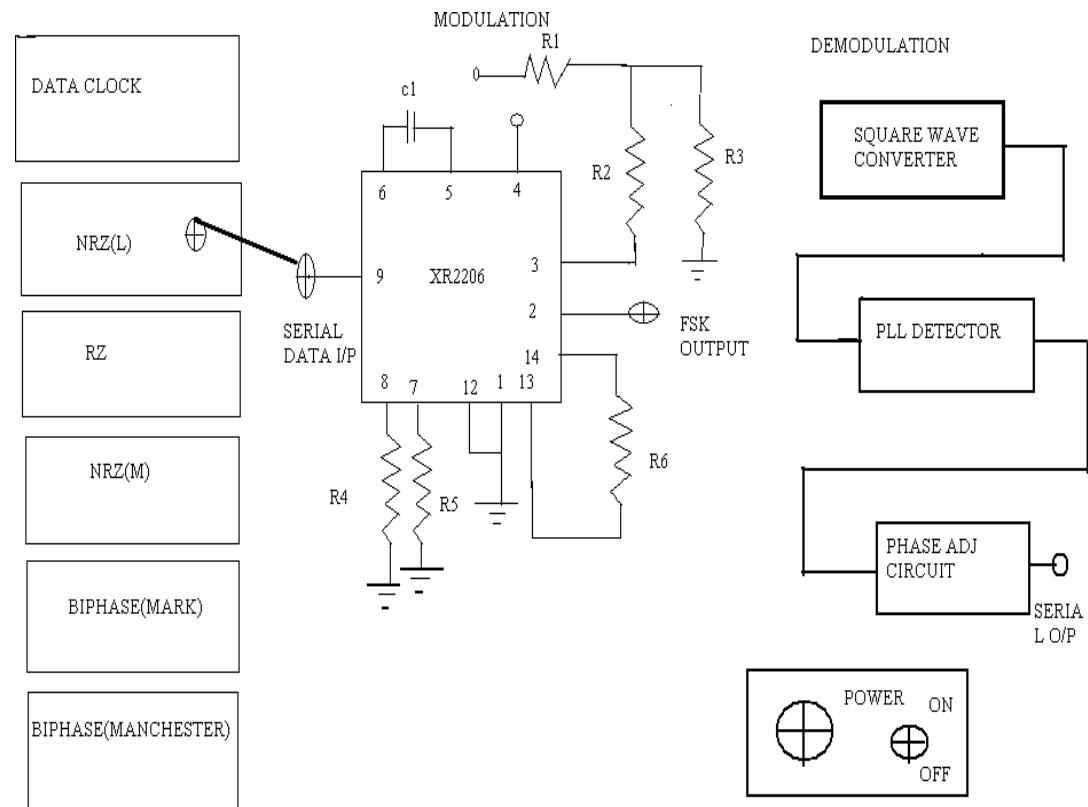
Aim:

1. To generate FSK Modulation
2. To Demodulate the FSK signals
3. To generate
NRZ(L), RZ, NRZ(M), BIPHASE(MARK), BIPHASE(MANCHESTER).

Apparatus:

1. Frequency Shift Keying kit
2. C.R.O (30MHz)
3. Patch cords

Circuit Diagram:



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Theory:-

Binary FSK is a form of constant-amplitude angle modulation and the modulating signal is a binary pulse stream that varies between two discrete voltage levels but not continuous changing analog signal. In FSK, the carrier amplitude(V_c) remains constant with modulation and the carrier radian frequency(ω_c) shifts by an amount equal to $\pm\Delta\omega/2$. The frequency shift is proportional to the amplitude and polarity of the input binary signal. For example, a binary 1 could be +1 volt and a binary zero could be -1 volt producing frequency shifts of $\pm\Delta\omega/2$ and $-\Delta\omega/2$ respectively. The rate at which the carrier frequency shifts is equal to the rate of change of the binary input signal $v_m(t)$. thus the output carrier frequency deviates(shifts) between $\omega_c+\Delta\omega/2$ and $\omega_c-\Delta\omega/2$ at the rate equal to f_m .

Data Formating:-

A modulation code is defined as a rule by which a serial train of binary data is converted to a signal suitable for transmission. Some of the commonly used codes are listed for study in this experiment. There are few others which are outside the scope of this experiment.

In serial data transmission, a ‘symbol’ is a signal level that is held for a length of time. The capacity of a channel is the symbol rate. This is the symbols per second or baud. Channel capacity has the units of symbols per second or baud. Some modulation codes require several symbols per bit of data. For example self clocking codes require two symbols per bit of data. The various codes are described below. Relative features of the codes are given in the table. The waveform diagram the patterns for the serial train 11001100.

Non-return to zero(NRZ):-

This is level type code and is one that is widely used in serial data transmission. A ‘0’ is low level and a ‘1’ is a high level.

Return to Zero(RZ):-

This is an impulse type code where a ‘1’ is represented by a high level that returns to zero. Its advantage is power conservation as transmission takes place only for ‘1’.

NRZ(M):-

If the logic ‘0’ is to be transmitted the new level is inverse of the previous level i.e., change in level occurs. If ‘1’ is transmitted the level remains unchanged.

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Biphase(Mark):-

This is an edge type invertible self-clocking code in which each bit cell starts with an edge and for a ‘0’ an additional edge occurs during the middle of the bit cell.

Biphase(Manchester):-

This is a level type of code in which a ‘1’ bit cell is initially high and then has a high to low transition in the middle of the bit cell. A ‘0’ bit cell is initially low and has a low to high transition in the middle of the bit cell.

Circuit Description:-

Data clock Generator:-

The bit clock generator is design around the tim IC 555(U1) operated in astable mode. The 100Kohm preset P1 in conjunction with .0047microfarad capacitor in the timing circuit facilitates the frequency to be set and at any chosen value from 300Hz to 1KHz. This output is available at TP1.

Data Selection:-

The 8 bit parallel load serial shift IC 74165(U2) is used to generate the required word pattern. A dip switch is used to set ONE&ZERO pattern. The bit pattern set by the switch is parallely loaded by controlling the logic level at pin 1. The last stage output Q7 is coupled to the first stage input D0 in the shift register. The serial shift clock is given at pin 2. The 8 bit data set by the switch and loaded with the register parallely is now shifted serially right and circulated respectively. Thus the 8 bit word pattern is generated cyclically which is used as modulating signal in the FSK modulator. It is available at TP12.

Fsk Modulation:-

The XR-2206 can be operated with two separate timing resistors, R24 and R25, connected to the timing pin 7 and 8, respectively. Depending on the polarity of the logic signal at pin 9, either one or the other of these timing resistors is activated. If pin 9 is open-circuited or connected to a bias voltage>2V, only R24 is activated. Similarly, if the voltage level at pin 9 is<1v, only R25 is activated. Thus, the output frequency can be keyed between two levels. F1 and F2.

$F1=1/R24C9$ and $f2=1/R25C9$. In our circuit $R24=3.9\text{Kohm}$, $R25=6.8\text{Kohm}$, $C9= 100\text{nf}$.For split-supply operation, the keying voltage at pin 9 is referenced to V. the FSK output can be monitored at TP8.

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Demodulation:-

Square Wave Converter:-

The incoming FSK modulated signal can be monitored at TP9. This signal is then attenuated by resistor network R43,R44 then AC coupled via capacitor C12 to remove any dc component in the signal. The signal is connected to SIGIN input of the U12. The signal is first squared up by an inbuilt comparator and is connected to one of the input of on chip2 input EX-OR gate. The other 5 input of the gate is connected to the COMPIN input of IC U12. The output is monitored at TP10.

PLL Detector:-

A very useful application of the 565 PLL is as a FSK demodulator. In the 565 PLL the frequency shift is usually accomplished by driving a VCO with the binary data signal so that the two resulting frequencies correspond to the logic 0 and logic 1 states of the binary data signal. The frequencies corresponding to logic 1 and logic 0 states are commonly called the mark and space frequencies. Capacitive coupling is used at the input to remove a dc level. As the signal appears at the input of the 565, the loop to the input frequency and tracks it between the two frequencies with a corresponding dc shift at the output. Preset p2 and capacitor C15 determine the free-running frequency of the VCO. A three-stage RC ladder filter is used to remove the carrier component from the output. The high cutoff frequency of the ladder filter is chosen to be approximately halfway between the max keying rate and twice the input frequency. This output signal can be made logic compatible by connecting voltage comparator(u11) between the output of ladder filter and pin 6 of PLL.

Phase Adjustment Circuit:-

U17,U18 used as phase adjustment circuit. The output of voltage comparator is fed to pin 2 of U17 which is connected as monostable mode. And the output of U17 is again fed to U18. The output is available at pin 3 of U18 can be monitored at TP11. This is serial date of output.

Procedure:

Modulation:

1. Switch ON the power supply.
2. Set the data selection switch ('DATA SELECTION') to the desired code(say 11001100).
3. Set the switch (DATA ON-OFF) ON position. Observe the 8 bit Word pattern at TP12.

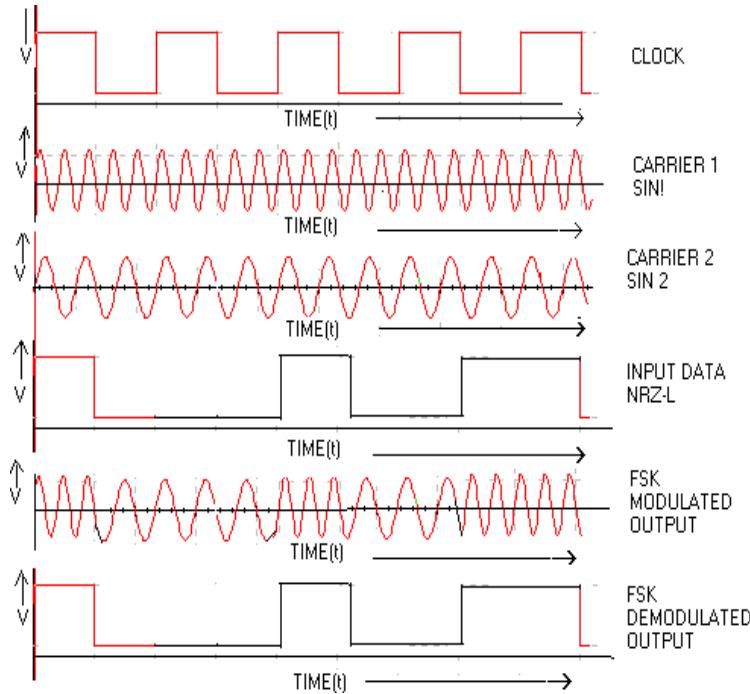
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4. Observe the data clock at TP1 and also observe the NRZ(L) at TP2,RZ at TP3,NRZ(M) at TP4, BIPHASE(MARK) at TP5,BIPHASE(MANCHESTER) at TP6.
5. Connect the patch cord as shown in diagram 1.Observe the corresponding FSK output at(when data is logic ‘1’, the frequency is high and data is logic ‘0’ the frequency is low)TP8.
6. Repeat the step 5 for other inputs.(like NRZ(M),RZ,BIPHASE) observe the corresponding FSK outputs.
7. Now change the data selection and repeat the above steps 3 to 6 and observe the corresponding FSK outputs.

Demodulation:

1. Connect the patch cords as shown in diagram.
2. The incoming FSK input is observed at TP9.
3. The output of ‘square wave converter’ is available at TP10. The serial data output is available at TP11.
4. Repeat the above steps 1,2,3 for other serial data inputs and observe the corresponding serial data outputs. These outputs are true replica of the orginal inputs.

Expected Waveforms:



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Result:

Questions:

- 1.Explain the concept of FSK?
- 2.Compare ASK, FSK & PSK?
- 3.Draw the waveforms of FSK?
4. What is M-ray signaling? What is its advantages over 2-ary signaling?
5. What are the different data coding formats & draw the waveforms what is advantages of Manchester coding over other formats?
6. Explain the demodulation scheme of FSK?
7. What is the formula for Band Width required in FSK?
8. What is the minimum B.W for an FSK signal transmitting at 2000bps(half duplex),if carriers are separated by 3KHz?
9. Is the FSK spectrum, a combination of two ASK spectra centered around two frequencies?
10. Is the FSK band width is more than ASK band width for a given band rate?
11. Is it more susceptible to noise than ASK?
12. What are the limiting factors of FSK?
13. Is the band rate & bit rate are same for FSK?

EXPERIMENT NO-7

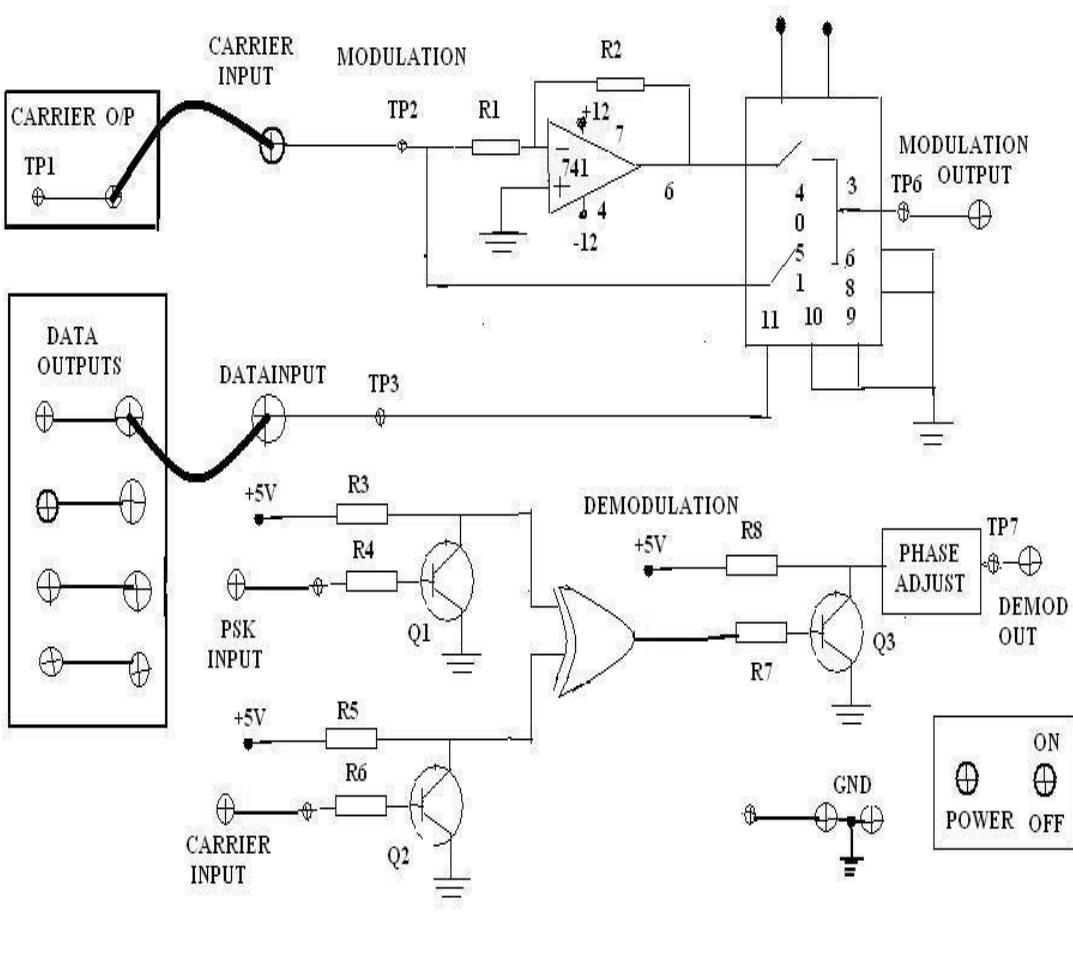
PHASE SHIFT KEYING

Aim: Study of carrier Modulation techniques by phase shift keying method.

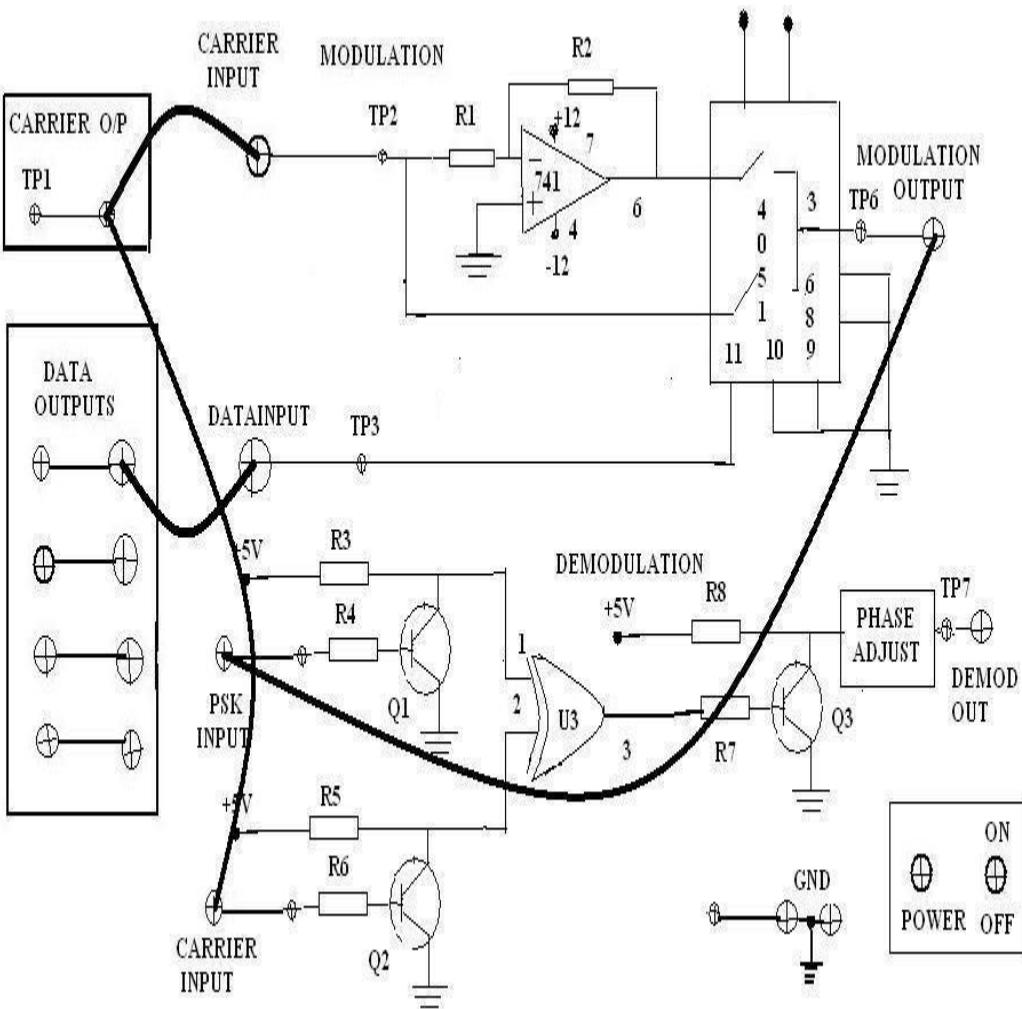
Apparatus:

1. Psk Modulation And Demodulation Trainer.
2. 30MHz Dual Trace Oscilloscope.
3. Patch chords

Circuit Diagram:



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Theory:

To transmit the digital data from one place to another, we have to choose the transmission medium. The simplest possible method to connect the transmitter to the receiver with a piece of wire. This works satisfactorily for short distances in some cases. But for long distance communication & in situations like communication with the aircraft, ship, vehicle this is not feasible. Here we have to opt for the radio transmission.

It is not possible to send the digital data directly over the antenna because the antenna of practical size works on very high frequencies, much higher than our data transmission rate.

To be able to transmit the data over antenna, we have to ‘modulate’ the signal i.e., phase, frequency or amplitude etc. is varied in accordance with the digital data. At receiver we separate the signal from digital information by the process of demodulation. After this process we are left with high frequency signal which we discard & the digital information, which we utilize.

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Modulation also allows different data streams to be transmitted over the same channel.

This process is called as ‘multiplexing’ & result in a considerable saving in bandwidth no of channels to be used. Also it increases the channel efficiency.

The variation of particular parameter variation of the carrier wave give rise to various modulation techniques. Some of the basic modulation techniques ASK,FSK, PSK,DPSK,QPSK.

Phase Shift Keying(PSK):

The PSK is a form of angle modulated, constant amplitude digital modulation. Digital communications because important with the expansion of the use of computers and data processing, and have continued to develop into a major industry providing the interconnection of computer peripherals and transmission of data between distant sites. Phase shift keying is a relatively new system, in which the carrier may be phase shifted by +90 degree for a mark, and by-90 degrees for a space. PSK has a number of similarities to FSK in many aspects, as in FSK, frequency of the carrier is shifted according to the modulating square wave.

Circuit Description:

In this IC 8038 is a basic wave form generator which generates sine, square, triangle waveforms. The sine wave generated by this 8038 IC is used as carrier signal to the system. This square wave is used as a clock input to a decade counter which generates the modulating data outputs.

The digital signal applied to the modulation input for PSK generation is bipolar i.e. have equal positive and negative voltage levels. When the modulating input is negative the output of modulator is a sine wave in phase with the carrier input. Where as for the positive voltage levels, the output of modulator is a sine wave which is shifted out of phase by 180 degree from the carrier input compared to the differential data stream. This happens because the carrier input is now multiplied by the negative constant level.

Thus the output changes in phase when a change in polarity of the modulating signal results. Fig shows the functional blocks of the PSK modulator & demodulator.

Modulation:-

IC CD 4051 is an analog multiplexer to which carrier is applied with and without 180 degree phase shift to the two multiplex inputs of the IC. Modulating data input is applied to its control input. Depending upon the level of the control signal,

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carrier signal applied with or without phase shift is steered to the output. the 180 degree phase shift to the carrier signal created by an operational amplifier using 741C.

Demodulation:-

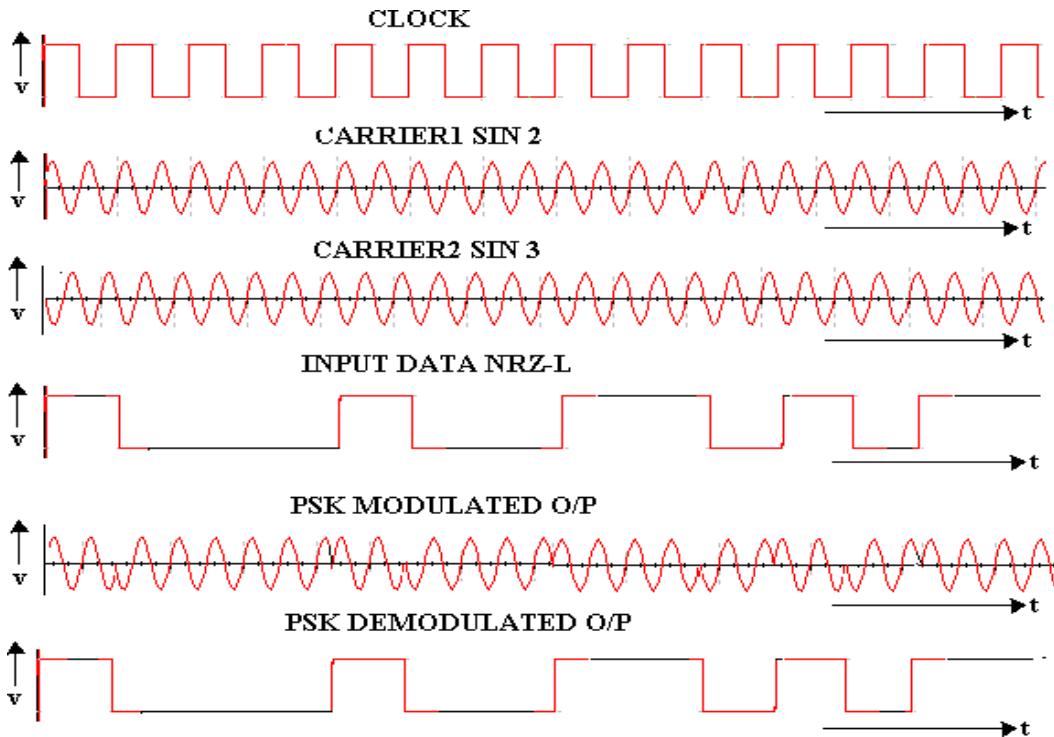
During the demodulation the PSK signal is converted into a +5volts square wave signal using a transistor and is applied to one input of an EX-OR gate. To the second input of the gate carrier signal is applied after conversion into a +5volts signal. So the EX-OR gate output is equivalent to the modulating data signal.

Procedure:

1. Now switch ON the trainer and see that the supply LED glows.
2. Observe the carrier output at TP1.
3. Observe the data outputs(D1,D2,D3,D4).
4. Now connect the carrier output TP1 to the carrier input of PSK modulator TP2 using patch chord(as shown in dig 1).
5. Connect the d1 to data input of PSK modulator TP3(As shown.in dig 1).
6. Observe the phase shifted PSK output waveform on CRO on channel 1 and corresponding data output on channel 2.
7. Repeat the steps 4,5,6 for data outputs D2,D3,D4 and observe the PSK outputs.
8. connect the PSK modulation output TP6 to the PSK input of demodulation TP4(as shown in dig 2).
9. connect the carrier output TP1 to the carrier input of PSK demodulation TP5.(As shown in dig 2).
10. Now, observe the PSK demodulated output at TP7 on CRO at channel 1 and corresponding data output on channel 2.
11. the demodulated output is true replica of data output.
12. Repeat the steps 8 to 10 for other data outputs D2,D3,D4.

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Expected Waveforms:



Result:

Questions:

1. Explain the concept of PSK?
2. Compare ASK, FSK, PSK?
3. Draw the waveforms of PSK?
4. What is M-ary signaling? What are its advantages over 2-ary signaling?
5. Explain the demodulation scheme of PSK?.
6. What is the advantage of PSK over ASK, FSK?
7. Will the smaller variations in the signal can be detected reliably by PSK?
8. Can we transmit data twice as for using 4-PSK as we can using 2-PSK?
9. What is the minimum B.W required in PSK?
10. Is the B.W in PSK is same as in ASK?
11. Is the maximum bit rate in PSK is greater than ASK?

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EXPERIMENT NO-8

DIFFERENTIAL PHASE SHIFT KEYING

Aim: To study operation Differential Phase shift Keying modulation & demodulation Techniques.

Apparatus:

1. DPSK MODULATION & DEMODULATION Trainer.
2. Oscilloscope 30MHz, Dual Channel
3. Path chords.

Block Diagram:

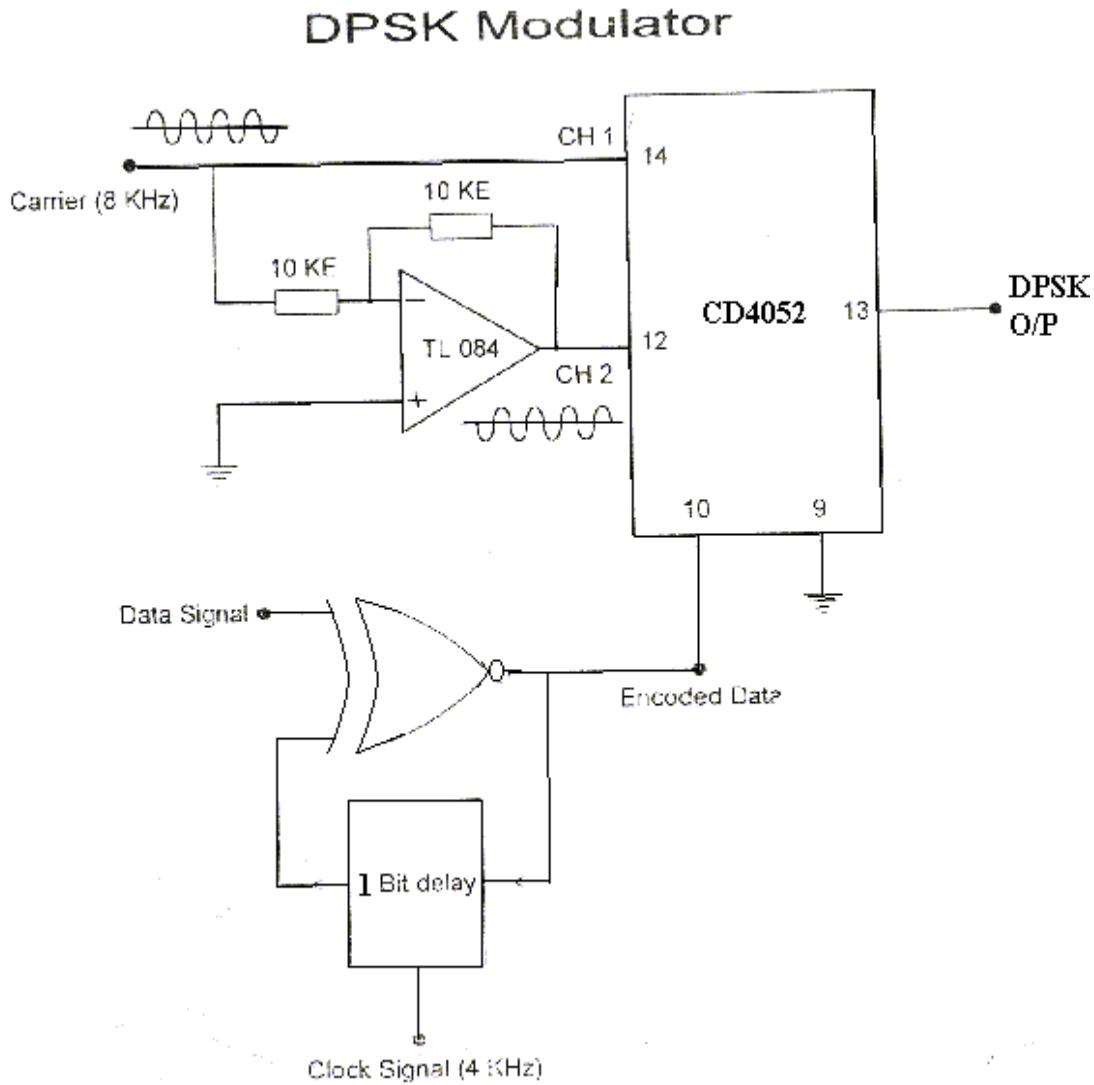
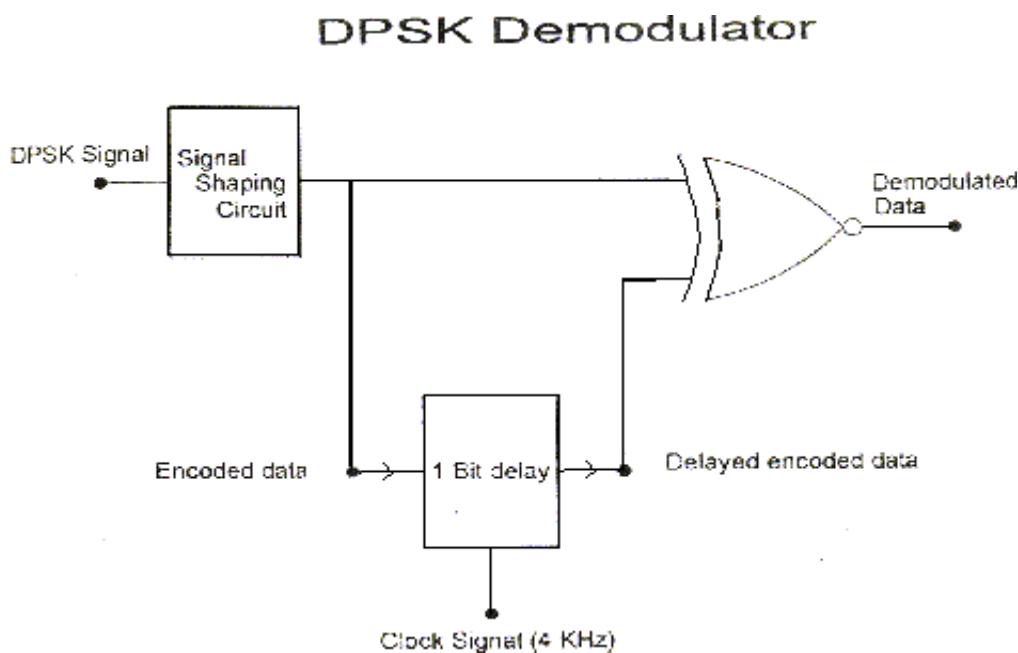


fig (1.1)



Theory:

To transmit the digital data from one place to another, we have to choose the transmission medium. The simplest possible method to connect the transmitter to the receiver with a piece of wire. This works satisfactorily for short distances in some cases. But for long distance communication & institutions like communication with the aircraft, ship, vehicle this is not feasible. Here we have to opt for the radio transmission.

It is not possible to send the digital data directly over the antenna because the antenna of practical size works on very high frequencies, much higher than our data transmission rate.

To be able to transmit the data over antenna, we have to ‘modulate’ the signal i.e. phase, frequency or amplitude etc. is varied in accordance with the digital data. At receiver we separate the signal from digital information by the process of demodulation. After this process we are left with high frequency signal(called as carrier signal) which we discard & the digital information, which we utilize.

Modulation also allows different data streams to be transmitted over the same channel(transmission medium).

This process is called as ’Multiplexing’ & result in a considerable saving in bandwidth no of channels to be used. Also it increases the channel efficiency.

The variation of particular parameter variation of the carrier wave give rise to various modulation techniques. Some of the basic modulation techniques are ASK,FSK,PSK,DPSK & QPSK.

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Differential Phase-Shift Keying(DPSK):-

The DPSK is a non-coherent version of PSK. In coherent detection, the carrier wave's phase reference should be known for obtaining optimum error performance.(However it is impractical to have knowledge of the carrier phase at the receiver).

The DPSK eliminates the need for a coherent reference signal at the receiver by combining two basic operations at the transmitter:

1. Differential Encoding of the input binary wave
2. Phase-shift keying

And hence the name differential phase shift keying. Thus to send symbol 0, we phase advance the current signal waveform by 180 degrees and to send 1, we have the phase of the current signal waveform unchanged. The receiver is equipped with a storage capability so that it can measure the relative phase difference between the wave forms received during two successive bit intervals. Provided that the unknown phase θ contained in the received wave varies slowly (slow enough and considered essentially constant over two bit intervals), the phase difference between waveforms received in two successive bit intervals will be independent of θ .

Circuit Description:-

In this IC 8038 is a basic wave form generator which generates sine, square, triangle waveforms. The sine wave generated by this 8038 IC is used as carrier signal to the system. This square wave is used as a clock input to a decade counter which generates the modulating data outputs.

The digital signal applied to the modulation input for DPSK generation is bipolar and have equal positive and negative voltage levels. When the modulating input is negative the output of modulator is a sinewave in phase with the carrier input. Where as for the positive voltage levels, the output of modulator is a sinewave which is shifted out of phase by 180 degrees from the carrier input compared to the differential data stream. This happens because the carrier input is now multiplied by the negative constant level.

Thus the output changes in phase when a change in polarity of the modulating signal results. Fig shows the functional blocks of the DPSK modulator & demodulator.

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Modulation:-

The differential signal to the modulating signal is generated using an X-OR gate and 1-bit delay circuit(it is shown in fig).CD 4051 is an analog multiplexer to which carrier is applied with and without 180 degrees phase shift(created by using an operational amplifier connected in inverting amplifier mode) to the two inputs of the ICTL084.Differential signal generated by X-OR gate is given to the multiplexer's control signal input. depending upon the level of the control signal,carrier signal applied with or without phase shift is steered to the output. 1-bit delay generation of differential signal to the input is created by using a D-flip-flop(IC7474).

Demodulation:-

During the demodulation, the DPSK signal is converted into a +5V square wave signal using a transistor and is applied to one input of an X-OR gate. to the second input of the gate, carrier signal is applied after conversion into a +5V signal. So the X-OR gate output is equivalent to the differential signal of the modulating data. This differential data is applied to one input of an X-OR gate and to the second input, after 1-bit delay the same signal is given. So the output of this X-OR gate is modulating signal.

Output Waveforms:-

To see the DPSK demodulation process, examine the input of DPSK demodulator with the demodulation output.

Check the various test points provided at the output of the functional blocks of the DPSK demodulator. This will help you fully grasp the DPSK demodulation technique.

Figure 1.4:

b'(t)	0	1	1	0	0
b(t)	1	0	0	0	1
Phase	0 ⁰	180 ⁰	180 ⁰	180 ⁰	0 ⁰
B(t)	0	1	1	1	0
Phase	180 ⁰	0 ⁰	0 ⁰	0 ⁰	180 ⁰

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Figure 1.5 Example for Complete DPSK operation (with arbitrary bit as 0):

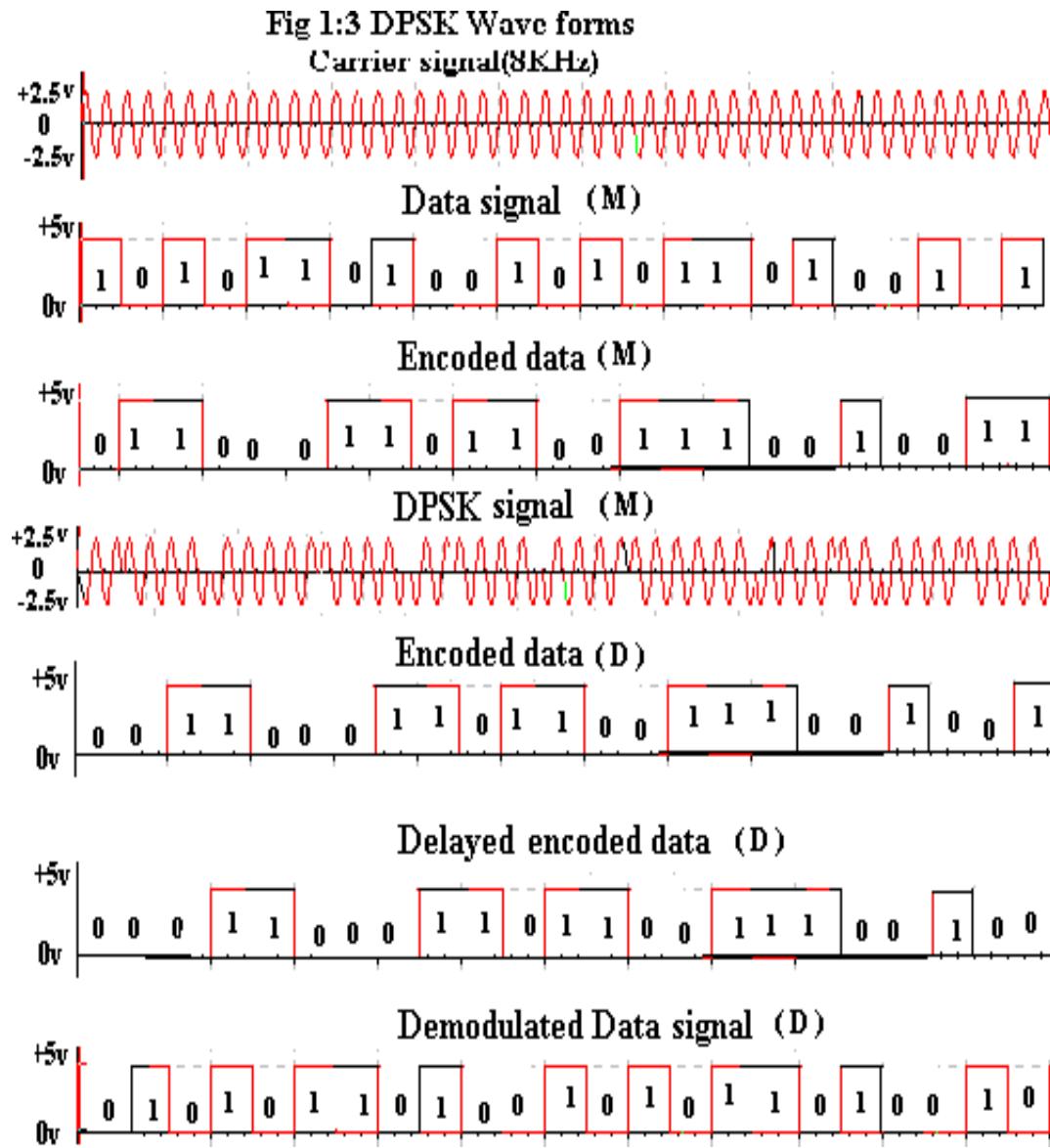
Message signal(to be transmitted)	0	1	1	0	0
Encoded data(differential data)	0	1	1	1	0
Trasnmitted signal phase:	180^0	0^0	0^0	0^0	180^0
Received signal phase :	180^0	0^0	0^0	0^0	180^0
Encoded data(differential data)	0	1	1	1	0
Message signal (Demodulation)	0	1	1	0	0

Procedure:

1. Now switch ON the trainer and see that the supply LED glows.
2. Connect data output from 4(D1,D2,D3,D4) data outputs to the data input of the DPSK modulator TP7.
3. Connect clock output TP1 to the clock input of the DPSK modulator TP8.
4. Now connect carrier output TP2 to the carrier input of the DPSK modulator TP10.
5. Observe the differential data output on the CRO at TP9 test point as shown on the front panel.
6. Observe the phase shifted DPSK output waveform on the CRO corresponding to the differential data output.
7. Connect DPSK MODULATOR output TP11 to the DPSK input of the DEMODULATOR TP12.
8. Connect carrier output TP2 to the carrier input of the DPSK Demodulator TP13.
9. Also connect clock output TP1 to the clock input of the DPSK demodulator TP14.
10. Now observe the DPSK demodulated output waveform TP15 on the CRO.

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Expected Waveforms:



RESULT:

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Questions:

1. How does DPSK differ from PSK?
2. Explain theoretical modulation & demodulation of DPSK using arbitrary bit sequence and assuming initial bit 0 and 1?
3. What is the advantage of DPSK over PSK?
4. Why do we need 1 bit delay in DPSK modulator & demodulator?
5. What does a synchronous detector (multiplier) do in DPSK demodulator?
6. what is the relation between carrier frequency & the bit interval ‘T’?
7. What is the disadvantages of DPSK.?
8. Is the error rate of DPSK is greater than PSK?
9. What is the expression for DPSK error?
- 10.What are the applications of DPSK?

EXPERIMENT 9

QUADRATURE PHASE SHIFT KEYING

AIM: Write a MATLAB program to implement the Quadrature Phase Shift Keying.

Software: MATLAB

Program:

```
clc;
clear all;
close all;
data=[0 0 0 1 1 0 1 1 0 0]; % information
figure(1)
stem(data, 'linewidth',3), grid on;
title(' Information before Transmiting ');
axis([ 0 11 0 1.5]);
% Data Represented at NRZ form for QPSK modulation
data_NRZ=2*data-1;
% S/P conversion of data
s_p_data=reshape (data_NRZ, 2, length (data)/2);
%Let us transmission bit rate 1000000
br=10.^6; f=br; % minimum carrier frequency
T=1;br; % bit duration
t=T/99:T/99:T; % Time vector for one bit information
% QPSK Modulation
y=[];
y_in=[];
```

```

y_qd=[];
for(i=1:length(data)/2)

    y1=s_p_data(1,i)*cos(2*pi*f*t); % inphase component
    y2=s_p_data(2,i)*sin(2*pi*f*t) ; % Quadrature component
    y_in=[y_in y1]; % inphase signal vector
    y_qd=[y_qd y2]; % quadrature signal vector
    y=[y y1+y2]; % modulated signal vector
end

Tx_sig=y; % transmitting signal after modulation

tt=T/99:T/99:(T*length(data))/2

figure(2)

subplot(3,1,1);
plot(tt,y_in,'linewidth',3), grid on;
title(' wave form for inphase component in QPSK modulation ');
xlabel('time(sec)');
ylabel(' amplitude(volt0)');

subplot(3,1,2);
plot(tt,y_qd,'linewidth',3), grid on;
title(' wave form for Quadrature component in QPSK modulation ');
xlabel('time(sec)');
ylabel(' amplitude(volt0)');

subplot(3,1,3);
plot(tt,Tx_sig,'r','linewidth',3), grid on;

```

```

title('QPSK modulated signal (sum of inphase and Quadrature phase signal)');
xlabel('time(sec)');
ylabel(' amplitude(volt0');

% QPSK Demodulation

Rx_data=[];
Rx_sig=Tx_sig; % Received signal
for(i=1:1:length(data)/2)

%% inphase coherent detector
Z_in=Rx_sig((i-1)*length(t)+1:i*length(t)).*cos(2*pi*f*t);

% above line indicates multiplication of received & inphase carrier signal

Z_in_intg=(trapz(t,Z_in))*(2/T); % integration using trapezoidal rule
if(Z_in_intg>0) % Decision Maker

    Rx_in_data=1;
else
    Rx_in_data=0;
end

%% Quadrature coherent detector

Z_qd=Rx_sig((i-1)*length(t)+1:i*length(t)).*sin(2*pi*f*t);

%above line indicates multiplication of received signal & Quadrature phase carrier signal

Z_qd_intg=(trapz(t,Z_qd))*(2/T); %integration using trapezoidal rule
if (Z_qd_intg>0) % Decision Maker

    Rx_qd_data=1;
else

```

```

Rx_qd_data=0;
end

Rx_data=[Rx_data Rx_in_data Rx_qd_data]; % Received Data vector
end

figure(3)

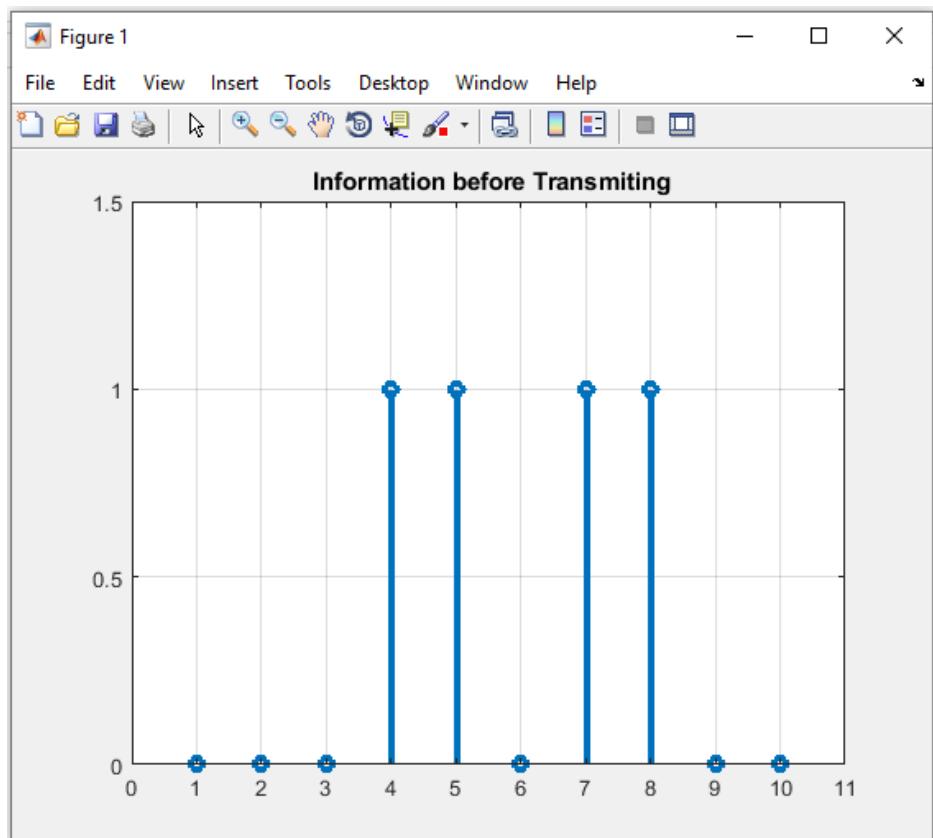
stem(Rx_data,'linewidth',3)

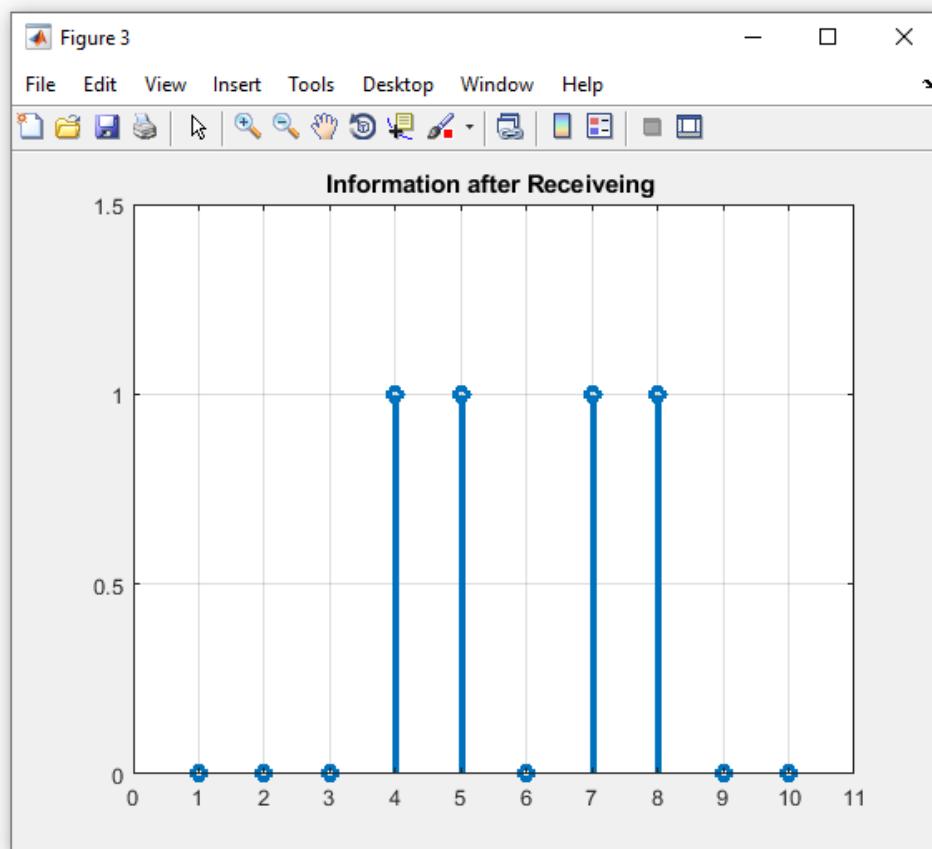
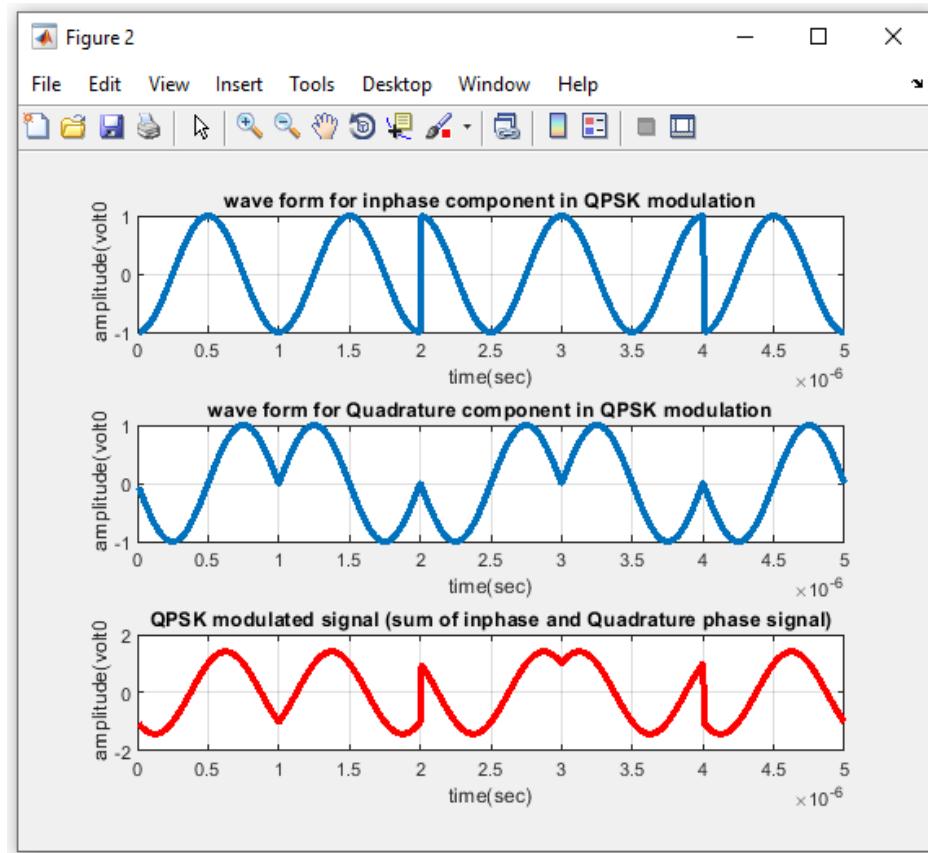
title('Information after Receiving ');
axis ([ 0 11 0 1.5]), grid on;

```

Result:

OUTPUT:





EXPERIMENT-10

DIGITAL COMPANDING (A-Law & μ -Law)

AIM: Write a MATLAB program to implement Digital companding using A-Law & μ -Law on a signal.

Software: MATLAB

Program:

μ -Law Companding

mu = 255; % Value of mu used

sig = exp(-4:0.1:4);

V = max(sig);

%Quantize the signal by using equal-length intervals.

%Set partition and codebook values, assuming 6-bit quantization.

partition = 0:2^6 - 1;

codebook = 0:2^6;

[~, ~, distortion] = quantiz(sig,partition,codebook); % Calculate the mean square distortion.

% Compress the signal by using the compand function.

%Apply quantization and expand the quantized signal.

compsig = compand(sig,mu,V,'mu/compressor');

[~,quants] = quantiz(compsig,partition,codebook);

newsig = compand(quants,mu,max(quants),'mu/expander');

distortion2 = sum((newsig - sig).^2)/length(sig); %Calculate the mean square distortion of the compounded signal.

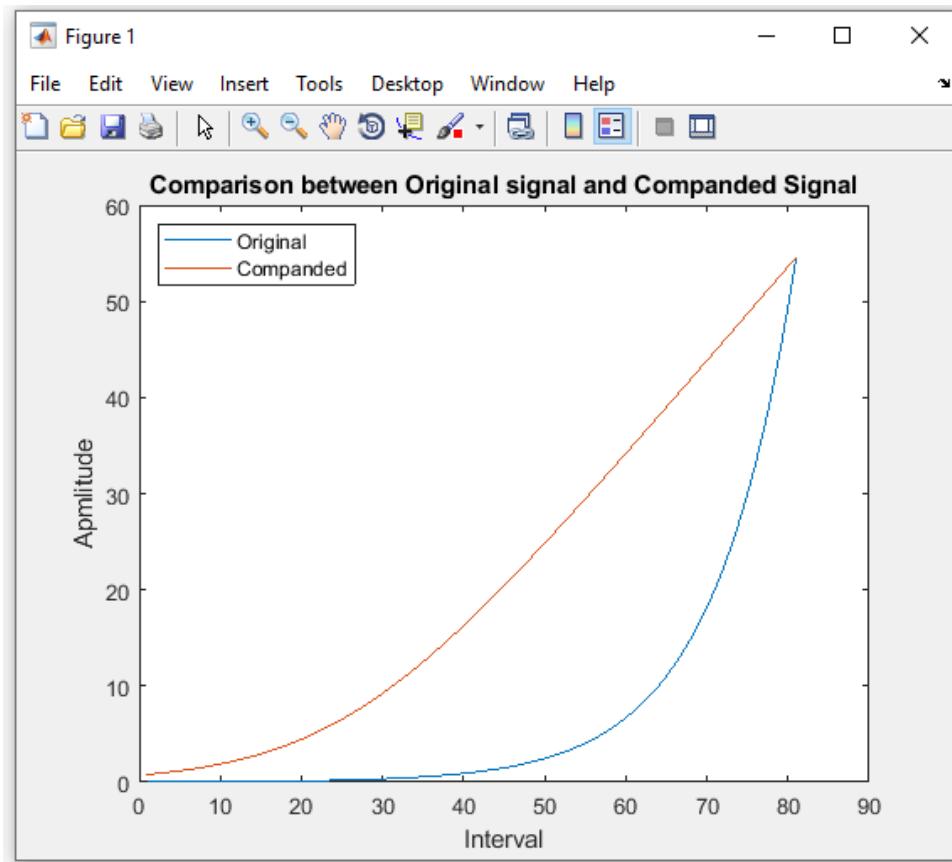
%Compare the mean square distortions.

[distortion, distortion2]

```
% Plot the original exponential signal and the companded signal
plot([sig' compsig']);
title('Comparison between Original signal and Companded Signal');
xlabel('Interval');
ylabel('Amplitude');
legend('Original','Companded','location','nw');
```

Output:

Comparison of distortion without and with companding respectively 0.5348
0.0397



A-Law Companding

$A = 87.6$; % Value of A used

```
sig = exp(-4:0.1:4);
```

```
V = max(sig);
```

```

%Quantize the signal by using equal-length intervals.

%Set partition and codebook values, assuming 6-bit quantization.

partition = 0:2^6 - 1;

codebook = 0:2^6;

[~,~,distortion] = quantiz(sig,partition,codebook); % Calculate the mean
square distortion.

% Compress the signal by using the compand function.

%Apply quantization and expand the quantized signal.

compsig = compand(sig,A,V,'A/compressor');

[~,quants] = quantiz(compsig,partition,codebook);

newsig = compand(quants,A,max(quants),'A/expander');

distortion2 = sum((newsig - sig).^2)/length(sig); %Calculate the mean square
distortion of the companded signal.

%Compare the mean square distortions.

[distortion, distortion2]

% Plot the original exponential signal and the companded signal

plot([sig' compsig']);

title('Comparison between Original signal and Companded Signal');

xlabel('Interval');

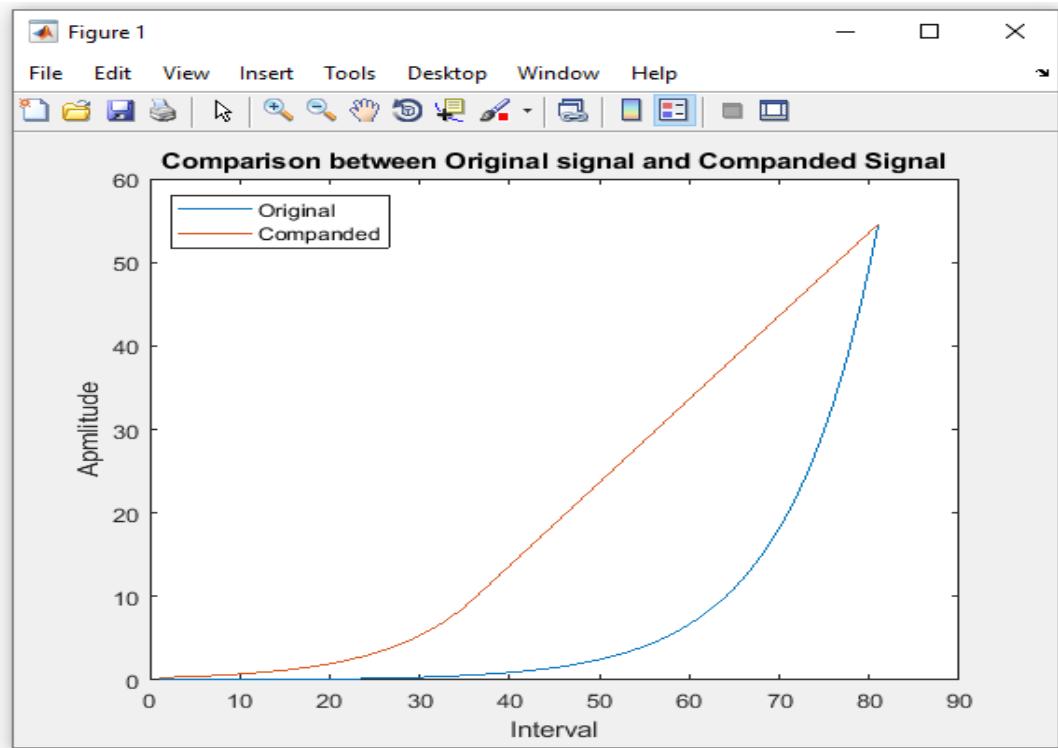
ylabel('Amplitude');

legend('Original','Companded','location','nw');

```

Output

Comparison of distortion without and with companding respectively 0.5348
0.0205



EXPERIMENT-11

LINEAR BLOCK CODE ENCODER AND DECODER

AIM: Write a MATLAB program to implement the Linear Block Code Encoder and Decoder.

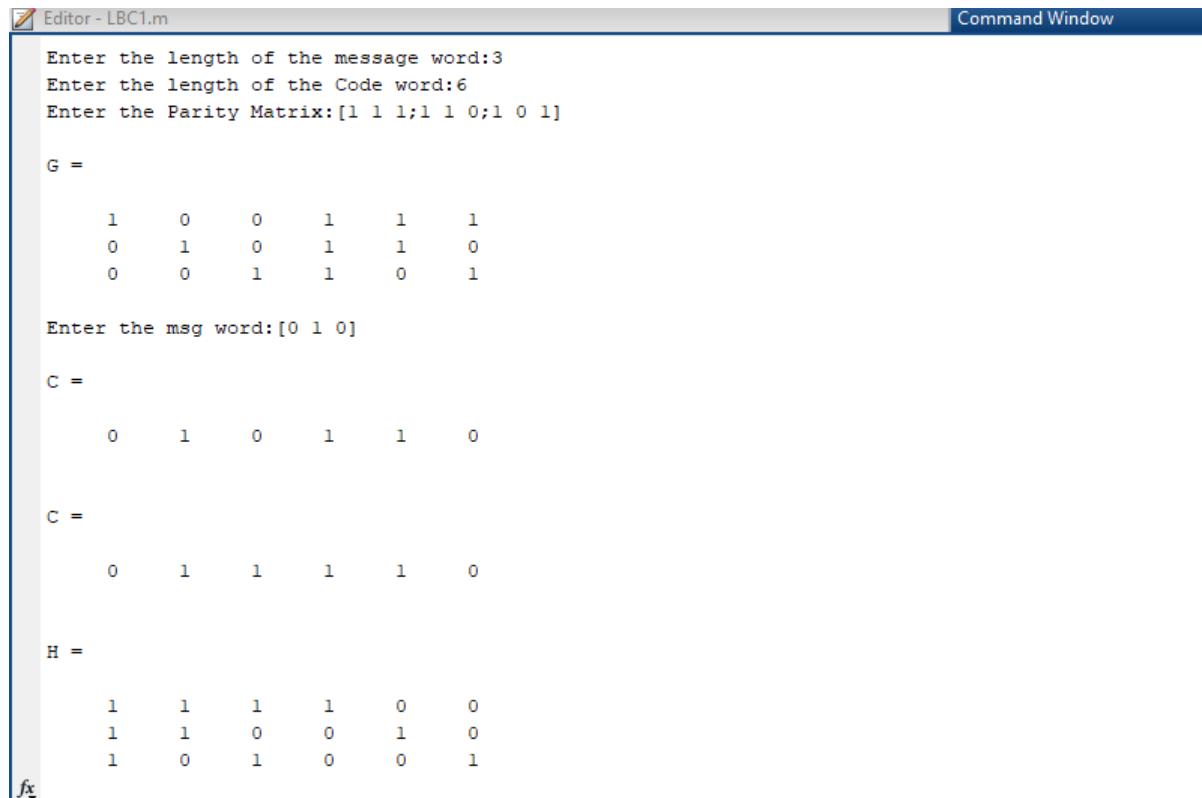
Software: MATLAB

Program:

```
clc;
clear all;
k=input('Enter the length of the message word:');
n=input('Enter the length of the Code word:');
P=input('Enter the Sub Matrix:');
G=[eye(k) P]
m=input('Enter the msg word:');
C1=rem(m*P,2);    msg * Submatrix
X=[m C1]    % Codevector
X(3)=~X(3)    %placing error in 3rd bit
H=[P' eye(n-k)]
Y=X  % Y is the received vector after error occurred
Ht=H'
S=rem(Y*Ht,2)
for i=1:1:size(Ht)
if (Ht(i,1:3)==S)
    Y(i)=1-Y(i);
    break
end
end
disp('The error is in bit')
disp(i)
```

```
disp('The corrected code word is')  
disp(Y)
```

Output:



The image shows a MATLAB interface with two windows. The left window is the 'Editor - LBC1.m' showing the M-file code. The right window is the 'Command Window' showing the execution of the code and its output.

```
Editor - LBC1.m  
Command Window  
  
Enter the length of the message word:3  
Enter the length of the Code word:6  
Enter the Parity Matrix:[1 1 1;1 1 0;1 0 1]  
  
G =  
  
1 0 0 1 1 1  
0 1 0 1 1 0  
0 0 1 1 0 1  
  
Enter the msg word:[0 1 0]  
  
C =  
  
0 1 0 1 1 0  
  
C =  
  
0 1 1 1 1 0  
  
H =  
  
1 1 1 1 0 0  
1 1 0 0 1 0  
1 0 1 0 0 1
```

Editor - LBC1.m

R =

0	1	1	1	1	0
---	---	---	---	---	---

Ht =

1	1	1
1	1	0
1	0	1
1	0	0
0	1	0
0	0	1

S =

1	0	1
---	---	---

The error is in bit
3

The corrected code word is

0	1	0	1	1	0
---	---	---	---	---	---

Result:

EXPERIMENT-12

BINARY CYCLIC CODES: ENCODER AND DECODER

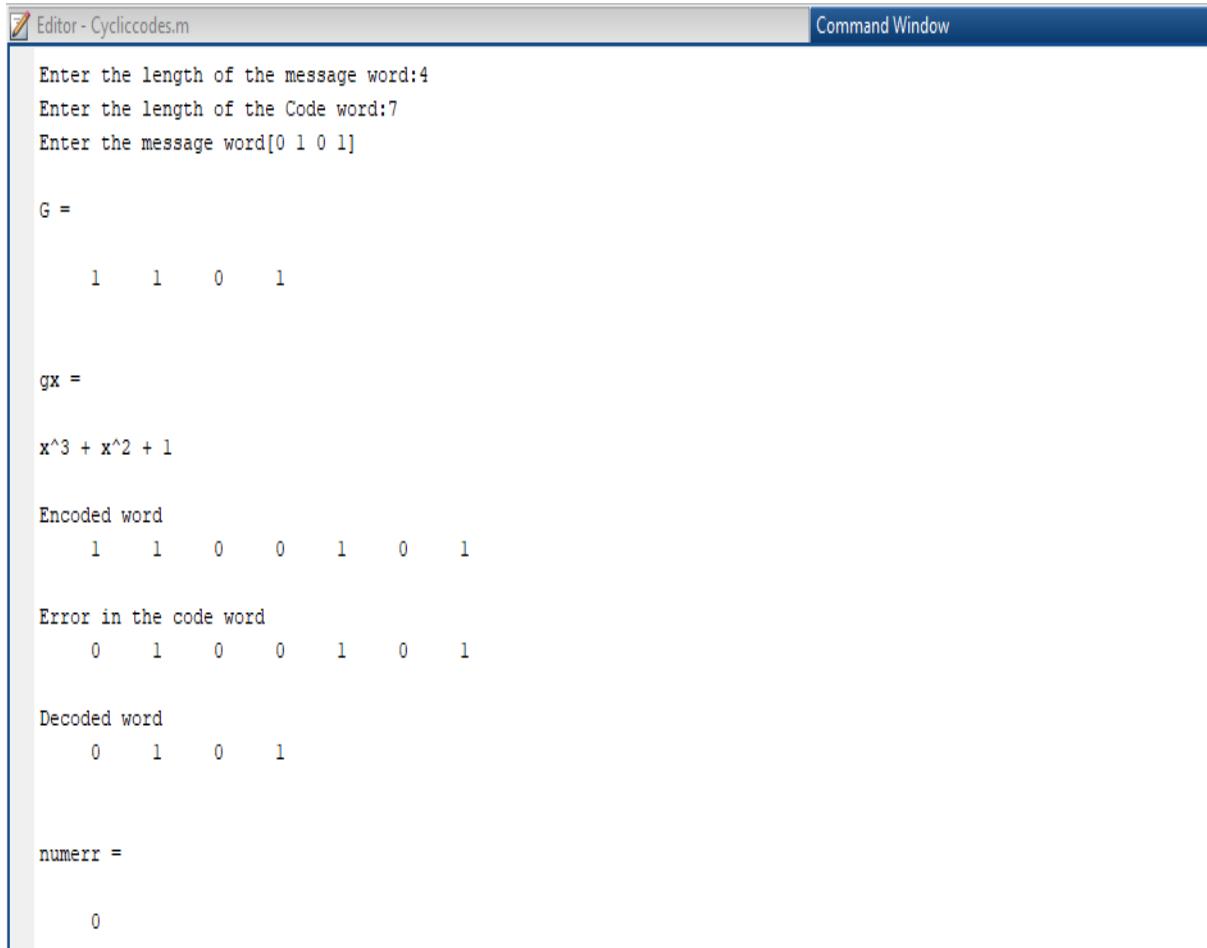
AIM: Write a MATLAB program for implementation of Binary Cyclic Codes Encoder and Decoder

Software: MATLAB

Program:

```
clc;  
clear all;  
  
k=input('Enter the length of the message word:');  
  
n=input('Enter the length of the Code word:');  
  
m=input('Enter the message word');  
  
G=cyclpoly(n,k,'max')  
  
gx=poly2sym(G)      %generates the generator polynomial  
  
C=encode(m,n,k,'cyclic',G)  % Cyclic codes encoding  
  
C(1)=~C(1)          % first bit is in error  
  
D=decode(C,n,k,'cyclic',G)  % Cyclic codes decoding  
  
numerr = biterr(m,D)    % decoding is done correctly
```

Output:



The image shows a MATLAB interface with two windows. The left window is titled 'Editor - Cycliccodes.m' and contains the script code. The right window is titled 'Command Window' and displays the execution results.

```
Editor - Cycliccodes.m
Command Window

Enter the length of the message word:4
Enter the length of the Code word:7
Enter the message word[0 1 0 1]

G =
1 1 0 1

gx =
x^3 + x^2 + 1

Encoded word
1 1 0 0 1 0 1

Error in the code word
0 1 0 0 1 0 1

Decoded word
0 1 0 1

numerr =
0
```