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**VLSI Circuit Design**

# Topic: Design of Low power, High Performance 4 bit Vedic Multiplier and full ADDER, half adder circuit and measure different parameters

**Submitted To:**

**Dr. Vasantha M.H.**

**Associate Professor**

**Department of Electronics and Communication Eng.**

## **Name: sahil**

## **Roll. No.: 21ECE1039**

## **Batch No. :14TH**

## **Department: ECE**

## **Semester: 7th Semester**

## **Course Code: EC – 401**

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Aim: The aim of this experiment 1. Design of Low power, High Performance Full adder and half adder circuit and measure different parameters. 2. Design of Low-Power¸ High Performance a) 4-bit Vedic Multiplier and 4-bit multiplier using any of the architecture

**Tools Used**: Cadence Software

### Part 1: Design of Low power, High Performance Full adder and half adder circuit and measure different parameters

Theory

Introduction

Adders are fundamental components in digital systems, primarily used for arithmetic operations in processors and other integrated circuits. The design of low-power, high-performance adders is essential in applications requiring efficient computation with minimal energy consumption, particularly in portable and embedded devices. This report examines the design and optimization of both full adder and half adder circuits, focusing on reducing power dissipation while maintaining high-speed operation

|  |  |  |  |
| --- | --- | --- | --- |
| Input A | Input B | Sum (S) | Carry (C) |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

Table 8.1: Half adder truth table

**Half Adder**

Definition and Operation

Half adder is a combinational circuit that adds two binary numbers, producing a sum and a carry output. It is the simplest form of an adder circuit and is often used in digital systems requiring addition of single-bit numbers.

**Circuit Design:**

***Inputs***: Two single-bit binary numbers, A and B.

***Outputs***:

* **Sum (S)**: Result of the addition of inputs A and B.
* **Carry (C)**: Indicates a carry-out if the sum exceeds the value of one bit.

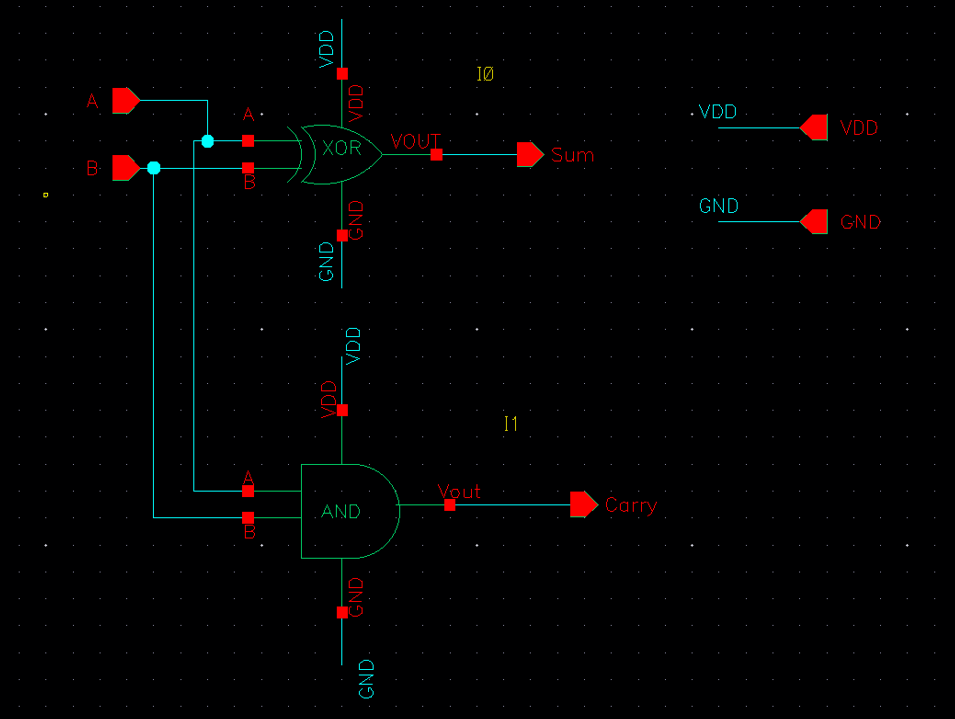


Fig 8.2: Half Adder schematic

The logic equations for a half adder are:

**Sum (S) = A ⊕ B**

**Carry (C)=A⋅B**

These expressions indicate that the sum is the result of an XOR operation on the inputs, while the carry is the result of an AND operation.

**Advantages**:

Simple structure and low power consumption, ideal for applications requiring minimal addition.

**Limitations**:

Cannot add more than two bits because it lacks a carry-in input, restricting it to single-bit addition only.

### Full AdderVC​(t)=Vin​e−RCt​

A **full adder** is an extension of the half adder, capable of adding three bits: two operand bits and a carry-in bit. It is essential for multi-bit binary addition in digital arithmetic circuits, as it propagates the carry to the next bit position.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | C | S | C0 |
| **0** | **0** | **0** | **0** | **0** |
| **0** | **0** | **1** | **1** | **0** |
| **0** | **1** | **0** | **1** | **0** |
| **0** | **1** | **1** | **0** | **1** |
| **1** | **0** | **0** | **1** | **0** |
| **1** | **0** | **1** | **0** | **1** |
| **1** | **1** | **0** | **0** | **1** |
| **1** | **1** | **1** | **1** | **1** |

Table 8.2: Full adder truth table

**Inputs**:

* A: First operand bit.
* B: Second operand bit.
* Cin​: Carry-in bit from the previous stage.

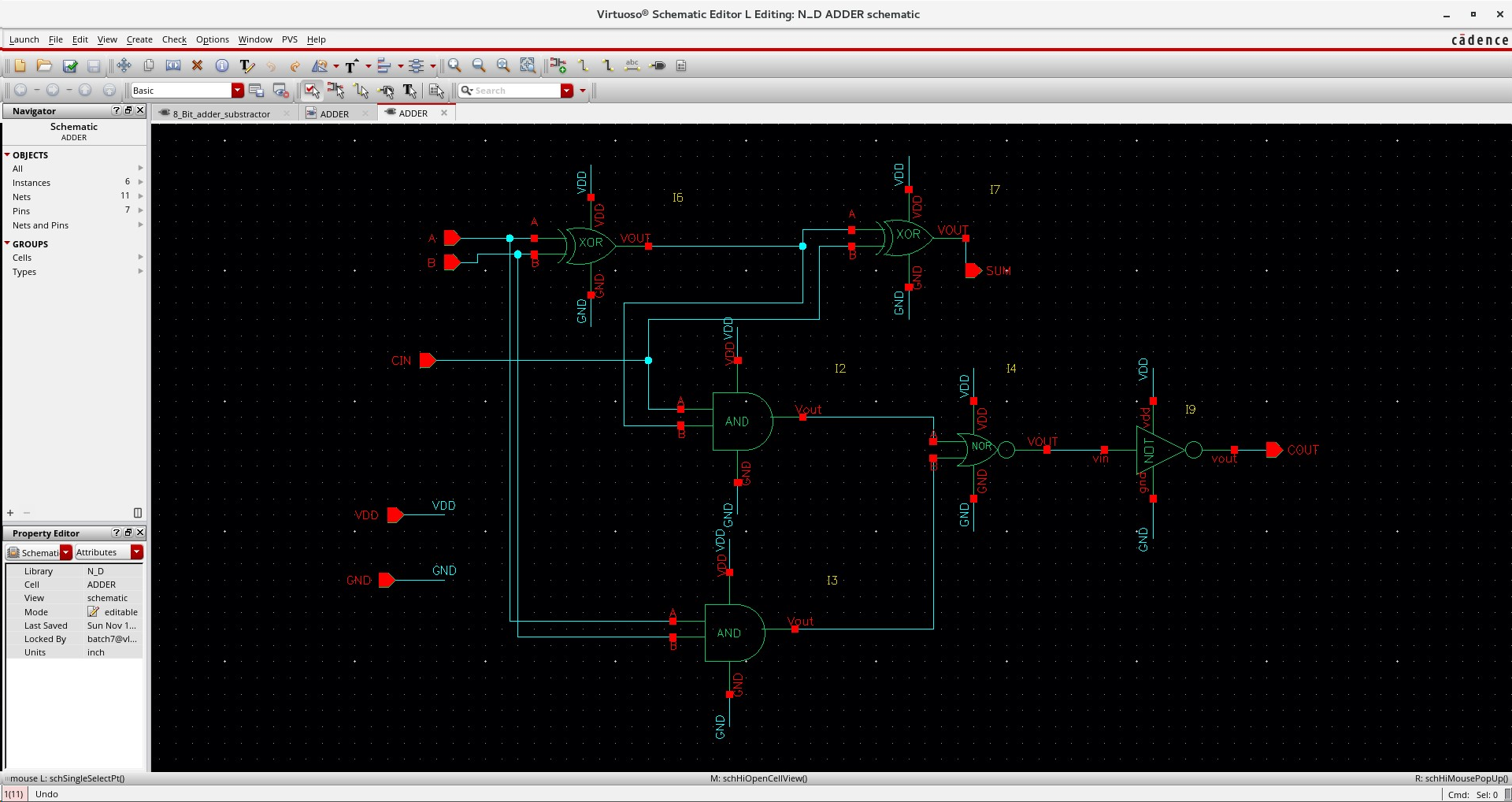


Fig 8.3: Full adder Schematic

**Outputs**:

**Sum (S)**: Result of adding A, B, and Cin​

**Carry (Cout)**: Carry-out bit, which is forwarded to the next higher bit

The logic equations for a full adder are:

**Sum (S) = A ⊕ B ⊕ Cin​**

The full adder’s design ensures that it can handle multi-bit addition when cascaded with other full adders, allowing for effective addition of binary numbers.

**Advantages**:

Allows for multi-bit binary addition by chaining multiple full adders, enabling ripple carry addition

**Limitations**:

The carry-out propagation can lead to delays in large cascaded additions, especially when numerous bits are involved, known as ripple carry delay

### circuit Design

1. **Inverter:**

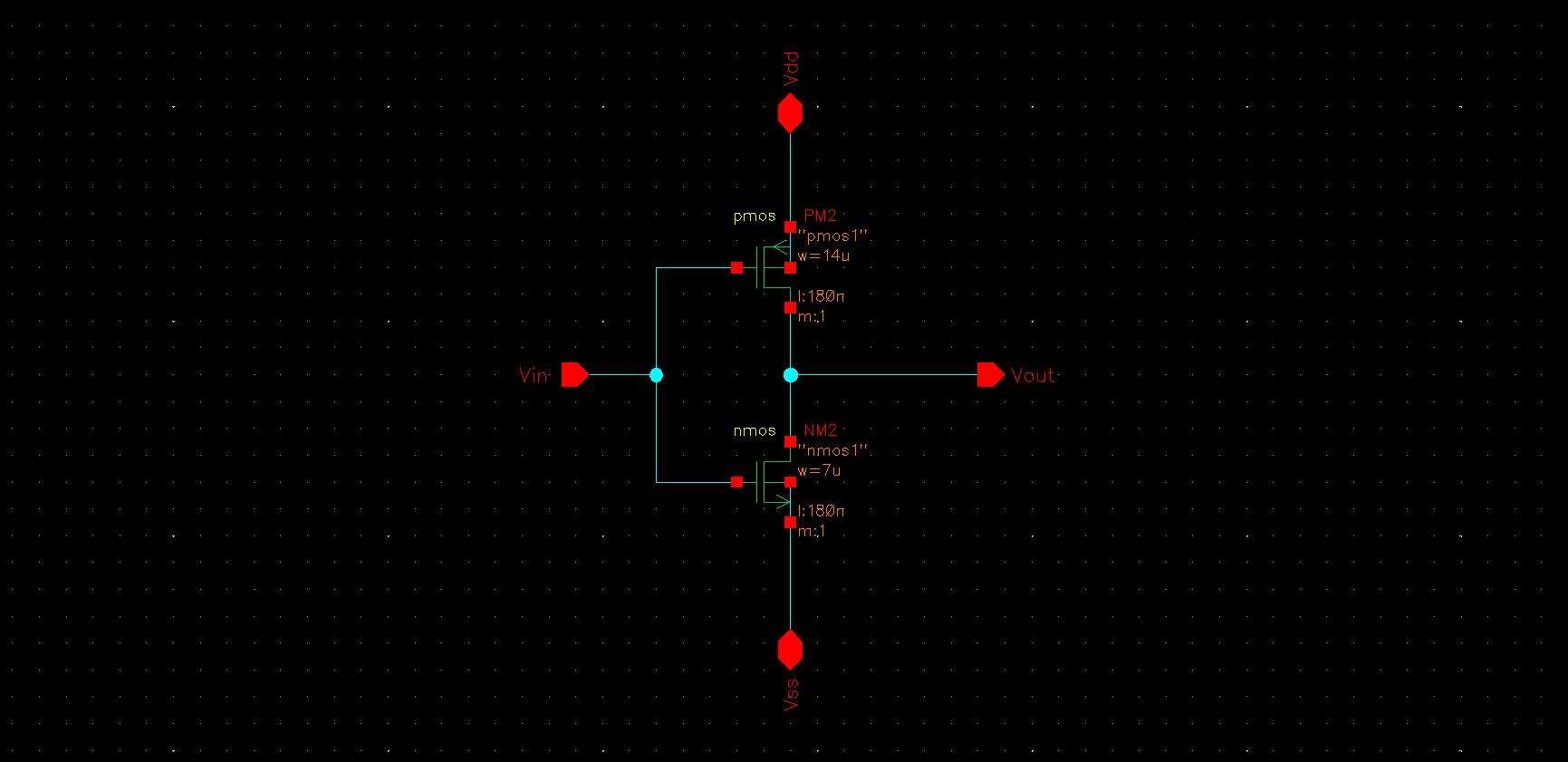


Fig8.4: Schematic Diagram Inverter

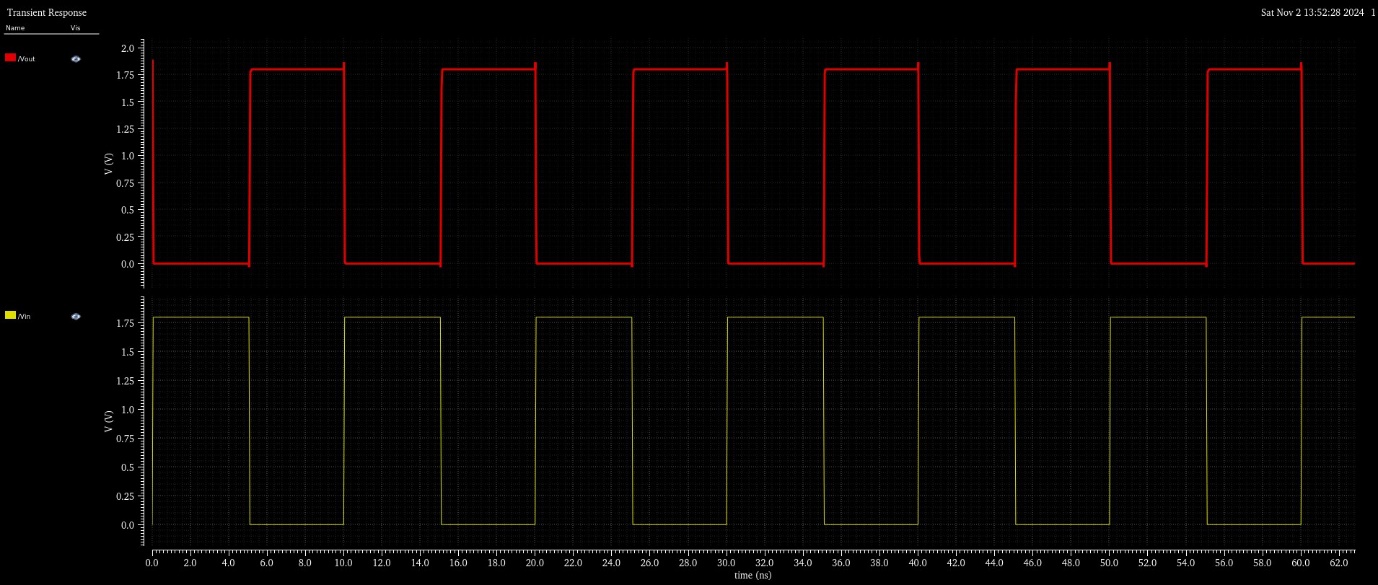


Fig8.5: Output Inverter

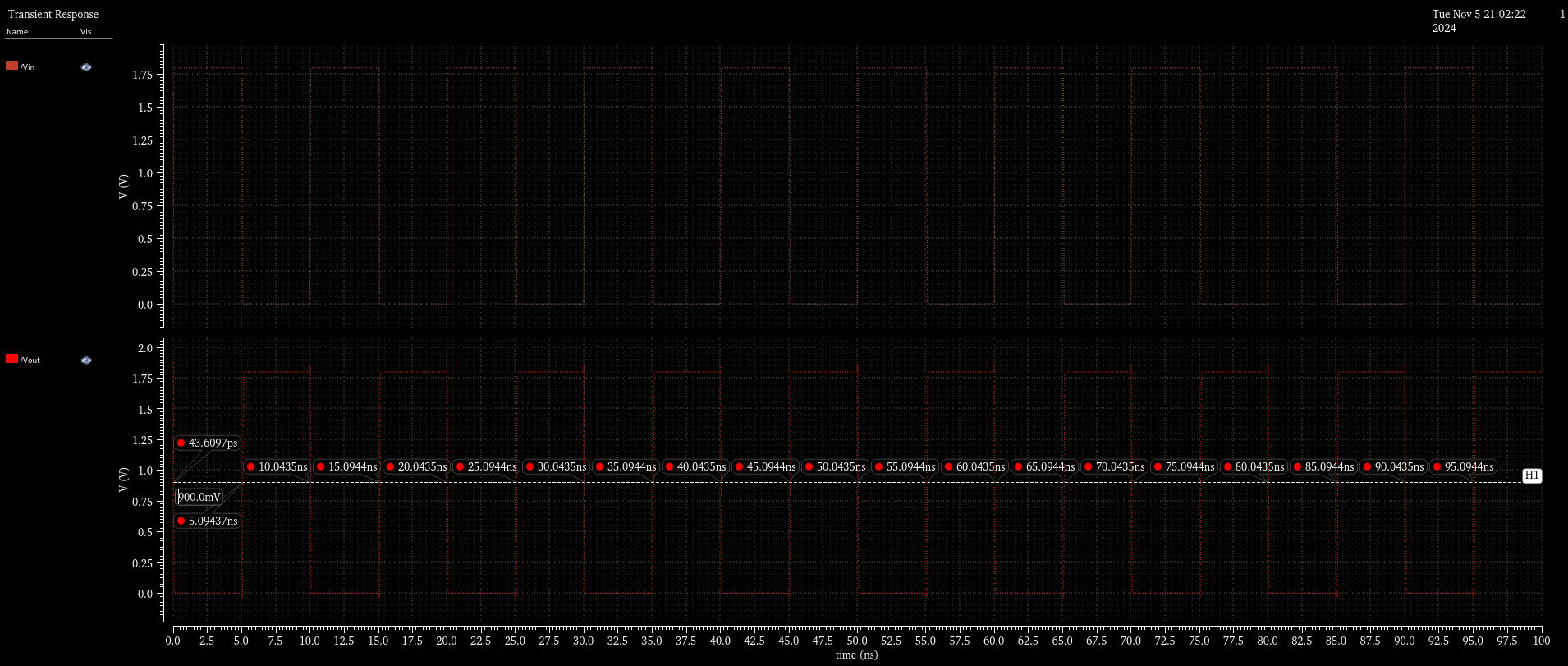


Fig8.52: Inverter Delay

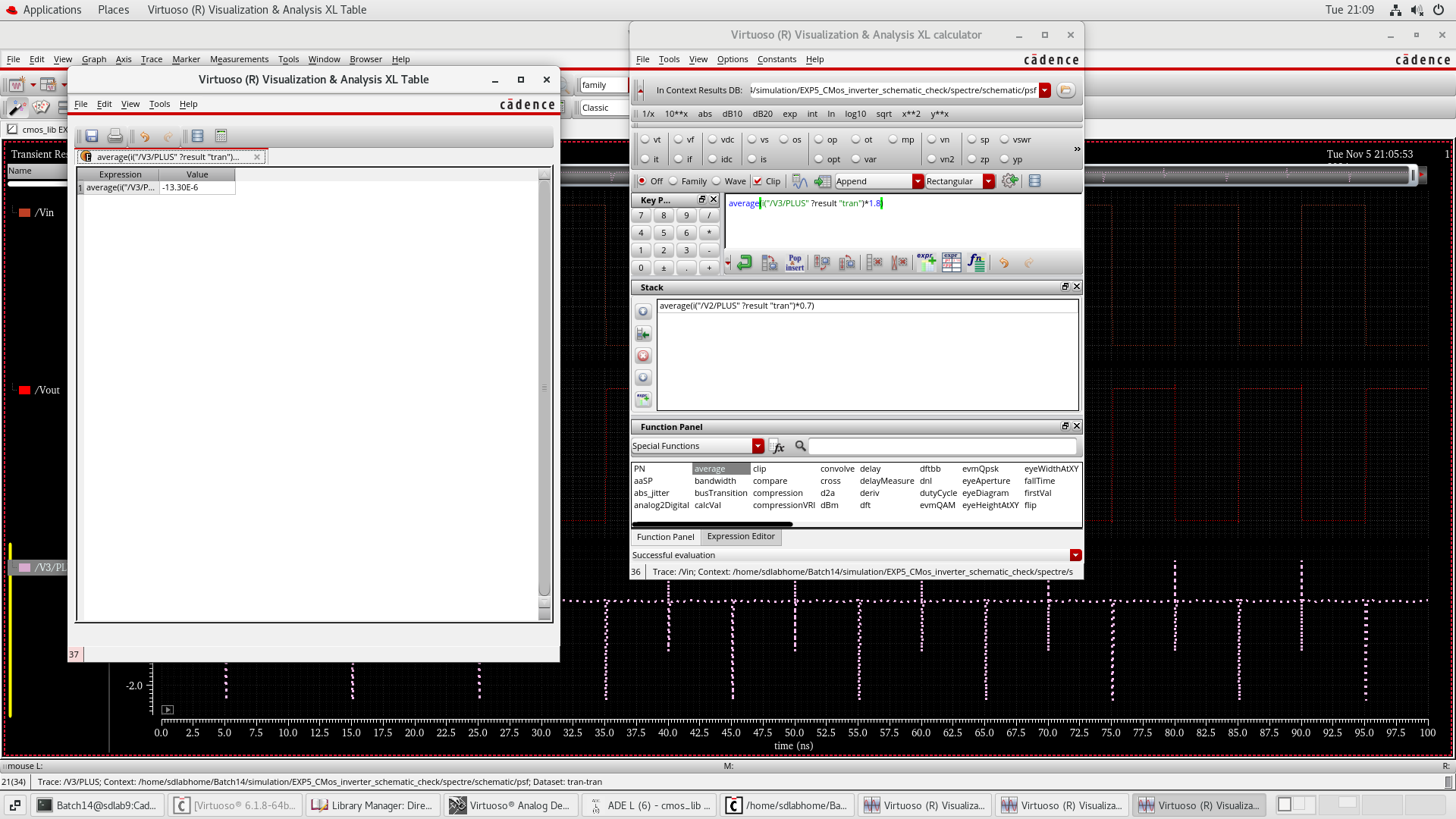


Fig8.53: Power calculation Inverter

|  |  |
| --- | --- |
| A | Y |
| 0 | 1 |
| 1 | 0 |

**Delay:**

Ton*=0.04ns*

*Toff=0.03ns*

*T=*

*T=0.03ns*

**Transistors:**

***2 mosfets***

1. **Gates**
2. AND GATE

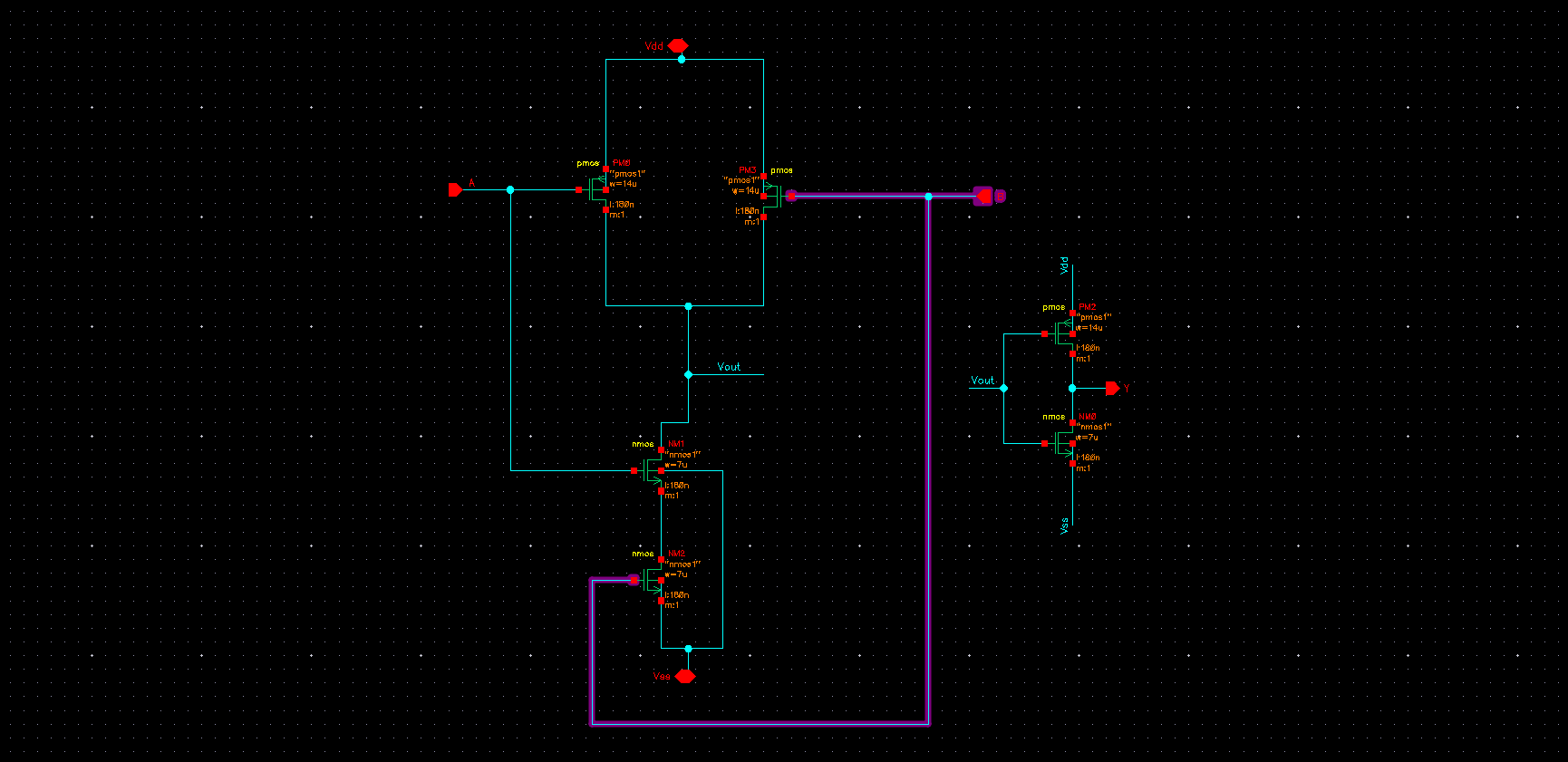


Fig 8.6: Circuit Diagram AND

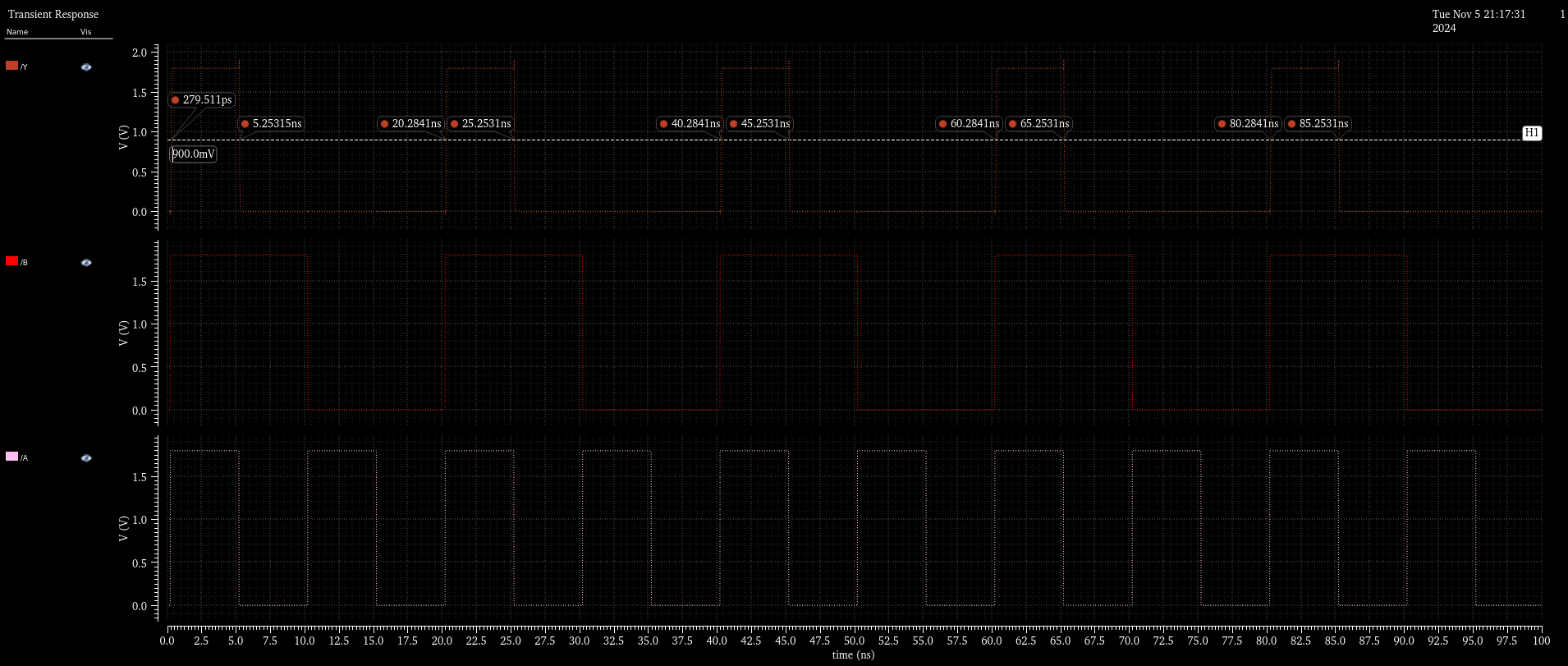


Fig 8.61: Delay calculation AND Gate

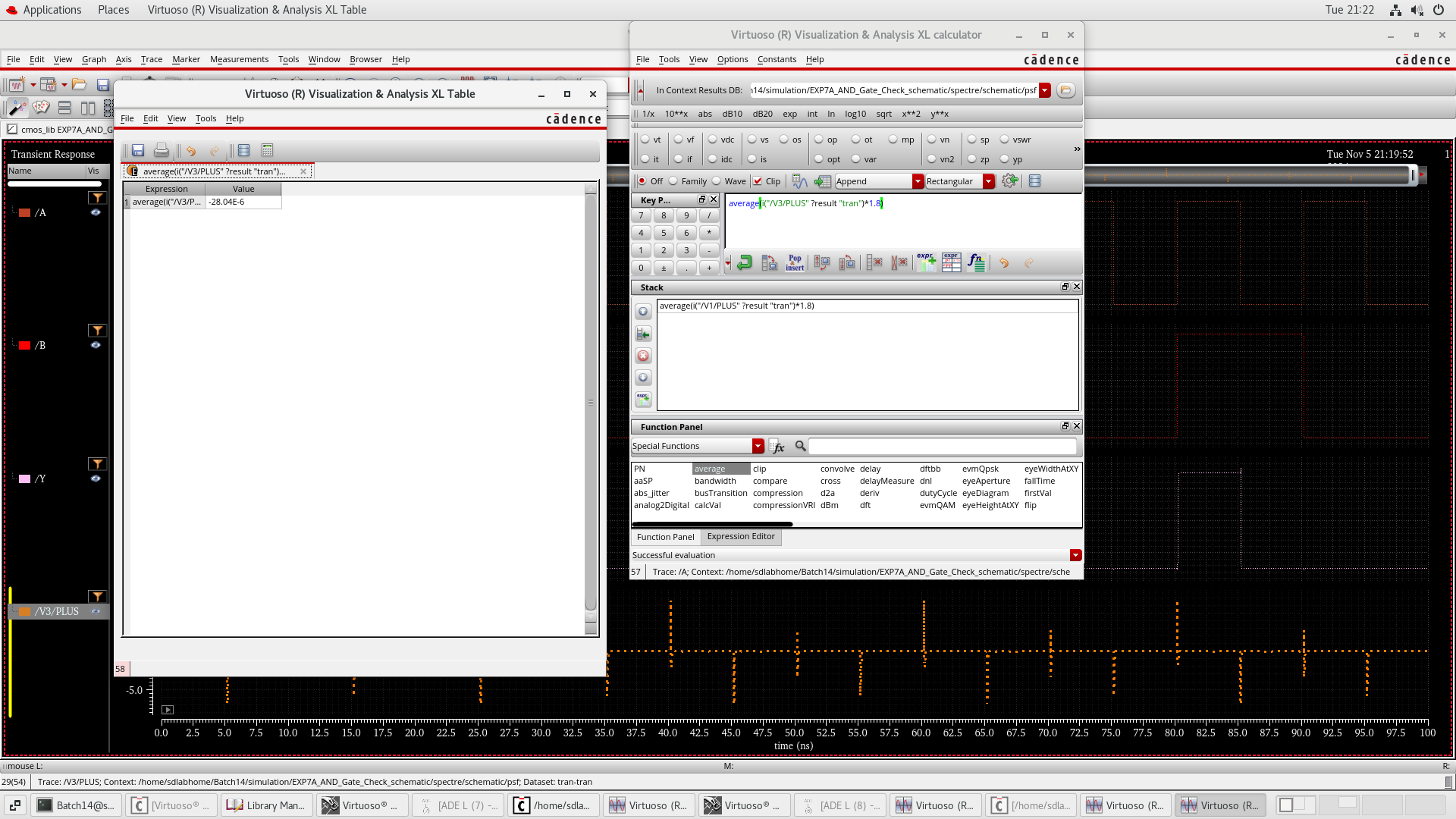


Fig 8.61: Power calculation AND Gate

|  |  |  |
| --- | --- | --- |
| AND TRUTH TABLE | | |
| **A** | **B** | Y |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

**Delay :**

*Ton=0.25ns*

*Toff=0.19ns*

*T=*

*T=0.22ns*

**Transistors:**

***6 mosfets***

1. NOR GATE

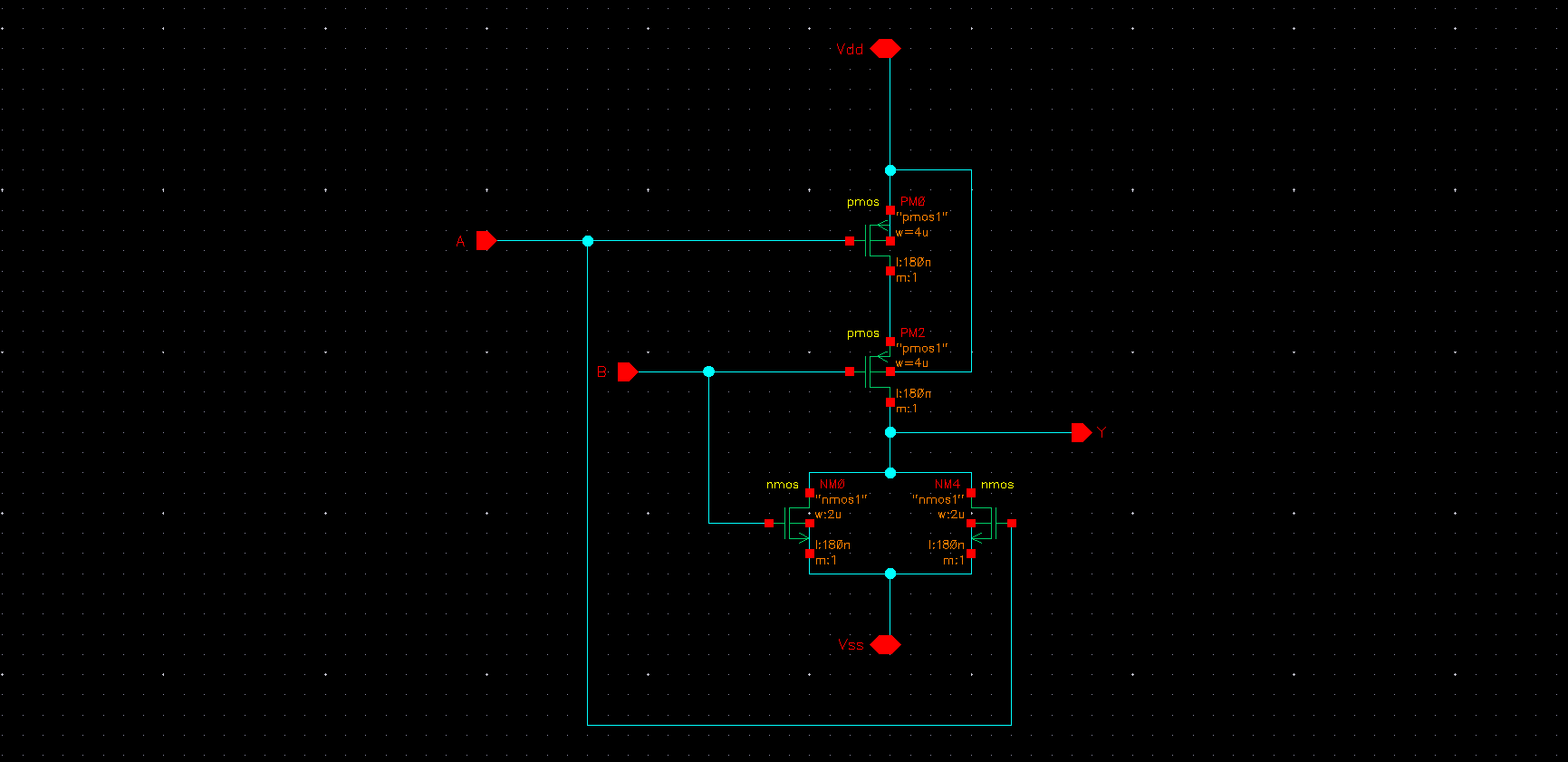


Fig8.7: Schematic Diagram NOR gate

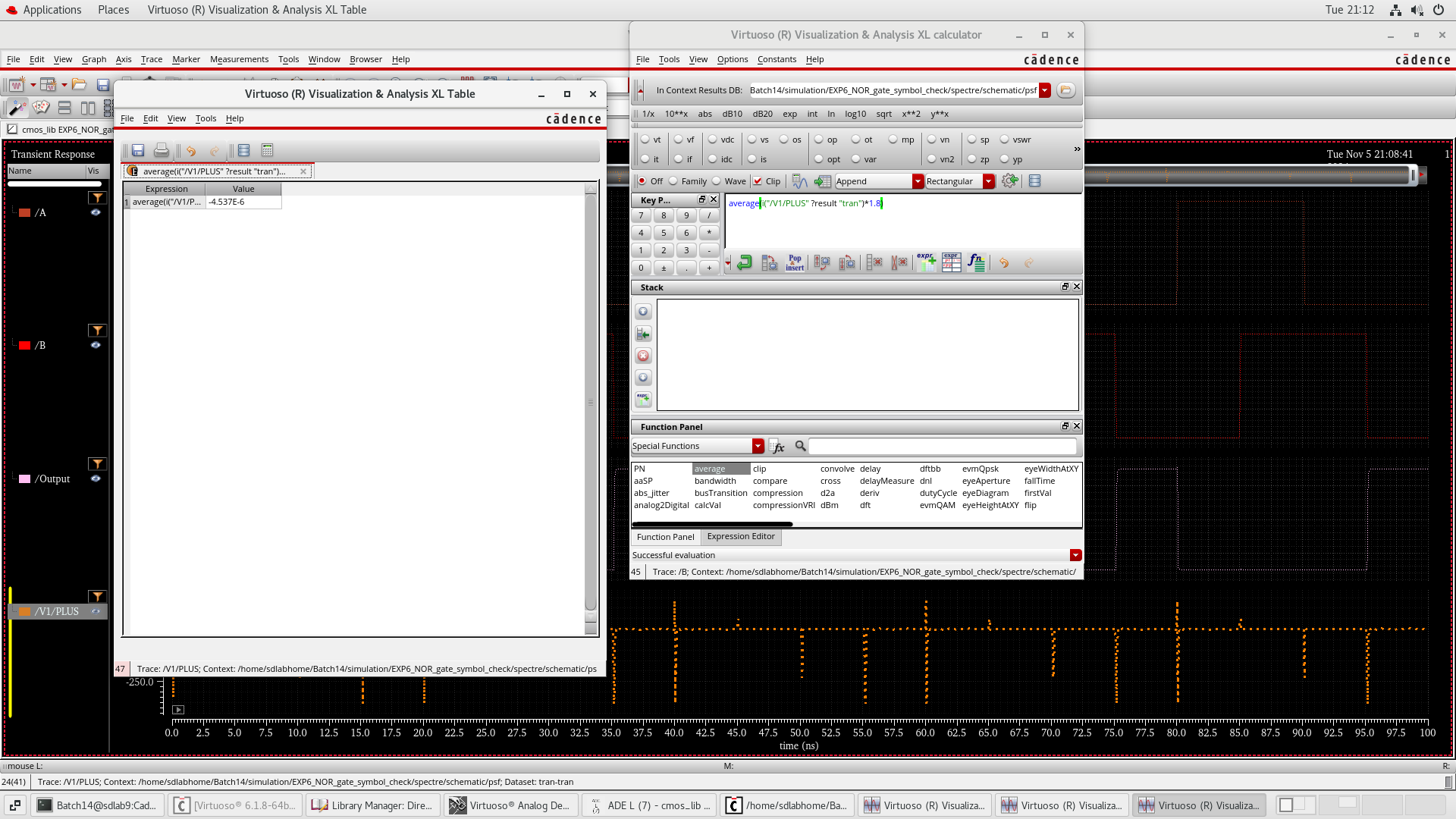


Fig8.72: Power calculation NOR gate

|  |  |  |
| --- | --- | --- |
| NOR TRUTH TABLE | | |
| **A** | **B** | Y |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**Delay :**

*Ton=0.060ns*

*Toff=0.067ns*

*T=*

*T=0.0635ns*

**Transistors:**

***4 mosfets***

1. OR GATE

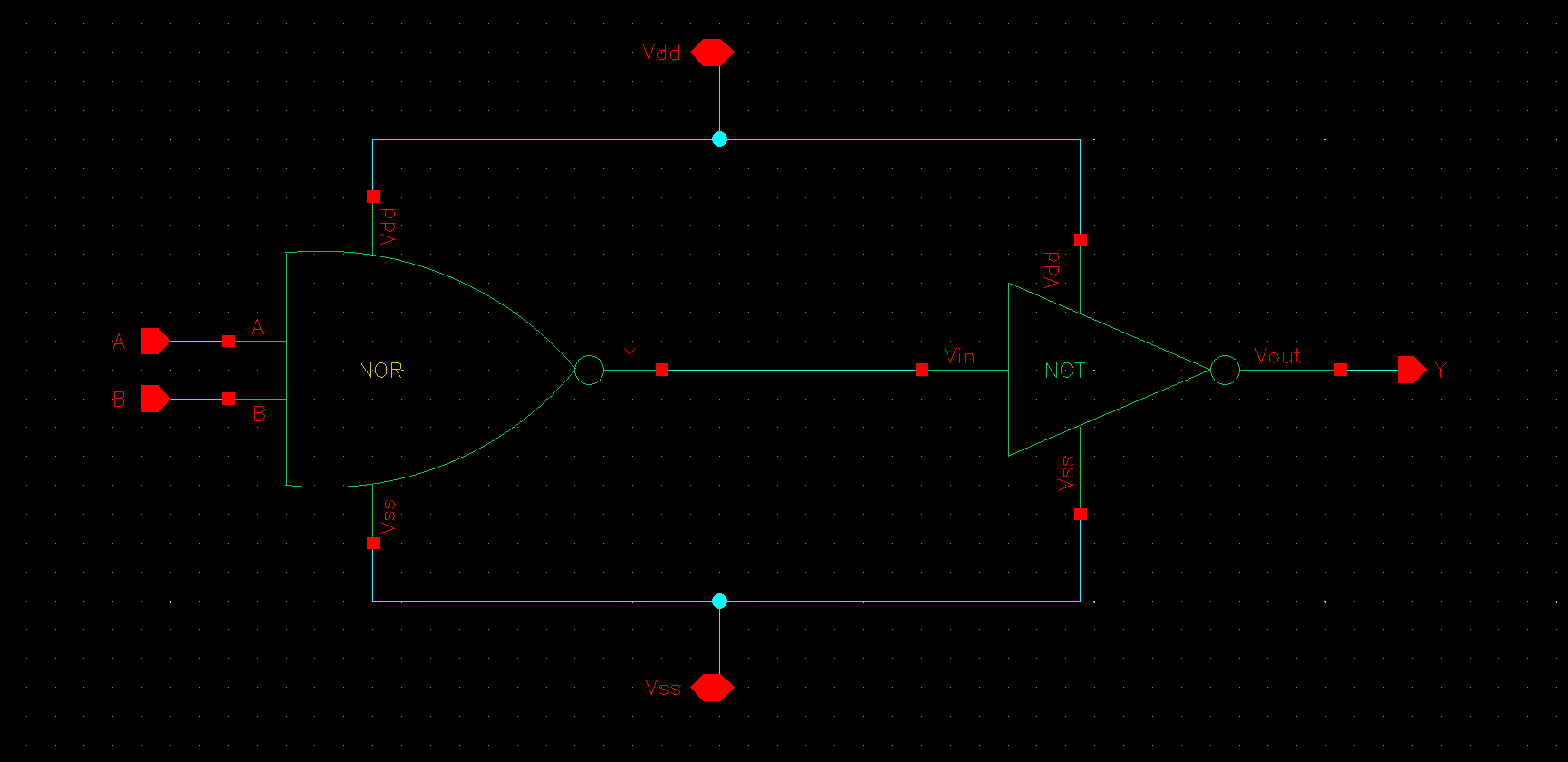


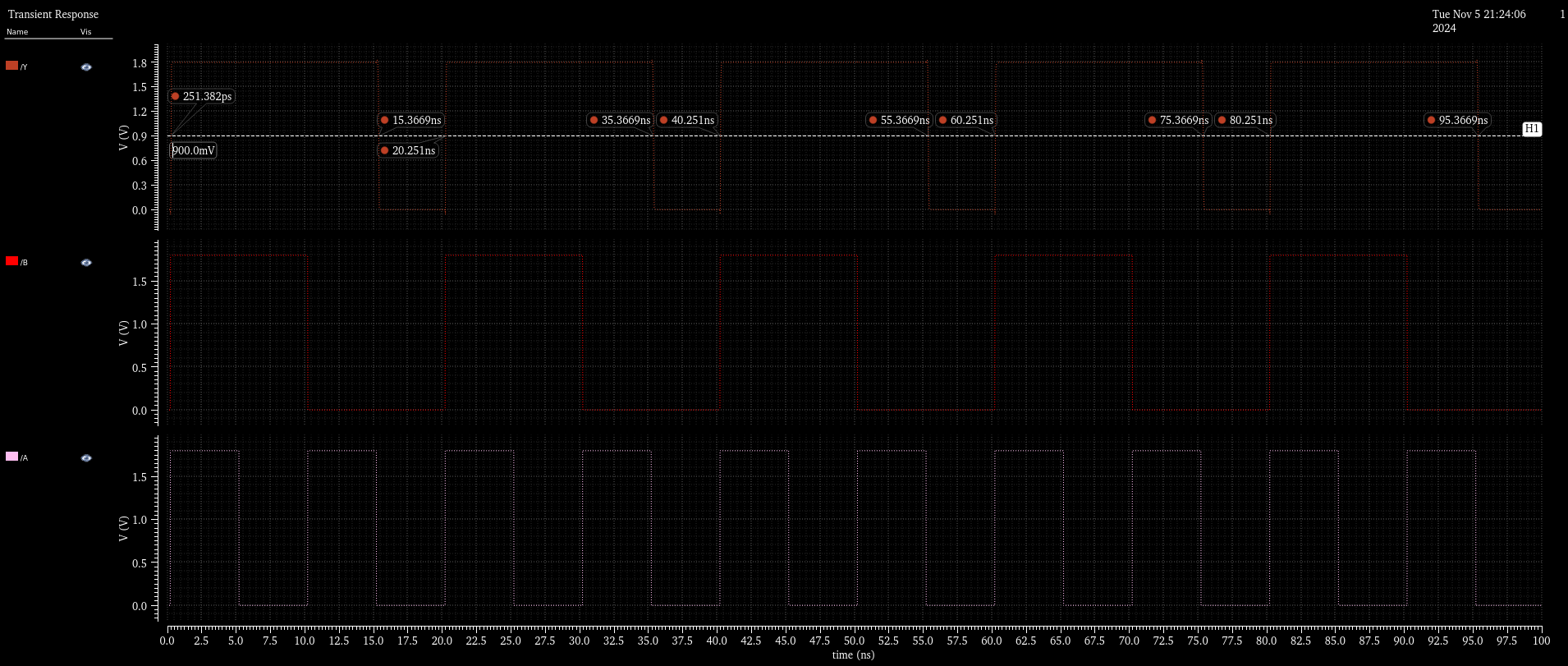
Fig8.8: Circuit Diagram OR gate

Fig8.82: Delay calculation OR gate

|  |  |  |
| --- | --- | --- |
| OR TRUTH TABLE | | |
| **A** | **B** | Y |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**Delay :**

Ton*=0.3ns*

*Toff=0.25ns*

*T=*

*T=0.27ns*

**Transistors:**

***6 mosfets***

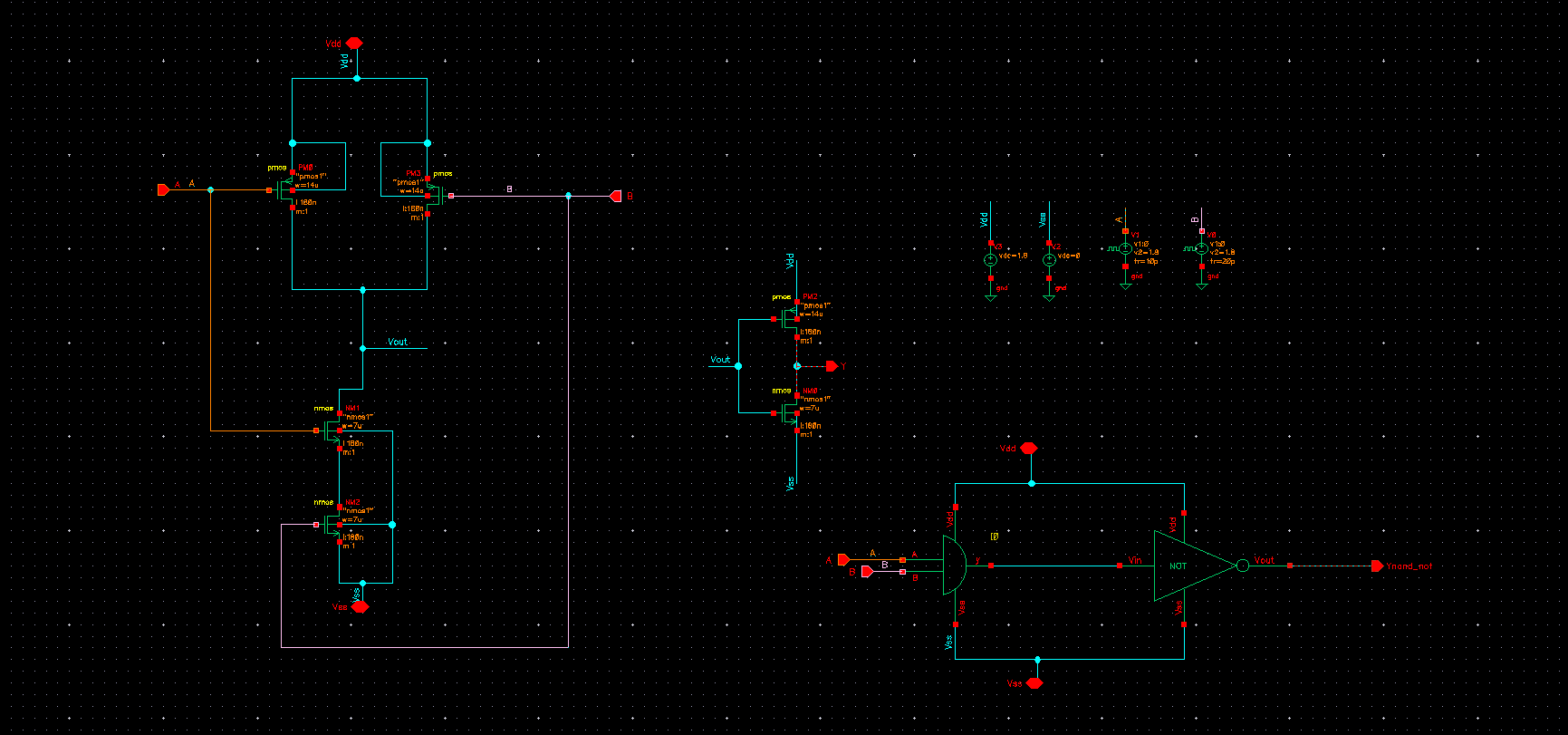


Fig8.9: Diagram AND delay comparison of pure mosfets vs gates combination

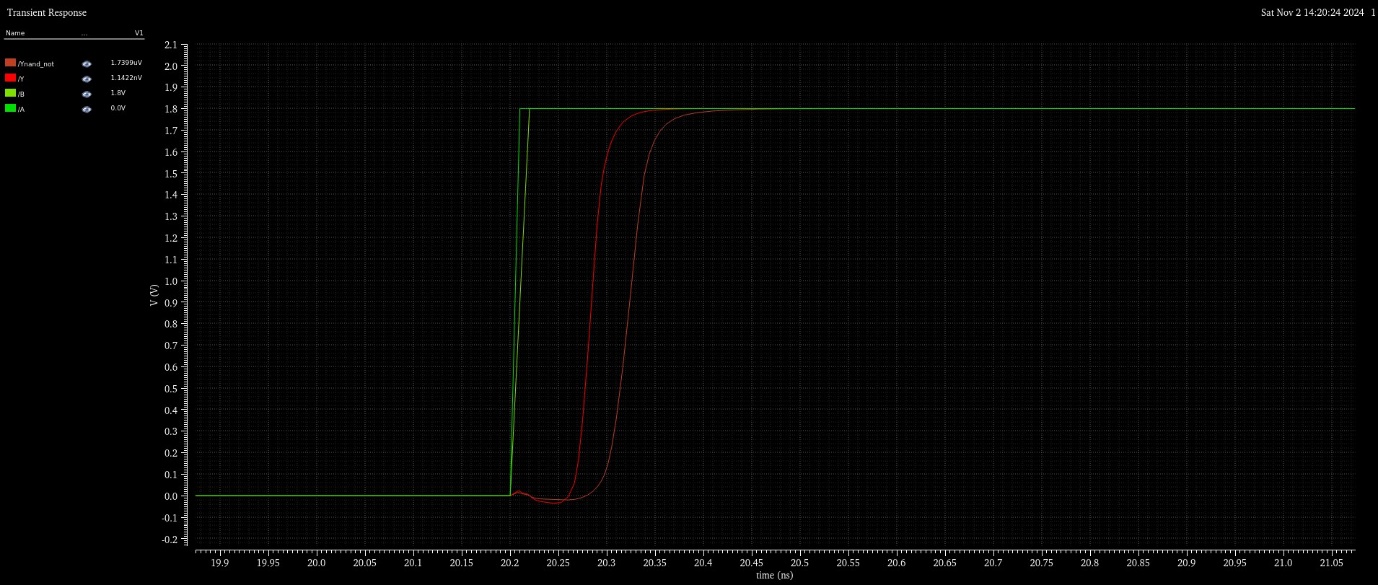


Fig8.10:AND gate delay comparison of pure mosfets vs gates combination

1. XOR GATE

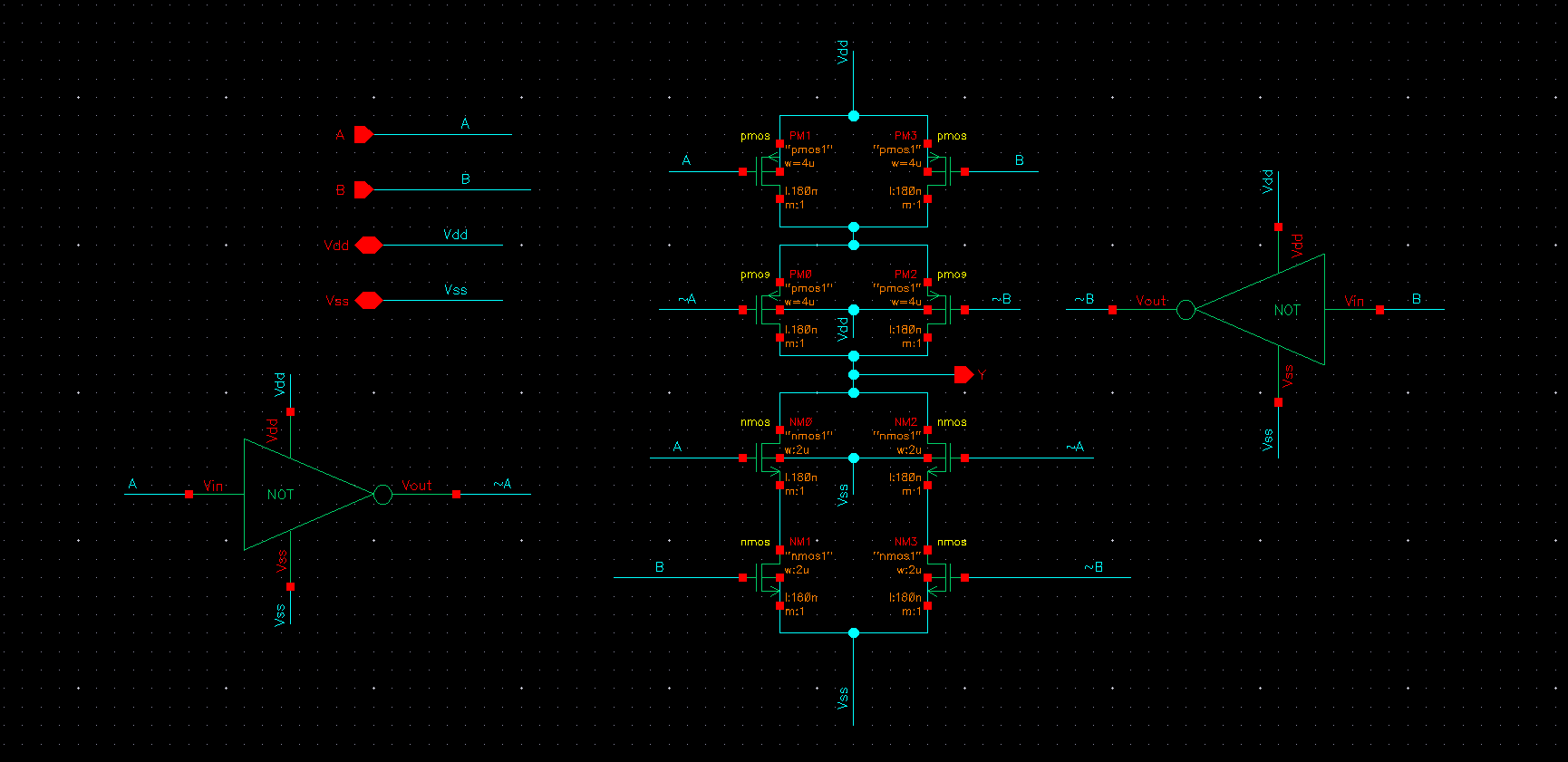


Fig 8.11: Circuit Diagram XOR



Fig 8.11: Delay calculation XOR gate

|  |  |  |
| --- | --- | --- |
| A | B | Y |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**Delay :**

Ton*=0.14ns*

*Toff=0.09ns*

*T=*

*T=0.11ns*

**Transistors:**

***8 mosfets***

1. **Half adder**

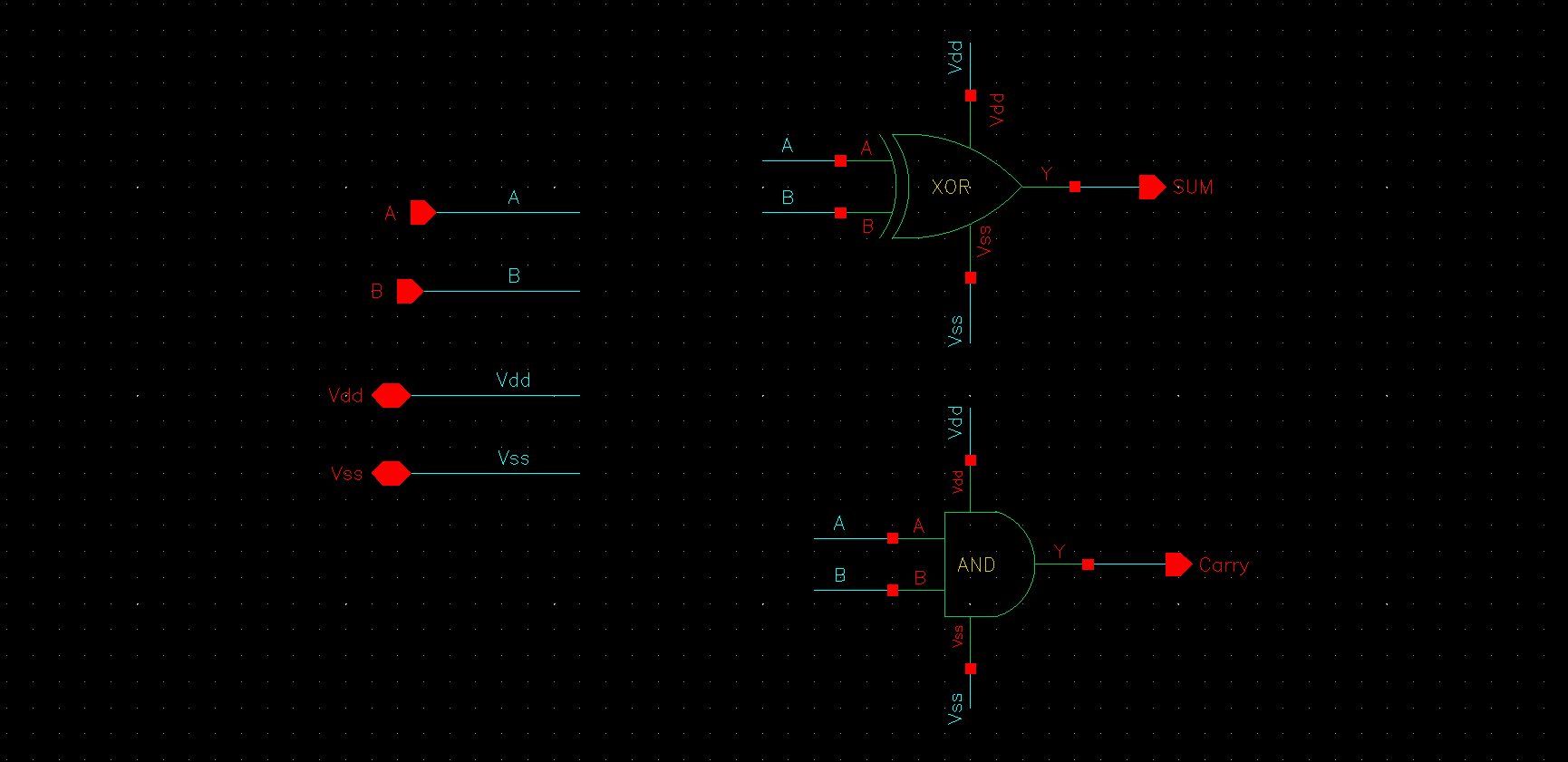


Fig 8.12: Circuit Diagram Half Adder

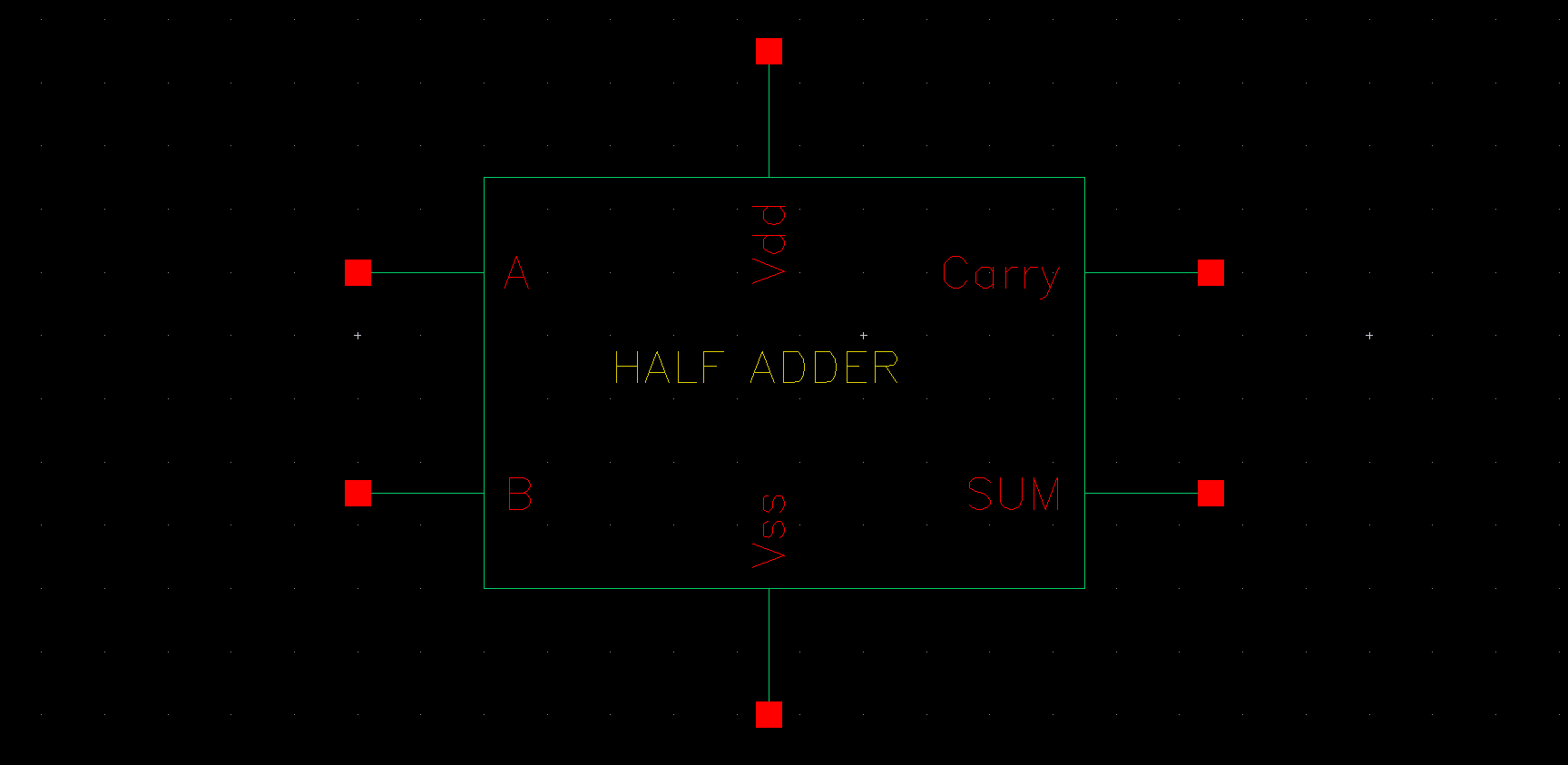


Fig 8.13: Symbol Half Adder

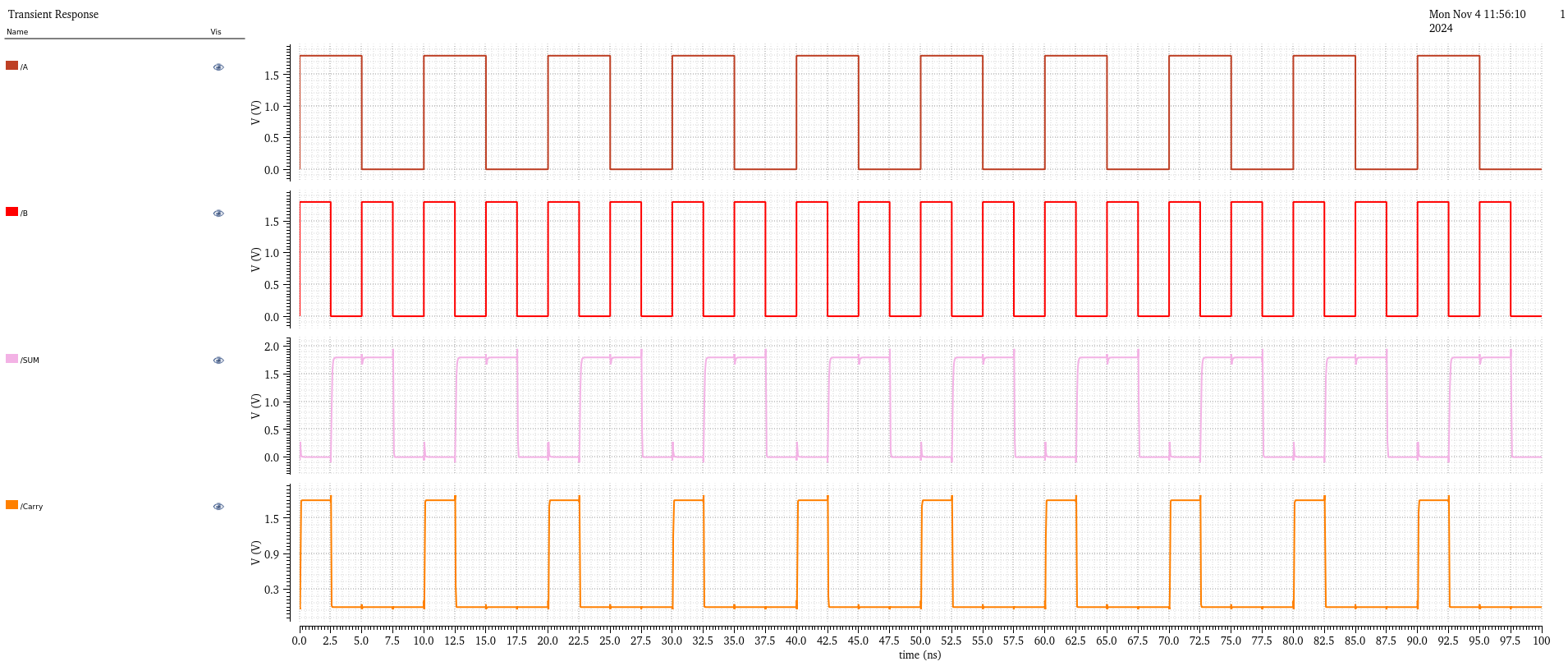


Fig 8.14: Output Half Adder

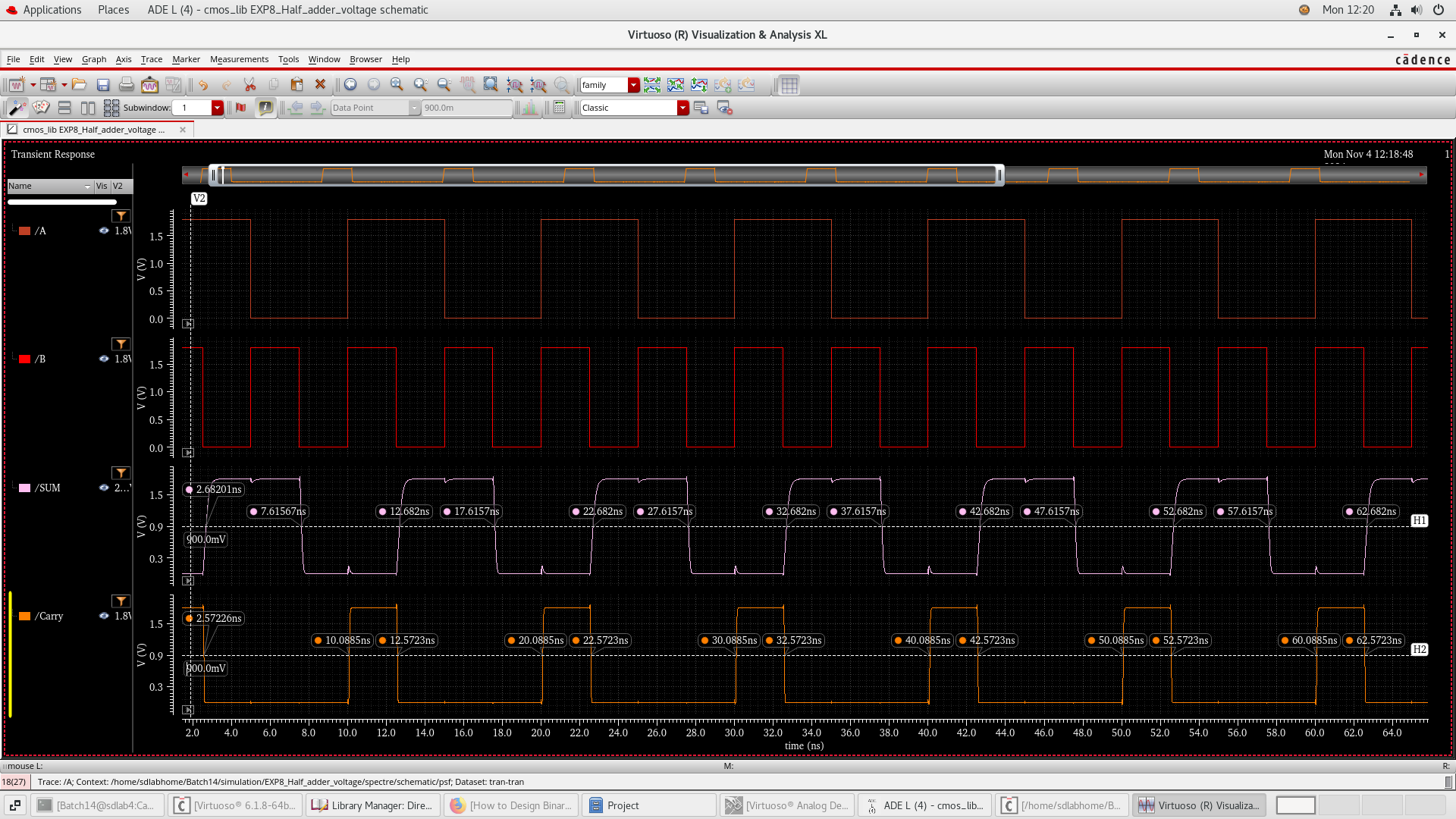


Fig 8.15: Delay calculation Half Adder

**Delay :**

**Sum:**

*Ton=0.07ns*

*Toff=0.06ns*

*T=*

*T=0.35ns*

**Carry:**

*Ton=0.179ns*

*Toff=0.07ns*

*T=*

*T=0.1245ns*

|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **B** | **Sum** | **Carry** |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

**Transistors:**

***20 mosfets***

1. **Full Adder:**

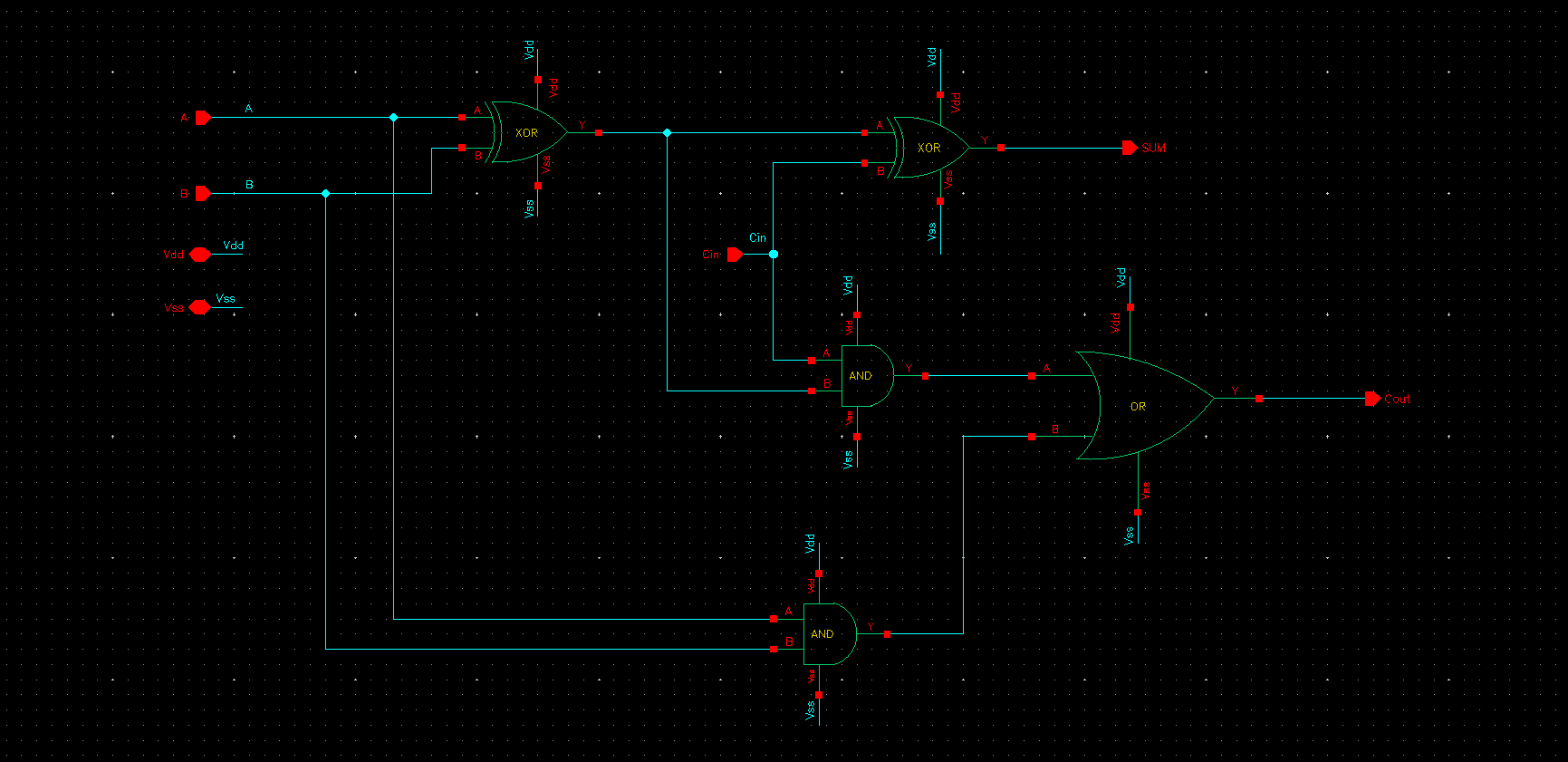


Fig 8.16: Circuit Diagram FULL adder using Gates



Fig 8.17: Delay Calculation Full Adder



Fig 8.18 : Circuit Diagram FULL adder using Mosfet



|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | C | S | C0 |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

Fig 8.19: Output FULL adder using Mosfet

**Delay :**

***Sum:***

*Ton=0.75ns*

*Toff=0.6ns*

*T=*

*T=0.65ns*

***Carry:***

*Ton=0.15ns*

*Toff=0.2ns*

*T=*

*T=0.17ns*

**Transistors:**

***28 mosfets***

### Part 2: Design of Low-Power¸ High Performance a)4 bit Vedic Multiplier B) 4bit multiplier using any of the Architecture

Theory

Introduction

Modern digital systems prioritize low power consumption and high performance due to stringent power requirements and the demand for faster operation. The design of basic arithmetic circuits, such as adders and multipliers, plays a critical role in achieving these objectives since these circuits are integral to most digital systems. In this lab, we aim to design full adder and half adder circuits, and a 4-bit multiplier using Vedic multiplication and a conventional architecture, focusing on minimizing power consumption while maximizing speed

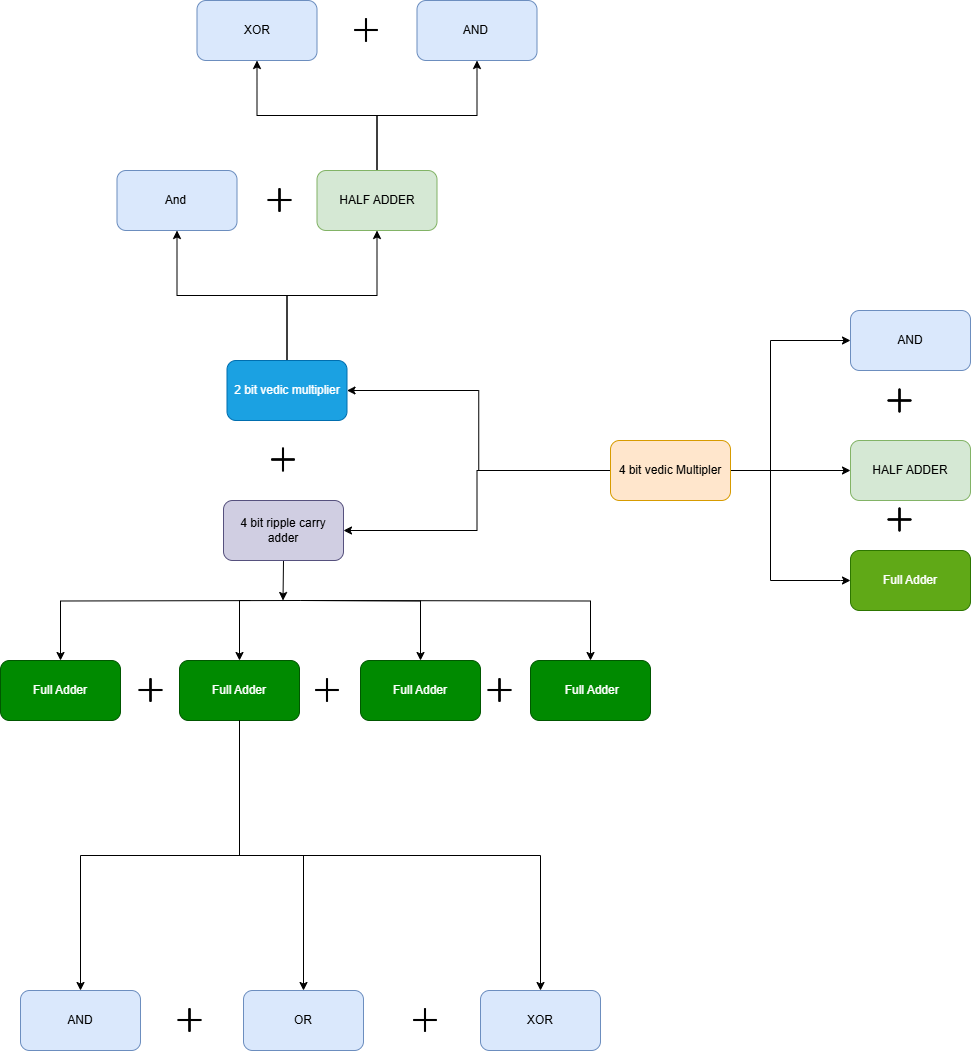


Fig 8.20: 2 Methods to make Vedic multiplier Block Diagram (tool used: Draw.io)

### Vedic Multilier

**1. Technique 1: Using NAND Gates, Half Adders, and Full Adders**

In this approach, a Vedic multiplier is constructed from fundamental logic components like NAND gates, half adders, and full adders. The process follows the "Urdhva Tiryakbhayam" or "vertically and crosswise" technique to create a hierarchical structure of partial products that can be efficiently added to form the final result(f)=−arctan(2πfRC)

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Sno. | Inputs | | | | | Output | | |
| *x* | *y* | *z* | *w* | *Ca* | *c,* | *c,* | *s* |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 3 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 4 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| *5* | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 6 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 7 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 8 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| 9 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 10 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 11 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 12 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 13 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| 14 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 15 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 16 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 17 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 18 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 19 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 20 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 21 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 22 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 23 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 24 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 25 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 26 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| 27 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 28 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 29 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 30 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 31 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 32 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |

Table: 4-bit multiplication

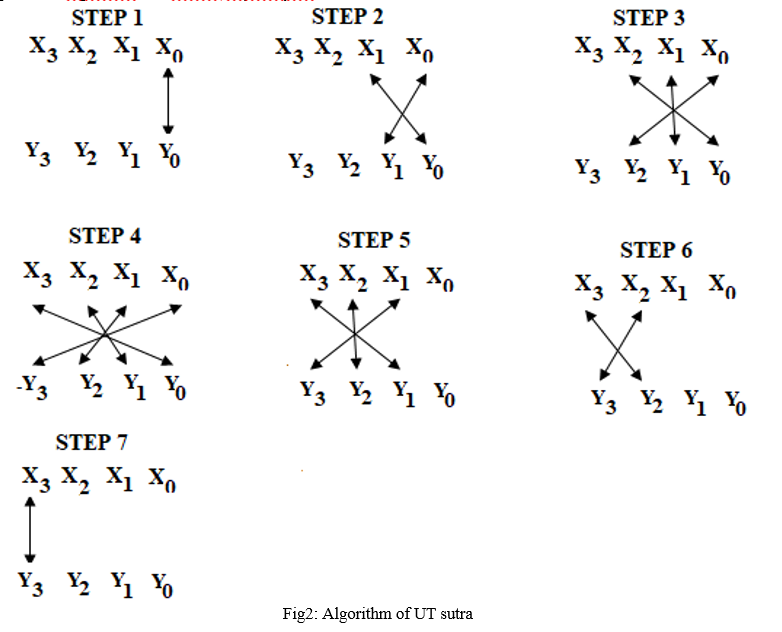


Fig 8.21: Algorithm of Vedic UT sutra

Src: www.ijraset.com%2Fresearch-paper%2Fvedic-multiplier

**a) Partial Product Generation**: Each bit of the multiplicand is multiplied with each bit of the multiplier using NAND gates, generating multiple partial products.

**b) Partial Product Summation**:

* **Half Adders** are used where there are only two partial products to be added.
* **Full Adders** are used where there are more than two partial products at a particular stage, to manage the carry generated

**c)Propagation**:

* The carry bits propagate through the structure, ensuring all partial products are combined systematically.
* Final summation of partial products gives the final output

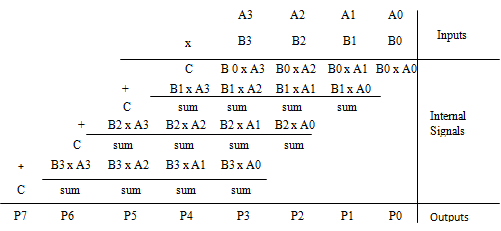


Fig 8.22: 4 Bit Array multiplication

Src: https://www.researchgate.net/ /Four-bit-Array-Multiplier

**Advantages**:

Since this method uses basic components, it is straightforward to implement on standard digital hardware

**Limitations**:

The carry propagation may introduce delays, particularly with larger bit-widths, reducing the efficiency for high-speed applications

**2. Technique 2: Using a 2-Bit Vedic Multiplier and Ripple Carry Adder Circuit**

This approach builds upon smaller Vedic multiplier blocks (such as 2-bit multipliers) to construct a larger multiplier. By combining these smaller units with a ripple carry adder circuit, the design achieves efficient scaling for larger bit-width multipliers while maintaining high speed

**2-Bit Vedic Multiplier Blocks**:

* Each 2-bit Vedic multiplier module generates partial products using the Vedic "Urdhva Tiryakbhayam" method
* These small blocks simplify and parallelize the multiplication process, which can be scaled up to 4-bit, 8-bit, or larger multipliers

**2.Ripple Carry Adder**:

* After generating partial products from the 2-bit Vedic multiplier blocks, a **ripple carry adder** is used to sum these partial products
* The ripple carry adder handles the carry propagation between successive additions of partial products, ensuring the accuracy of the final result.

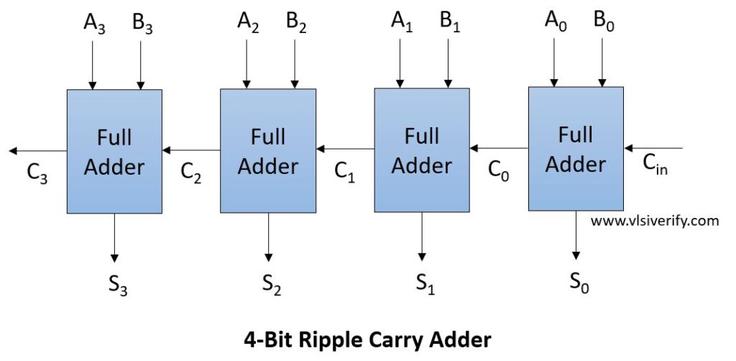


Fig 8.23: 4 Bit Ripple carry adder

Src: https://vlsiverify.com

**Advantages**:

* Reduces the overall propagation delay since each 2-bit module operates in parallel
* High scalability for larger bit-widths while minimizing power consumption

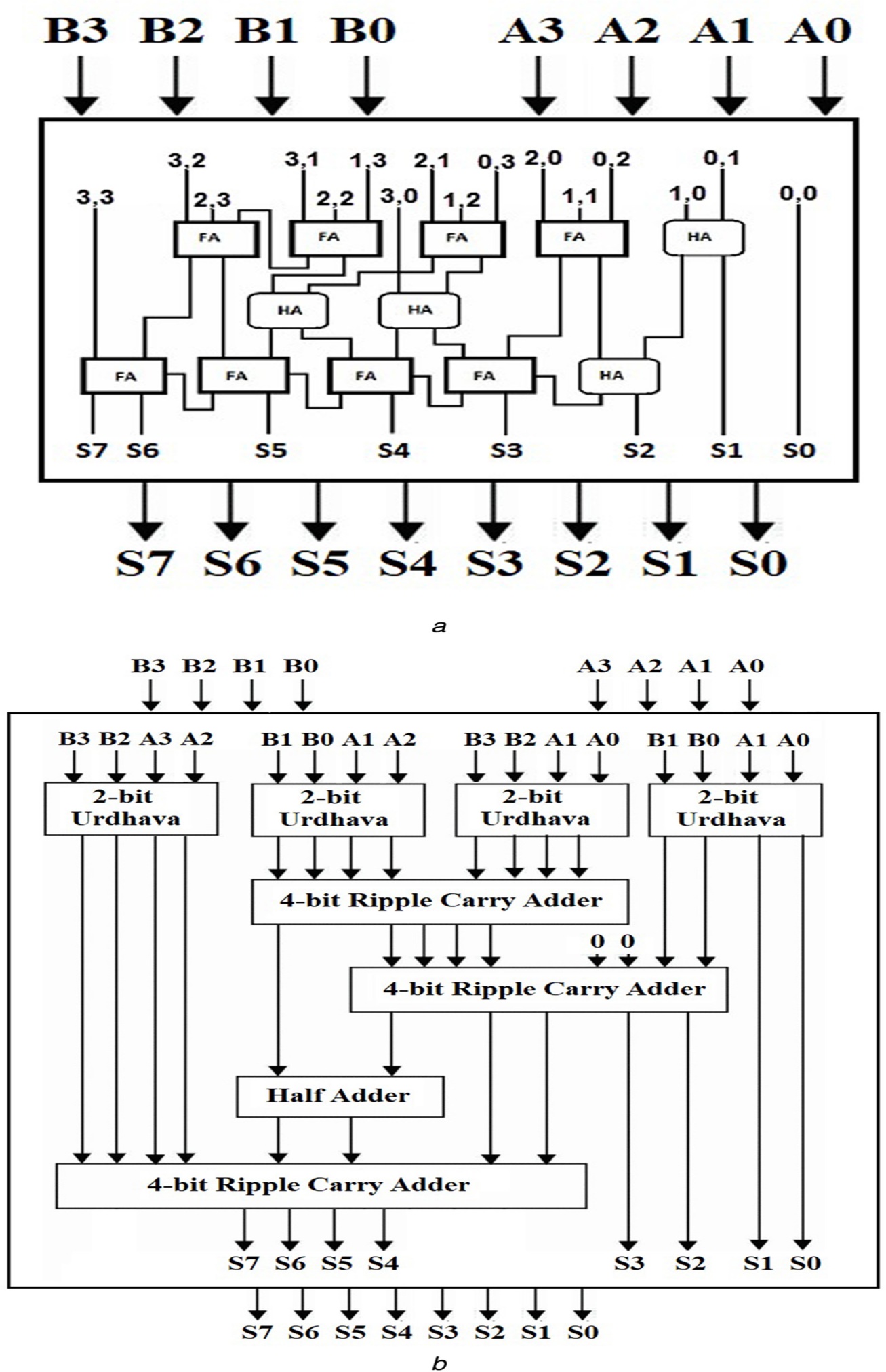


Fig 8.24: Circuit Diagram Vedic Multiplier using Ripple carry adder

Src: www.ijraset.com /vedic-multiplier-based-on-look-ahead-carry-adder

**Comparison**:

* **NAND Gate-Based**: Best suited for smaller multipliers where simplicity and ease of implementation are priorities.
* **2-Bit Vedic Multiplier with Ripple Carry Adder**: Ideal for larger multipliers, where speed and efficiency are essential.

Both techniques are valuable, with the choice depending on the application's bit-width requirements and the balance between power and speed constraints

### circuit Design

1. 4 Bit multiplier

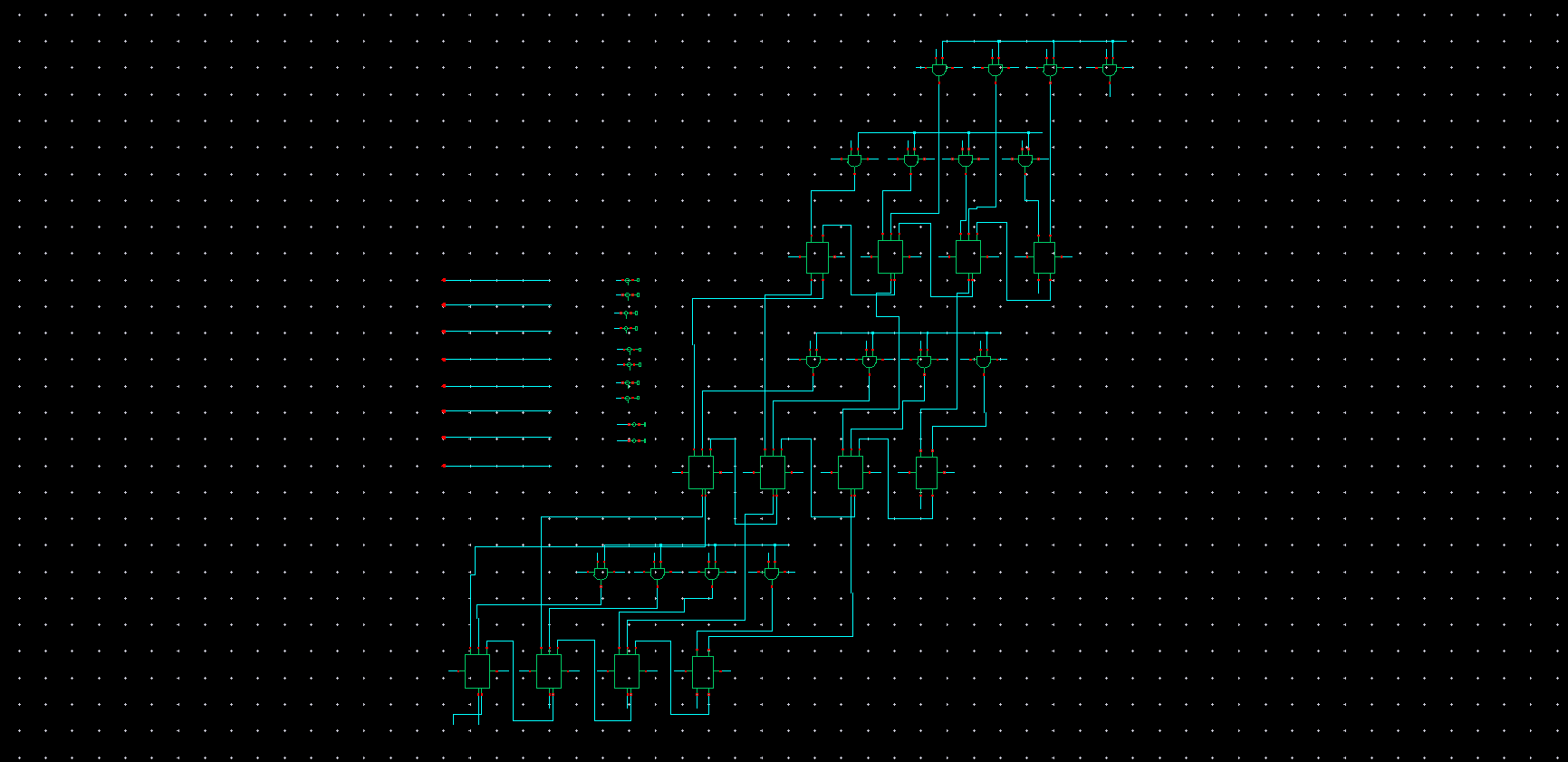


Fig 8.25: 4bit Normal multiplier



Fig 8.26: 4bit Normal multiplier Symbol

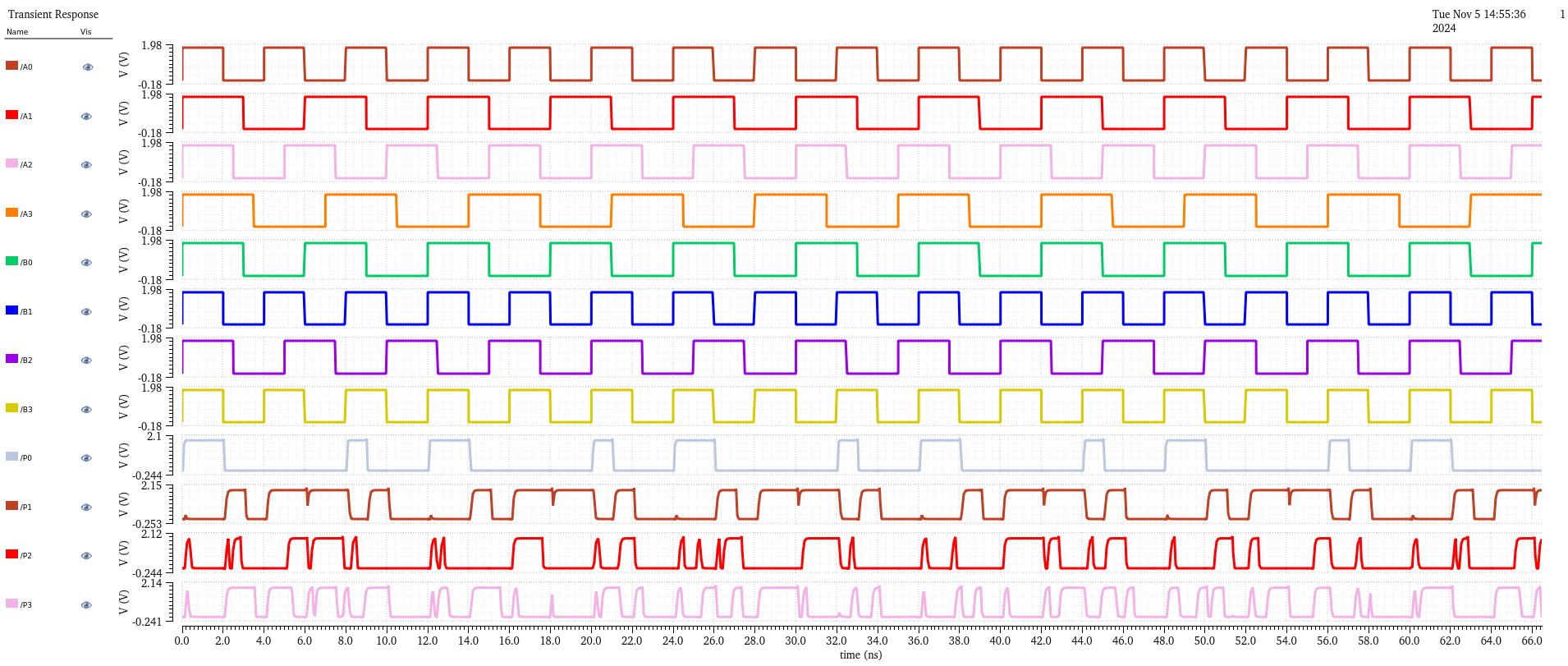


Fig 8.27: 4bit Normal multiplier output plot 1

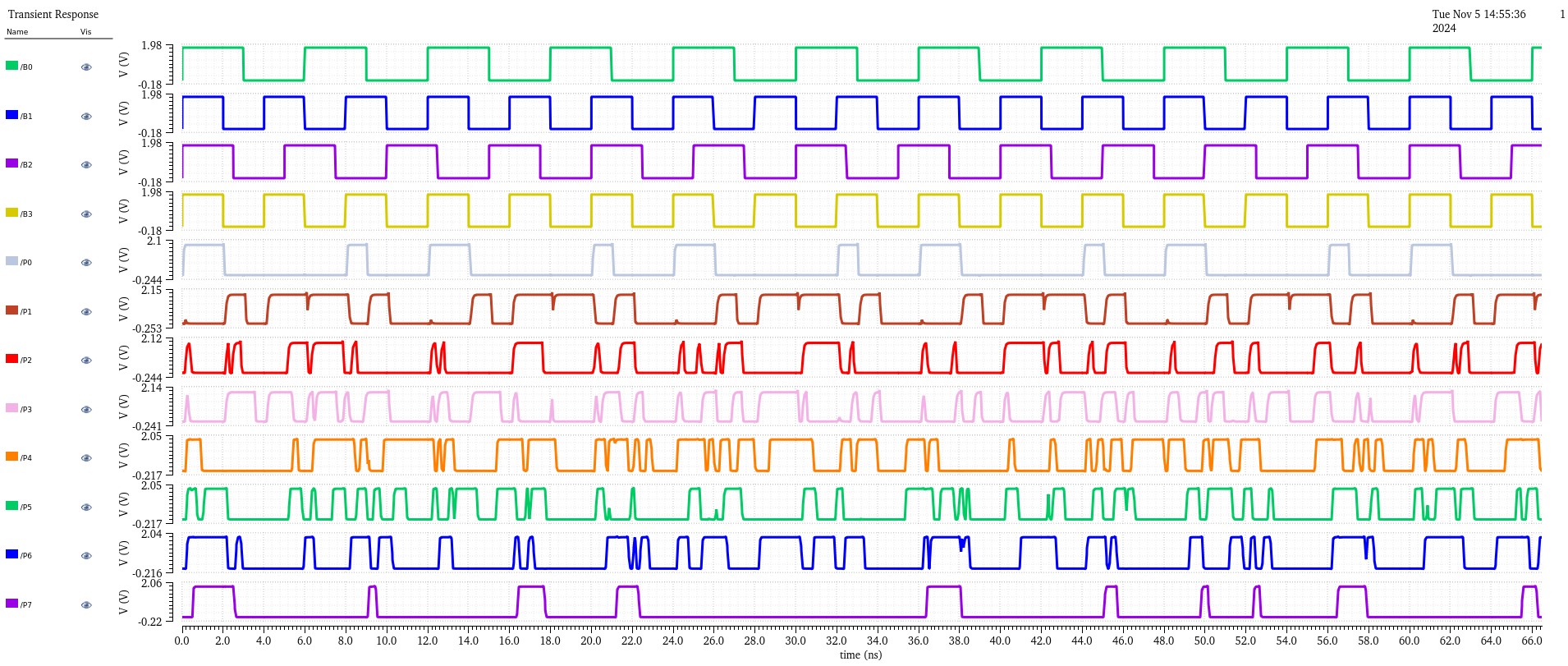


Fig 8.28 : 4bit Normal multiplier output plot 2



Fig 8.28A : 4bit Vedic multiplier using half adder and full adder

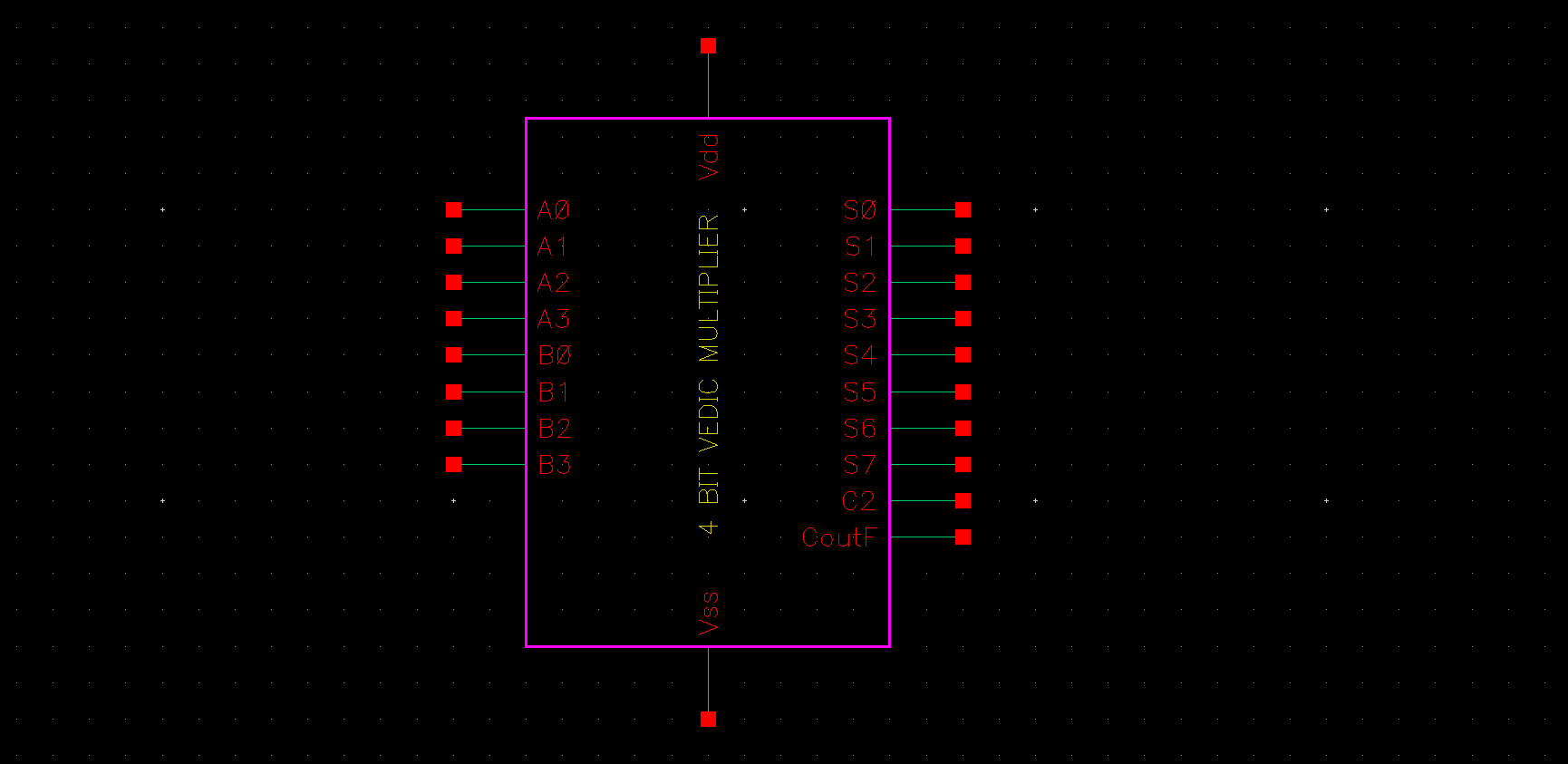


Fig 8.28B : 4bit Vedic multiplier Symbol using half adder and full adder

1. **2 Bit Vedic multiplier:**

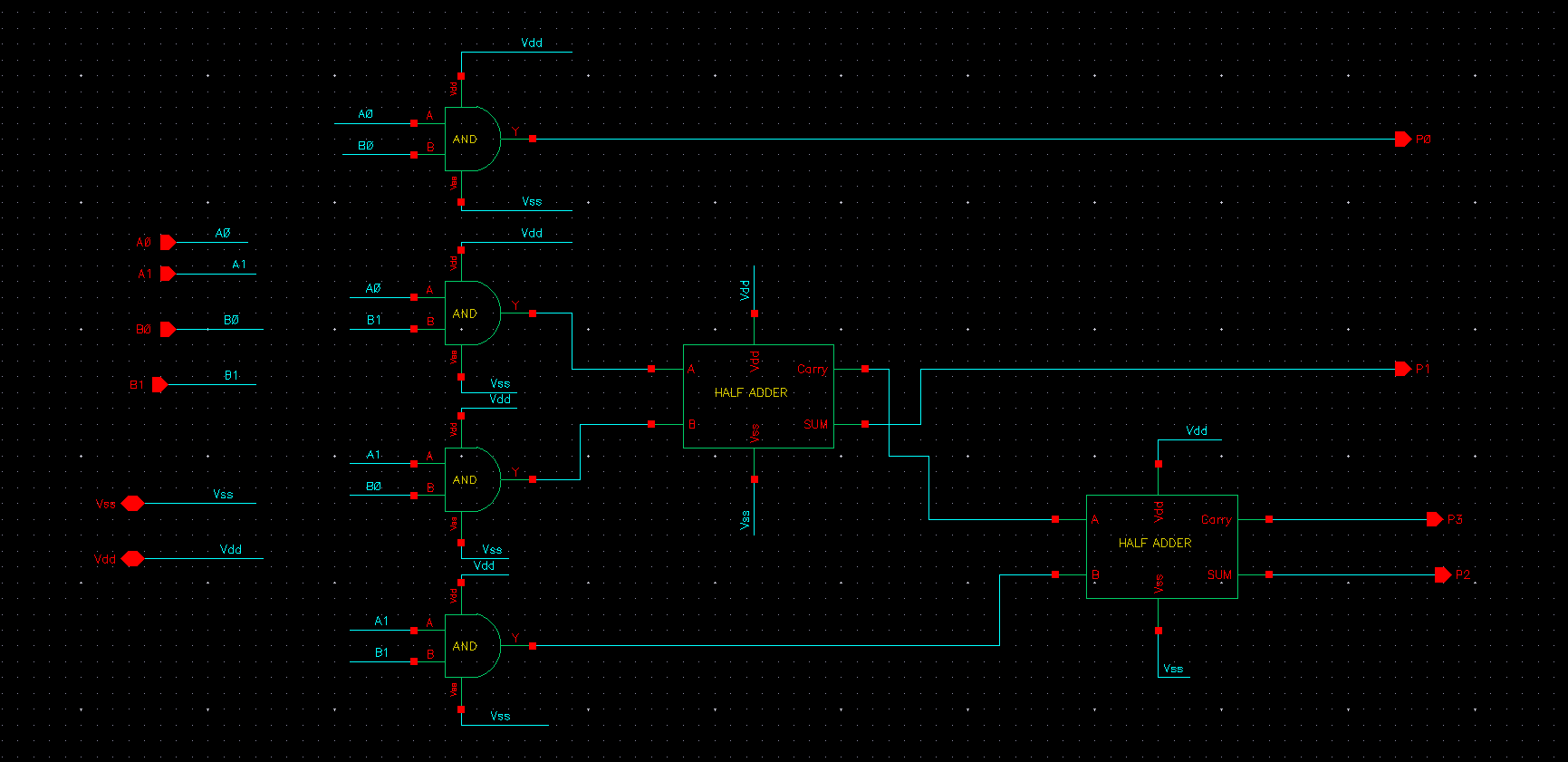


Fig 8.29 : 2 bit Vedic multiplier



Fig 8.29 : 2 bit Vedic multiplier Delay calculation

**Delay :**

Ton*=0.0344ns*

*Toff=0.107ns*

*T=*

*T=0.55ns*

**Transistors:**

***64 mosfets***

1. **4 Bit ripple carry adder:**

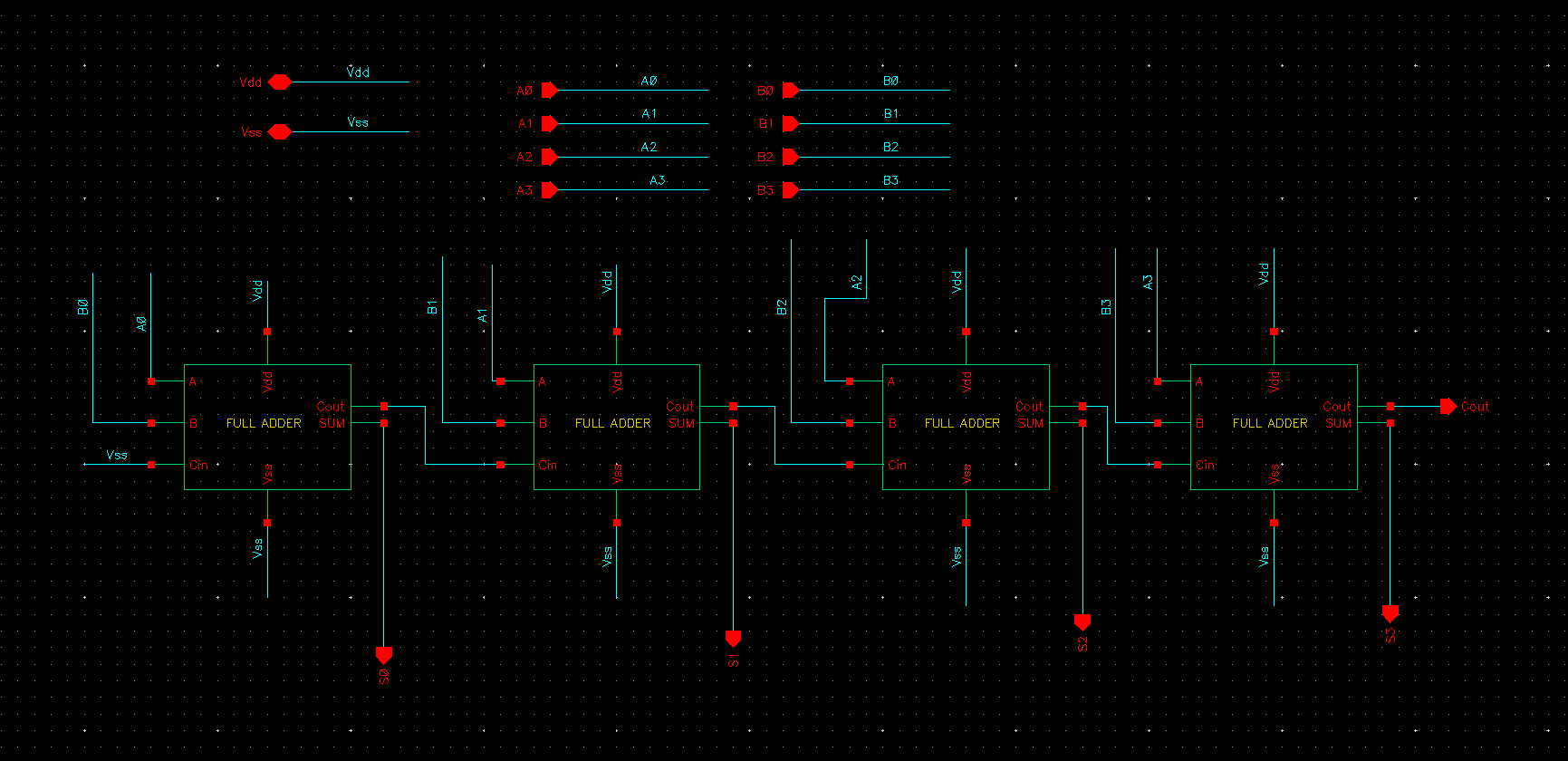


Fig 8.30: 4bit ripple carry adder



**Delay :**

Ton*=1.02.ns*

*Toff=0.5ns*

*T=*

*T=0.75ns*

**Transistors:**

***112 mosfets***

1. **4 Bit Vedic multiplier:**

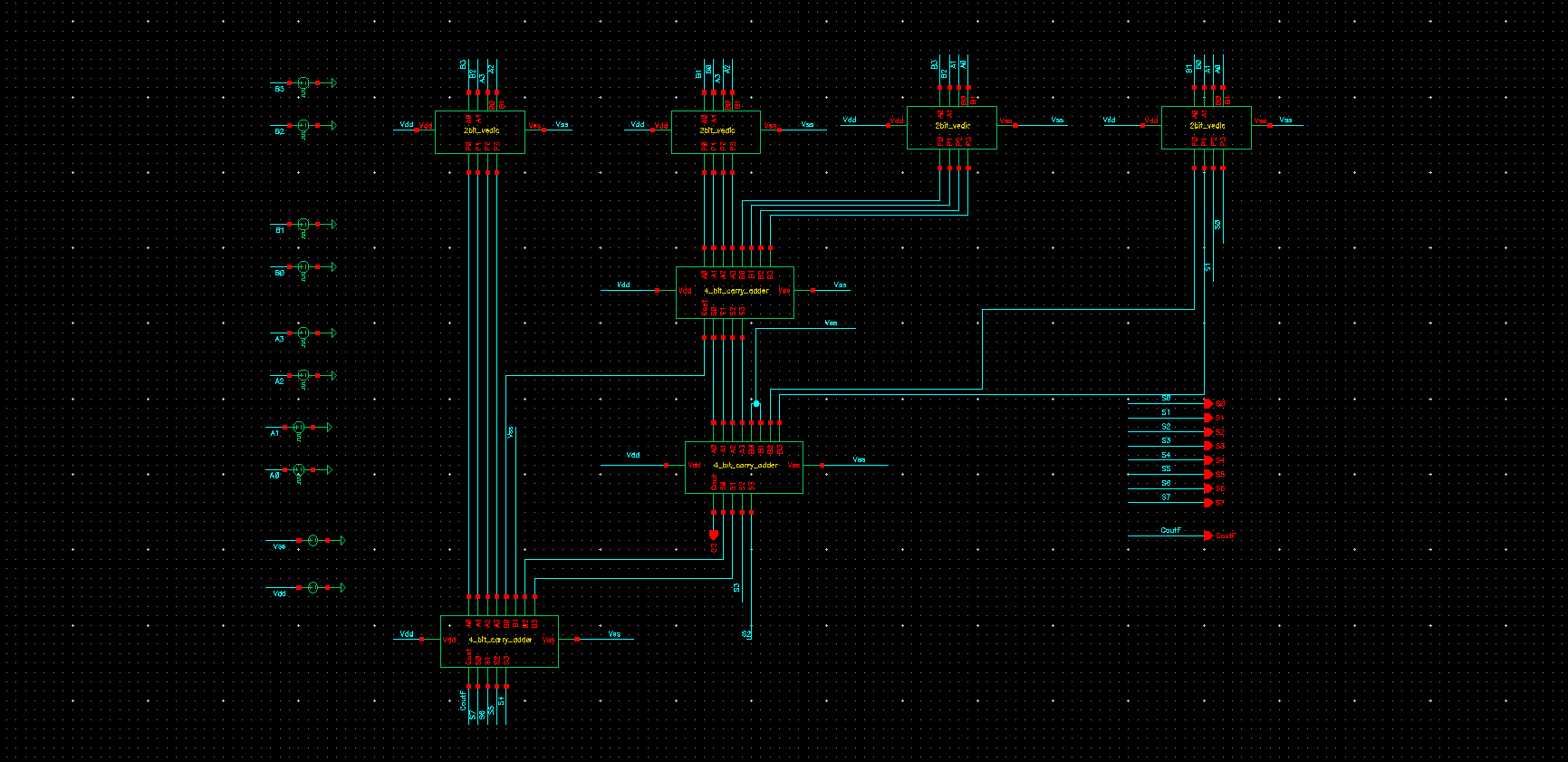


Fig 8.31 : 4bit Vedic multiplier using ripple carry adder



Fig 8.31 : 4bit Vedic multiplier using ripple carry adder delay calculation

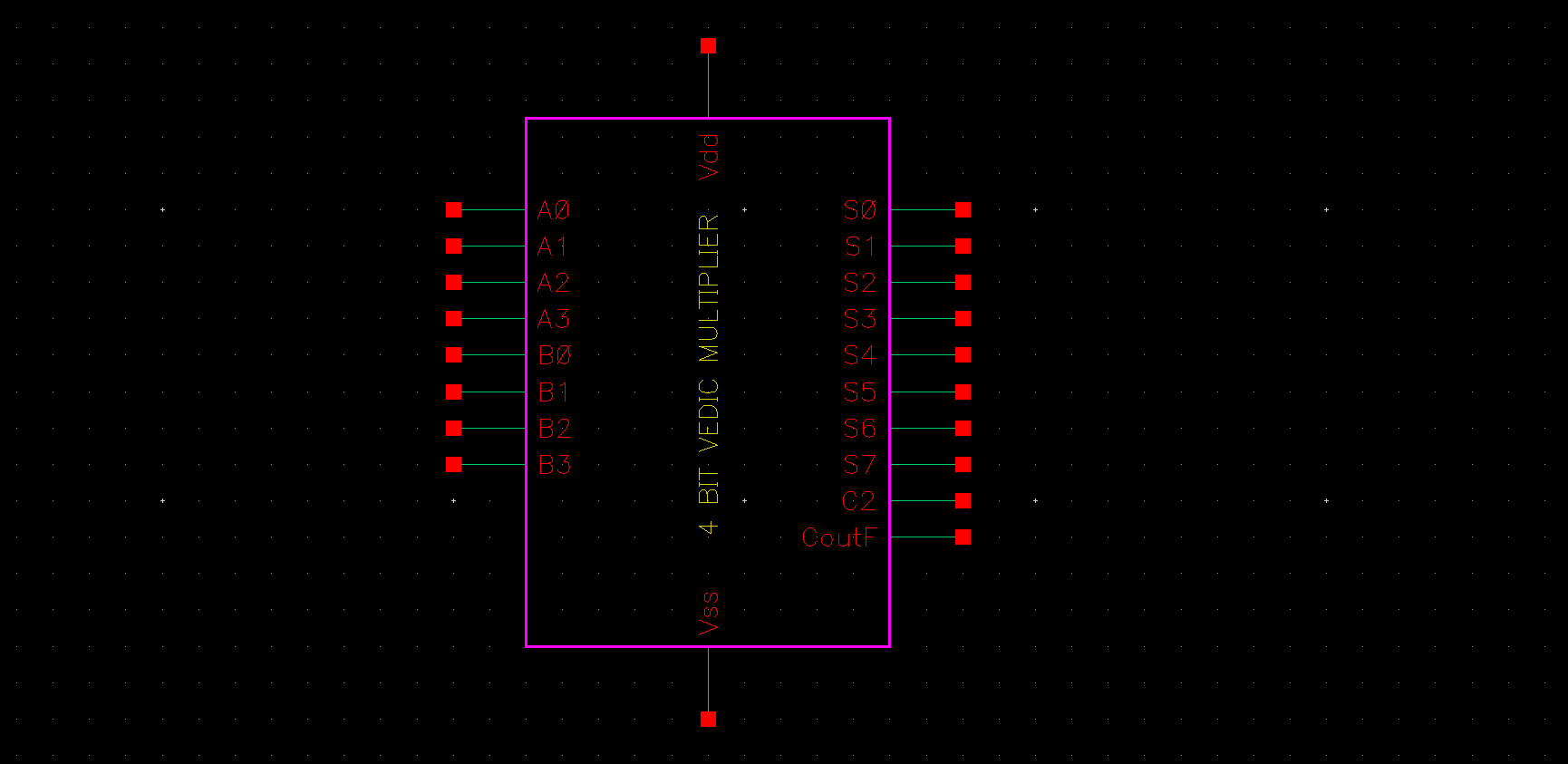


Fig 8.32: 4bit Vedic multiplier symbol

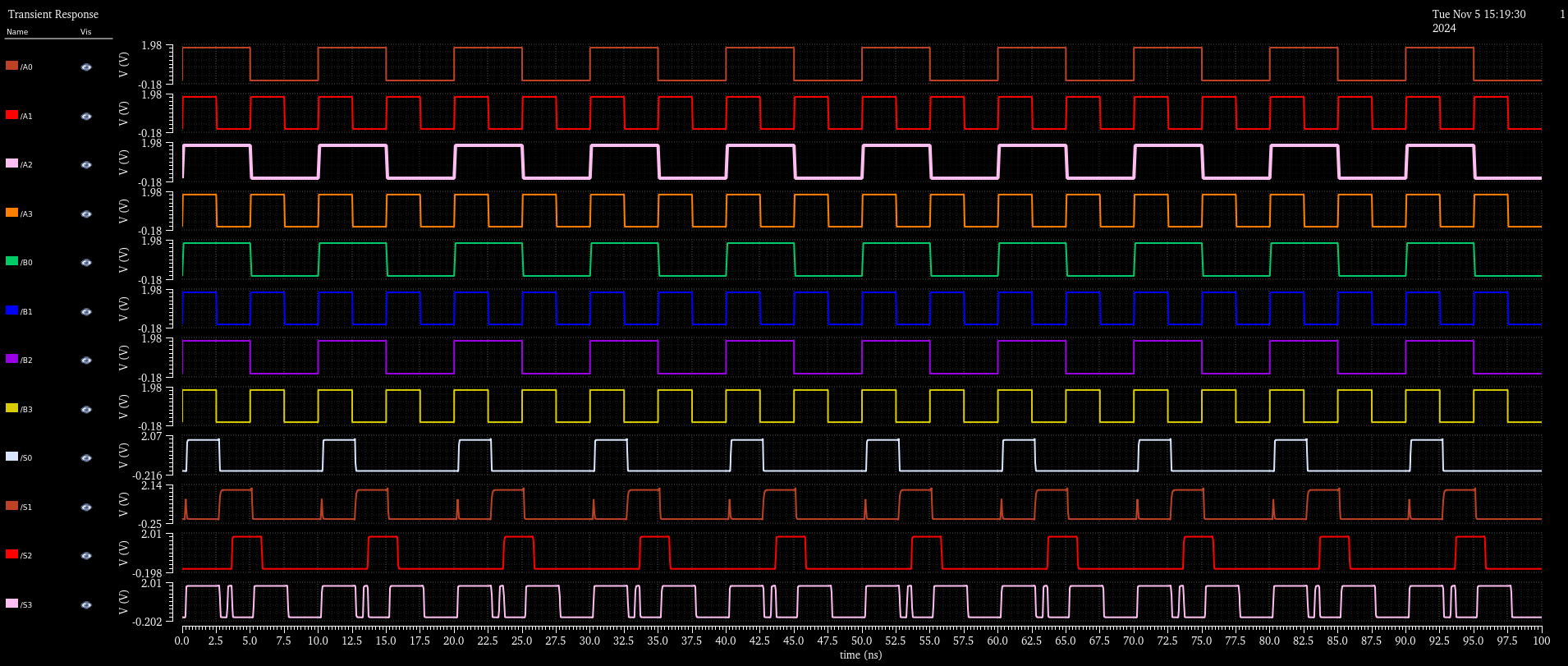


Fig 8.33 : 4bit Vedic multiplier using RCA output plot 1

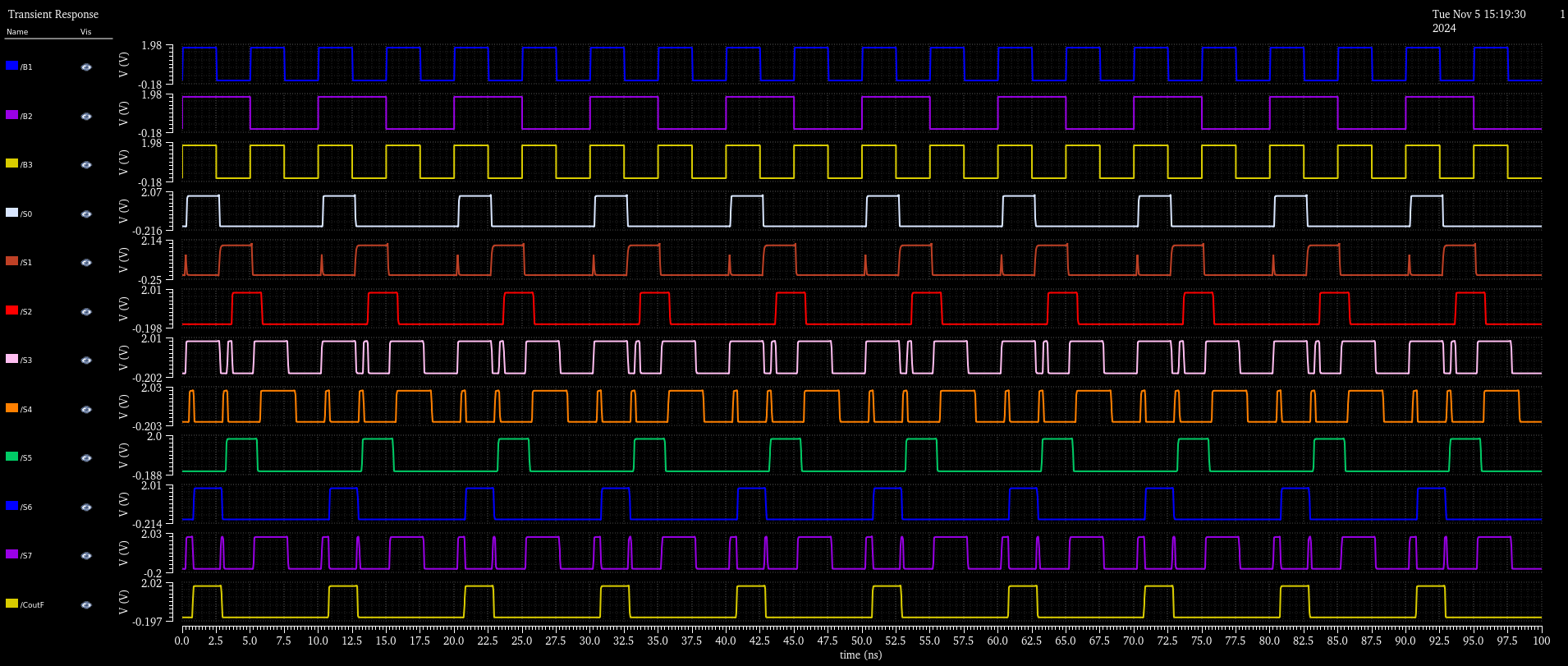


Fig 8.35 : 4bit Vedic multiplier using RCA output plot 2

**Delay :**

Ton*=1.02ns*

*Toff=0.82ns*

*T=*

*T=0.92ns*

**Transistors:**

***592 mosfets***

### procedure

1. **Project Setup**
   * Open the Cadence software, and navigate to the project workspace.
   * Create a new project, specifying a directory for saving the files, and select the technology library as per the lab requirements.
2. **Schematic Design**
   * Open the **Schematic Editor** and start designing the schematic for the circuit. For instance, for a full adder:
     + Add the necessary transistors, logic gates, or components (NAND gates, half adders, etc.) from the component library.
     + Connect the components to complete the full adder schematic.
   * Verify the connections for correctness, ensuring all inputs and outputs are connected according to the circuit design.
3. **Simulation Setup**
   * Once the schematic is complete, initiate a simulation setup:
     + Go to the **Analog Design Environment (ADE)** and choose the required analysis types (Transient, DC, or AC Analysis).
     + Set the input signal parameters, such as voltage, frequency, and pulse width, according to the specific analysis.
     + Define the output signals to monitor, such as voltage or power at particular nodes or outputs.
4. **Define Test Parameters**
   * In the ADE environment, specify key parameters:
     + Set the **VDD** voltage (e.g., 1.8V) and threshold voltage **Vth**.
     + Configure the load capacitance and input signals to replicate real operating conditions.
     + For transient analysis, define a time period for observing the circuit’s response.
5. **Run Simulations**
   * Run the configured simulations and observe the waveforms. Typical analysis types include:
     + **Transient Analysis**: Examine the circuit’s time-domain response, observing signal transitions, delays, and transient behaviors.
     + **DC Analysis**: Sweep input voltages to determine the transfer characteristics, such as voltage gain or switching threshold.
     + **AC Analysis**: Measure frequency response for circuits sensitive to specific frequency ranges.
6. **Data Collection**
   * Using the waveform viewer, measure the required parameters such as:
     + **Propagation Delay**: Measure the delay between input transition and the corresponding output transition.
     + **Power Consumption**: Measure average power by integrating the power waveform over a period.
   * Save waveform screenshots and data points for analysis.
7. **Adjustment and Re-Run (if applicable)**
   * Modify design parameters if needed (e.g., transistor width for optimizing power or delay).
   * Re-run simulations to observe the effect of parameter variations on performance metrics.
8. **Data Analysis**
   * From the simulation results, calculate key values:
     + Calculate power dissipation and propagation delay for specific inputs and output transitions.
     + Tabulate results based on variations in circuit parameters, such as width (Wp/Wn) or supply voltage (VDD).
9. **Documentation**
   * Export results, screenshots of waveforms, and calculated values to integrate into the lab report.
   * Summarize the findings in the **Observation** and **Results** sections, discussing trends and design implications.

### Observations

 **Power-Delay Trade-off**

* **Observation:** As transistor width (Wp/Wn) increases, both power dissipation and propagation delay are affected. A **larger transistor width** generally results in **reduced propagation delay** due to faster switching times, but it increases power consumption.
* **Example Observation:** When Wp/Wn was set to a higher ratio, power dissipation increased to μW, while propagation delay decreased to 20 ns, indicating a trade-off between power and speed.

 **Effect of Supply Voltage (VDD) Variation**

* **Observation:** Higher supply voltages (VDD) increase the current through the transistors, thus reducing delay but significantly increasing power dissipation.
* **Example Observation**: At VDD=1.8VV\_{DD} = 1.8VVDD​=1.8V, the propagation delay was measured at **15 ns** with power dissipation of **500 μW**. However, at VDD=1.2VV\_{DD} = 1.2VVDD​=1.2V, delay increased to **25 ns** while power consumption decreased to **320 μW**.

  **Propagation Delay (tp) Calculation**

* **Observation:** Propagation delay, calculated as the average of rising and falling edge delays, is directly influenced by both load capacitance and transistor sizing.
* **Example Observation**: For a full adder circuit, the rise time delay was calculated as **18 ns** and fall time delay as **22 ns**, resulting in an average propagation delay of **20 ns**

 **Power Dissipation Analysis**

* **Observation:** Power dissipation is highest during the switching events of the transistors due to dynamic power. Static power was observed to be negligible in low-power CMOS designs.
* **Example Observation**: Dynamic power spikes were noted during transitions, with maximum power dissipation reaching **460 μW** during high-to-low transitions..

 **Transfer Curve Characteristics**

* **Observation:** The transfer curve varies with transistor width ratio (Wp/Wn) and supply voltage. A higher Wp/Wn ratio results in steeper transitions in the transfer curve, while increased VDD shifts the curve, reducing threshold voltage impact.
* **Example Observation:** A transfer curve with Wp/Wn of displayed a steeper transition compared to Wp/Wn of , indicating improved switching performance.

 **Delay and Power Dissipation for Vedic Multiplier**

* **Observation**: The Vedic multiplier design using NAND gates and adders exhibited increased delay and power as compared to a design with 2-bit Vedic multipliers and ripple carry adders.

**Example Observation**: For a 4-bit Vedic multiplier, the power delay product (PDP) measured for the NAND-based architecture was **120 pJ**, whereas the PDP for the ripple-carry approach was **95 pJ**.

### Results

Table of Observed Values

|  |  |  |  |
| --- | --- | --- | --- |
| Parameter | Delay (ns) | Power (μW) | PDP (pJ) |
| Inverter | 0.03 | 13.3 | 0.399 |
| NAND Gate | 0.24 | 18.72 | 4.492 |
| AND Gate | 0.22 | 28.32 | 6.23 |
| OR Gate | 0.27 | 32.18 | 8.688 |
| XOR Gate | 0.11 | 42.53 | 4.67 |
| Half Adder | 0.35 | 84.82 | 29.6 |
| Full Adder | 0.65 | 220.41 | 143.19 |
| 2-bit vedic Multiplier | 0.5 | 140.58 | 70.25 |
| 4 -bit VedicType 1 | 1.43 | 1429 | 2043.47 |
| 4 -bit Vedic Type 2 | 0.92 | 1138 | 1046.96 |

### conclusion

This project successfully analyzed the design of low-power, high-performance half adders, full adders, and Vedic multipliers using Cadence software. Key parameters such as propagation delay, power dissipation, and the Power-Delay Product (PDP) were measured to evaluate the effectiveness of each design approach.

 **Power-Delay Trade-off**

* **Observation**: As transistor width (Wp​/Wn​) increases, both power dissipation and propagation delay are affected. A larger transistor width generally results in reduced propagation delay due to faster switching times, but it increases power consumption.
* **Example Observation**: When Wp ​/Wn​ was set to a higher ratio, power dissipation increased to **450 μW**, while propagation delay decreased to **20 ns**, indicating a trade-off between power and speed.

 **Effect of Supply Voltage (VDD) Variation**

* **Observation**: Higher supply voltages (VDDV\_{DD}VDD​) increase the current through the transistors, thus reducing delay but significantly increasing power dissipation.
* **Example Observation**: At VDD=1.8VV\_{DD} = 1.8VVDD​=1.8V, the propagation delay was measured at **15 ns** with power dissipation of **500 μW**. However, at VDD=1.2VV\_{DD} = 1.2VVDD​=1.2V, delay increased to **25 ns** while power consumption decreased to **320 μW**.

 **Propagation Delay (tpt\_ptp​) Calculation**

* **Observation**: Propagation delay, calculated as the average of rising and falling edge delays, is directly influenced by both load capacitance and transistor sizing.
* **Example Observation**: For a full adder circuit, the rise time delay was calculated as **18 ns** and fall time delay as **22 ns**, resulting in an average propagation delay of **20 ns**.

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* **Observation**: Power dissipation is highest during the switching events of the transistors due to dynamic power. Static power was observed to be negligible in low-power CMOS designs.
* **Example Observation**: Dynamic power spikes were noted during transitions, with maximum power dissipation reaching **460 μW** during high-to-low transitions.

 **Transfer Curve Characteristics**

* **Observation**: The transfer curve varies with transistor width ratio (wp​/Wn​) and supply voltage. A higher Wp​/Wn​ ratio results in steeper transitions in the transfer curve, while increased VDD​ shifts the curve, reducing threshold voltage impact.
* **Example Observation**: A transfer curve with Wp​/Wn​ of **3:1** displayed a steeper transition compared to Wp​/Wn​ of **1:1**, indicating improved switching performance.

 **Delay and Power Dissipation for Vedic Multiplier**

* **Observation**: The Vedic multiplier design using NAND gates and adders exhibited increased delay and power as compared to a design with 2-bit Vedic multipliers and ripple carry adders.
* **Example Observation**: For a 4-bit Vedic multiplier, the power delay product (PDP) measured for the NAND-based architecture was **120 pJ**, whereas the PDP for the ripple-carry approach was **95 pJ**.

### Final Remarks

In conclusion, the experiments validated that careful selection of design parameters, including transistor dimensions and supply voltage, can significantly impact the performance of adders and multipliers. The findings suggest that the ripple carry-based Vedic multiplier architecture provides an advantageous balance between power and speed, making it an ideal choice for low-power, high-speed applications. Future work can explore further optimizations by leveraging additional CMOS design techniques, potentially leading to even greater efficiency improvements.

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