www.orbitmentor.com **GATE ESE 2020 TARGET**

ECE ENGINEERING

www.orbitmentor.com **GATE ESE 2020 TARGET** BE HAPPY DO HARDWORK

GATE ESE PSU's 2019-20

GATEACADEMY

104 DIGITAL SYSTEM_GATEACADEMY

TOTAL PAGE DIGITAL SYSTEM-320 PGAE

LATEST GATEACADEMY CLASSROOM HANDWRITTING

CONTENT COVERED:

1. Theory Notes
2. Explanation
3. Derivation
4. Example
5. Shortcut & Formula Summary
6. Previous year Paper Q. Sol.

Noted-: Single Source Follow, Revise

Multiple Time Best key of Success

http://www.orbitmentor.com Email-gateiesinfo4mech@gmail.com

Number System

* **Binary**

Radix = 2

Unique digit: 0 1

Sequence: 0, 1, 10, 11, 100, 101, 110, 111, 1000

Octal

Radix = 8

Unique digit: 0, 1, 2, 3, 4, 5, 6, 7

Sequence:

0	10 ···	70	100
1	11 ···	71	101
2	12 ···	72	102
3	13 ···	73	103
4	14 ···	74	104
5	15 ···	75	105
6	16 ···	76	106
7	17 ···	77	107

Decimal

Radix = 10

Unique digit: 0 1 2 3 4 5 6 7 8 9

Sequence:

0	10 ···	90	100
1	11	91	101
2			
3			
4			
5			
6			
7			
8			
9	19	99	109

Hexadecimal

Radix = 16

Unique digit: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F

Sequence

0	10 ··	90	A0 ··	F0
1	11			
2	12			
3	13			
4	14			
5	15			
6	16			
7	17			
8	18			
9	19			
A	1A			
B	1B			
C	1C			
D	1D			
E	1E			
F	1F	9F	AF	FF

* **Any Number System to Decimal Number System Conversion**

1. $(10101.1101)_2$

Sol: $2^4 \quad 2^2 \quad 2^0 \quad 2^{-1} \quad 2^{-2} \quad 2^{-4}$

$\Rightarrow 21 + \frac{1}{2^7} = (21.8278)_{10}$

2. $(714.35)_8 = 7\times8^2 + 1\times8^1 + 4\times8^0 + 3\times8^{-1} + 5\times8^{-2}$

$= (460.45)_{10}$

3. $(A2.C37)_{16} = A\times16^1 + 2\times16^0 + 12\times16^{-1} + 3\times16^{-2} + 7\times16^{-3}$

$= 160 + 2 + \frac{12}{16} + \frac{3}{256} + \frac{7}{4096}$

$= (162.763)_{16}$

4. $(45.12)_6 = 4\times6 + 5 + \frac{1}{6} + \frac{2}{36}$

$= 29 + \cancel{} = (29.22)_6$

5) $(25.31)_9$

Sol $2\times9+5+\frac{3}{9}+\frac{1}{81}$

$\Rightarrow 23+\frac{27+1}{81}$

$\Rightarrow 23+\frac{28}{81} = (23.34)_{10}$

* Decimal number System to any number System.

1) $(29.20)_{10} \longrightarrow (\quad)_2$

Sol

2	29	
2	14	1
2	7	0
2	3	1
2	1	1
	0	1

$(29)_{10} = (11101)_2$

0.20×2
$= 0.40\times2$ — 0
$= 0.80\times2$ — 0
$= 1.60$ — 1
$= 0.60\times2$ — 1
$= 1.20$
:

$(0.20)_2 = (0011)_2$

$(29.20)_{10} \longrightarrow (11101.00110)_2$

0.20×2	=	0.40
0.40×2	=	0.80
0.80×2	=	1.60
0.60×2	=	1.20
0.20×2	=	0.40

② $(321.35)_{10} \longrightarrow (\quad)_8$

Sol

8	321	
8	40	→ 1
8	5	→ 0
	0	→ 5

$0.35 \times 8 = 2.80$
$0.80 \times 8 = 6.40$
$0.40 \times 8 = 3.20$
$0.20 \times 8 = 1.60$
$0.60 \times 8 = 4.80$
$0.80 \times 8 = 6.40$

$(0.35)_{10} = 263146$

$(321.35)_{10} \longleftrightarrow (501.263146)_8$

③ $(1250.25)_{10} \longleftrightarrow (\quad)_{16}$

Sol

16	1250	
16	78	2
16	4	14
	0	4

$(2E2)_{16}$

$0.25 \times 16 = 4.00$
$0.00 \times 16 = 0.00$

(4)

$(1250.25)_{10} \longleftrightarrow (2E2.40)$ //.

Quo. $(523.4)_6 \longleftrightarrow (\quad)_9$

$(\quad)_{10}$

Sol $(523.4)_6$

523

$\downarrow$

$5\times6^2 + 2\times6^1 + 3\times6^0 + \frac{4}{6} \rightarrow (195.66)_{10}$

$$\begin{array}{r|l}
9 & 195 \\ \hline
9 & 21 \rightarrow 6 \\
9 & 2 \rightarrow 3 \\
 & 0 \rightarrow 2
\end{array}$$

$0.66 \times 9 = 5.94$

$0.94 \times 9 = 8.46$

$0.46 \times 9 = 4.14$

$0.14 \times 9 = 1.26$

$0.26 \times 9 = 2.34$

$(523.4)_6$ —— $(236.5841)_9$

Que. The decimal equivalent of Binary number (10110.11) is ——

Sol $22 + \frac{2+1}{4} = (22.75)_{10}$

Que. $\sqrt{(224)_r} = (13)_r \quad r = ?$

$\Rightarrow \sqrt{2\times r^2 + 2\times r^1 + 4\times r^0} = 1\times r + 3$

$2r^2 + 2r + 4 = r^2 + 6r + 9$

$r^2 - 4r - 5 = 0$

$\frac{4 \pm \sqrt{16+20}}{2} \rightarrow \frac{4\pm6}{2} = 5$ ✓ & -1

(r cannot be negative)

Que. The number of one's present in binary Represtn of $15 \times 256 + 5 \times 16 + 3$ are $\underline{8}$

Sol $15 \times 16^2 + 5 \times 16^1 + 3 \times 16^0$

$(F\ 5\ 3)_{16} \longrightarrow 1111\ 101\ 011$

- **Hexadecimal & Octal to Binary:**

1) $(641.23)_8 \longrightarrow (\quad)_2$

6 4 1 . 2 3

110 100 001 010 011

$\Rightarrow (110100001.010011)_2$

II) $(C59.4)_{16} \longrightarrow (\quad)_2$

1100 0101 1001 . 0100

$(110001011001.0100)_2$

Que.

* **Binary to octal & Hexadecimal:**

1) $(1101.10101)_2 \longrightarrow (\quad)_8$

Sol 001 101 . 101 010 $\rightarrow (15.52)_8$

1101 . 1010 1000 $\longrightarrow (D.A8)_{16}$

* Octal addition

$$\begin{array}{r} \overset{1}{7}\,4\,\overset{1}{2}\cdot\overset{1}{5}\,3 \\ 5\,4\,3\cdot 2\,7 \\ \hline (1\,5\,0\,6\cdot 0\,2)_8 \end{array}$$

OR $10 - 8 = 2$

$$\begin{array}{c|l} 8 & 10 \\ \hline 8 & 1 \\ & 0 \end{array} \quad \begin{array}{l} \rightarrow 2 \\ \rightarrow 1 \end{array} \uparrow$$

Base 6 addition :

$$\begin{array}{r} \overset{1}{3}\,\overset{1}{4}\,\overset{1}{3}\cdot\overset{1}{2}\,5 \\ 5\,3\,2\cdot 3\,4 \\ \hline (1\,3\,2\,0\cdot 0\,3)_6 \end{array}$$

$$\begin{array}{c|l} 6 & 9 \\ \hline & 1 \quad 3 \end{array}$$

$$\begin{array}{c|l} & 8 \\ \hline & \end{array}$$

don't divide
Subtract by radix.

Que. $(135)_x + (144)_x = (323)_x$

Sol

$$\begin{array}{r} 1\,3\,5 \\ 1\,4\,4 \\ \hline \end{array}$$

note

$9 - x = 3$

$x = 6$ //.

Que. $24 + 14 = 21$

$8 - x = 1$

$x = 7$ //.

Que. $(2.3)_4 + (1.2)_4 = (y)_4$

Sol

$$\begin{array}{c|l} 3 & \\ 2 & \\ \hline 6 & \end{array} \quad \cancel{-4 = 2}$$

$$\begin{array}{r} \overset{1}{2}\cdot 3 \\ 1\cdot 2 \\ \hline 1\,0\cdot 1 \end{array}$$

$(10.1)_4$ //.

Que $(235)_{R_1} = (565)_{R_0} = (865)_{R_2}$

Sol $2 \times R_1^2 + 3 \times R_1 + 5 =$

$2R_1^2 + 3R_1 + 5 = 565$

$\cancel{-3 \pm \sqrt{9 - 40}}$

$\Rightarrow 2R_1^2 + 3R_1 - 560 = 0$

$\Rightarrow R_1 = \dfrac{-3 \pm \sqrt{9 + 560 \times 4 \times 2}}{4}$

$R_1 = 16$

Que. (R) $(43)_x = (y3)_8$ no. of possible solⁿ is

Sol $4x + 3 = 8y + 3$

$4x = 8y$

$\dfrac{x}{y} = 2$

$x = 2y$ $\qquad y = \cancel{1, 2}, 3$

$x = 9$

x	y
2	1
4	2
6	3
8	4
10	5
12	6
14	7
16	8

5 solⁿ

Scanned by CamScanner

Que. $(123)_5 = (x8)_y$

Sol $25 + 10 + 3 = xy + 8$

$xy = 30$

$y = \frac{30}{x}$

y	x
30	1
15	2
10	3
~~7~~	~~4~~
	~~5~~
~~5~~	~~6~~
~~6~~	~~5~~
~~1~~	~~30~~
~~2~~	~~15~~
~~3~~	~~10~~

∴ 3 possible Sol^n

$\boxed{\begin{array}{l} ①\ (x<y) \\ ②\ Y_{min} = 9 \end{array}}$

* **Representation of Signed binary Number**

- Sign Magnitude form
- Complement form
  - 1's Complement
  - 2's Complement

1) $-29 \longrightarrow$ Signbit Magnitude (29)

$\underbrace{1}_{\text{signbit}}\ \underbrace{11101}_{\text{magnitude bit}}$

This is Sign Magnitude form.

ii) -29 in 1's Complement $\Rightarrow$ $\underbrace{1}_{\text{Signbit}},\ \underbrace{00010}_{\text{1's comp of 29}}$

iii) -29 in 2's Complement $\Rightarrow$

$$\begin{array}{r} 1\,|\,00010 \\ +1 \\ \hline 1\,|\,00011 \end{array} = 100011$$

- Self Complementing Code is a Code in which we can obtain Codeword for 9's Complement of N by from the Code of N by Complementing each bit in Code of N

- 2421 is a Self Complementing Code. Any Code which has repeated weight (2 in this Case) are Self Complementing.

- Self Complementing property must hold to write Codewords. Hence there are many Sequence of 2421 BCD are possible

* Gray Code

Distance

Distance	Gray Code	
	0 0 0 0	
1	0 0 0 1	Mirror
1	0 0 1 1	
1	0 0 1 0	Mirror
1	0 1 1 0	
1	0 1 1 1	
1	0 1 0 1	
1	0 1 0 0	Mirror
1	1 1 0 0	
1	1 1 0 1	
1	1 1 1 1	
1	1 1 1 0	
1	1 0 1 0	
1	1 0 1 1	
1	1 0 0 1	
1	1 0 0 0	

1

- Gray code is non weighted code.
- Gray Code is also called reflective code
- Gray code is not a BCD code because Gray code can be of 2 bit, 3 bit 4 bit &bit but BCD is only 4 bit.

note:- Gray Code are Unit distance Code

Distance between Code → difference in no. of bit

- Gray Code is also called Cyclic Code

Unit-2 Combinational Circuit

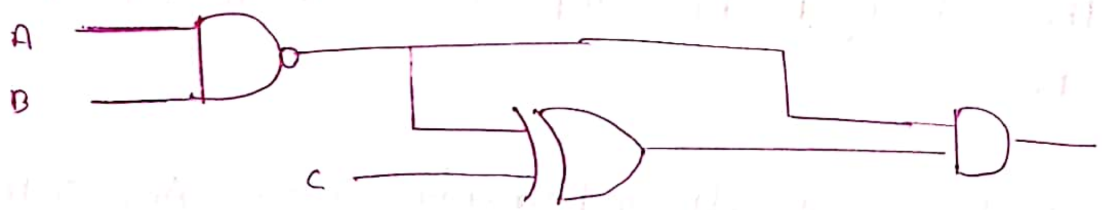
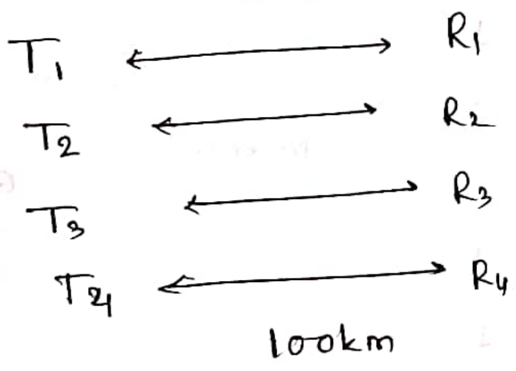


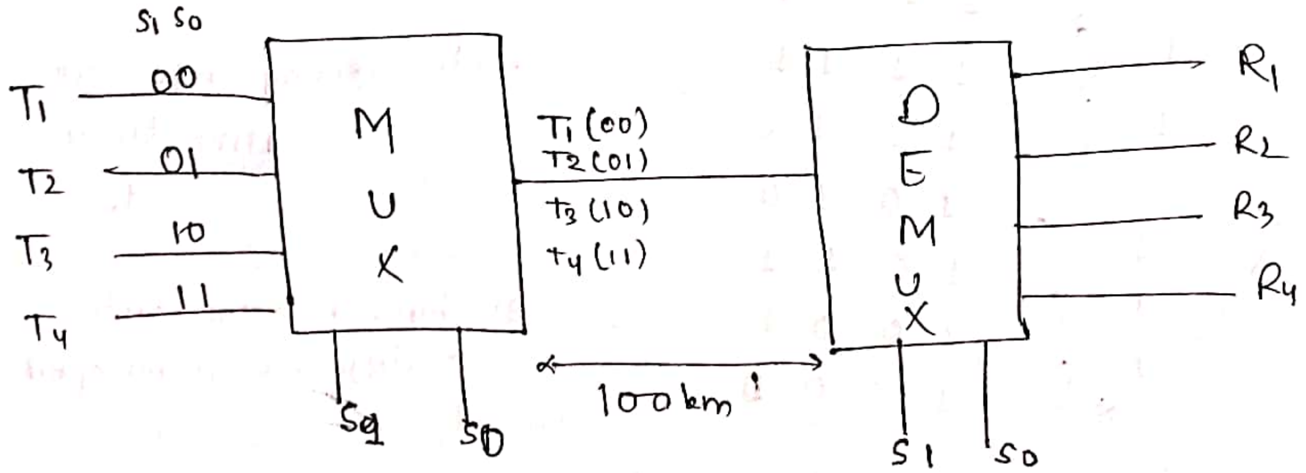
fig. Combinational ckt

· Combinational Ckt is a Circuit made up of Combination of Logic gate. In Combinational ckt the o/p at any time depend on present i/p

* Multiplexer



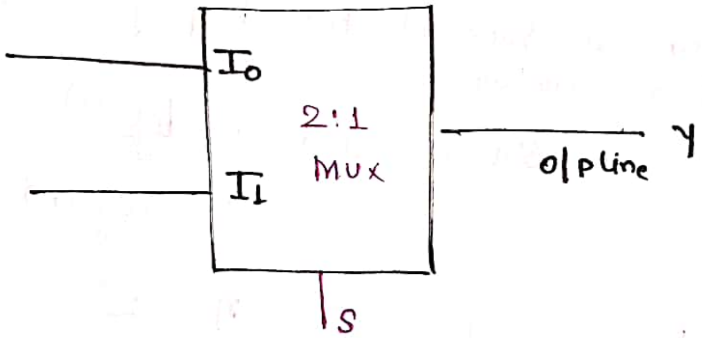
Total Cable required for 1 to 1 X mission = 400km

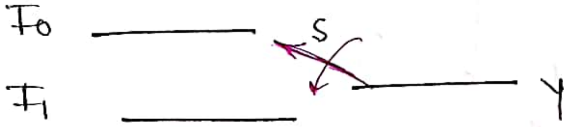


Only 100km Cable Req.

1) 2x1 Mux (2:1 Mux)

2 line to 1 line Mux





S	Y
0	I_0
1	I_1

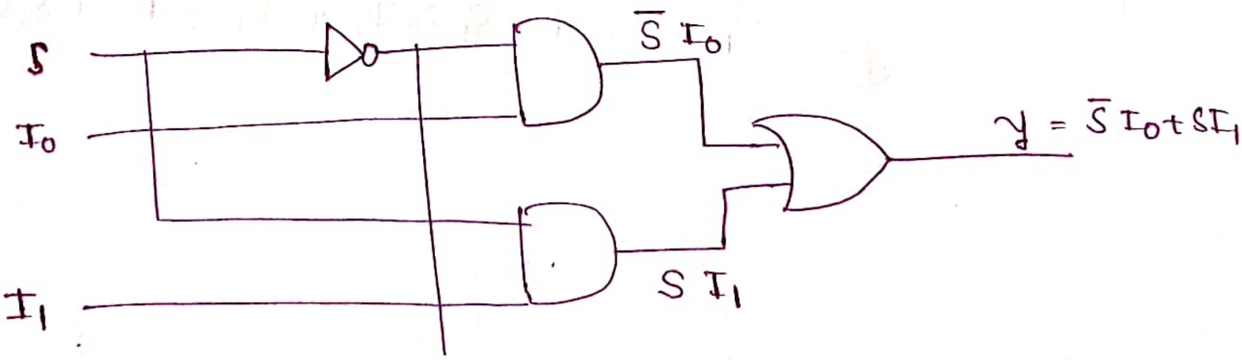
$$Y = \bar{S} I_0 + S I_1$$

Check :- $S = 0$

$$Y = 1 \cdot I_0 + 0 I_1$$
$$Y = I_0$$

$S = 1$

$$Y = 0 I_0 + 1 I_1$$
$$= I_1$$



logic ckt of 2:1 Mux

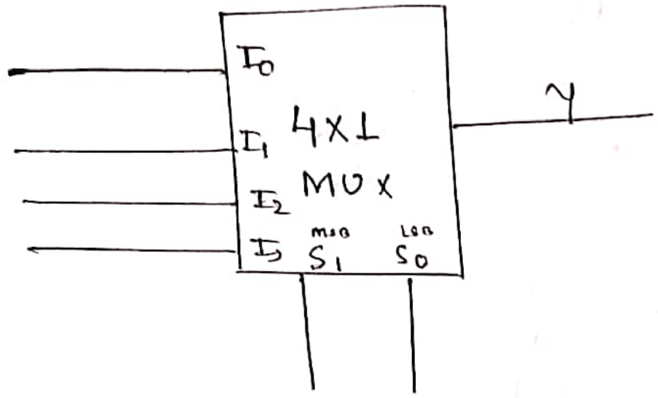
Multiplexer :- It is a Combinational ckt which accepts data through multiple i/p line and passes o/p through Single output line. The Routing of Multiple i/p data into Single o/p line is done with the help of extra i/p line called as Selection line.

Selection line $s = \log_2(n)$: n no of i/p

$s = \log_2(n)$

$n = 2^s$

4 X 1 MUX



Table

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

Equation :-

$$y = \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3$$

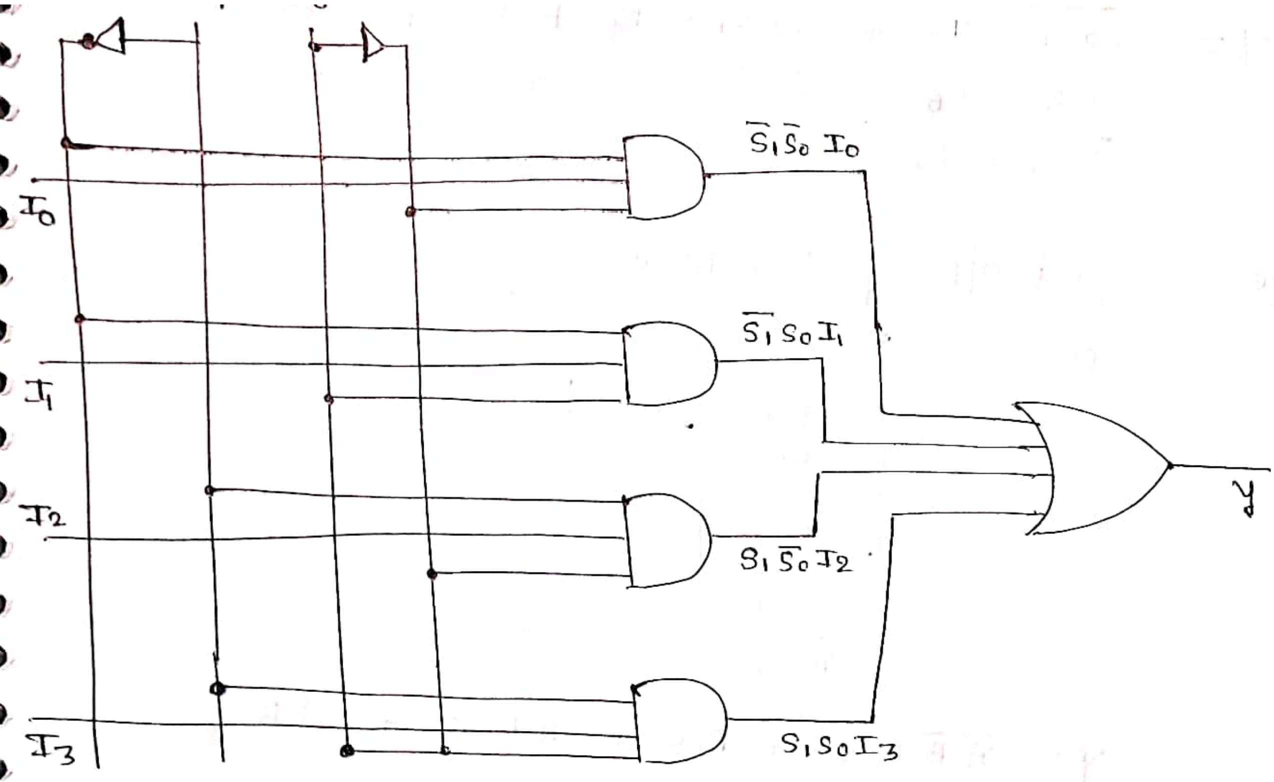
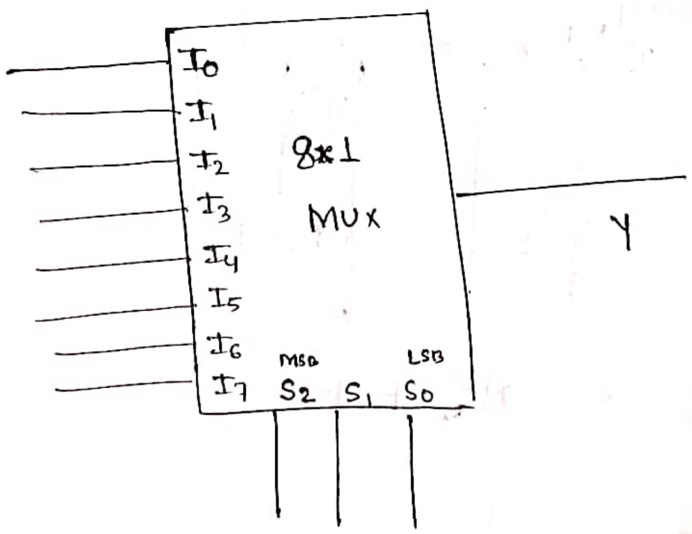


fig. 4x1 MUX logic diagram

8x1 MUX



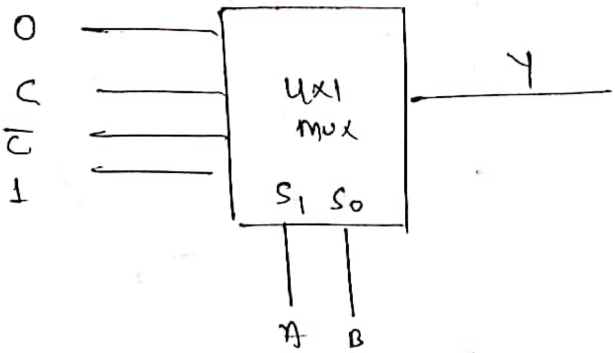
S_0 always LSB

Table

S_2	S_1	S_0	Y
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

$$Y = \overline{S_2 S_1 S_0}\, I_0 + \bar{S}_2 \bar{S}_1 S_0 I_1 + \bar{S}_2 S_1 \bar{S}_0 I_2 +$$
$$S_2 S_1 \bar{S}_0 I_6 + S_2 \bar{S}_1 \bar{S}_0 I_4 + S_2 \bar{S}_1 S_0 I_5 +$$
$$\bar{S}_2 S_1 S_0 I_3 + S_2 S_1 S_0 I_7$$

Que. find o/p of given MUX



$$Y = \bar{A}\bar{B}0 + \bar{A}BC + A\bar{B}\bar{C} + AB$$
$$Y = AB + \bar{A}BC + A\bar{B}\bar{C}$$

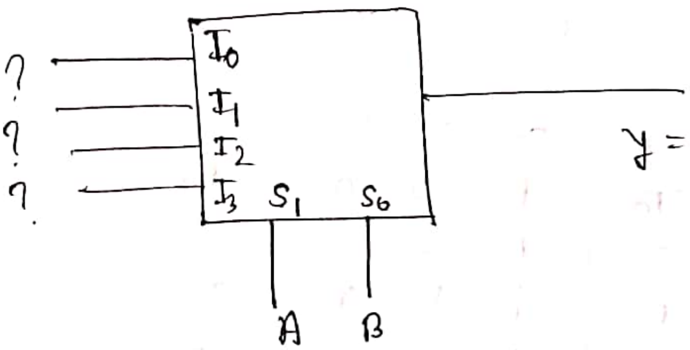
In std SOP $Y_{ssop} = AB\bar{C} + ABC + \bar{A}BC + A\bar{B}\bar{C}$

Y_{minsop} :-

A \ BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
			1	
	1		1	1

$$Y = A\bar{C} + BC$$

Que.



$y = BC + A\bar{C}$

Sol) $\bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3 = BC + A\bar{C}$

$\bar{A}\bar{B} I_0 + \bar{A} B I_1 + A \bar{B} I_2 + A B I_3 = BC + A\bar{C}$ ——— (1)

$Y = BC + A\bar{C}$

$Y = ABC + \bar{A}BC + AB\bar{C} + A\bar{B}\bar{C}$

$Y = ABC + AB\bar{C} + \bar{A}BC + A\bar{B}\bar{C} + \bar{A}\bar{B}\cdot 0$

$Y = AB1 + \bar{A}BC + A\bar{B}\bar{C} + \bar{A}\bar{B}\cdot 0$ ——— (2)

Compare eq (1) & (2)

$I_3 = 1$

$I_2 = \bar{C}$

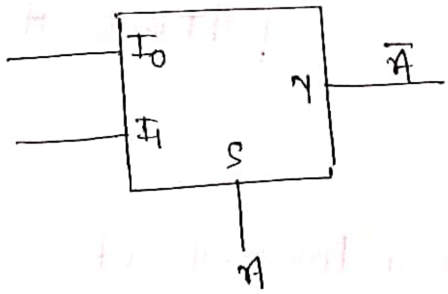
$I_0 = 0$

$I_1 = C$

obtaining o/p is called designing
getting o/p is called Analysis

Que. Design following function using 2:1 MUX

(1) NOT $Y = \bar{A}$



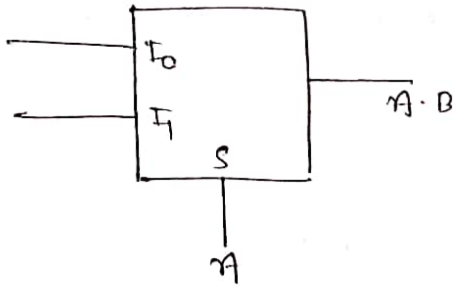
$Y = \bar{S} I_0 + S I_1$

$Y = \bar{A} I_0 + A I_1$

$I_0 = 1$, $I_1 = 0$

$Y = \bar{A}$ //

2. AND $Y = A \cdot B$



$Y = \bar{S} I_0 + S I_1$

$Y = \bar{A} I_0 + A I_1$

$Y = AB + \bar{A} \cdot 0$

$Y = AB$

$I_1 = B$

$I_0 = 0$ //.

3. OR $Y = A+B$

$Y = I_0 \bar{A} + I_1 A$

$Y = A + B(A+\bar{A})$

$= A + AB + \bar{A} B$

$= A(1+B) + \bar{A} B$

$= A \cdot 1 + \bar{A} B$

~~$Y = I_0 \bar{A} + I_1 A + A \cdot 0$~~

~~$I_0 = I_1 = B$~~

$Y = I_0 \bar{A} + I_1 A$

$\boxed{A+B = A + \bar{A} B}$

on Comp.

$I_0 = B \quad I_1 = 1$

note:- 2to1 MUX is also a Universal ckt

4) NOR gate

$$y = \overline{A+B}$$

$$y = \bar{A} \cdot \bar{B} \qquad \text{Take } S = A$$

$$y = \bar{S} \cdot I_0 + S I_1$$

$$y = \bar{A} I_0 + A I_1$$

$$y = \bar{A}\bar{B} + A \cdot 0$$

on Comp. $\bar{B} = I_0$, $I_1 = 0$ //

5) $$y = \overline{A \cdot B}$$

$$y = \bar{A} + \bar{B}$$

$$= \bar{A} \cdot 1 + \bar{A}\bar{B} + A\bar{B}$$

$$= \bar{A}(1 + \bar{B}) + A\bar{B}$$

$$= \bar{A} \cdot 1 + A\bar{B}$$

OR

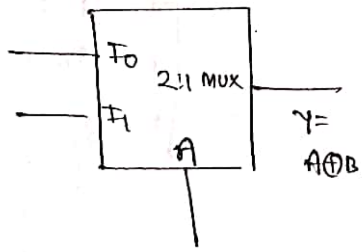
$$y = \bar{A} + \bar{B}$$

$$= \bar{A} + A\bar{B}$$

$I_0 = 1 \qquad I_1 = \bar{B}$

6) $$y = A \oplus B = \bar{A}B + A\bar{B}$$

$I_0 = B \qquad I_1 = \bar{B}$



7) $$y = A \odot B = \bar{A}\bar{B} + AB$$

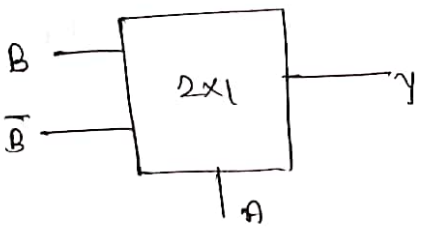
$I_0 = \bar{B} \qquad I_1 = B$

Scanned by CamScanner

Que 1 What are the Minimum number of 2:1 MUX required to generate a two i/p AND gate and a two Input EXOR gate

Sol for two i/p AND gate
Only 1 2X1 MUX Req

for two i/p EXOR gate = 2 2X1 MUX



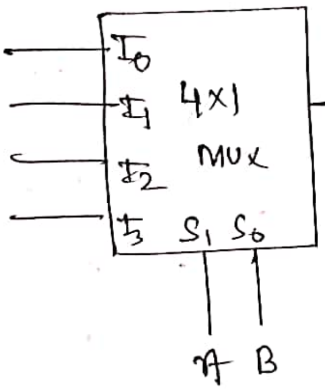
one more for $\bar{B}$

Ans. 1 & 2 ||.

Que. Design using 4X1 MUX

1) $Y = A \oplus B$

$Y = \bar{A}B + A\bar{B}$



$Y = \bar{S_1}\bar{S_0} I_0 + \bar{S_1} S_0 I_1 + S_1 \bar{S_0} I_2 + S_1 S_0 I_3$

$= \bar{A}\bar{B} I_0 + \underline{\bar{A} B I_1 + A\bar{B} I_2} + AB I_3$

On Compar.

$I_0 = 0$

$I_3 = 0$

$I_1 = 1$

$I_2 = 1$

II) $y = \overline{A \cdot B}$

Std. eqⁿ $Y = \bar{A}\bar{B} I_0 + \bar{A} B I_1 + A \bar{B} I_2 + A B I_3$

$y = \bar{A} + \bar{B}$

$= \bar{A} B + \bar{A}\bar{B} + \bar{A}\bar{B} + A\bar{B}$

$= \bar{A}\bar{B} + \bar{A} B + A\bar{B} + AB \cdot 0$

On Comp.

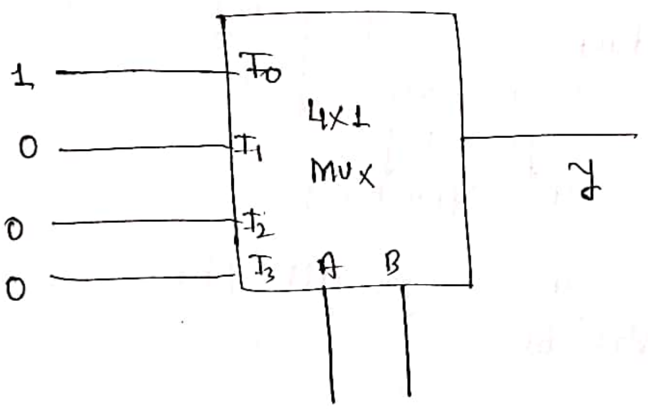
$I_0 = 1$

$I_1 = 1$

$I_2 = 1$

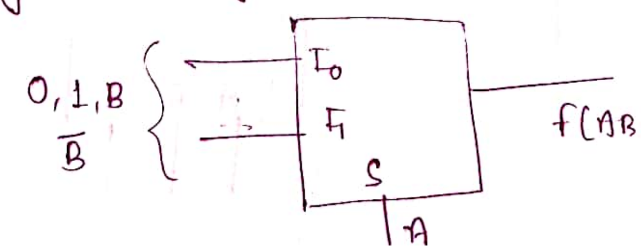
$I_3 = 0$ //

III) $y = \overline{A + B}$



Imp pts.

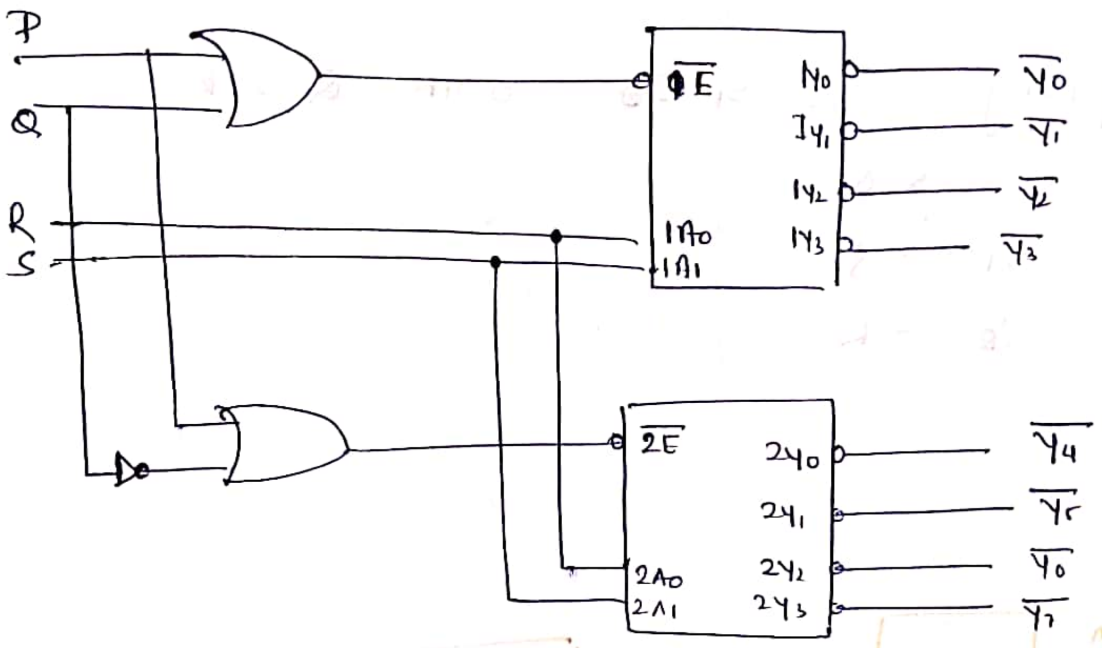
1. With a 2x1 MUX, we can design some but not all functions of 2 variable

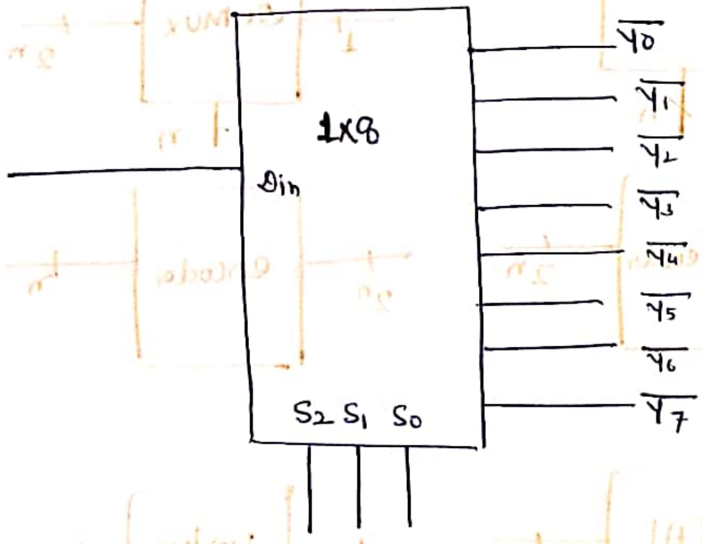


necessarily in this order. The respective Input Connection to P Q R & S terminal should be

A) S_2 D_{in} S_0 S_1 B) S_1 D_{in} S_0 S_2

c) D_{in} S_0 S_1 S_2 d) D_{in} S_2 S_0 S_1





Sol: $P = 0$ fixed (to make device on)

as $P = 0$ and o/p is active low

hence '0' will propagate from $\overline{Y_0}$ to $\overline{Y_7}$

$P = D_{in}$

Scanned by CamScanner

given $A_1 \longrightarrow S$

$A_0 \longrightarrow R$

for $Q = 0$ $\quad \overline{Y_0}$ to $\overline{Y_3}$ activalid

for $Q = 1$ $\quad \overline{Y_4}$ to $\overline{Y_7}$ activated

Hence Comparing $S_2 \ S_1 \ S_0$ with $Q \ S \ R$

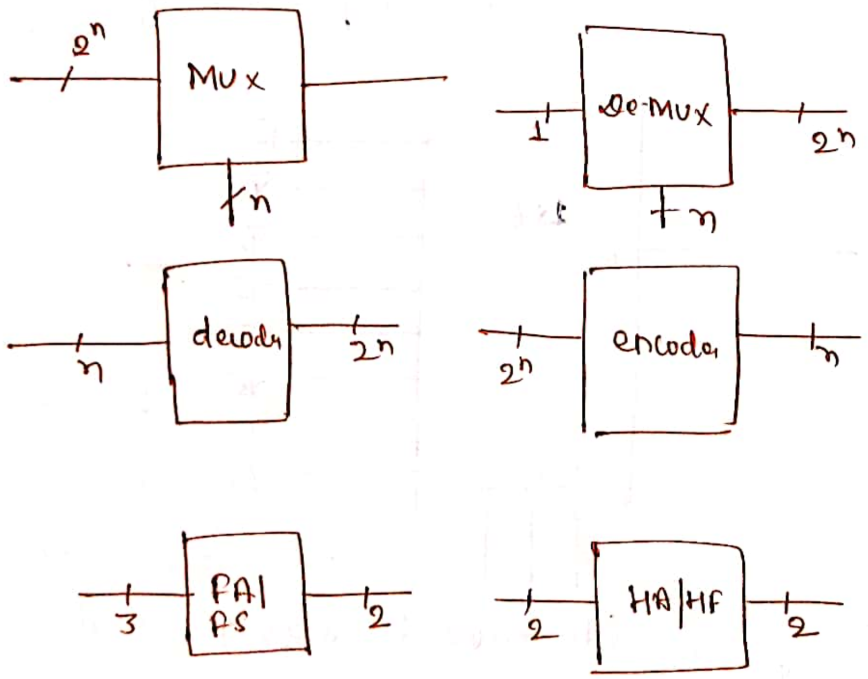
$S_2 \longrightarrow Q$

$S_1 \longrightarrow S$

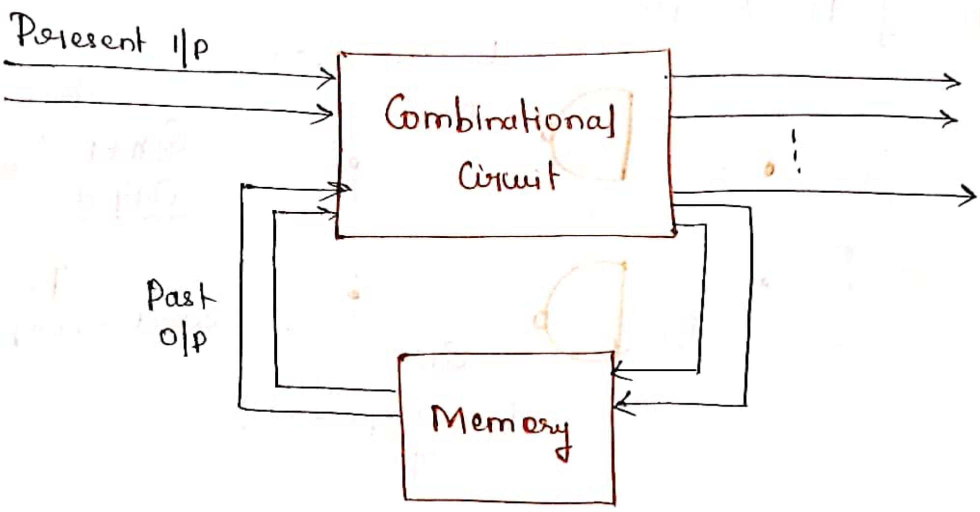
$S_0 \longrightarrow R$

Option D

Note:



Unit-3 Sequential Circuits



1. In Combinational ckt, o/p at any time depends only on the present inputs. where as in Sequential Circuit the o/p at any time depends on present input as well as past output.

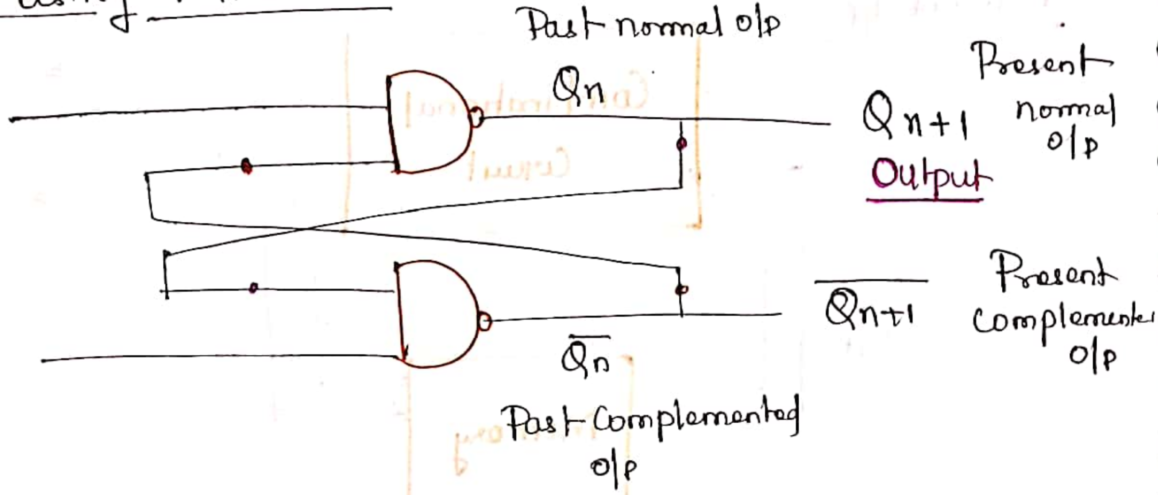
2. As the o/p of Sequential ckt also depend on past o/p, there is a requirement of Memory element which is Connected in the feed back path. Where as in Combinational ckt there is no requirement of Memory element or feedback path.

3. Due to the feedback path, Sequential ckt may be reffered as closed System where as Combinational ckt is reffered as open System.

4. The Memory element used in digital Sequential ckt are –
   i) latch
   ii) Flip flop

* Latch (Cross Coupled Gates)

* Latch using NAND Gate



Output states of a latch / flipflop

① SET state

- Latch / ff is said to be in SET state if present normal o/p or main output is at logic HIGH

i.e $Q_{n+1} = $ '1'

& $\overline{Q_{n+1}} = $ '0'

② RESET state

- latch / ff is said to be in RESET state if present normal o/p is at logic Low

i.e $Q_{n+1} = $ '0'

$\overline{Q_{n+1}} = $ '1'

III. HOLD state

latch | ff is said to be in hold state if the present o/p is same as the past o/p. i/e

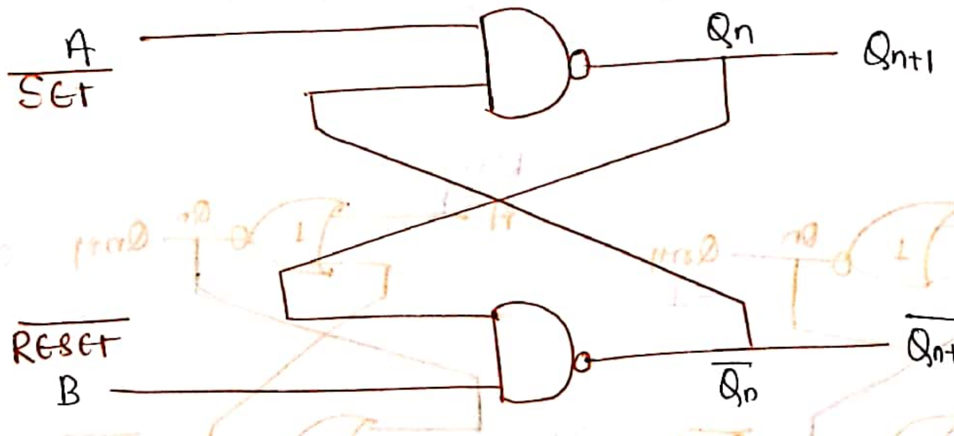
$$Q_{n+1} = Q_n$$
&
$$\overline{Q_{n+1}} = \overline{Q_n}$$

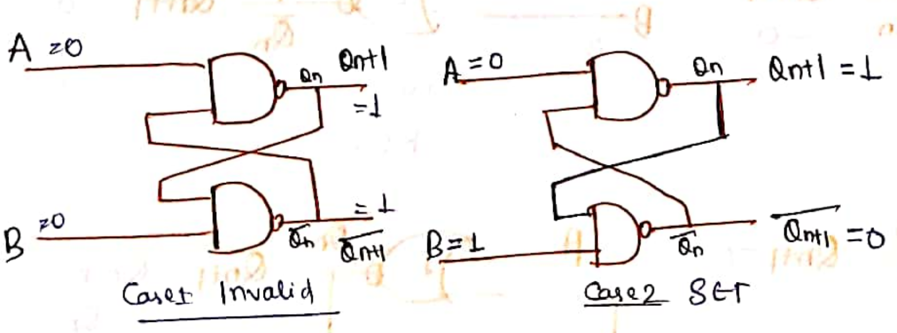
IV Invalid state

latch | ff is said to be in Invalid state if normal o/p is equal to complemented o/p.

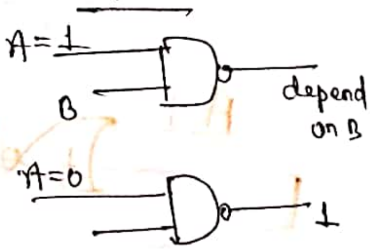
i,e $Q_{n+1} = \overline{Q_{n+1}}$

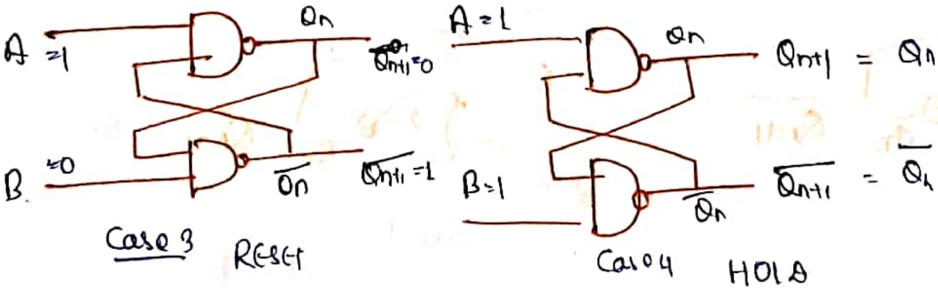
* SR Latch Using NAND gate :-





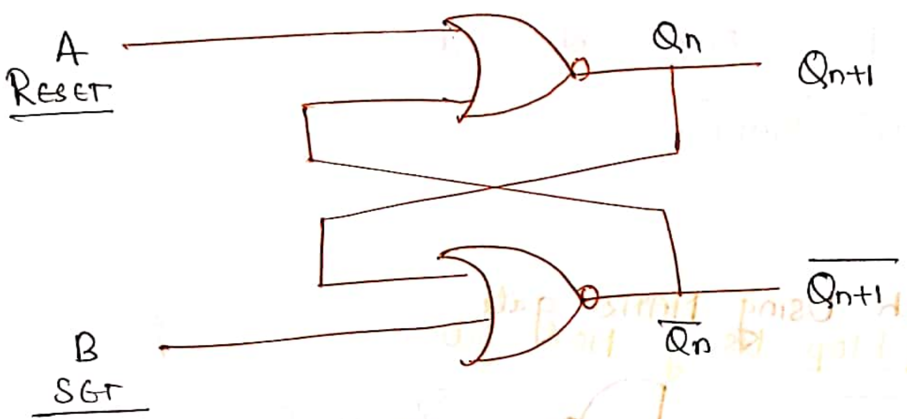
note

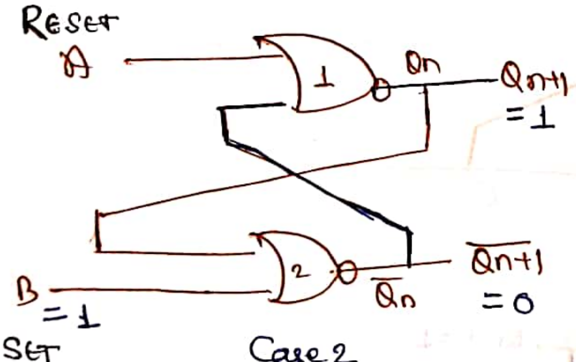




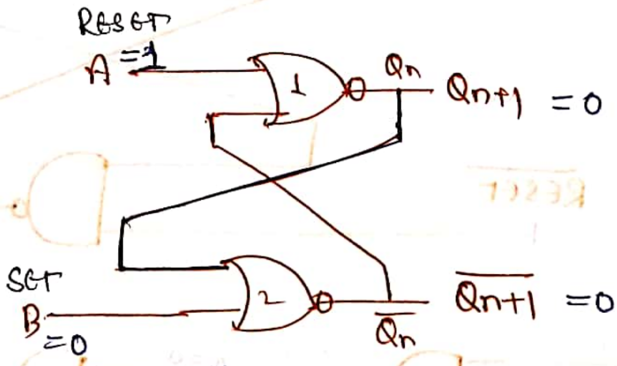
A	B	Q_{n+1}	~~State~~ $\overline{Q_{n+1}}$	State
0	0	1	1	INVALID
0	1	1	0	SET
1	0	0	1	RESET
1	1	Q_n	$\overline{Q_n}$	HOLD

* SR Latch using NOR gate

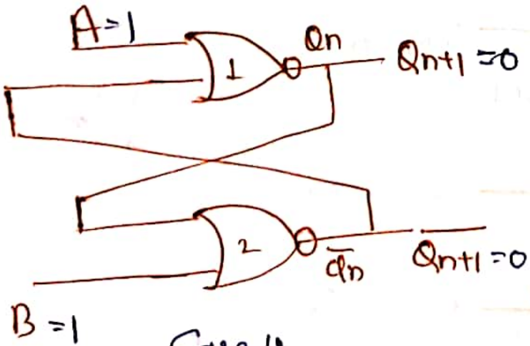




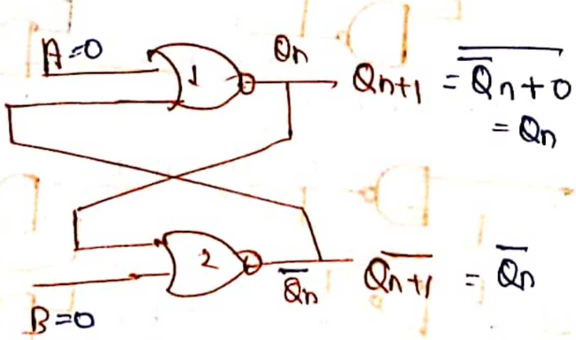
Case 2
SET



Case = 3
RESET



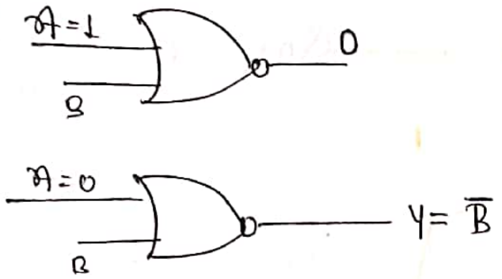
Case 4
Invalid



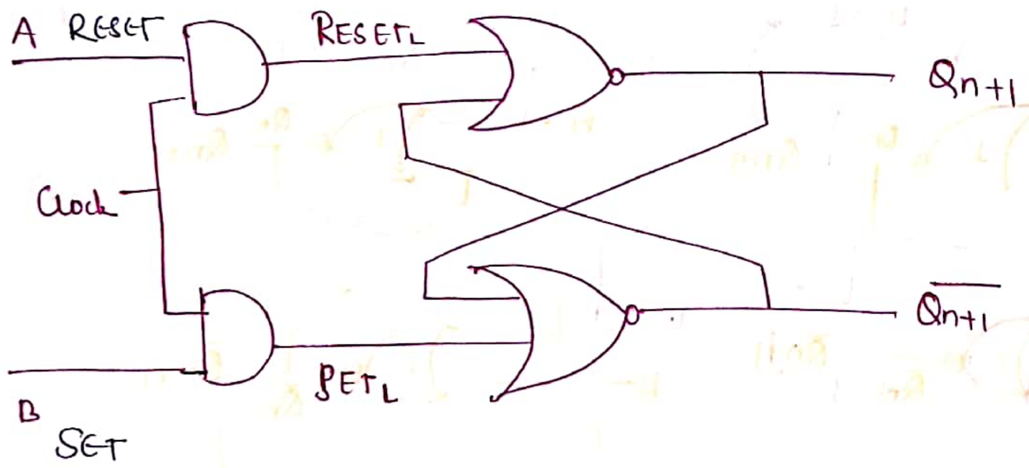
Case 1
Hold

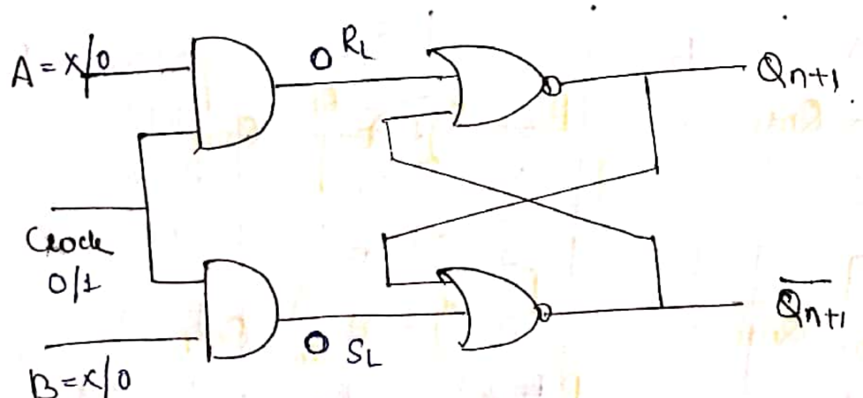
A	B	Q_{n+1}	$\overline{Q_{n+1}}$	State
0	0	Q_n	$\overline{Q_n}$	HOLD
0	1	1	0	SET
1	0	0	1	RESET
1	1	0	0	INVALID

note:

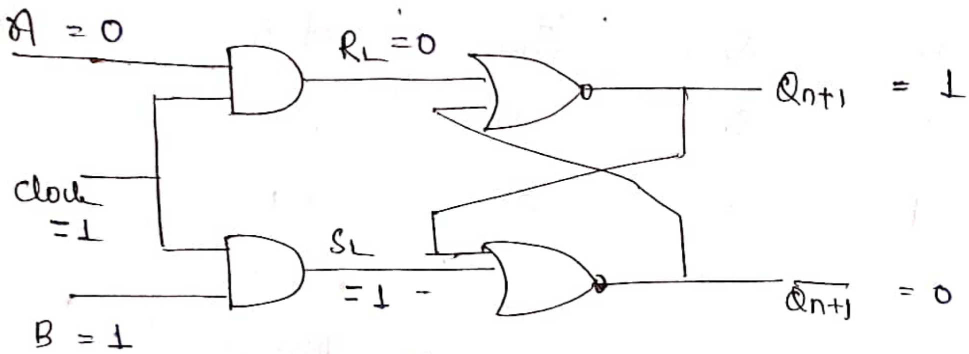


* SR FlipFlop Using NOR gate

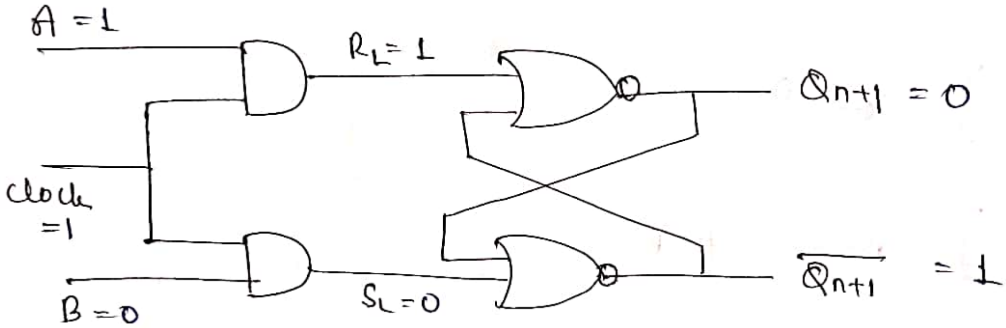




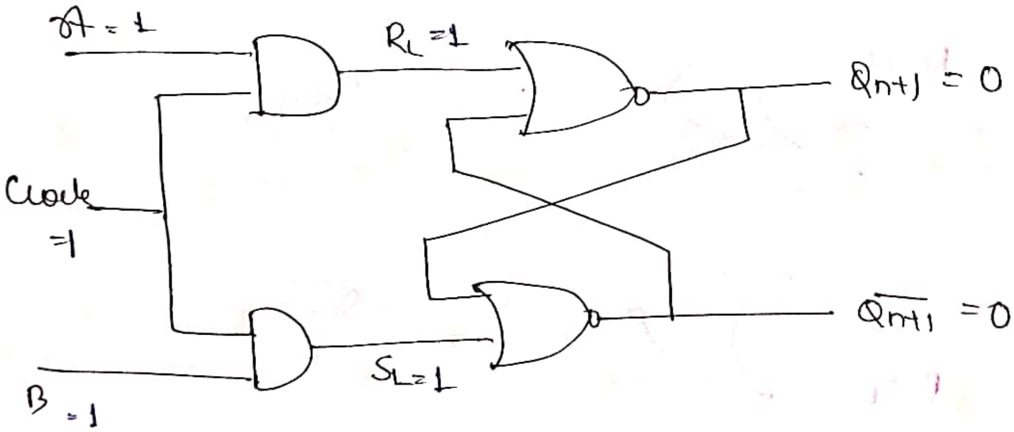
Case 1 & 2



Case3



Case4

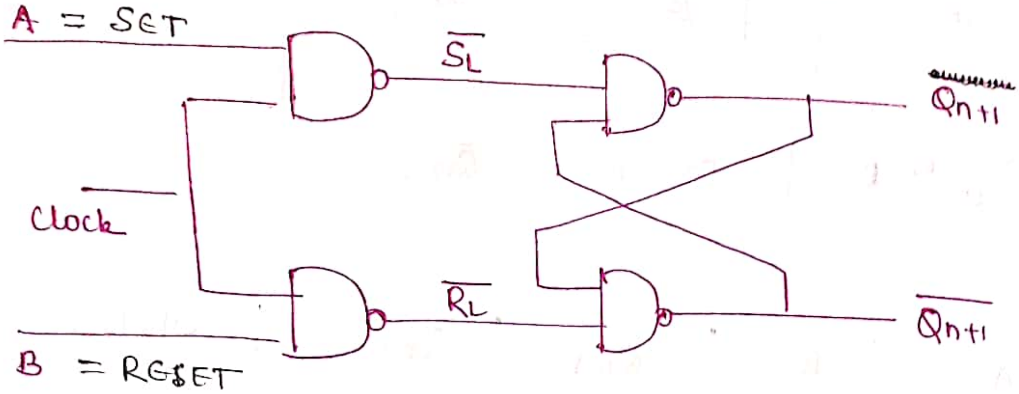


Table

Clock	A	B	Q_{n+1}	$\overline{Q_{n+1}}$	State
0	X	X	Q_n	$\overline{Q_n}$	HOLD
1	0	0	Q_n	$\overline{Q_n}$	HOLD
1	0	1	1	0	SET
1	1	0	0	1	RESET
1	1	1	~~In Valid~~ 0	0	Invalid

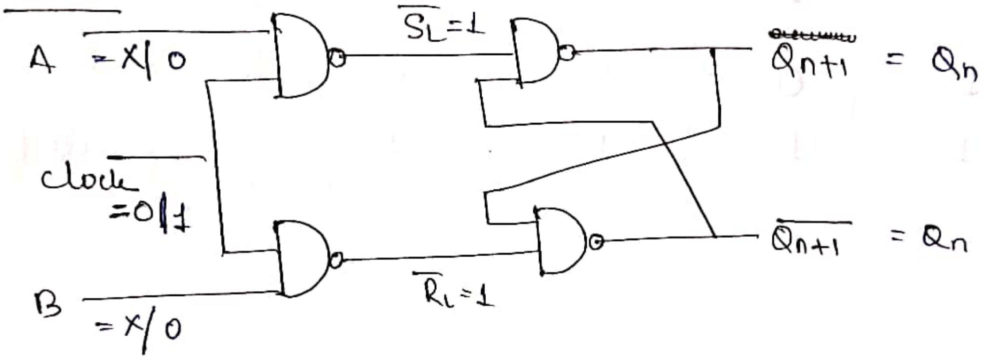
∴ B = SET A = RESET

* SR Flipflop using NAND gate

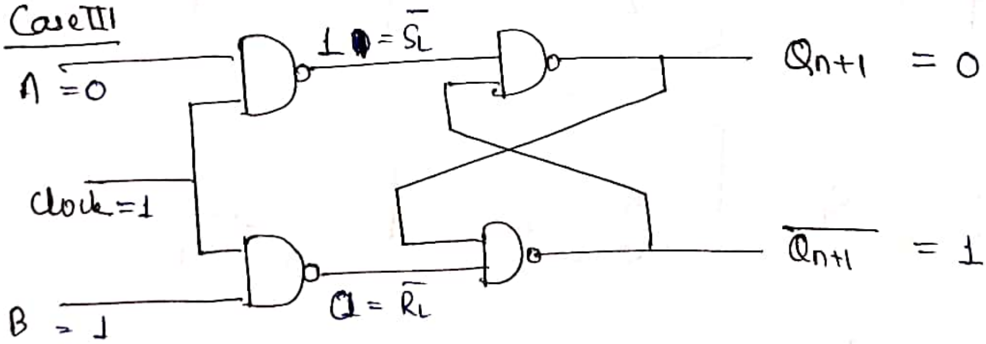


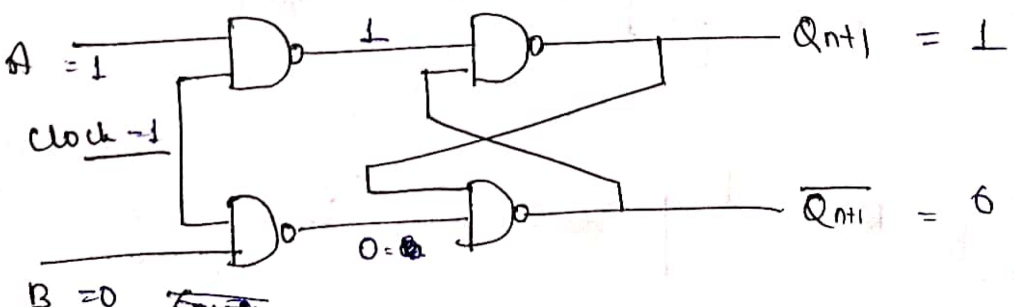
Working

Case I



Case III





~~Case IV~~

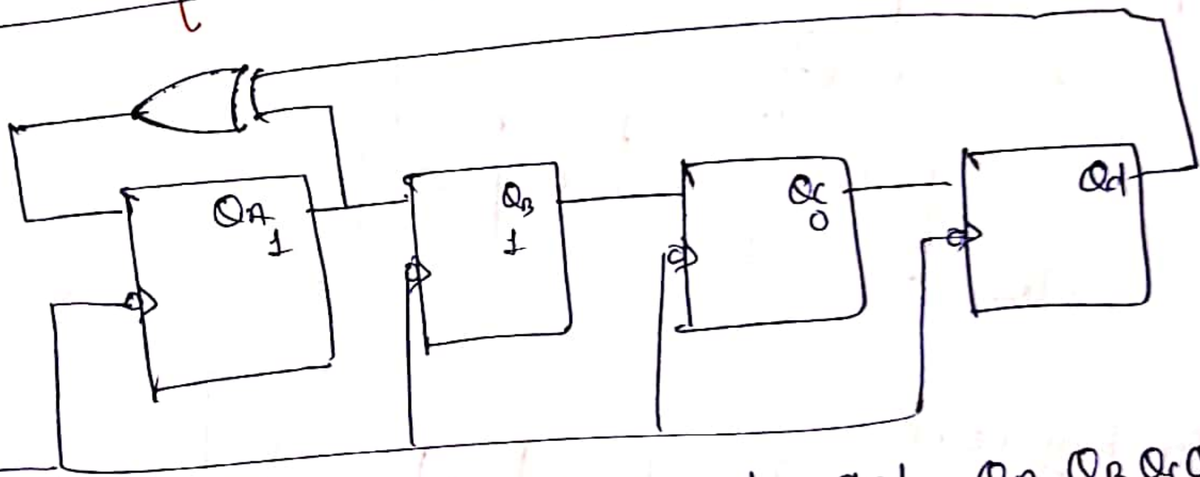
Case IV

4 bit Ring ⇒ Mod 4 Counter
n bit Ring ⇒ Mod n Counter

4 bit Johnson ⇒ Mod 8
n bit Johnson ⇒ Mod 2n

	Ring	Johnson
used state	n	$2n$
unused state	$2^n - n$	$2^n - 2n$

Que.



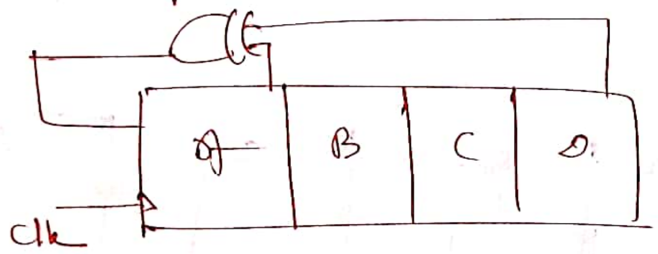
How many clock pulse Req. to get QA QB QC Qd = 1111

Sol

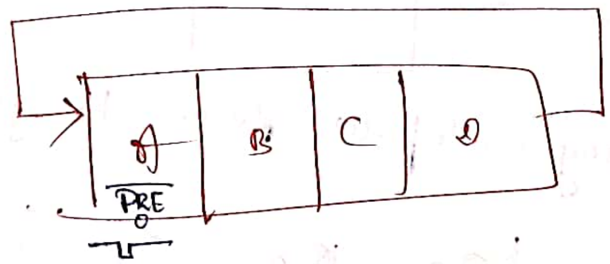
CP	QA	QB	QC	QD	CP
0	1	1	0	1	1
1	0	1	1	0	2
2	0	0	1	1	3
3	1	0	0	1	4
4	0	1	0	0	5

CP	Q_A	Q_B	Q_C	Q_D	CP
4	0	0	0	0	5
5	0	0	0	1	6
6	1	0	0	0	7
7	1	1	0	0	8
8	1	1	1	0	9
9	1	1	1	1	10
					Clk

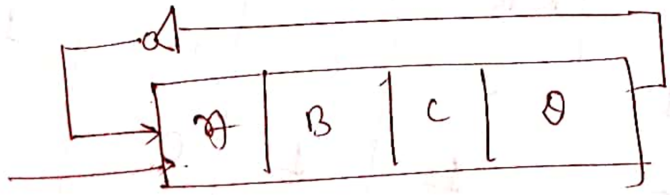
equivalent Representation



for Ring Counter



Johnson



Q99. 10

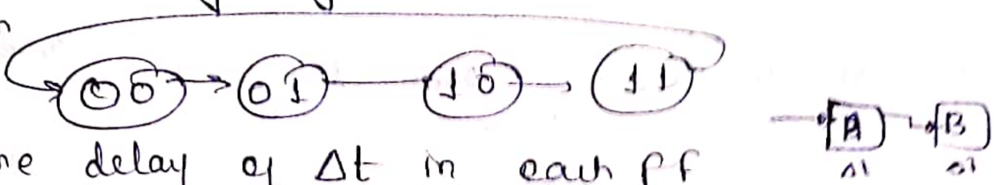
Q114.

	A	B	C	D		A_{n+1}	$B_{n+1} = A$	$C_{n+1} = B$	$D_{n+1} = C$
0	1	0	1	0		$B \oplus D$			
1	1	1	0	1	1				
2	0	1	1	0	2				
3	0	0	1	1	3				
4	0	0	0	1	4				
5	1	0	0	0	5				
6	0	1	0	0	6				
7	1	0	1	0	7				

Shift Reg. Questⁿ Can also be Solved by synchronous Counter approach. (Shift Reg. is Sync. Counter)

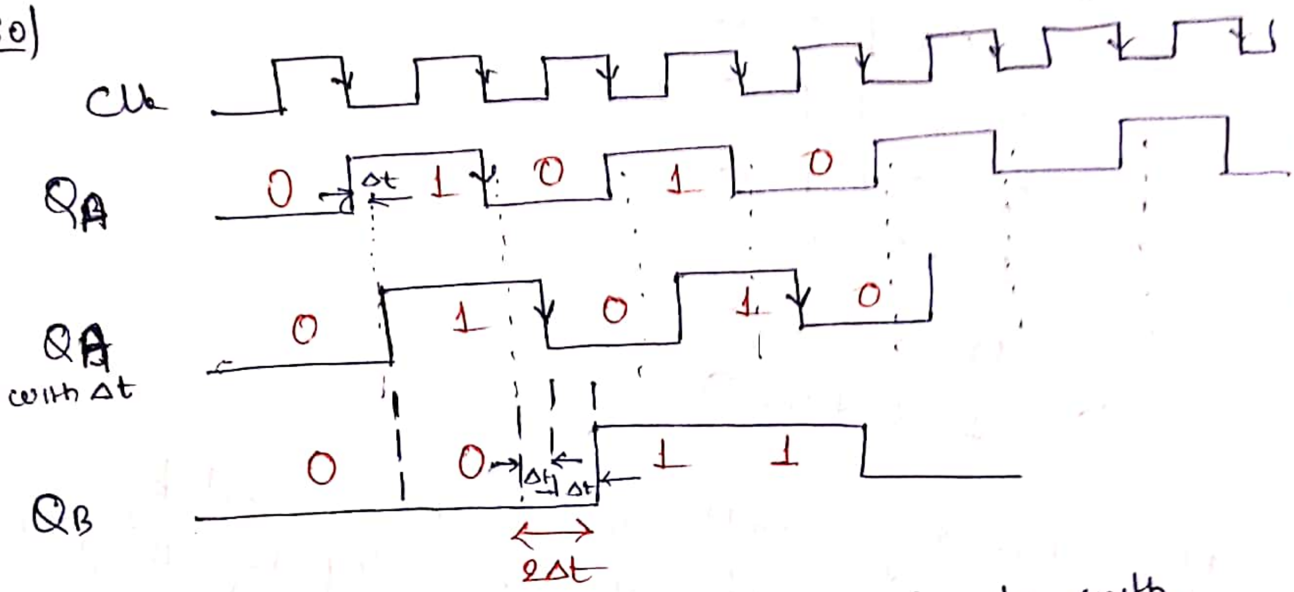
PS				FF Input				NS			
Q_A	Q_B	Q_C	Q_d	$D_A = Q_A \oplus Q_d$	$D_B = Q_A$	$D_C = Q_B$	$Q_d = Q_C$	Q_{A+1}	Q_{B+1}	Q_{C+1}	Q_{d+1}

Que1 Draw waveform for a Async. Counter with state diagram

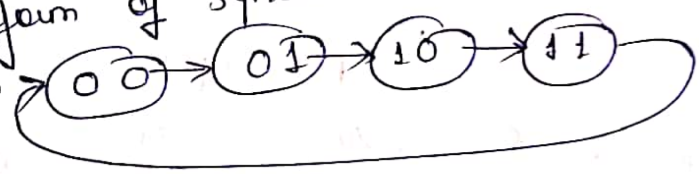


Assume delay of Δt in each FF

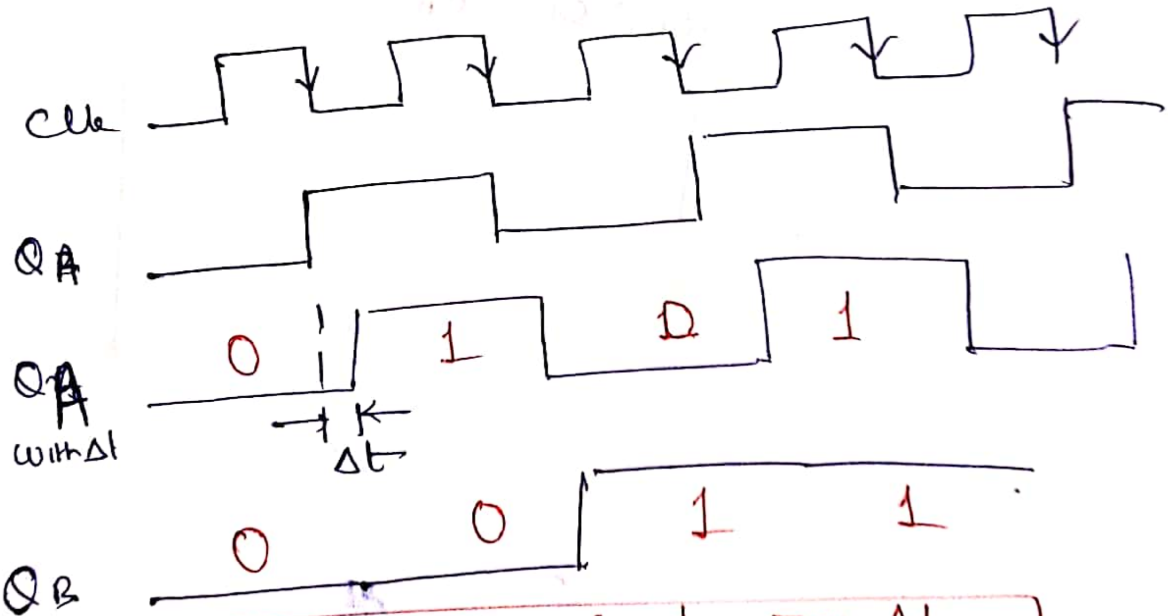
Sol



Que2 Draw waveform of Synchronous Counter with state diagram



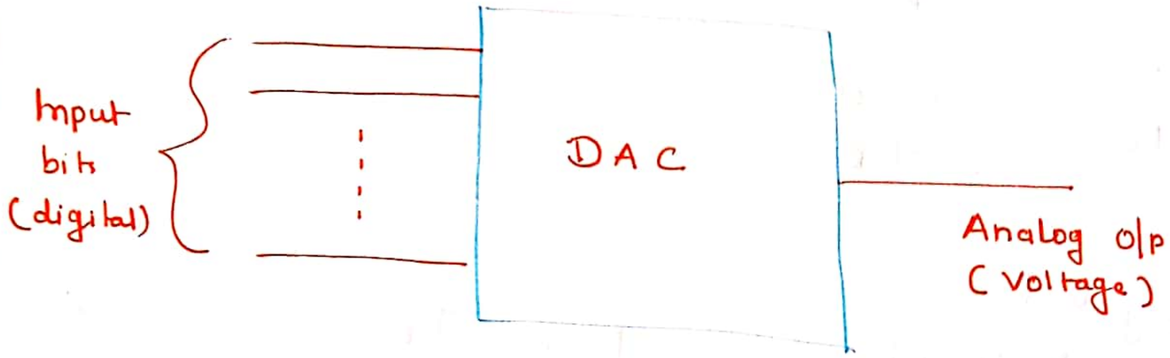
Sol



Conclusion → Delay of Async. Counter $= n\,\Delta t$
where n = no of f/f in Async. Counter, and Δt is delay in each f/f.
Delay of Sync. Counter (n FF) $= \Delta t$

Ripple Counter ⟶ Async. Counter

Unit-4 ADC & DAC



Analog output (Voltage) $\propto$ Digital Inputs (bits)

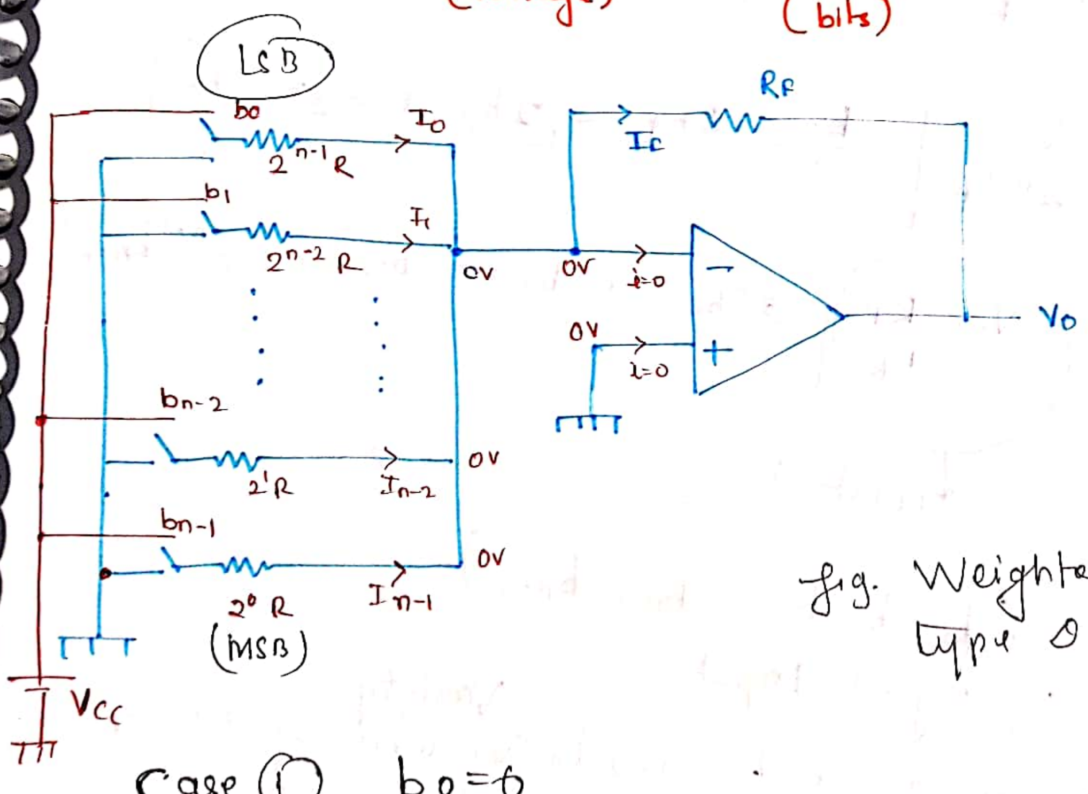


fig. Weighted Resistor type DAC

Case (1) $b_0 = 0$

Ohm's Law at $2^{n-1}R$

$$\frac{0-0}{2^{n-1}R} = I_0$$

Scanned by CamScanner

Case 2 $b_0 = 1$

Ohm's Law at $2^{n-1}R$

$$\frac{V_{cc} - 0}{2^{n-1}R} = I_0$$

$\therefore$

$$I_0 = \frac{b_0 V_{cc} - 0}{2^{n-1}R}$$

Apply kcl

$$I_0 + I_1 + I_2 \cdots I_{n-1} = I_f$$

$$\frac{b_0 V_{cc}}{2^{n-1}R} + \frac{b_1 V_{cc}}{2^{n-2}R} + \cdots \frac{b_{n-1}}{2^0 R} V_{cc} = \frac{-V_0}{R_f}$$

$$\Rightarrow -\frac{V_0}{R_f} = \frac{V_{cc}}{2^{n-1}R}\left[\frac{b_0}{1} + 2b_1 + 2^2 b_2 + \cdots 2^{n-1} b_{n-1}\right]$$

$$\Rightarrow V_0 = \frac{-V_{cc} R_f}{2^{n-1}R}\left[2^0 b_0 + 2^1 b_1 + 2^2 b_2 + \cdots 2^{n-1} b_{n-1}\right]$$

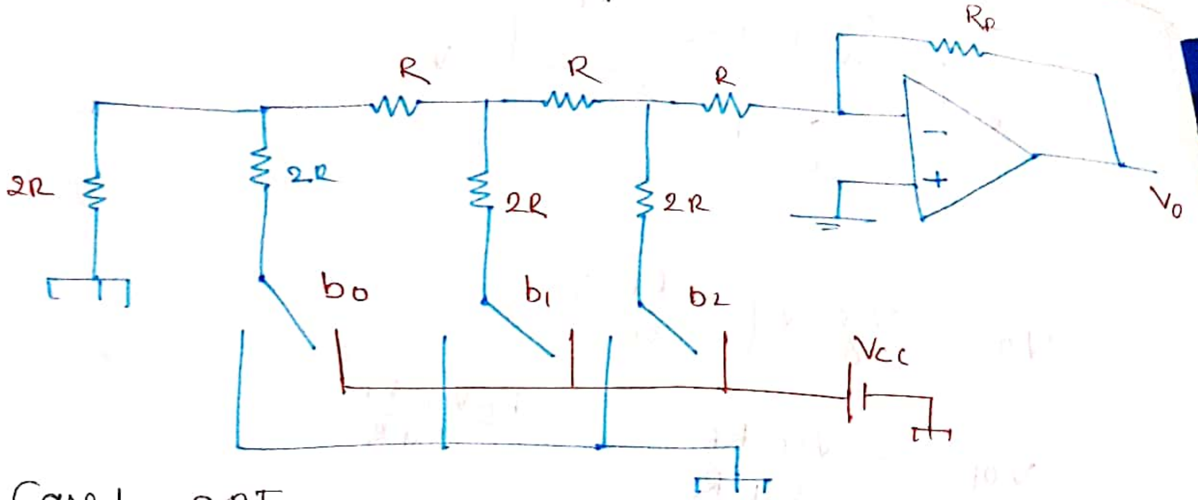
Constant

$$V_0 \propto (b_0, b_1, b_2 \cdots b_{n-2}\ b_{n-1})$$

Output $\propto$ Digital Input

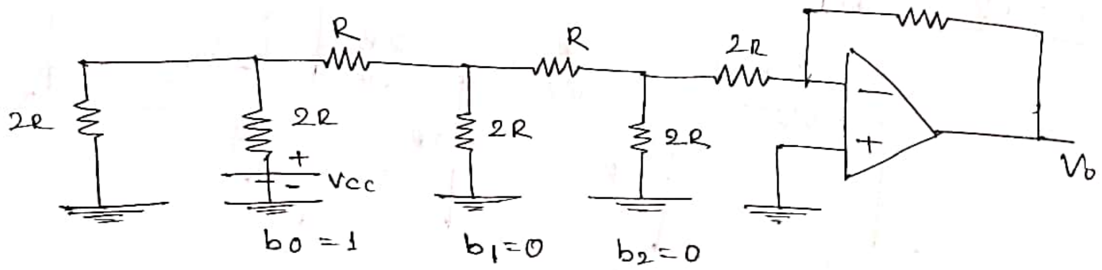
1) Design is Simple but wide Variety of Results are Req (~~...~~ Disadvantage) ~~Wide Variety of Resistance are required.~~

② R-2R ladder type DAC



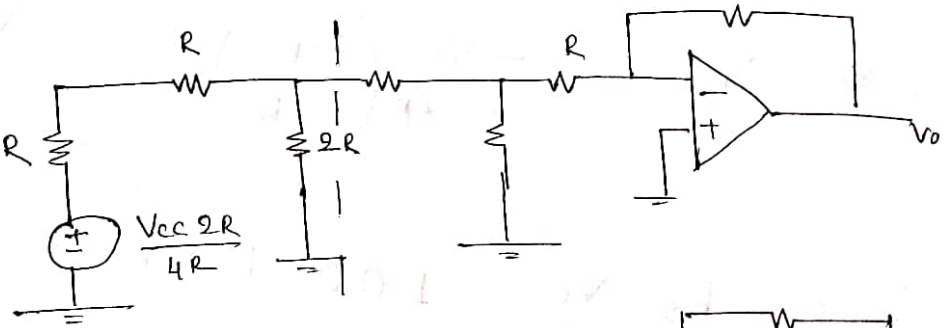
Case I SPT

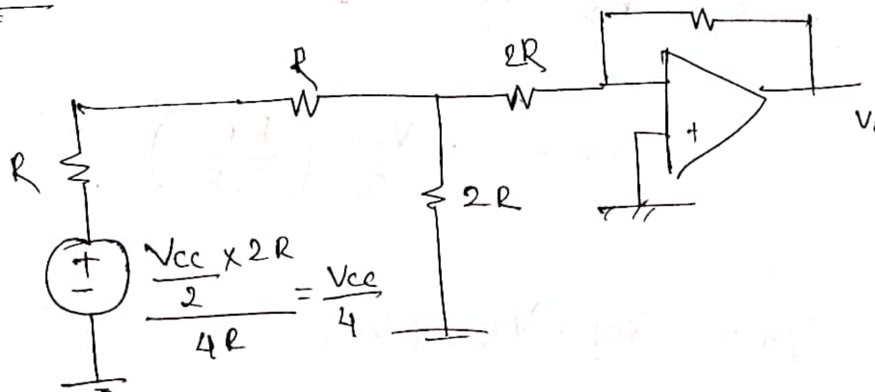
$b_2 b_1 b_0 = 0\ 0\ 1$



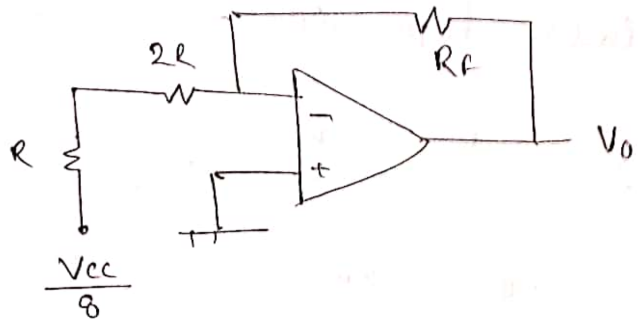
(fig a)

By Thevnin theorem





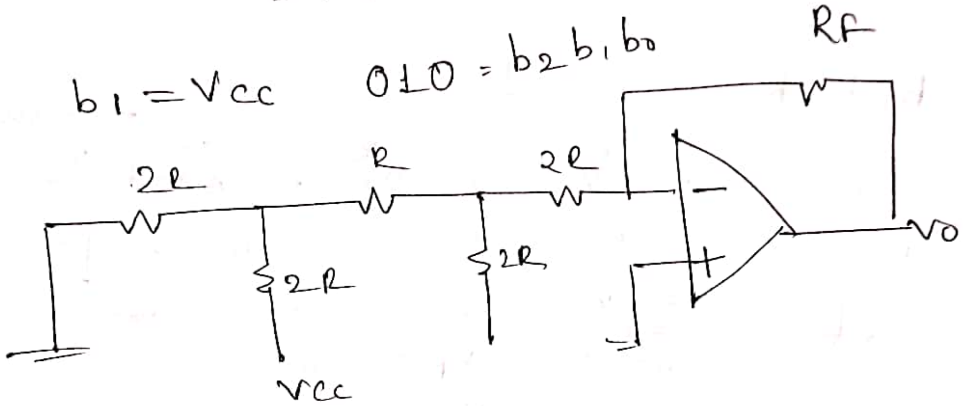
$$\frac{\frac{Vcc \times 2R}{2}}{4R} = \frac{Vcc}{4}$$



$$V_0 = \frac{V_{cc}}{8} \times \left(-\frac{R_f}{3R}\right)$$

$$V_{01} = -\frac{V_{cc} R_f}{24 R} = -\frac{b_0 V_{cc} R_f}{24 R}$$

<u>Case 2</u> $b_1 = V_{cc}$ $010 = b_2 b_1 b_0$



$$V_{02} = -\frac{V_{cc}}{4}\left(\frac{R_f}{3R}\right) = -\frac{V_{cc} R_f}{12 R}$$

$$= -\frac{b_1 V_{cc} R_f}{12 R}$$

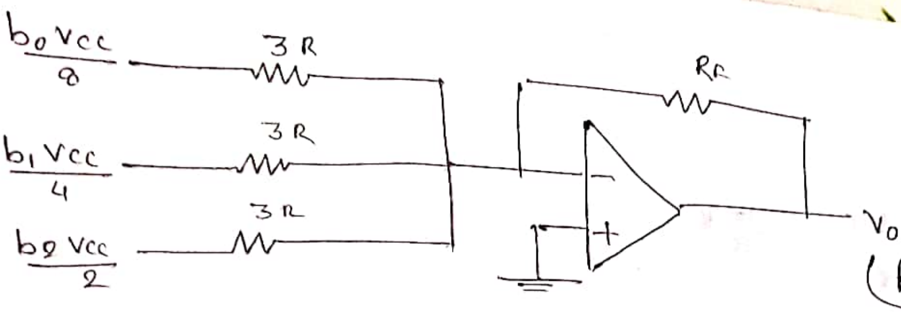
<u>Case 3</u> $b_2 = V_{cc}$ $100 = b_2 b_1 b_0$

$$V_{03} = -\frac{V_{cc}}{2}\left(\frac{R_f}{3R}\right) = -\frac{V_{cc} R_f}{6 R}$$

$$= -\frac{V_{cc} b_2 R_f}{6 R}$$

$$V_0 = V_{01} + V_{02} + V_{03}$$

Scanned by CamScanner



* fig b

(Remember fig A ⇒ fig b)

$$V_o = -\left[\frac{b_0 V_{cc} R_f}{24R} + \frac{b_1 V_{cc} R_f}{12R} + \frac{b_2 V_{cc} R_f}{6R}\right]$$

$$V_o = -V_{cc} R_f \left[\frac{b_0 + 2b_1 + 4b_2}{24R}\right]$$

$$V_o = \frac{-V_{cc} R_f}{24R}\left[2^0 b_0 + 2^1 b_1 + 2^2 b_2\right]$$

High on weight
Hence b_2 is MSB
b_0 is LSB

$$V_o \propto (b_0, b_1, b_2)$$

Generalization for n bit

$$\boxed{V_o = -\frac{V_{cc} R_f}{2^n 3R}\left[2^0 b_0 + 2^1 b_1 + 2^2 b_2 + \cdots 2^{n-1} b_{n-1}\right]}$$

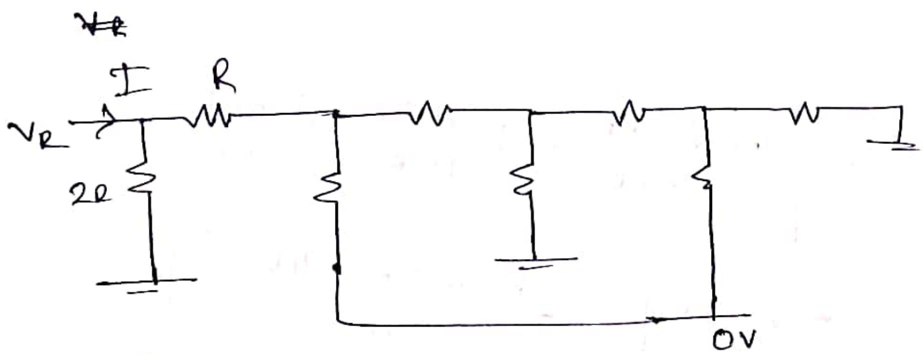
$(2^n \cdot 3R)$

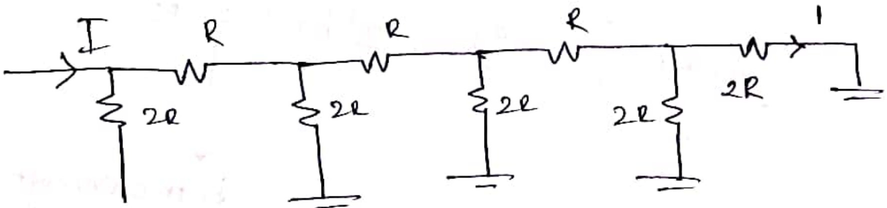
Que 9 & 10

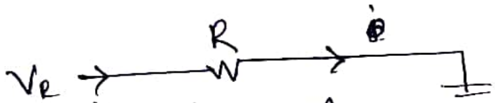
Sol

$\cancel{\dfrac{3R \times 2R}{5R}}$ $\quad \dfrac{6}{5}R$

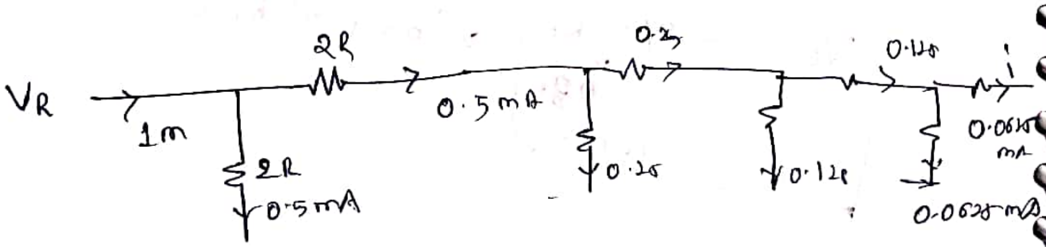
~~Vk~~







$I = \dfrac{10}{10} = 1mA$



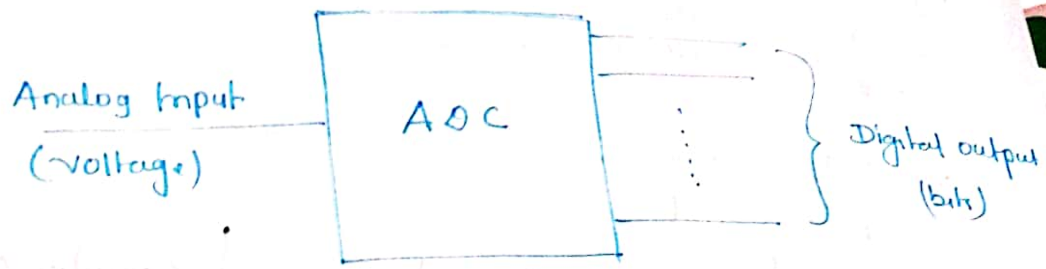
11) $I_{inv} = 0.25 + 0.0625$

$= 0.3125$

KCL at inverting ⇒ $\quad -0.3125 + \dfrac{0 - V_o}{10} = 0$

$V_o = -3.125\ V$ //

Analog To Digital Converter



Digital Output $\propto$ Analog I/p
(bits) (Voltage)

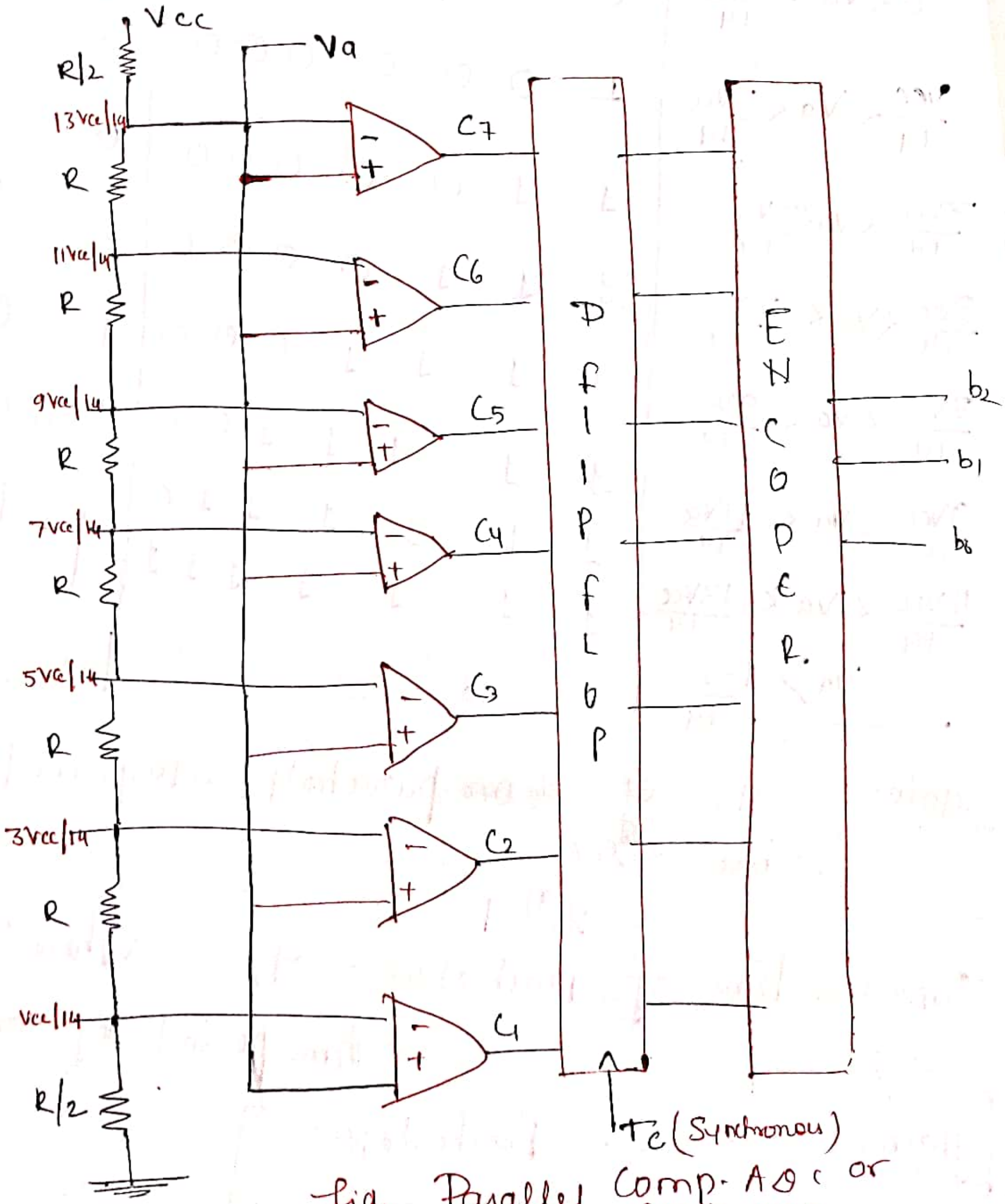


fig. Parallel Comp. ADC or Flash ADC

By VDR (volt division)

$$\frac{V_{cc} \times R/2}{7R} = \frac{V_{cc}}{14}$$

$$\frac{V_{cc} \times \frac{3R}{2}}{7R} = \frac{3V_{cc}}{14}$$

Range of V_a	Comparator o/p							encoder o/p		
	C_1	C_2	C_3	C_4	C_5	C_6	C_7	b_2	b_1	b_0
$0 < V_a < \frac{V_{cc}}{14}$	0	0	0	0	0	0	0	0	0	0
$\frac{V_{cc}}{14} < V_a < \frac{3V_{cc}}{14}$	1	0	0	0	0	0	0	0	0	1
$\frac{3V_{cc}}{14} < V_a < \frac{5V_{cc}}{14}$	1	1	0	0	0	0	0	0	1	0
$\frac{5V_{cc}}{14} < V_a < \frac{7V_{cc}}{14}$	1	1	1	0	0	0	0	0	1	1
$\frac{7V_{cc}}{14} < V_a < \frac{9V_{cc}}{14}$	1	1	1	1	0	0	0	1	0	0
$\frac{9V_{cc}}{14} < V_a < \frac{11V_{cc}}{14}$	1	1	1	1	1	0	0	1	0	1
$\frac{11V_{cc}}{14} < V_a < \frac{13V_{cc}}{14}$	1	1	1	1	1	1	0	1	1	0
$V_a > \frac{13V_{cc}}{14}$	1	1	1	1	1	1	1	1	1	1

Note: no. of comparators required for n bit ADC

$$= 2^n - 1$$

Conversion time of flash ADC $= T_c$. where T_c is time period of one clock pulse

$$\boxed{\text{flash ADC} \Longrightarrow \text{Fastest ADC}}$$

Scanned by CamScanner

Sol

Range of Vin	Comp. o/p x_1 x_2 x_3	encoder o/p y_1 y_0
~~$0 < Vin < 0.5$~~		
~~$0.5 < Vin <$~~		
$0 < Vin < \frac{\frac{3}{2}}{3} = \frac{1}{2}$	0 0 0	0 0
		0 1
$0.5 < Vin < 1.5$	1 0 0	1 0
$1.5 < Vin < 2.5$	1 1 0	1 1
$2.5 < Vin < 3$	1 1 1	

$$\boxed{y_1 = x_2}$$

$x_1 \backslash x_2x_3$				
	X	X	X	X
	X	X	X	X

$$y_0 = x_1 + x_3$$

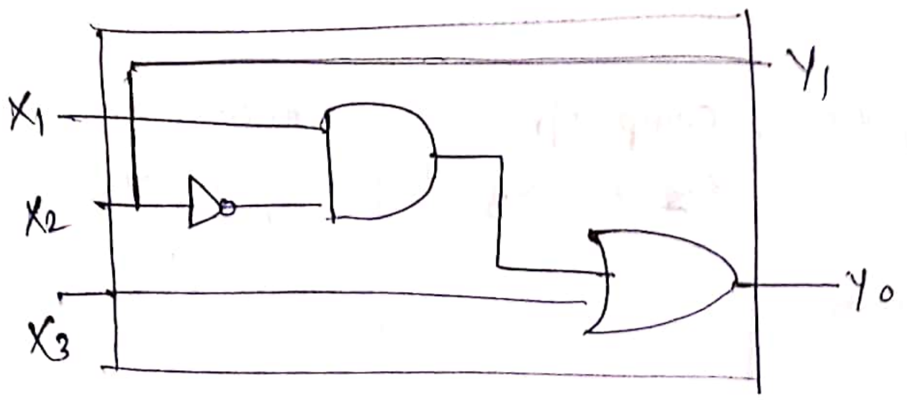
$x_1 \backslash x_2x_3$	$\bar{x}_2\bar{x}_3$	$\bar{x}_2x_3$	x_2x_3	$x_2\bar{x}_3$
$\bar{x}_1$	0	X	X	X
x_1	1	X	1	0

$$\boxed{y_0 = x_3 + x_1\bar{x}_2}$$

$$\cancel{y_0 = x_1\bar{x}_2\bar{x}_3 + x_1x_2x_3}$$

$$\cancel{= x_1[x_2 \odot x_3]}$$

$$\boxed{y_0 = x_1}$$



Q17

Sol Range Vin

X_0	X_1	X_2	B_1	B_0
0	0	0	0	0
1	0	0	0	1
1	1	0	1	0
1	1	1	1	1

B_0 :

$x_0 \backslash x_1x_2$				
0	0	X	X	X
1	1	X	1	0

$= B_0 = \bar{x}_2 + \bar{x}_1 x_0$

$= \cancel{x_2} + \cancel{x}$

not Matching with answer

Hence from table

$X_0 \bar{X}_1 \bar{X}_2 + X_0 X_1 X_2$

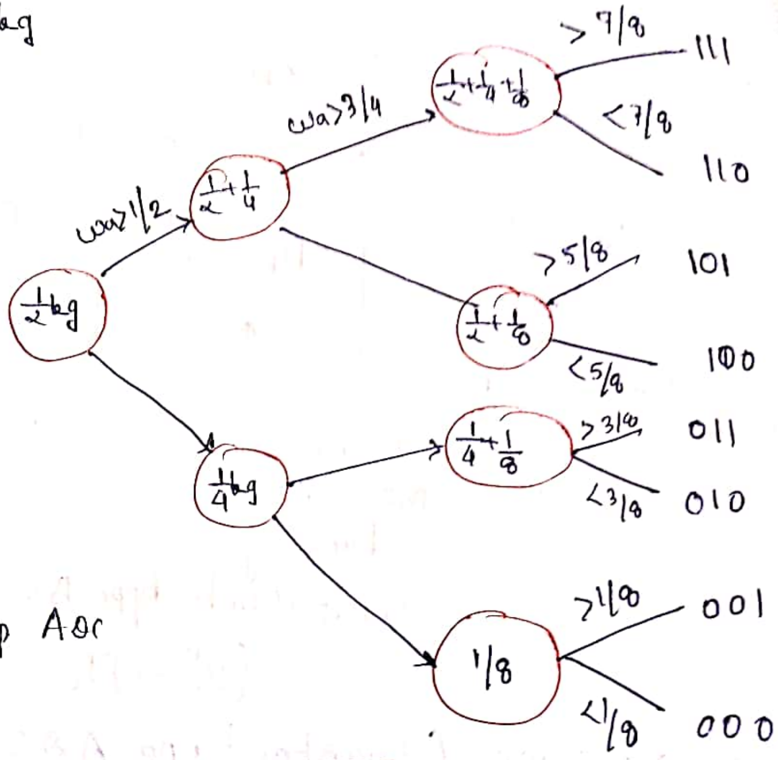
$\Rightarrow X_0 [\bar{X}_1 \bar{X}_2 + X_1 X_2]$

$\Rightarrow X_0 [\overline{X_1 \oplus X_2}]$ //

* Successive Approximation ADC

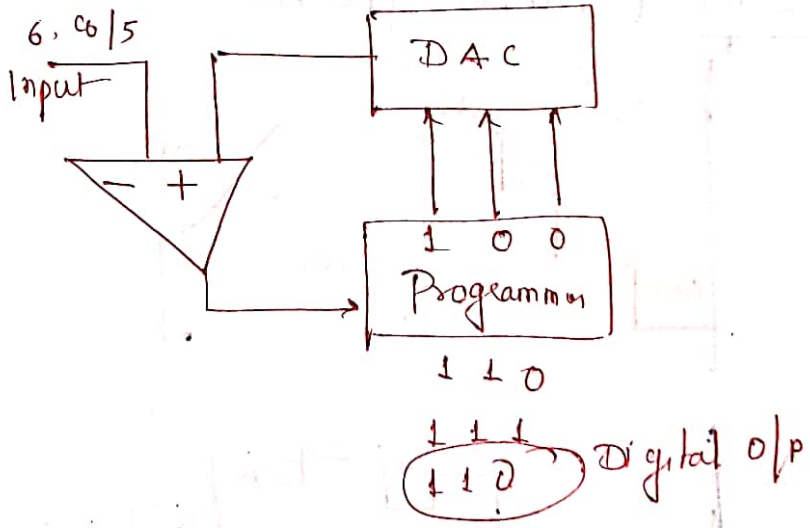
$\frac{1}{2}kg \quad \frac{1}{4}kg \quad \frac{1}{8}kg$

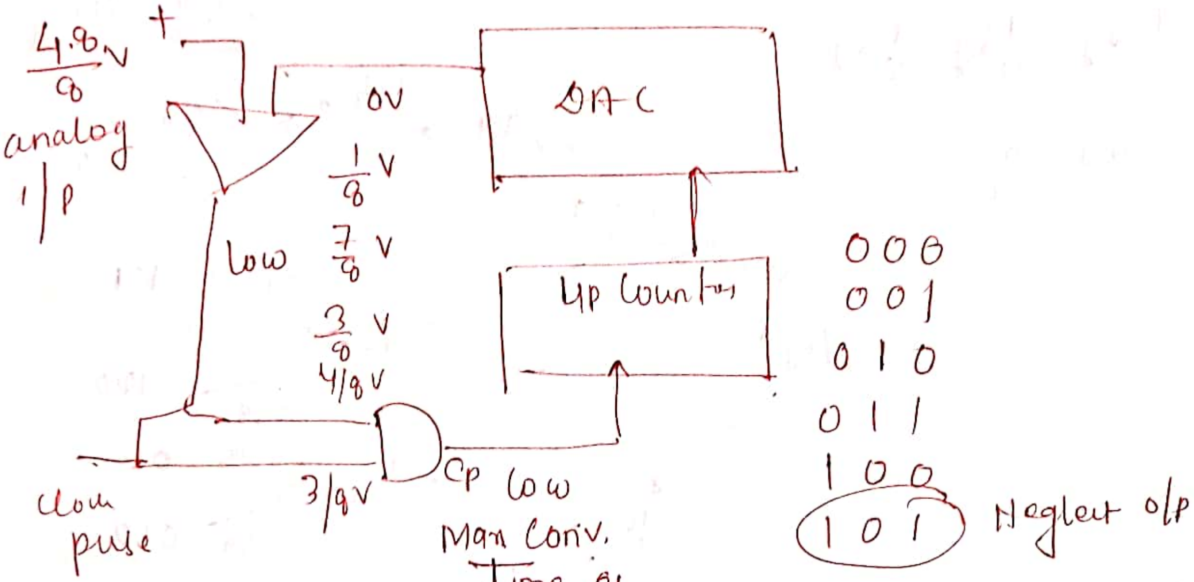
$wa = \frac{6.5}{8}$



Conversion time of nbit Successive App ADC

$= nT_c$





Max Conv. Time of n bit Counter type ADC

$$= (2^n - 1) T_c$$

* Single slope (Counter type ADC also Called SS ADC)

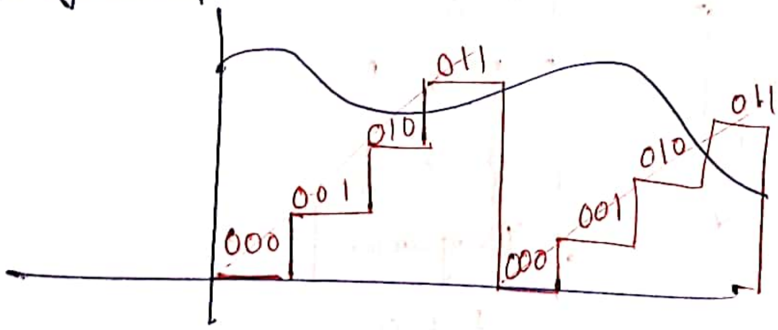


fig. Tracking type ADC

Scanned by CamScanner