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ECE ENGINEERING

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GATE ESE PSU's 2019-20

GATEACADEMY

101 ANALOG SYSTEM_GATEACADEMY

TOTAL PAGE ANALOG SYSTEM-754 PGAE

LATEST GATEACADEMY CLASSROOM HANDWRITTING

CONTENT COVERED:

1. Theory Notes
2. Explanation
3. Derivation
4. Example
5. Shortcut & Formula Summary
6. Previous year Paper Q. Sol.

Noted-: Single Source Follow, Revise

Multiple Time Best key of Success

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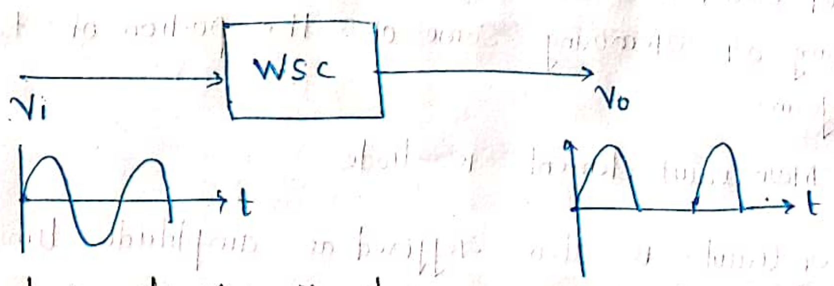
Diode Circuits

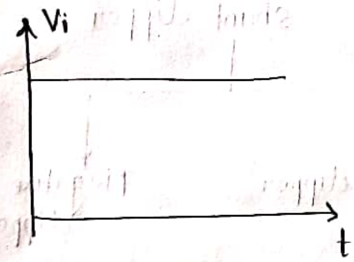
* Wave shaping Circuits

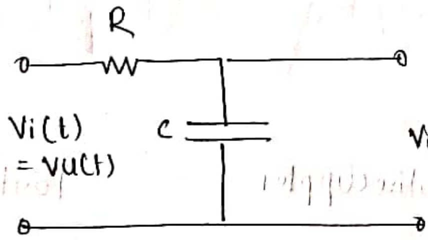


- It is used for changing the shape of waveform.

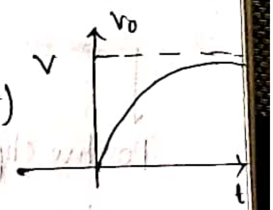
WSC

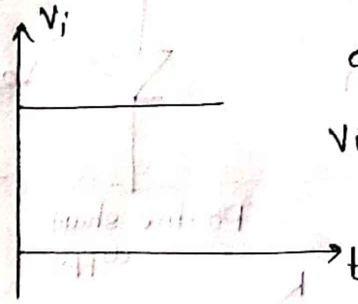
Linear WSC	Non-Linear WSC
based on linear element R, L, C	Based on Nolinear element like diode
eg. RC HPF LPF	eg Half wave Rectifier

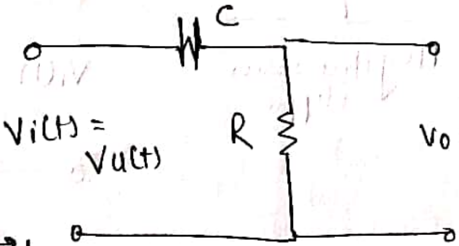




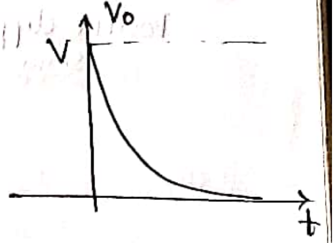
$V_{out} = V(1 - e^{-t/RC})$







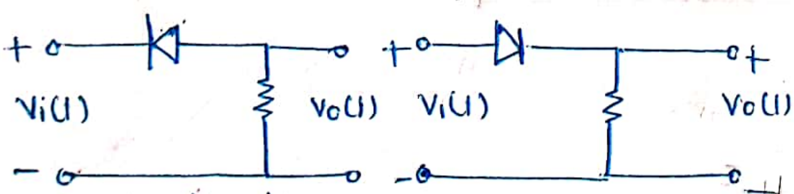
$V_o = V e^{-t/RC}$



* Clipper Circuits

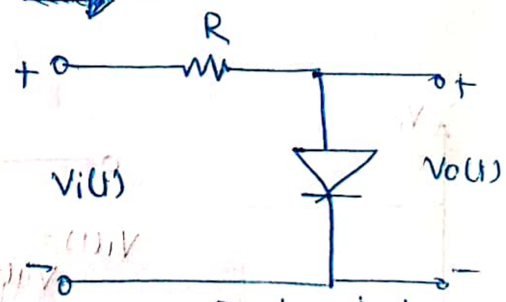
- Clipper Circuit is a non linear WSC which is used for clipping or removing some of the portion of transmitted waveform.
- The Main Circuit element is diode
- Clipper Circuit is also reffered as amplitude limiter or amplitude Selector Circuit.
- Classification of clipper Circuit

Clipper Circuit
- Series Clipper
  - Positive clipper
  - Negative clippter
- shunt clipper
  - Positive clipper
  - Negative clipper

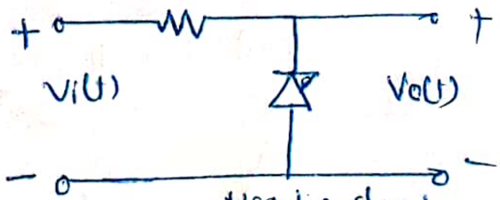


Positive clipper series

Negative series clipper

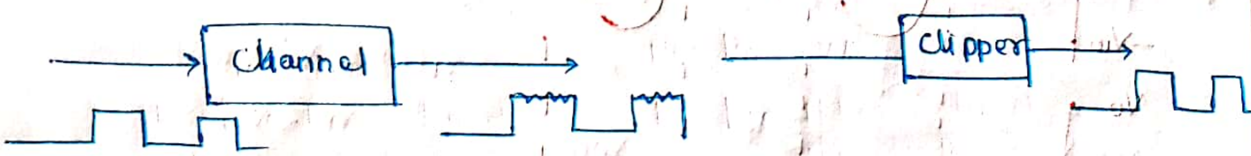


Positive shunt clipper

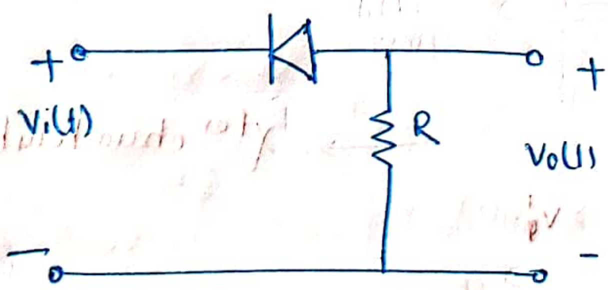


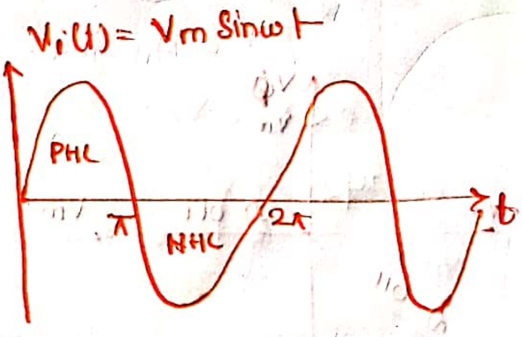
Negative shunt clipper

- In Series clipper Circuit diode is Connected in Series and in shunt clipper Circuit diode is Connected in parallel (structure wise)
- Positive clipper Circuit removes maximum Positive portion of $x$mitted wave form.
- Negative clipper circuit remove maximum Negative portion of $x$mitted waveform.
- Clipper Circuit Can be used for eliminating the effect of noise from waveform in digital Communication.



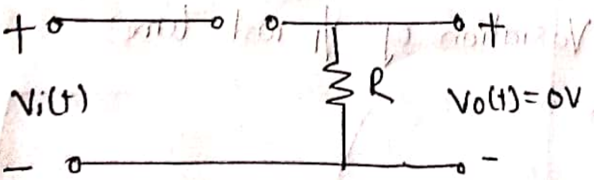
* Positive Series Clipper Circuit





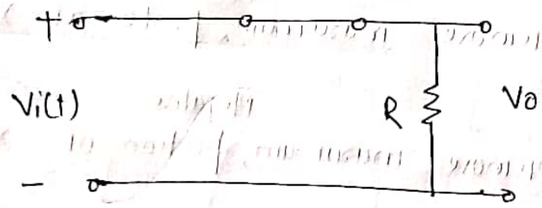
- During positive half cycle (PHC) $(0 < \omega < \pi)$

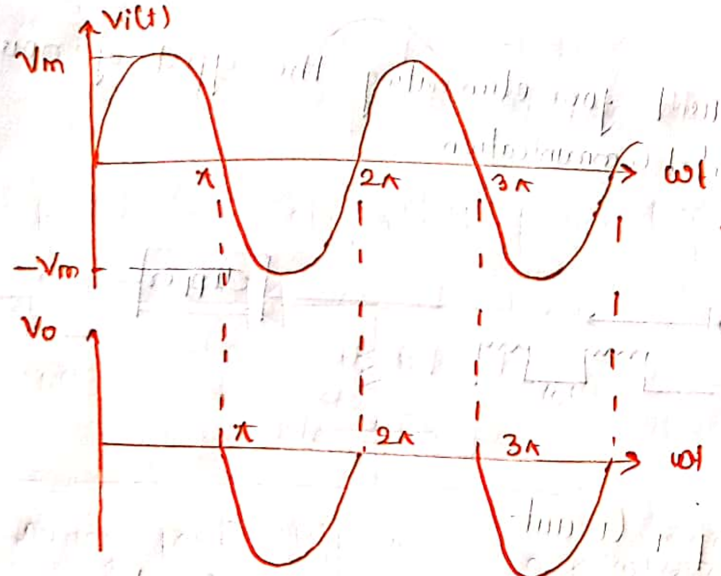
Diode = Reverse Bias (RB)



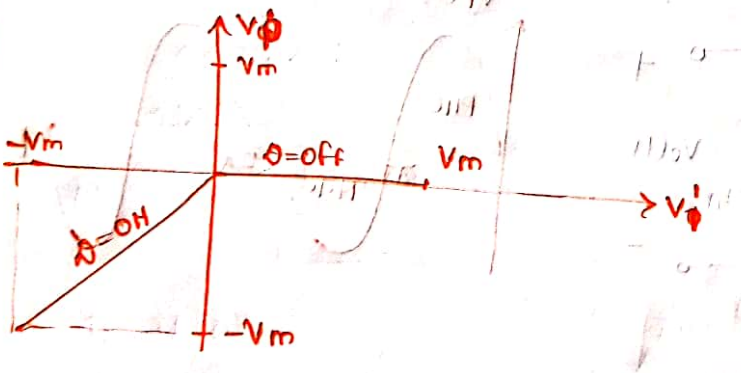
• During Negative Half cycle   Diode = forward Bias (FB)

$\pi < \omega t < 2\pi$





→ output characteristic

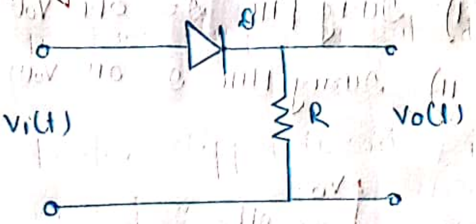


→ Xfer characteristic

• output characteristic describe the Variation of o/p wrt time

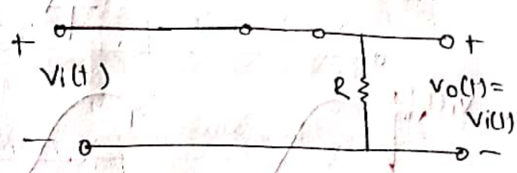
• Xfer characteristic describe Variation of i/p wrt time.

* Negative Series clipper



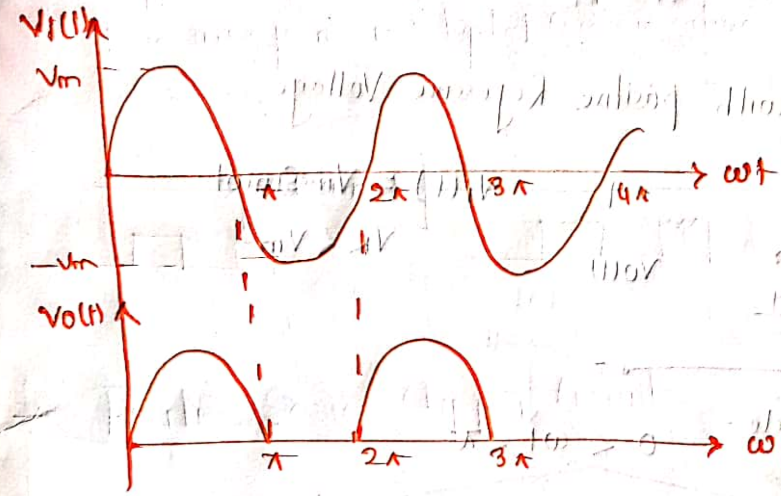
i) During positive half cycle $0 < \omega t < \pi$

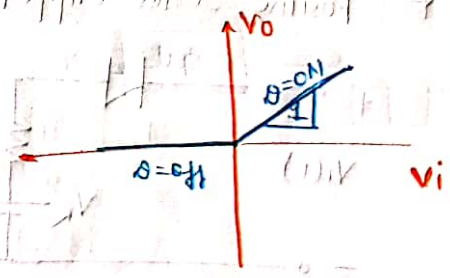
Diode = ON (FB)



ii) During Negative half cycle $\pi < \omega t < 2\pi$

D = off

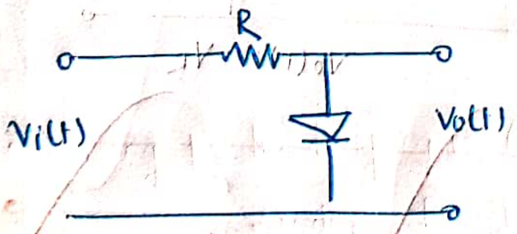




$V_o(avg) = \frac{V_m}{\pi}$

Output charac.

* Positive shunt clipper Circuit



i) PHC

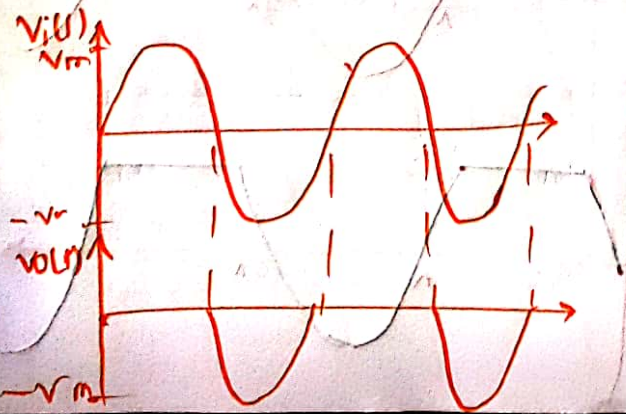
D → ON

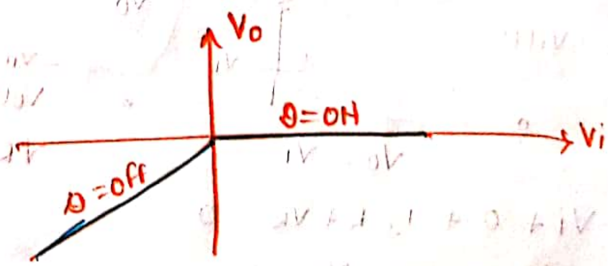
Vo(t) = ~~Vi(t)~~ 0

ii) NHC

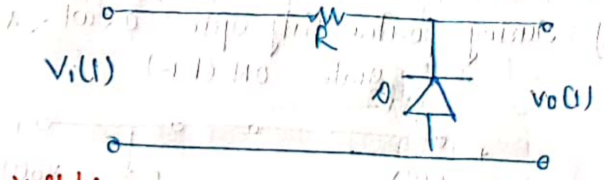
D → off

Vo(t) = Vi(t)



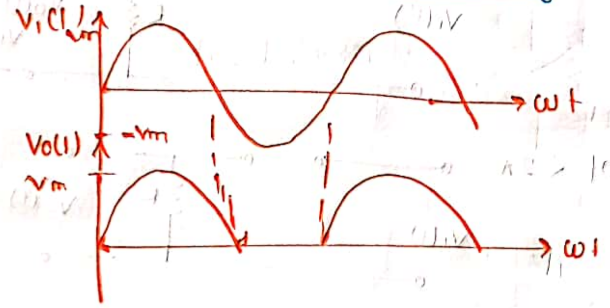


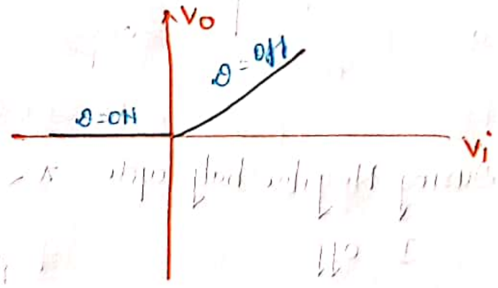
* Negative shunt clipper Circuit



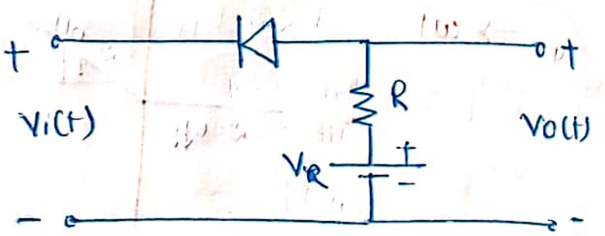
i) During PHC $D =$ off $V_o(t) = V_i(t)$

ii) During NHC $D =$ ON $V_o(t) = 0$





* Positive Series clipper with positive Reference Voltage

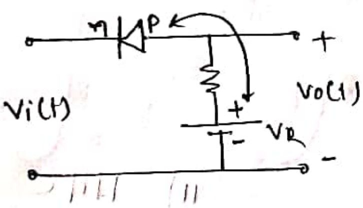


$V_i(t) = V_m \sin\omega t$

$V_R < V_m$

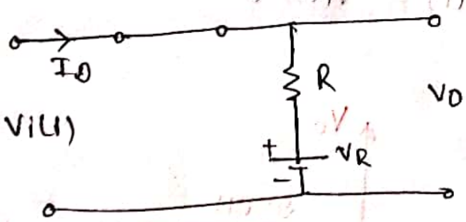
1) During positive Half cycle :- $0 < \omega t < \pi$

$0 < V_i < V_\gamma$



$I_D = f(V_R)$

$D =$ ON



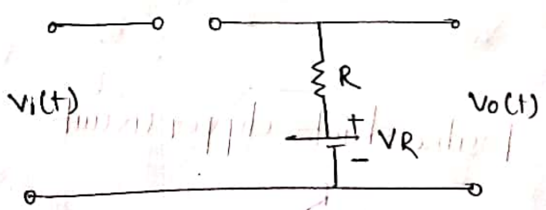
$V_o = V_i$

$-V_i + 0 + I_D R + V_R = 0$

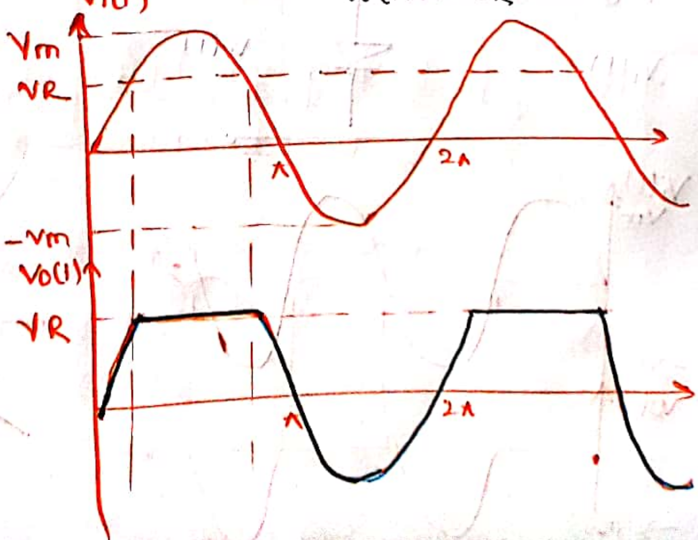
$I_D = \dfrac{V_i - V_R}{R}$

$V_o = I_D R + V_R = V_i$

$V_R < V_i < V_m$

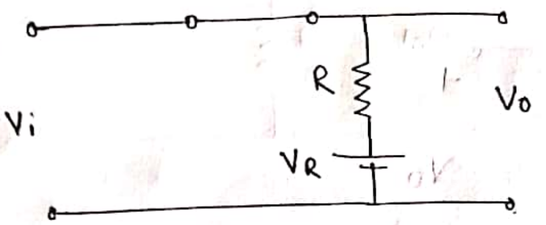


$V_o(t) = V_R$



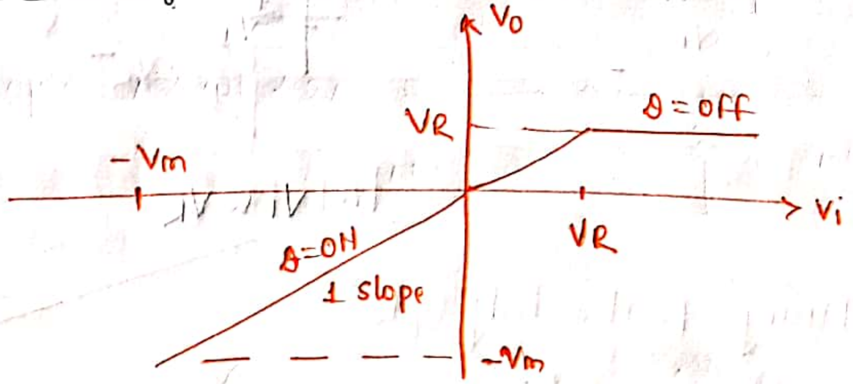
2) During Negative half Cycle :

$\pi < \omega t < 2\pi$

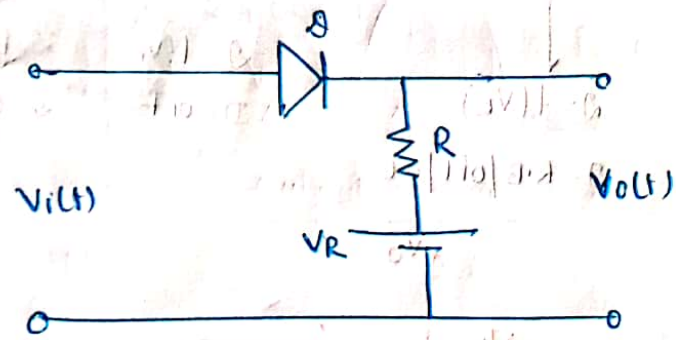


$D = f(V_i)$ or $D = f(V_R)$

$V_o(t) = V_i(t)$



* Negative Series clipper Circuit with Positive reference Voltage



$V_R < V_m$

i) $V_i > V_R$

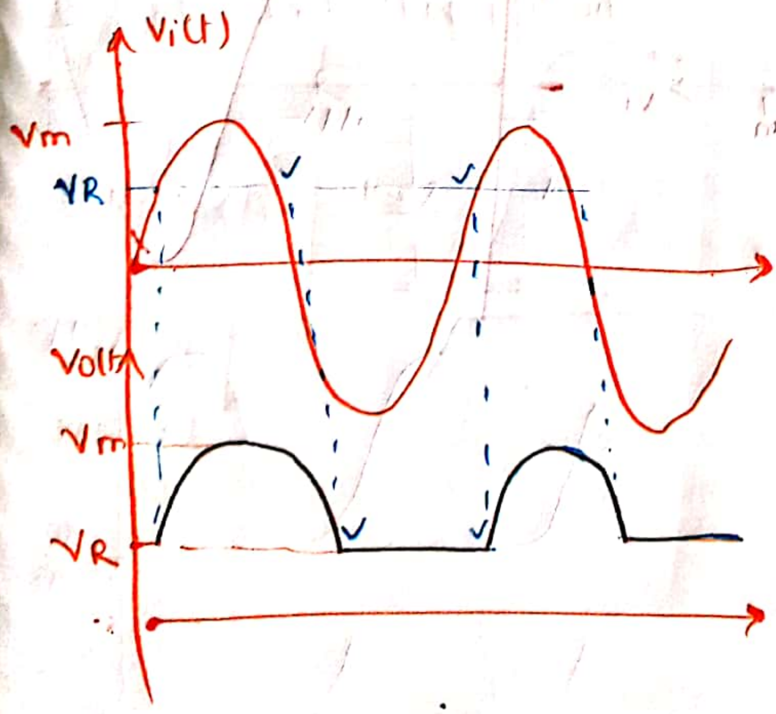
$D = f(V_i)$ $D \rightarrow ON$

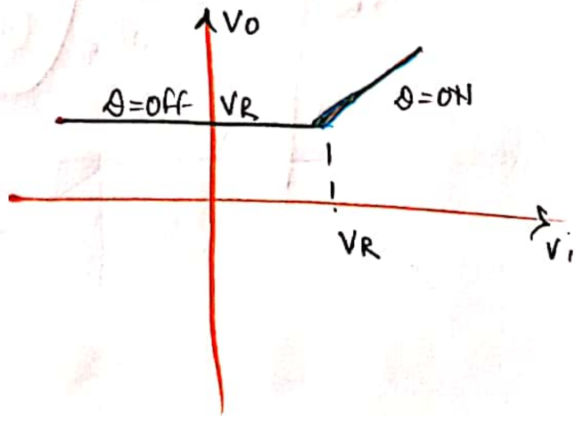
$V_o = V_i$

ii) $V_i < V_R$

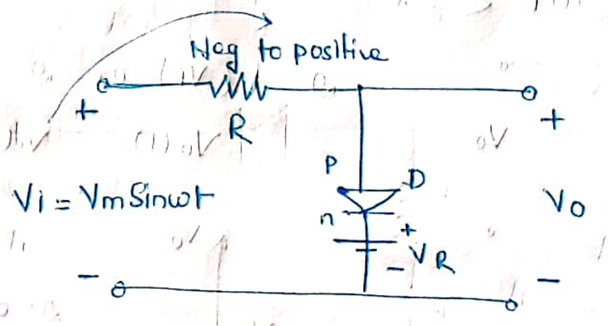
PMC	NMC
$D \rightarrow f(V_R)$	$D \rightarrow f(V_i)$
$D \rightarrow off$	or
	$D \rightarrow f(V_R)$
	$D \rightarrow off$

$V_o = V_R$





* Positive shunt clipper Circuit with Positive Reference Voltage



V_i & V_R

$V_i > V_R$

Positive Half Cycle (PHC)

$D = f(V_i)$

D = ON | FB | S.C

$V_o = V_R$

$V_i < V_R$

PHC Small

↓

$D = f(V_R)$

D = R.B | off | o.c

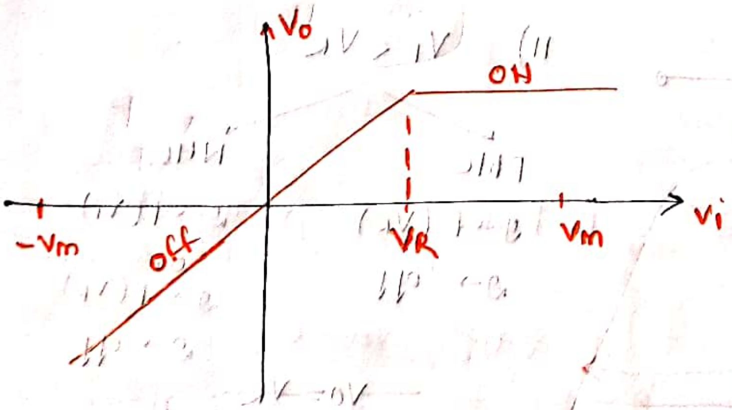
NHC

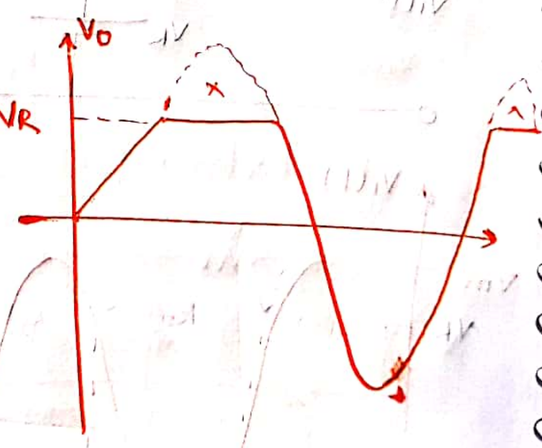
$D = f(V_i)$

D = off

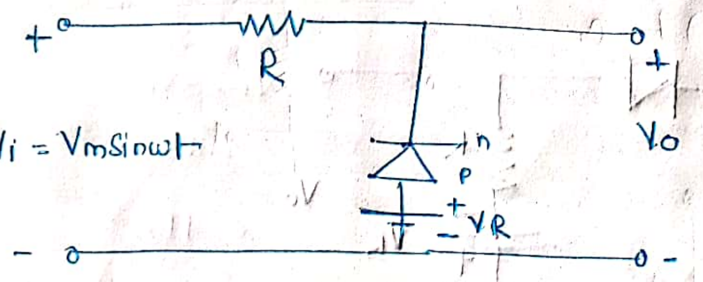
$D = f(V_R)$

D = off





* Negative shunt clipper circuit with positive Ref. Voltage



V_i & V_R

$V_i > V_R$

PHC

$D = f(V_i)$

D = off | RB | oc

$V_o = V_i$

$V_i < V_R$

PHC small

$D = f(V_R)$

D = ON | FB | SC

NHC

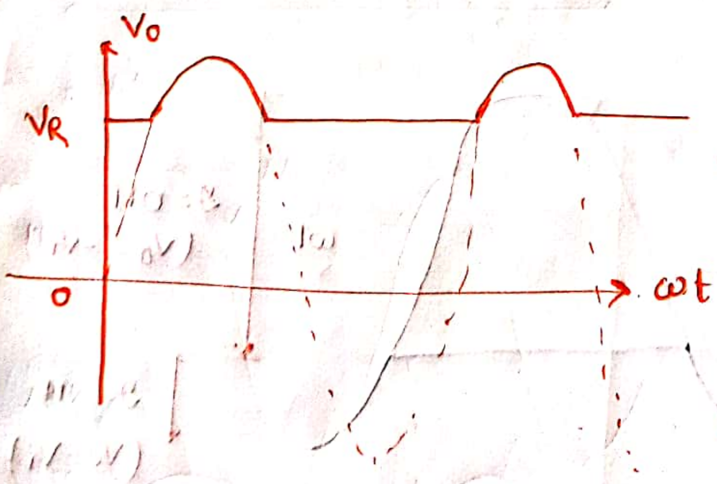
$D = f(V_i)$

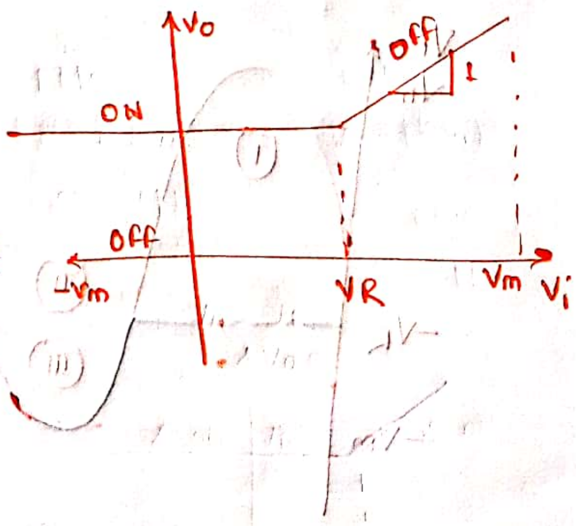
D = ON

$D = f(V_R)$

D = ON

$V_o = V_R$





WANT ECE BEST QUALITY-2019-20

LATEST HANDWRITING NOTES

BY

GATE ACADEMY CLICK HERE

SAMPLE NOTES WANT FULL NOTES CLICK

Noted-: Above ECE GATE/IES GATEACADEMY 2019-20 CLASSROOM BEST QUALITY Handwriting Notes Unique and Good Handwriting. Above Notes Enough for your Preparation..................

Noted-: Dear Aspirants If you do practice previous year paper 50% your work finished.so Guys daily at least 30minutes give previous year.

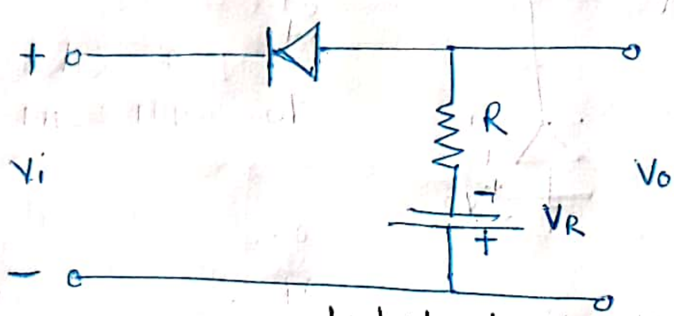
1. Previous year paper 4-5 times practice before final exam.

2. Subject wise study reference STD book

3. Test series practice more n more (Try to latest test series 2-3 fully solve then join online test series.)

Noted-: Single Source Follow, Revise Multiple Time Best key of Success

* Positive Series Clipper Circuit with negative reference Voltage



$|V_R| < |V_m|$

During positive half Cycle

(I) $0 < \omega t < \pi$

$V_i = +ve$

$V_R = -ve$

$D = f(V_i)$ — $D = OFF$

$D = f(V_R)$ — $D = ON$

$\boxed{V_o = -V_R}$

During Negative Half cycle

(II) $V_i > -V_R$

$D = f(-V_R)$

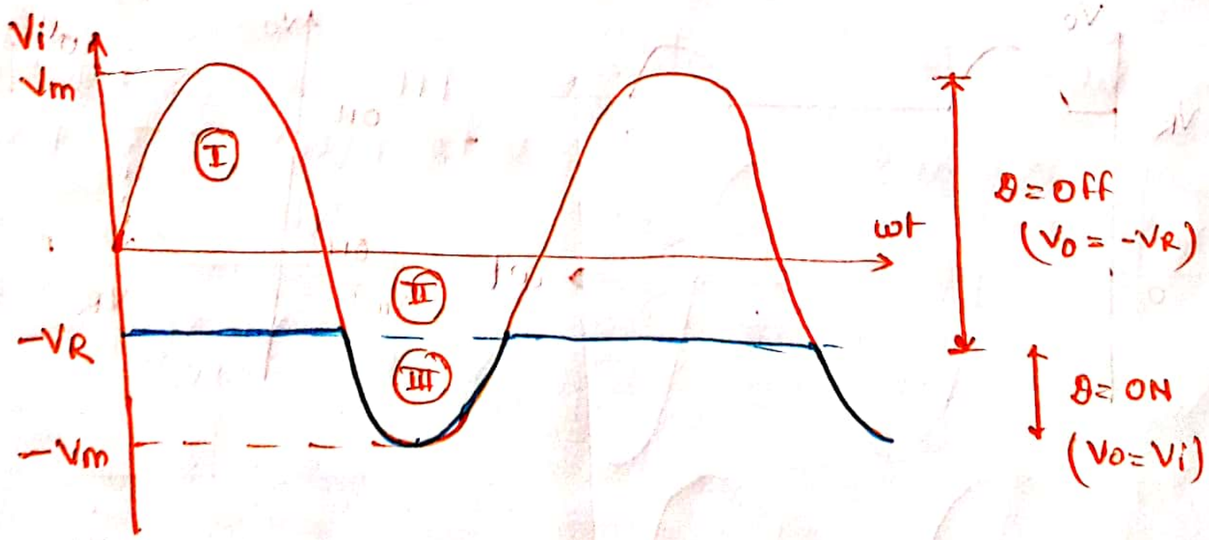
Diode = OFF

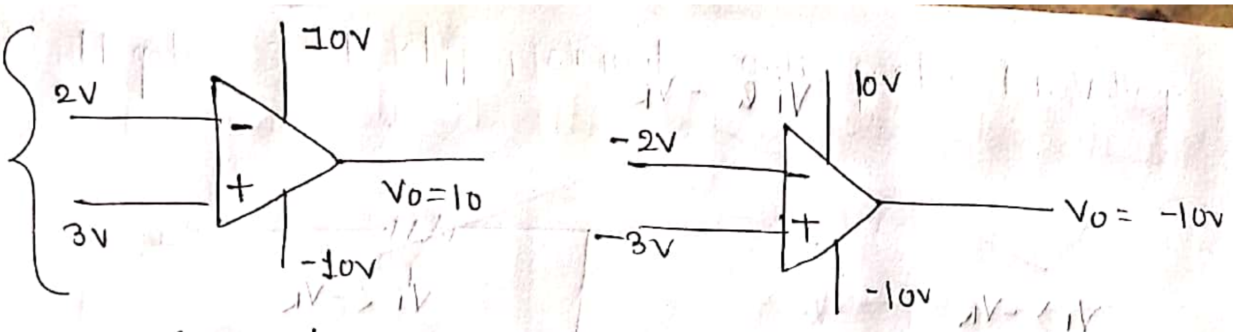
(III) $V_i < -V_R$

$D = f(V_i)$

Diode = ON

$V_o = V_i$



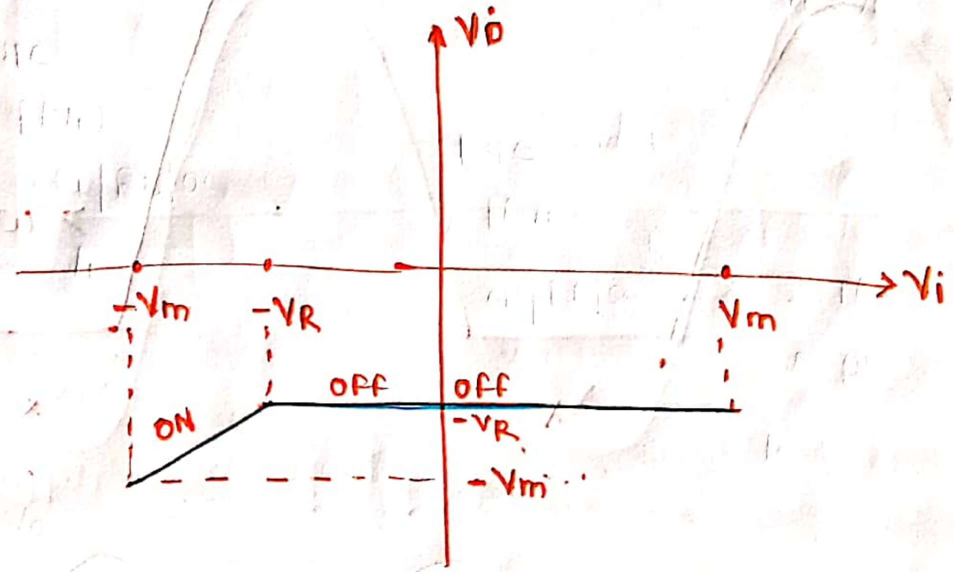


Comparator

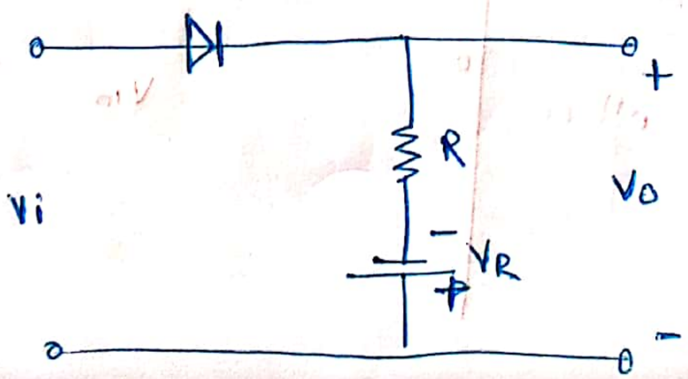
i) non inverting > Inverting   ii) Non Inverting < Inverting

In Comparator greater numbers decide the output

In Case of diode greater potential decide the output



* Negative Series Clipper Circuit with Negative Reference Voltage



* Frequency Response of Amplifier *

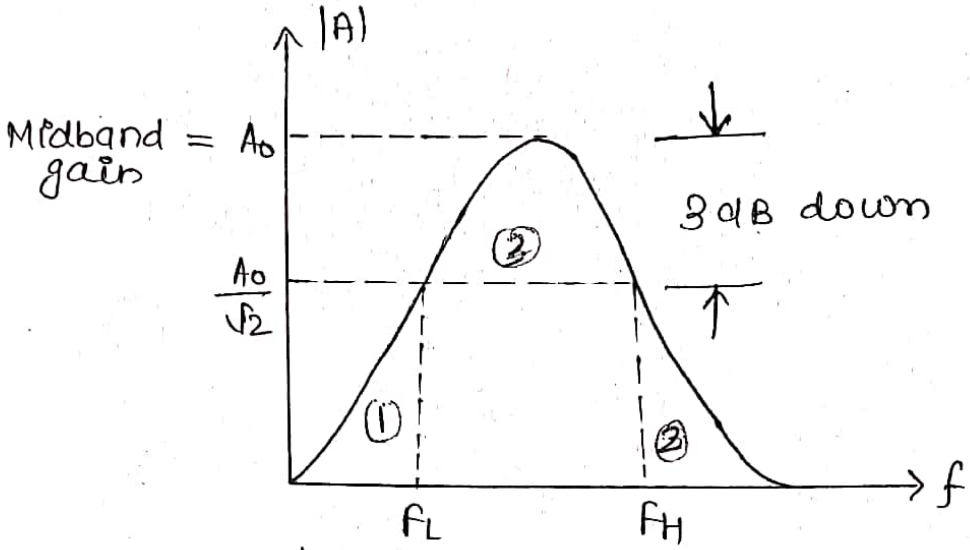


Fig (a) Practical frequency Response of Amplifier.

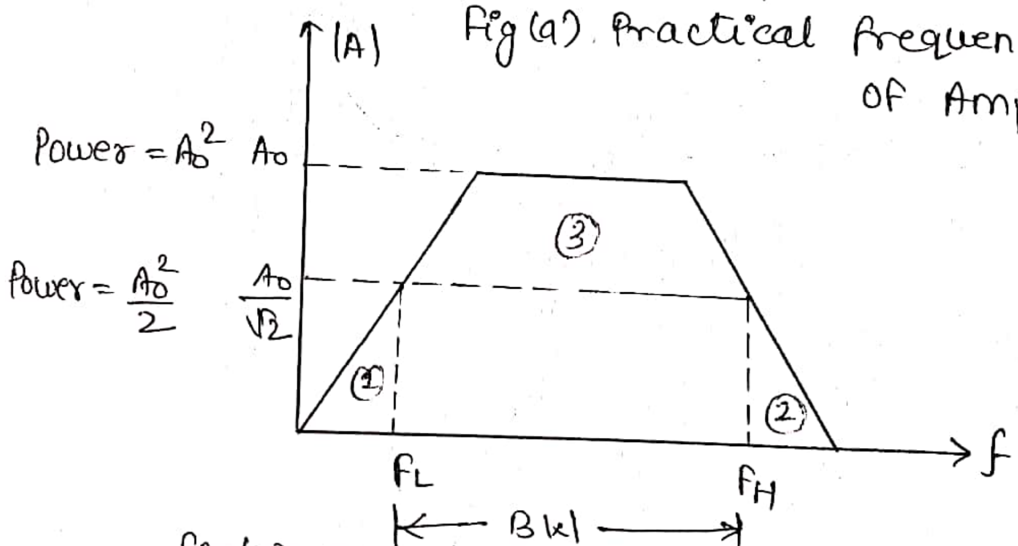


fig (b) Ideal frequency Response of Ampr.

* 3dB frequency is also known as half power frequency because power gets half at 3dB down.

f_L / f_H = 3- dB frequency
= Half Power frequency
= cut-off frequency
= Corner frequency.

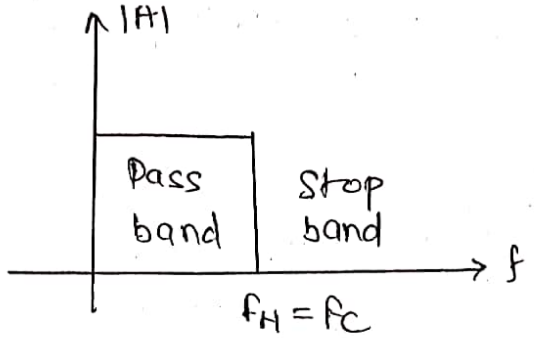


Fig Low pass filter

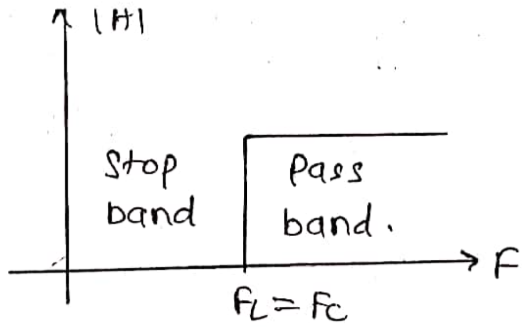


Fig High pass filter

R-1 = low frequency region
R-2 = High frequency region
R-3 = midband frequeny | flat freq. region.

* Low frequeny region is described by the characteristics of High Pass filter.
* High frequeny region is described by the characteristics of low pass filter.
* In both low and high frequeny region, gain decreases with frequency.
* Midband gain region describes the max. gain of Ampr.
* BW of Amplifier is given by, $BW = f_H - f_L$
* If $f_L = 0$ then $BW = f_H$

<u>example:-</u> If 3 dB freq. of Ampr is 3MHz then BW will be -

$$BW = 3MHz.$$

(If only one 3dB freq. is defined then by default it is upper 3dB freq. i.e. f_H)

* Analysis of higher 3 dB frequency (f_H) —

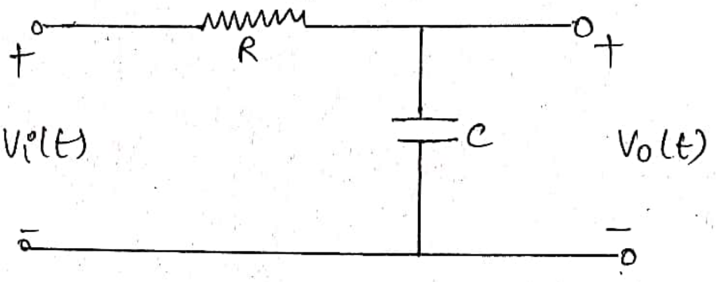
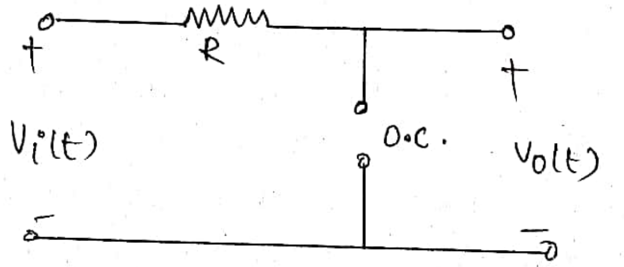


Fig: First order RC Network

(i) Low frequency signal (i/p)

Ideal ($f=0$) $\therefore$ $X_C = \frac{1}{2\pi f C} = \infty$

$C \rightarrow O \cdot C$

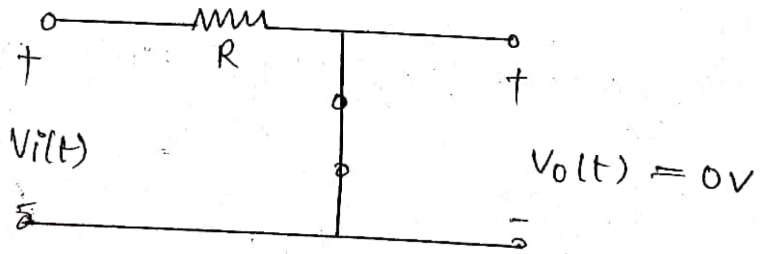


$\boxed{V_o(t) = V_i(t)}$

$\therefore$ This n/w passes the low freq. signal.

(ii) High frequency signal (i/p)

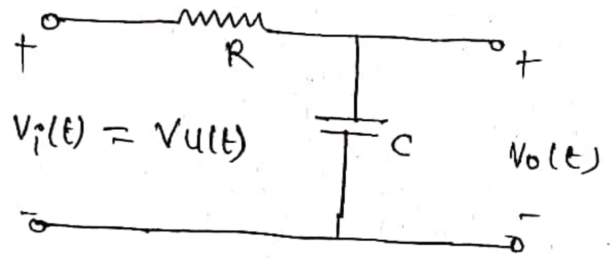
Ideal ($f=\infty$) $\therefore$ $X_C = \frac{1}{2\pi f C} = 0$ $\therefore$ $C \rightarrow S \cdot C$

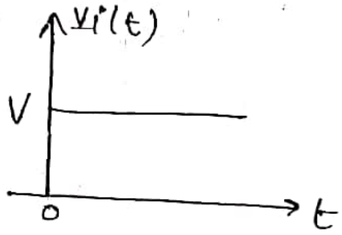


$\therefore$ This n/w stops the high freq. i/p signal.

$\therefore$ The network is a low pass filter circuit (LPF :- gives min. attenuation (signal pass) in low freq. and max. attenuation (stops) in high freq i/p signal) ← Practically

* This RC network is referred as <u>charging circuit</u> or <u>integrator circuit</u>.





$$v_c(t) = v_o(t) = V\left[1 - e^{-t/RC}\right]$$

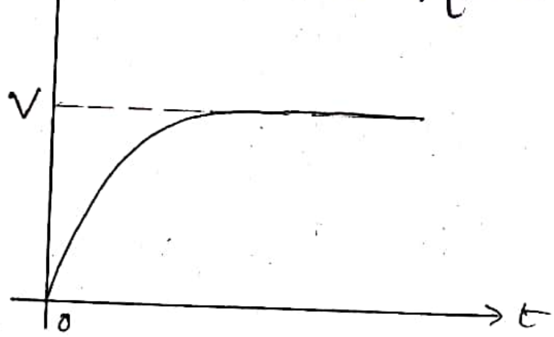
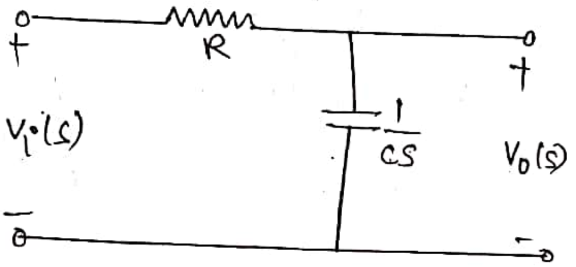


Fig: Step response of RC low pass filter

→ Transform domain

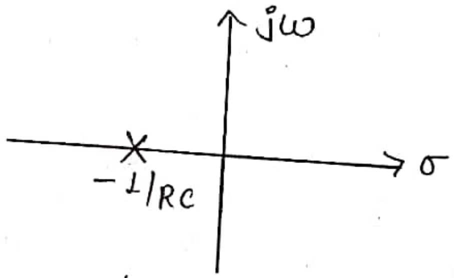


$$V_o(s) = V_i(s) \times \frac{\frac{1}{CS}}{R + \frac{1}{CS}}$$

$$\boxed{H(s) = \frac{V_o(s)}{V_i(s)} = \frac{1}{1 + RCS}}$$

$H(s=0) = 1.0$

$H(s=\infty) = 0.0$



* finite left hand pole in a s-plane represents first order LPF.

$$H(j\omega) = \frac{1}{1 + j\omega RC}$$

$$H(j\omega) = \frac{1}{1 + j2\pi f RC}$$

$$H(j\omega) = \frac{1}{1 + j\,\omega/\omega_H}, \text{ where } \omega_H = \frac{1}{RC} \text{ rad/sec}$$

Imp

* $H(j\omega) = \dfrac{1}{1 + j\omega/\omega_H}$ where $\omega_H = \dfrac{1}{RC}$ rad/sec

* $H(j\omega) = \dfrac{1}{1 + jf/f_H}$ where $f_H = \dfrac{1}{2\pi RC}$ Hz.

$$|H(j\omega)| = \frac{1}{\sqrt{1 + (f/f_H)^2}} = \text{Magnitude spectrum}$$

$$|H(j0)| = 1.0$$

$$|H(jf_H)| = \frac{1}{\sqrt{2}} = 0.707$$

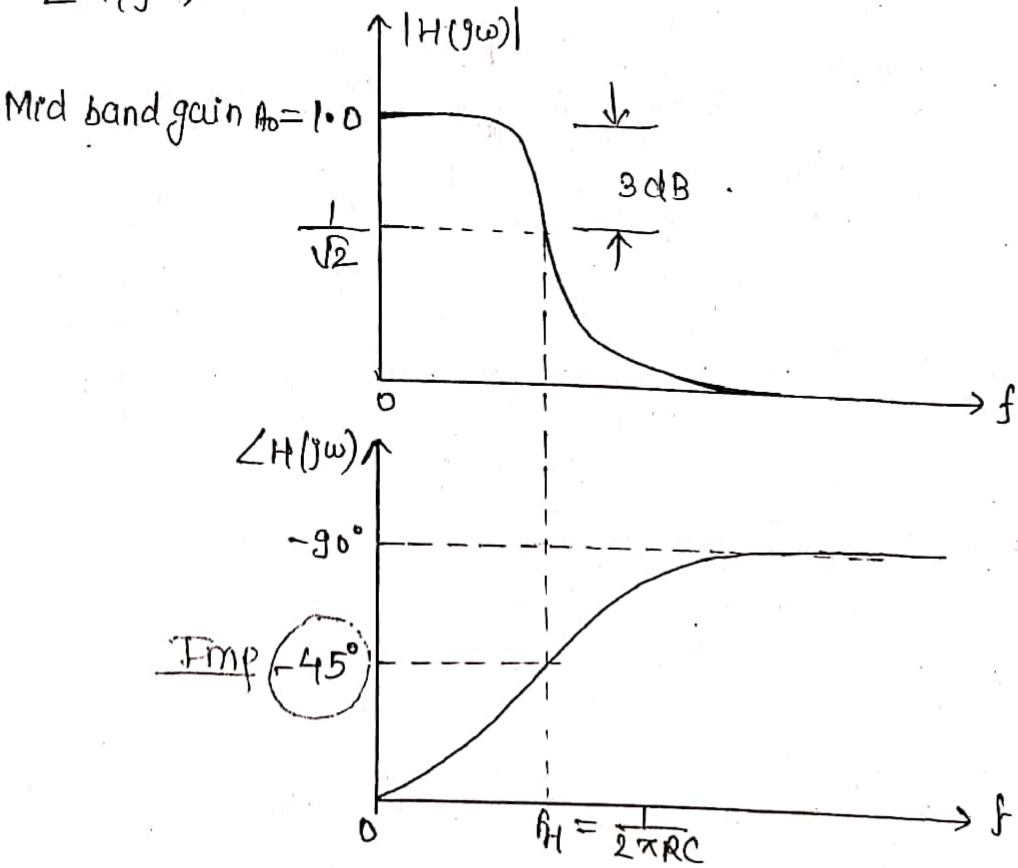
$$|H(j\infty)| = 0.0$$

$$\angle H(j\omega) = -\tan^{-1}(f/f_H) = \text{Phase spectrum}$$

$$\angle H(j0) = 0^\circ$$

$$\angle H(jf_H) = -45^\circ$$

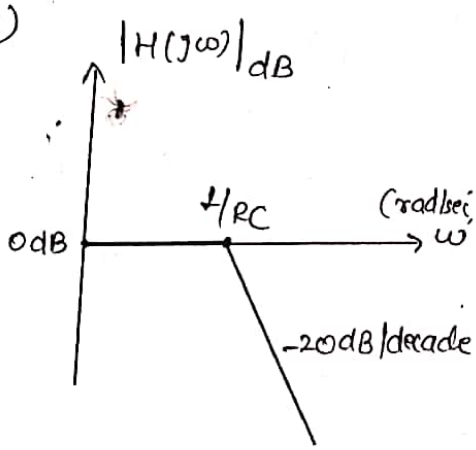
$$\angle H(j\infty) = -90^\circ$$



* RC low pass filter is referred as Lagging Network or Lag compensator because it provides (-ve) angle for all positive values of frequency.

→ $H(s) = \frac{1}{1+RCs}$

Bode Plot : $H(s) = \frac{1}{1 + s/(1/RC)}$



$K = 1.0$

Corner freq $(\omega_c) = \frac{1}{RC}$ rad/sec

Pole $= \frac{1}{RC}$

Slope $= -20$ dB/dec.

* Analysis of Lower 3-dB Frequency :-

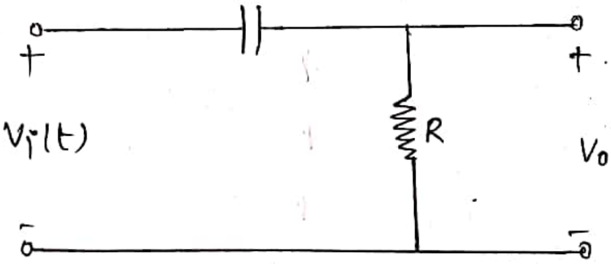


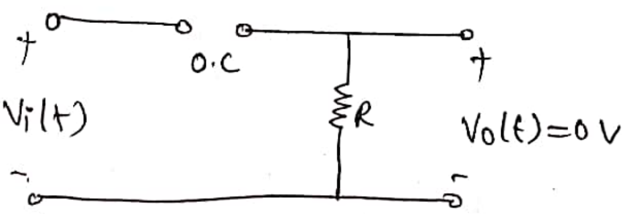
Fig:- RC Network

(i) Low Frequency

ideal $(f=0)$

$X_C = \infty$

$C = O.C$



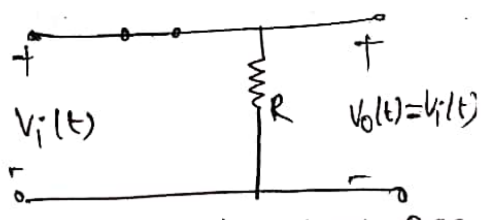
∴ stops the low freq. i/p signal

(ii) High Frequency

ideal $(f=\infty)$

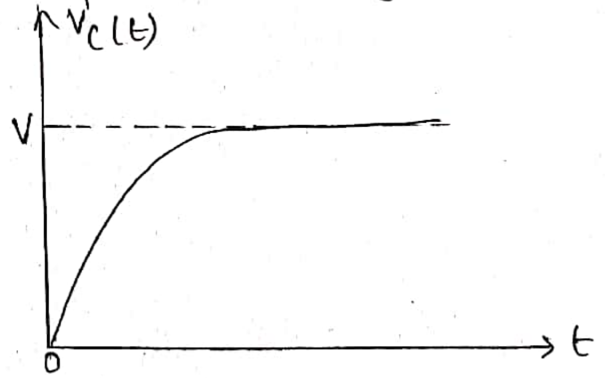
$X_C = \frac{1}{2\pi f C} = 0$

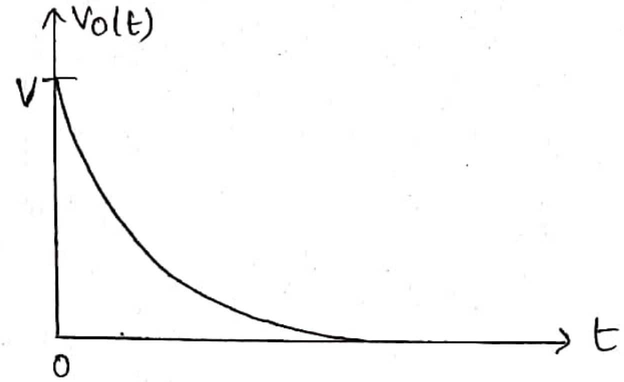
$C = S.C.$



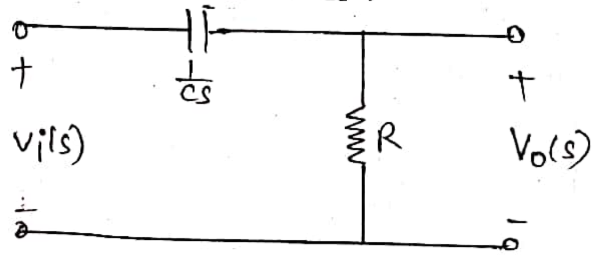
∴ passes the high freq. i/p signal.

∴ This Network represents High Pass Filter :-



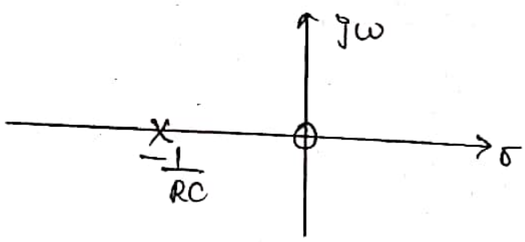


Transform domain—



$$V_0(s) = V_i(s) \times \frac{R}{R + 1/Cs}$$

$$\boxed{\frac{V_0(s)}{V_i(s)} = H(s) = \frac{RCs}{1+RCs}}$$



$H(s=0) = 0.0$

$H(s=\infty) = 1.0$

* One 'zero' at origin and one left hand pole in s-plane represents a HPF.

$$H(j\omega) = \frac{j\omega RC}{1 + j\omega RC}$$

$$H(j\omega) = \frac{1}{1 + \frac{1}{j\omega RC}}$$

$$H(j\omega) = \frac{1}{1 - j/\omega RC}$$

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$$H(j\omega) = \frac{1}{1 - j/2\pi f C R}$$

$*$ $$H(j\omega) = \frac{1}{1 - j\,\omega_L/\omega} \quad \text{where } \omega_L = \frac{1}{RC} \text{ rad/sec}$$

$*$ $$H(j\omega) = \frac{1}{1 - j f_L/f} \quad \text{where } f_L = \frac{1}{2\pi RC} \text{ Hz.}$$

$$|H(j\omega)| = \frac{1}{\sqrt{1 + (f_L/f)^2}}$$

$$\angle H(j\omega) = \tan^{-1}\left(\frac{f_L}{f}\right)$$

$|H(j0)| = 0.0$

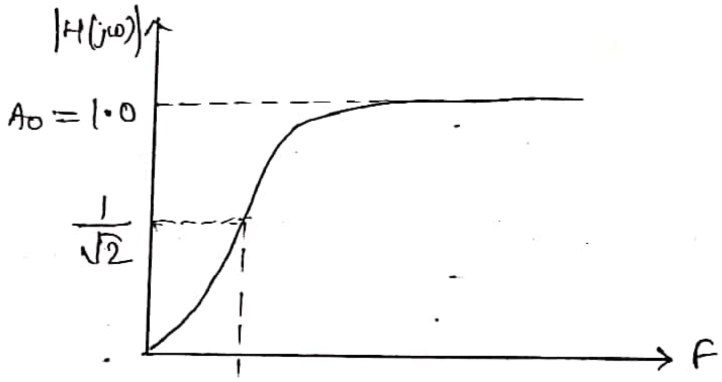
$|H(jf_L)| = \frac{1}{\sqrt{2}}$

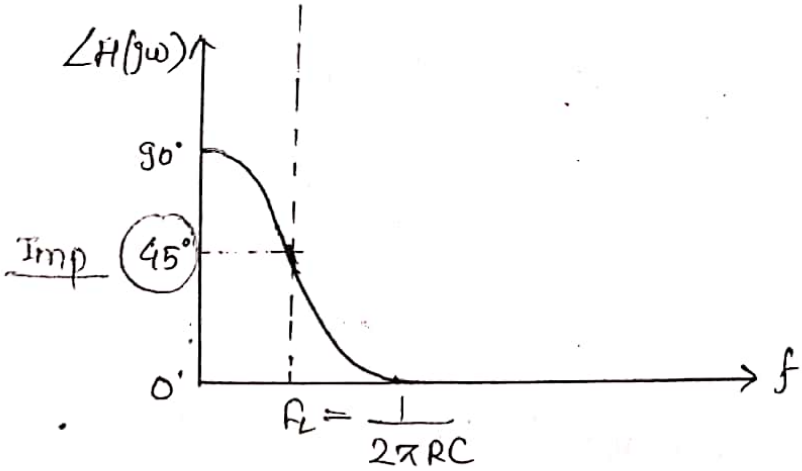
$|H(j\infty)| = 1.0$

$\angle H(j0) = 90^\circ$

$\angle H(jf_L) = 45^\circ$

$\angle H(j\infty) = 0^\circ$





Bode Plot:

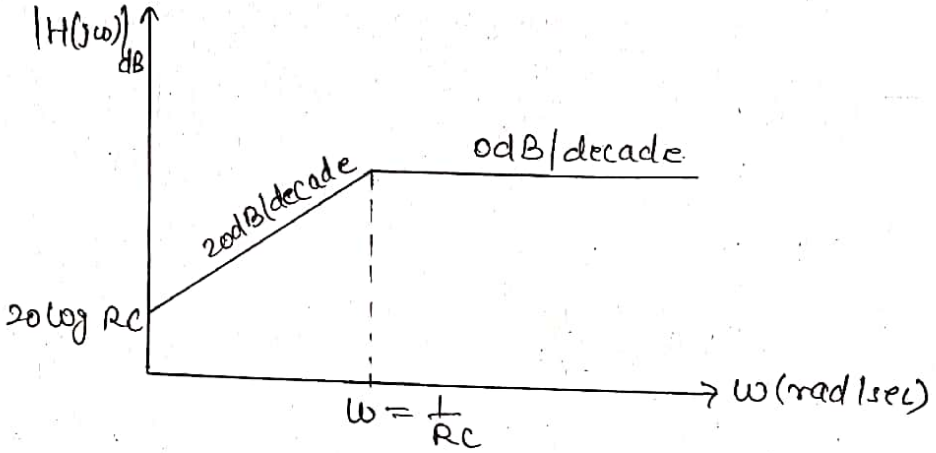
$$H(s) = \frac{RCs}{1+RCs}$$

$$H(s) = \frac{RCs}{1+s/(1/RC)}$$

zero = origin , slope = 20 dB/decade

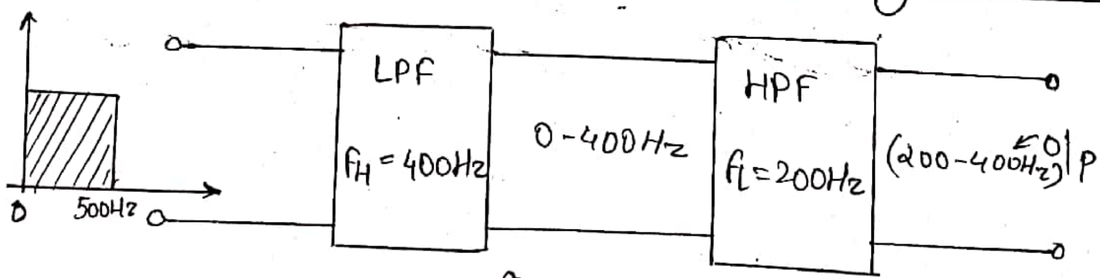
Pole = $-\frac{1}{RC}$, slope = −20dB/dec.

$K = RC$

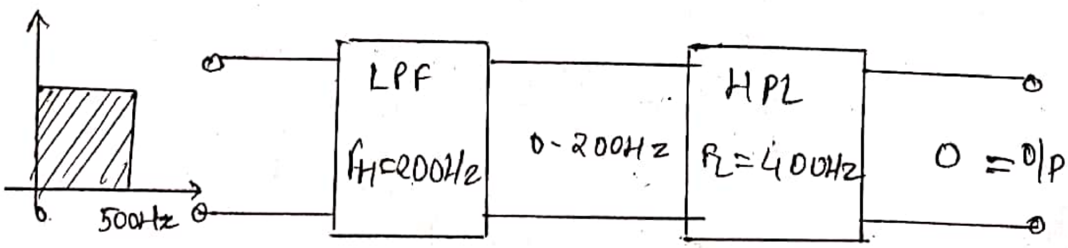


* High pass filter is referred as Leading N/w or Lead compensator.

* Cascade Connection of Low and High Pass filter:



fig(a) $f_H > f_L$



fig(b) $f_L > f_H$

CURRENT MIRROR CIRCUIT

The ckt in which the o/p current is forced to equal the i/p current is referred as Current Mirror ckt. (o/p current is mirror image of i/p current)

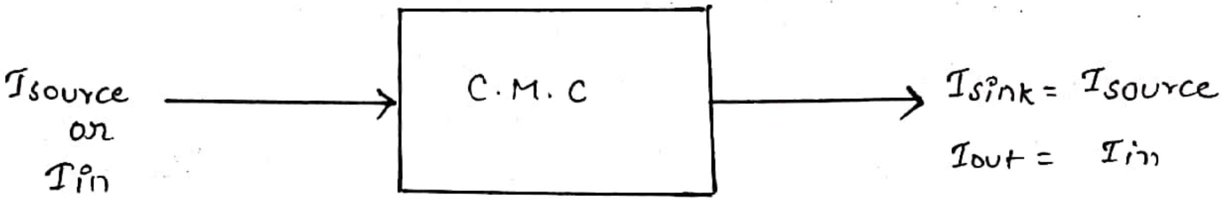
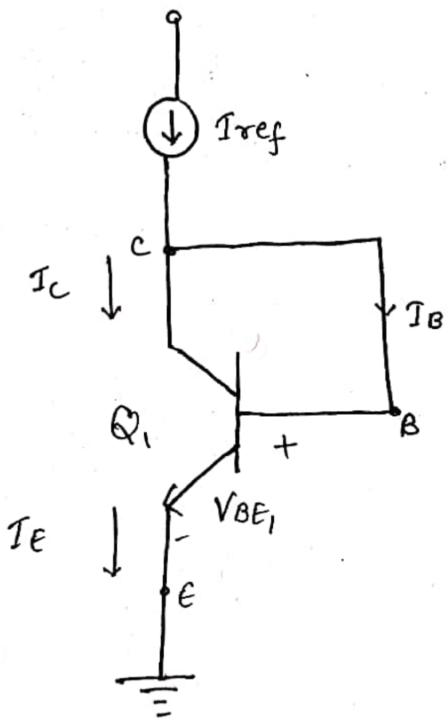


Fig Basic Block diagram.

Concept :-



Fig(a) Diode connected Transistor
(VCB = 0 V)

$V_{CB} = 0V$

Assume: β = very large

$I_B = 0A$

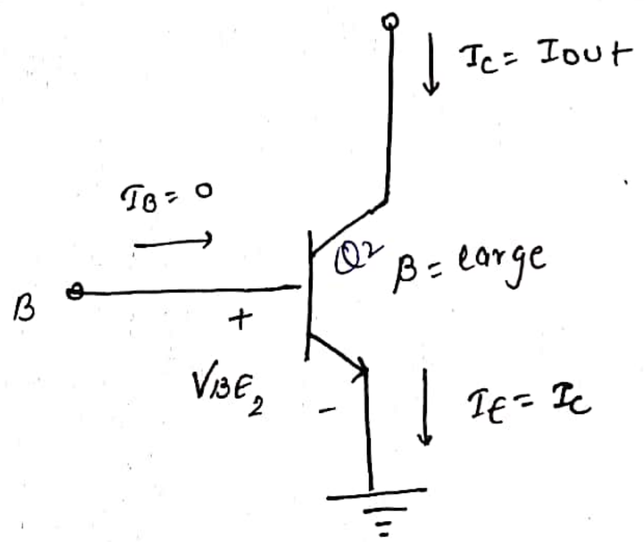
i.e $I_C = I_E = I_{ref}$

$$I_{ref} = I_0 e^{V_{BE_1}/V_T}$$

$$\frac{I_{ref}}{I_0} = e^{V_{BE_1}/V_T}$$

$$\ln\left(\frac{I_{ref}}{I_0}\right) = \frac{V_{BE_1}}{V_T}$$

$$V_{BE_1} = V_T \ln\left(\frac{I_{ref}}{I_0}\right) \quad \text{— (1)}$$



$$I_{out} = I_0 e^{\frac{V_{BE2}}{V_T}}$$

$$\frac{I_{out}}{I_0} = e^{V_{BE2}/V_T}$$

$$\ln\left(\frac{I_{out}}{I_0}\right) = \frac{V_{BE_2}}{V_T}$$

$$V_{BE_2} = V_T \ln\left(\frac{I_{out}}{I_0}\right) \quad \text{— (2)}$$

if $V_{BE_1} = V_{BE_2}$

$$\cancel{V_T} \ln\left(\frac{I_{ref}}{I_0}\right) = \cancel{V_T} \ln\left(\frac{I_{out}}{I_0}\right)$$

$$\frac{I_{ref}}{I_0} = \frac{I_{out}}{I_0}$$

$$I_{out} = I_{ref}$$

$$\boxed{I_{out} = I_{ref}}$$

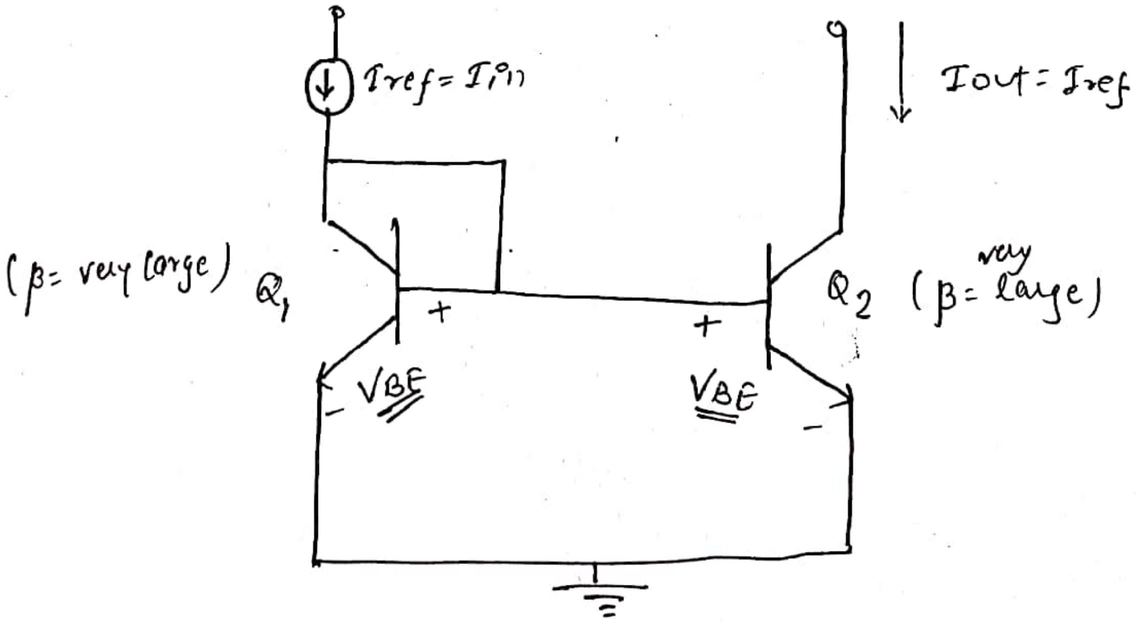


fig Basic ckt Diagram of C.M.C

Since the O/P current is mirror image of I/P curr
therefore ckt is referred as current mirror ck

Requirement of Current Mirror ckt :-

① Both Xsistors should be in Active Region

② Both Xsistors should be identical or perfectly matched

2.1) $V_{BE_1} = V_{BE_2} = V_{BE}$

2.2) $\beta_1 = \beta_2 = \beta$ (large)

2.3) $I_{B_1} = I_{B_2} = I_B$

2.4) $I_{C_1} = I_{C_2} = I_C$

③ Emitter Junction Area of both Xsistors should be Identical

$$\text{Area}[J_{E_1}] = \text{Area}[J_{E_2}]$$

Note :-

Reverse Sat. current, $I_0 \propto$ Area of J_E

$$I_E \propto I_0$$

$$I_E \propto \text{Area of } J_E$$

If there is no info. of Area of emitter junc^n then we assume identical Emitter & junc^n Area of both Xsistor

If $\beta \neq \infty$

$I_B \neq 0\,A$

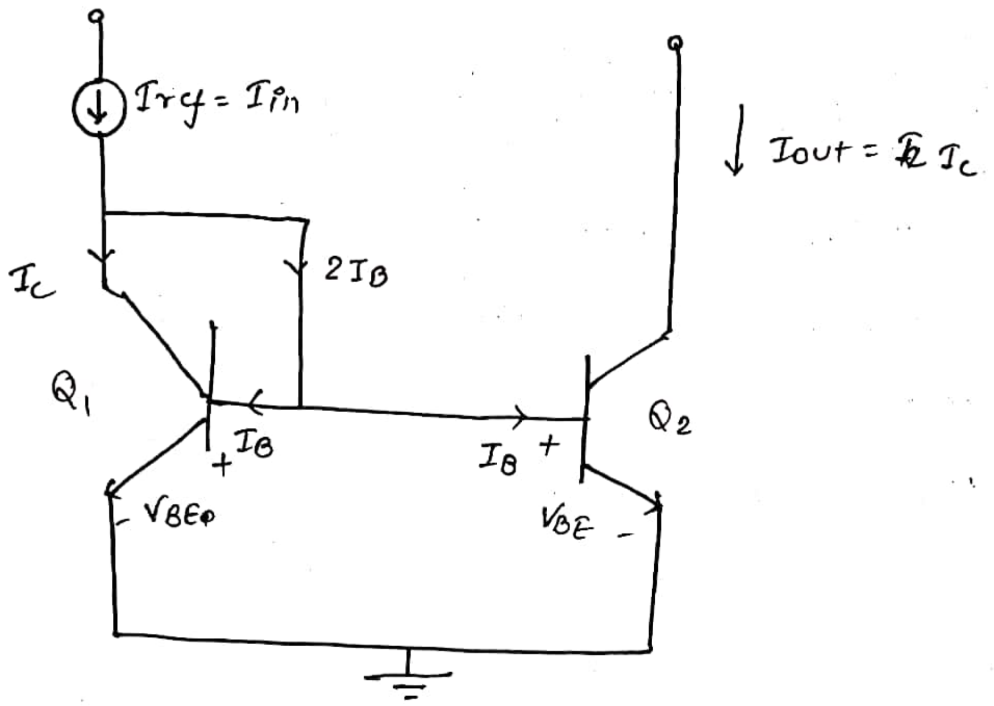


fig a)

From fig

$$I_{ref} = I_C + 2I_B$$

$$I_C(Q_1) = \beta I_B$$

$$I_{ref} = \beta I_B + 2I_B$$

$$I_{ref} = (\beta + 2)I_B$$

$$I_B(Q_2) = \frac{I_C}{\beta} = \frac{I_{out}}{\beta}$$

$$I_{ref} = (\beta+2)\frac{I_{out}}{\beta}$$

$$I_{out} = \left(\frac{\beta}{\beta+2}\right) I_{ref}$$

*** Imp

$$\boxed{I_{out} = \left(\frac{\beta}{\beta+2}\right) I_{ref}}$$

i) if $\beta = \infty$ then

$$I_{out} = I_{ref}$$

ii) if $\beta \rightarrow$ high

$$I_{out} \approx I_{ref}$$

Another form of Current Mirror ckts

P.T.O

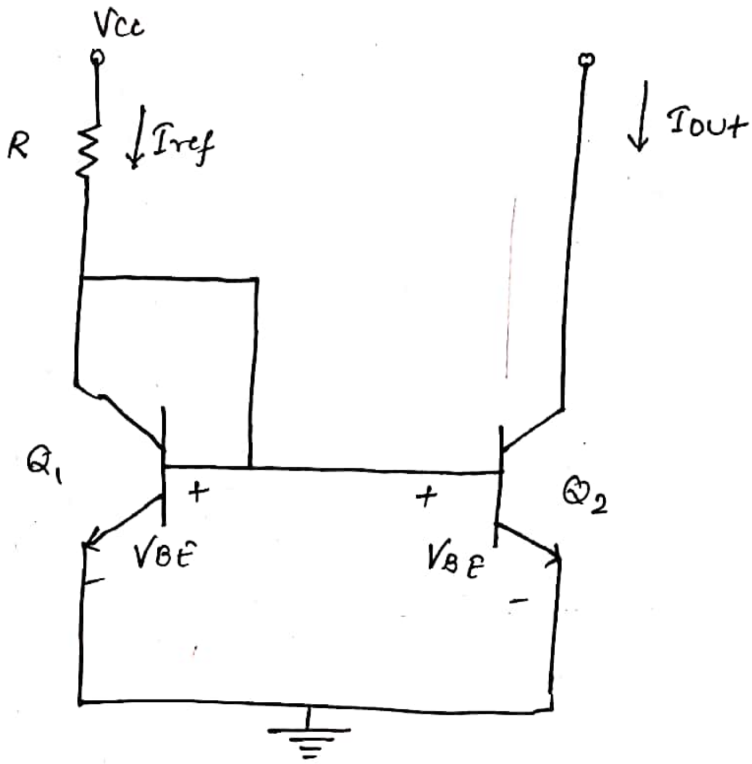


Fig b>

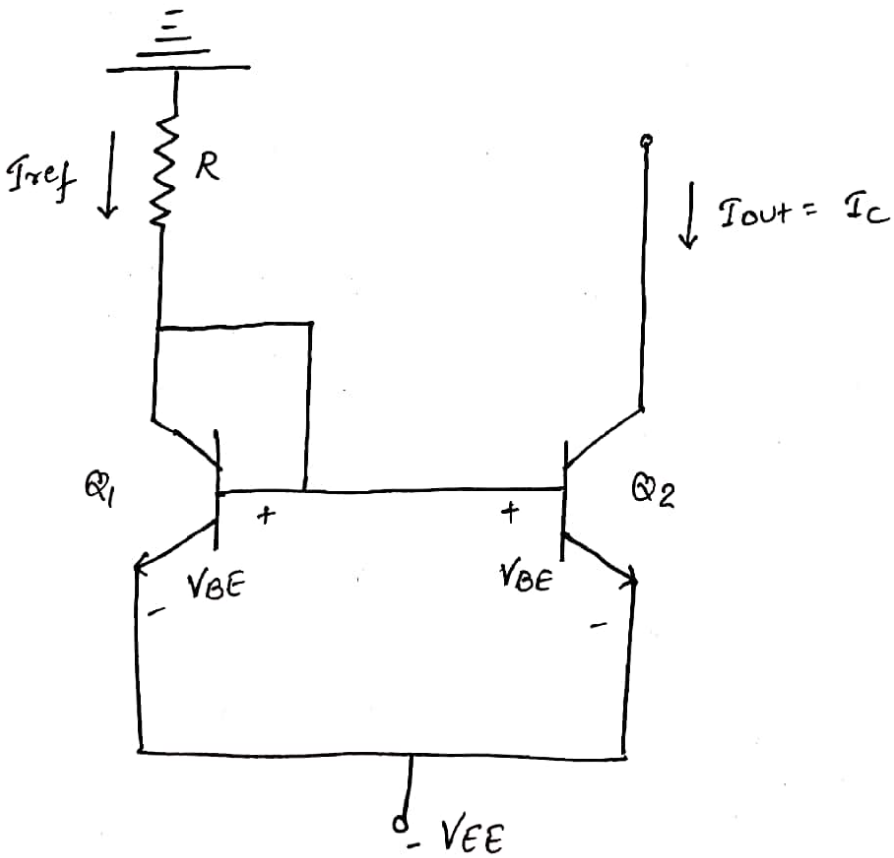


Fig c>

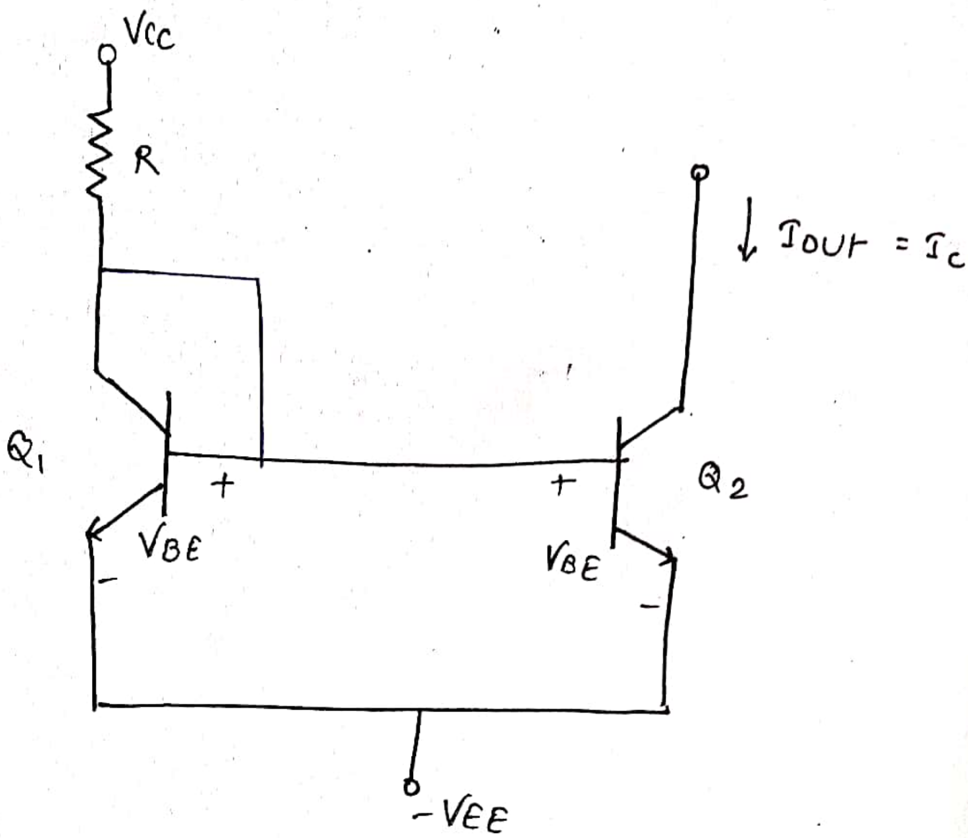


fig d>

from fig b> :-

$$V_{CC} = I_{ref} R + 0 + V_{BE} \quad \text{—} (1)$$

$$I_{ref} = \frac{V_{CC} - V_{BE}}{R}$$

$$I_{out} = \left(\frac{\beta}{\beta+2}\right) I_{ref}$$ Ans

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from fig c>

$$0 = I_{ref}R + 0 + V_{BE} - V_{EE}$$

$$I_{ref} = \frac{V_{EE} - V_{BE}}{R}$$

$$I_{out} = \left(\frac{\beta}{\beta+2}\right) I_{ref}$$

from fig d>

$$V_{CC} = I_{ref}R + 0 + V_{BE} - V_{EE}$$

$$I_{ref} = \frac{V_{CC} + V_{EE} - V_{BE}}{R}$$

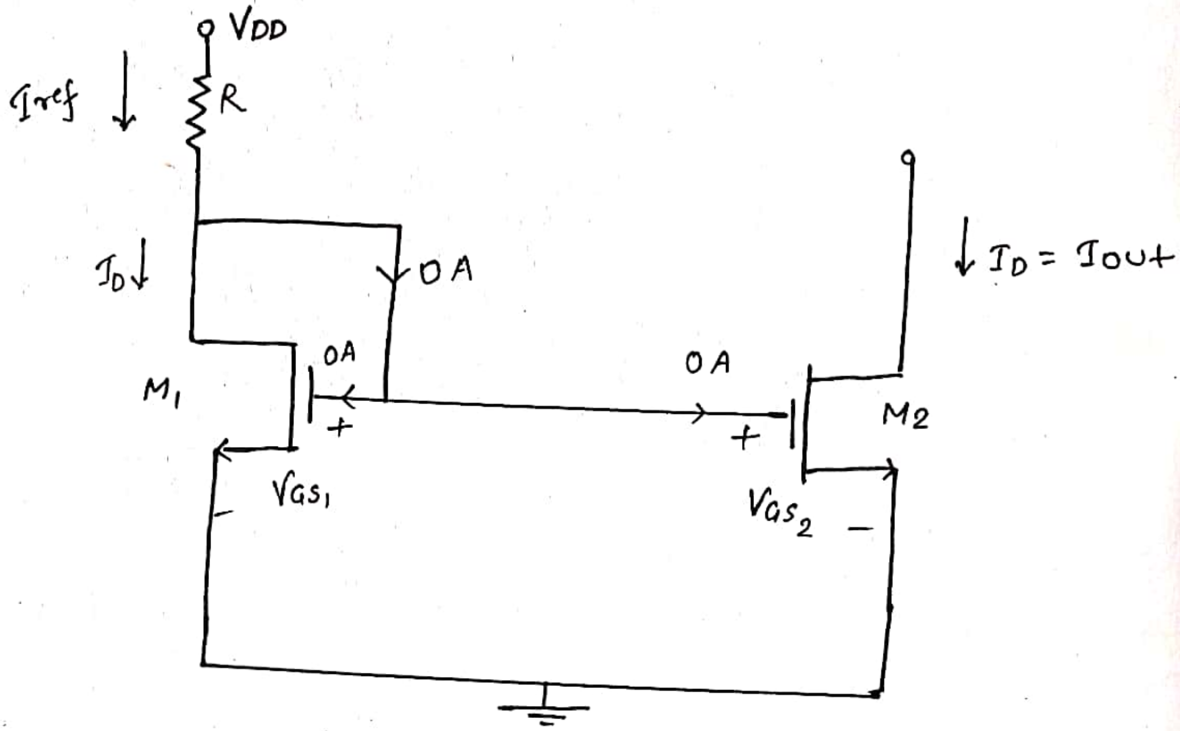
$$I_{out} = \left(\frac{\beta}{\beta+2}\right) I_{ref}$$

β	$I_{out} = \left(\frac{\beta}{\beta+2}\right) I_{ref}$
5	$0.714\ I_{ref}$
10	$0.83\ I_{ref}$
50	$0.96\ I_{ref}$

Conclusion:-

for small value of β I_{out} is not mirror image of I_{ref}

MOSFET CURRENT MIRROR CKT



when $V_{DG} = 0$ then

$V_{DS} > V_{GS} - V_{TN} = V_{OV}$

i.e NMOS → saturation Region.

M_1 = saturation Region

$I_{D1} = I_{D2}$

$I_{D1} = I_{out}$

$$k_{n1} \left[V_{GS1} - V_{TN1} \right]^2 = k_{n2} \left[V_{GS2} - V_{TN2} \right]^2$$

I_{D1} and I_{D2} are equal only if

i> $k_{n1} = k_{n2}$

ii> $V_{TN1} = V_{TN2}$

iii> $V_{GS1} = V_{GS2}$

$\Big\}$ then only $\boxed{I_{out} = I_{ref}}$

Operational Amplifier (Op-Amp)

1. Op-amp is a high gain DC amplifier (Direct Coupler Ampl^r) which can perform some mathematical operation like addition, substraction, multiplication, division, integration, differentiation, log, anti log etc.

2. Op-amp can amplify both DC and AC signal from 0 to 10^6 Hz.

*3. Op-amp is referred as Voltage Controlled Voltage Source device

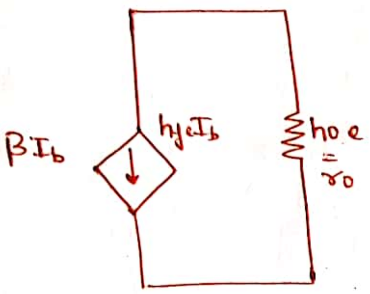


fig. BJT (CCCS)

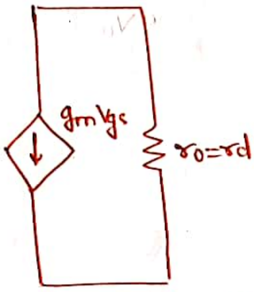


fig. JFET/MOSFET (VCCS)

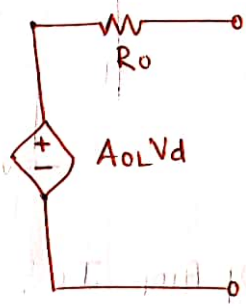


fig. Opamp [VCVS]

4. Symbolic Representation

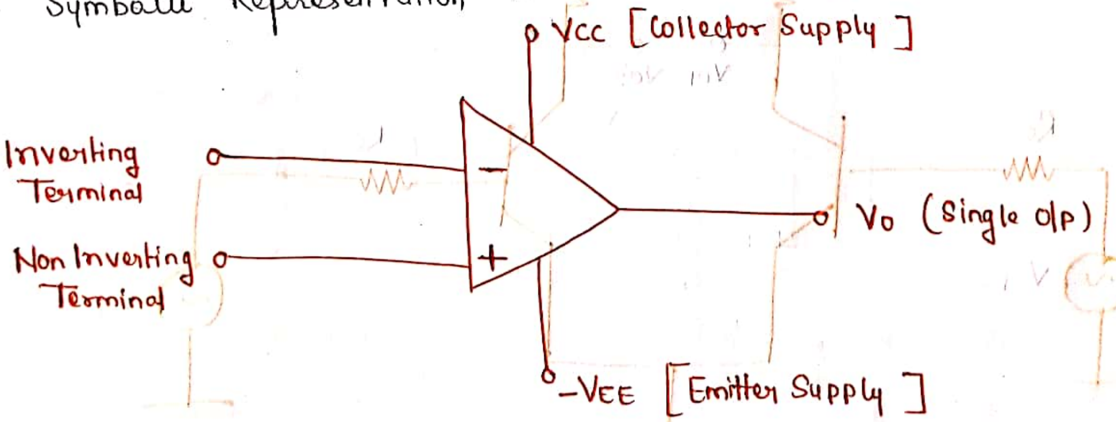


fig a. Unbalanced o/p (Single o/p) op-amp.

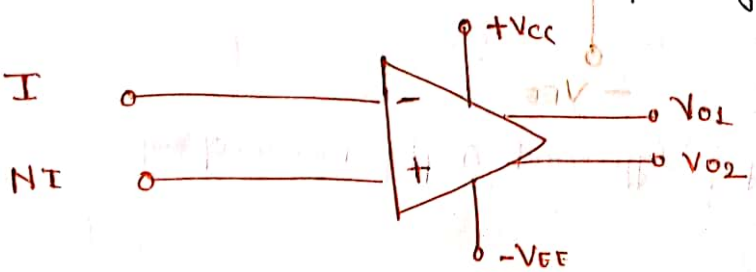


fig b. Balanced o/p (Two o/p) opamp.

If $|V_{cc}| = |-V_{EE}|$

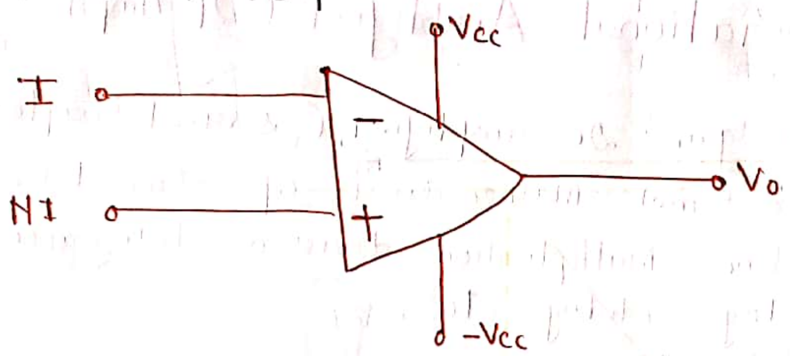
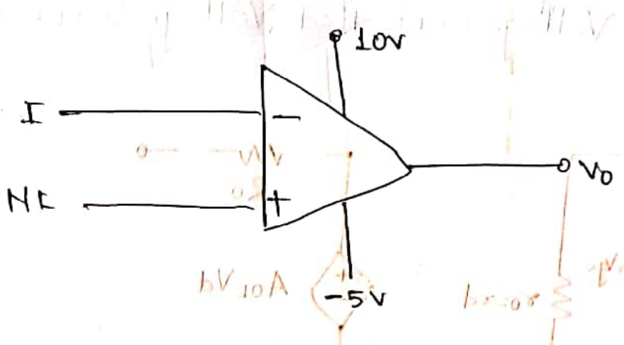


fig (c)

eg.



• Inside Op-Amp IC :

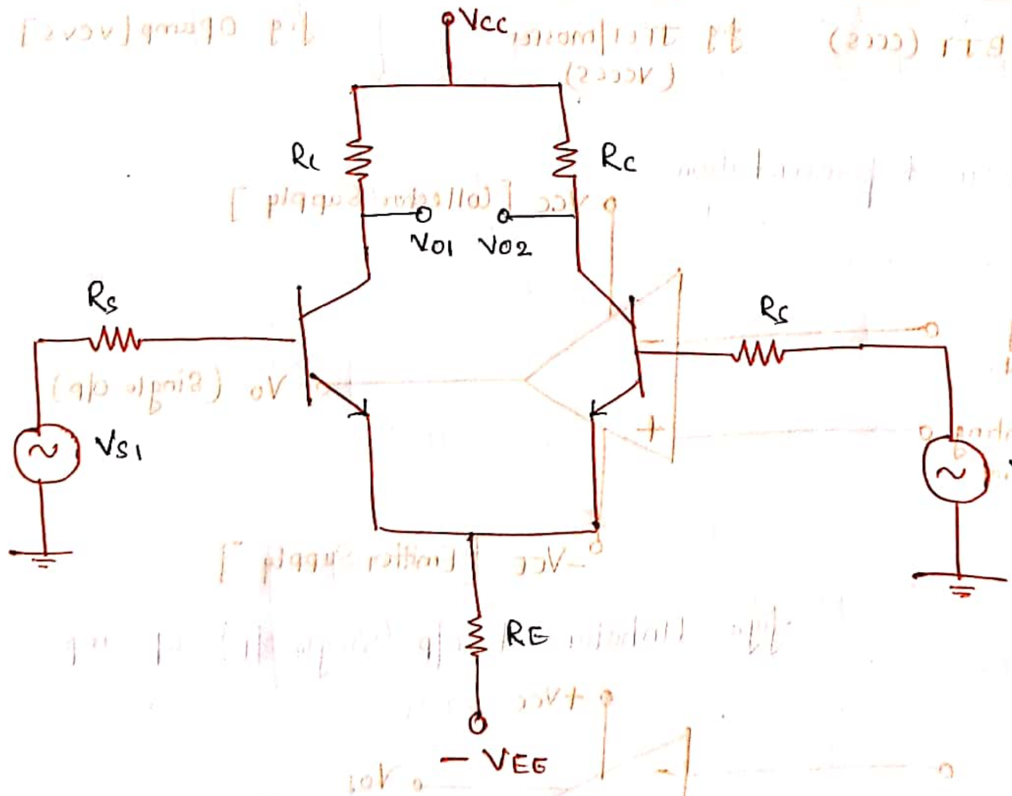
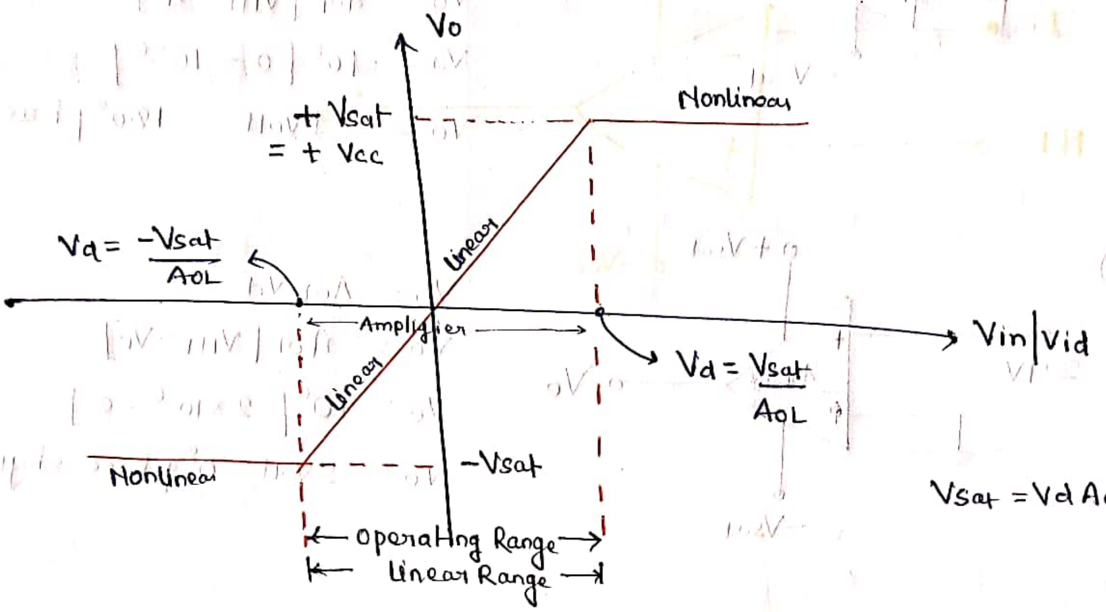


fig. differential Amplifier inside op-amp.

5: Transfer characteristic



$V_{sat} = V_d A_{OL}$

Maximum positive Output Voltage = $+V_{sat}$

Maximum Negative o/p Voltage = $-V_{sat}$

V_{in} = Input Voltage = $V_{NI} - V_I$

V_d = difference Voltage = $V_{NI} - V_I$

$V_{in} = V_d = V_{NI} - V_I$

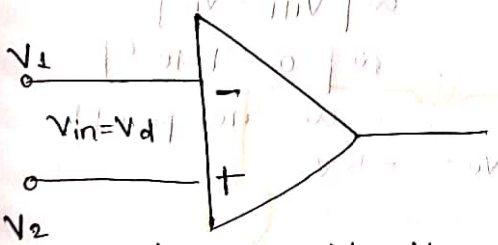


fig. $V_d = V_{NI} - V_I$

$V_d = V_2 - V_1$

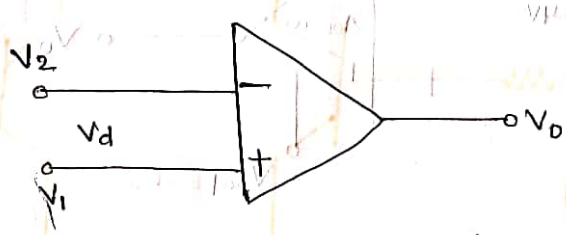


fig. $V_d = V_{NI} - V_I$

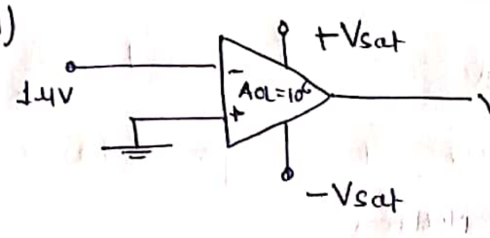
$V_d = V_1 - V_2$

$$\boxed{\frac{-V_{sat}}{A_{OL}} < V_d < \frac{V_{sat}}{A_{OL}}}$$

→ for operation in linear Region

→ above that Range Op-amp Saturates.

eg 1)



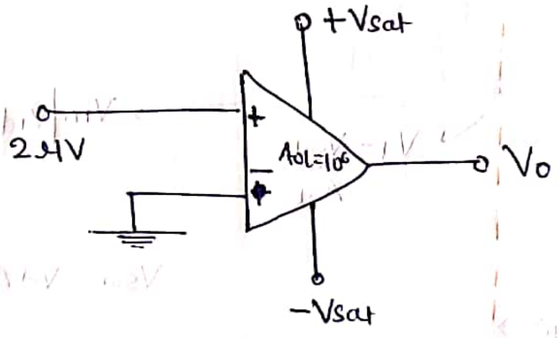
$V_o = A_{OL} V_d$

$V_o = A_{OL}[V_{NI} - V_I]$

$V_o = 10^6[0 - 10^{-6}]$

$V_o = -1\,\text{Volt}$ 180° phase shift

eg 2)



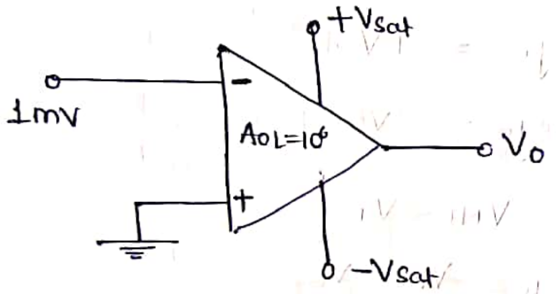
$V_o = A_{OL} V_d$

$V_o = A_{OL}[V_{NI} - V_I]$

$V_o = 10^6[2\times10^{-6} - 0]$

$V_o = 2\,\text{Volt}$ 0° phase shift

eg 3)



$V_o = A_{OL} V_d$

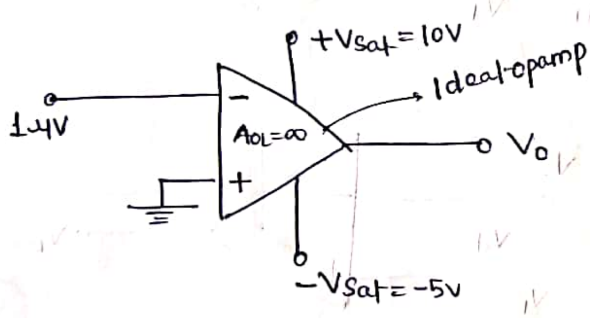
$V_o = A_{OL}[V_{NI} - V_I]$

$V_o = 10^6[0 - 1\times10^{-3}]$

$V_o = -1000\,V$ Not possible

$V_o = -V_{sat}$ 180° phase shift

eg 5)



$V_o = A_{OL} V_d$

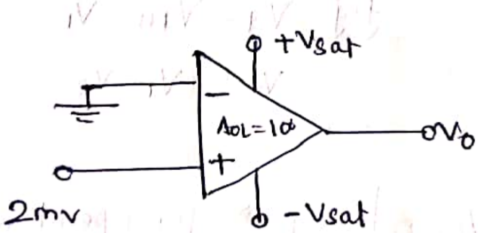
$= \infty[V_{NI} - V_I]$

$= \infty[0 - 1\times10^{-6}]$

$= -\infty$ not possible

$V_o = -5\,V$

eg 4)



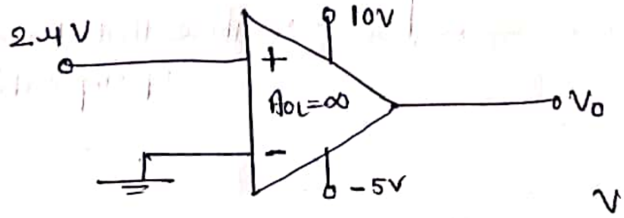
$V_{oL} = A_{OL}[V_{NI} - V_I]$

$= 10^6[2\times10^{-3} - 0]$

$= 2000$ Not possible

$V_o = +V_{sat}$

eg 6)



$V_o = A_{OL} V_d$

$= A_{OL}[V_{NI} - V_I]$

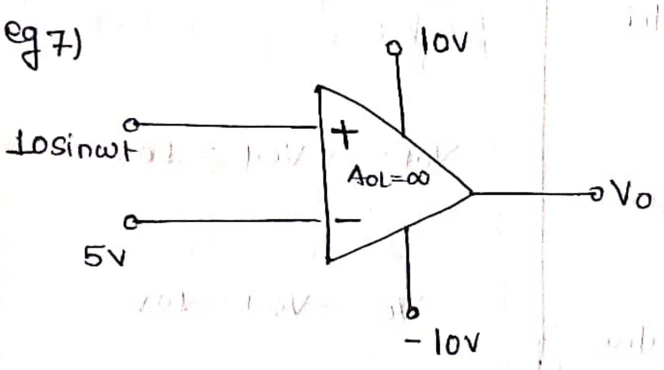
$= \infty[2\times10^{-6} - 0]$

$= \infty$ Not possible

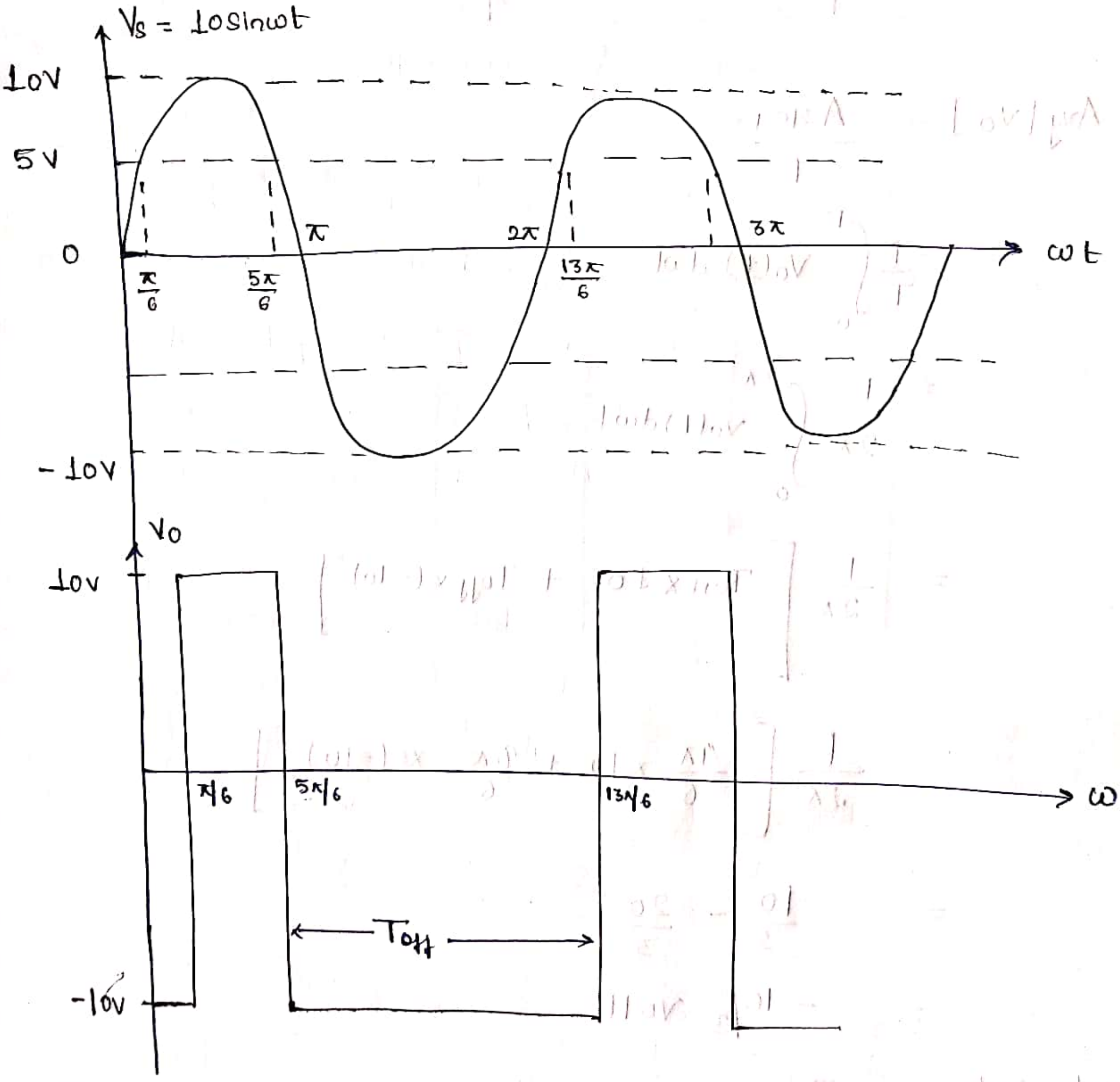
$V_o = 10V$

Key point:- If there is no Information of op-amp then by default we assume Ideal opamp that means $\boxed{A_{OL} = \infty}$.

eg 7)



Comparator Circuit



Time period of i/p = 2π

Time period of o/p = 2π

ωt	$V_d = V_{NI} - V_I$	$V_o = A_{OL} V_d$
$0 < \omega t < \pi/6$	$I > NI$ V_d = Negative	$V_o = -V_{sat} = -10V$
$\frac{\pi}{6} < \omega t < \frac{5\pi}{6}$	$NI > I$ V_d = Positive	$V_o = +V_{sat} = 10V$
$\frac{5\pi}{6} < \omega t < \frac{13\pi}{6}$	$I > NI$ V_d = Negative	$V_o = -V_{sat} = -10V$

$$Avg[V_o] = \frac{Area}{T}$$

$$= \frac{1}{T}\int_0^T V_o(t)\, d\omega t$$

$$= \frac{1}{2\pi}\int_0^{2\pi} V_o(t)\, d\omega t$$

$$= \frac{1}{2\pi}\left[T_{ON} \times 10 + T_{off} \times (-10)\right]$$

$$= \frac{1}{2\pi}\left[\frac{4\pi}{6} \times 10 + \frac{8\pi}{6} \times (-10)\right]$$

$$= \frac{10}{3} - \frac{20}{3}$$

$$= -10/3 \text{ Volt}$$

$$\text{Duty cycle} = \frac{T_{ON}}{T} \times 100\%$$

$$= \frac{T_{ON}}{T_{ON} + T_{OFF}} \times 100 = \frac{4\pi/6}{2\pi} \times 100 = 33.33\%$$

Note:

(i) $T_{on} < T_{off}$

$\% D < 50\%$

$Avg[V_o] =$ Negative

(ii) $T_{on} > T_{off}$

$\% D > 50\%$

$Avg[V_o] =$ positive

} Rectangular waveform

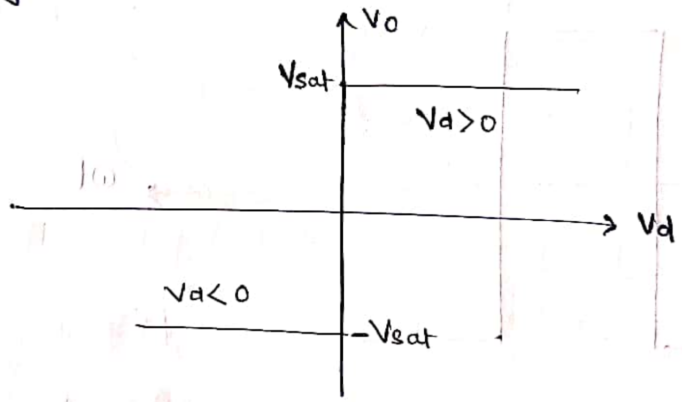
(iii) $T_{on} = T_{off}$

$\% D = 50\%$

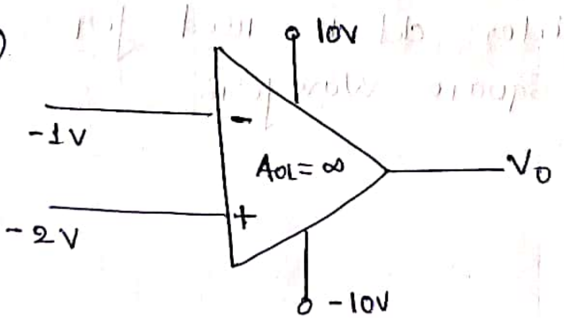
$Avg[V_o] =$ Zero

} Square Waveform

Transfer characteristic of Ideal opamp. (Comparator Circuit)



eg(8)



$V_o = A_{OL} V_d$

$= A_{OL}[-2+1]$

$= -\infty$

$V_o = -10V$

Sol $V_o = -10V$

$I > NI$

$V_o = -V_{sat} = -10$

eg (9)

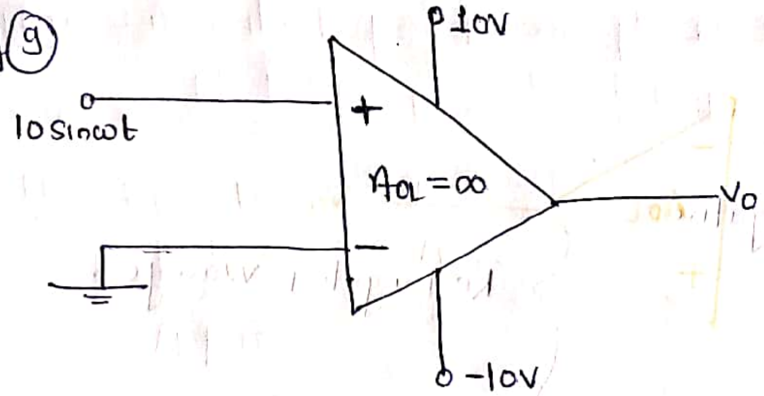
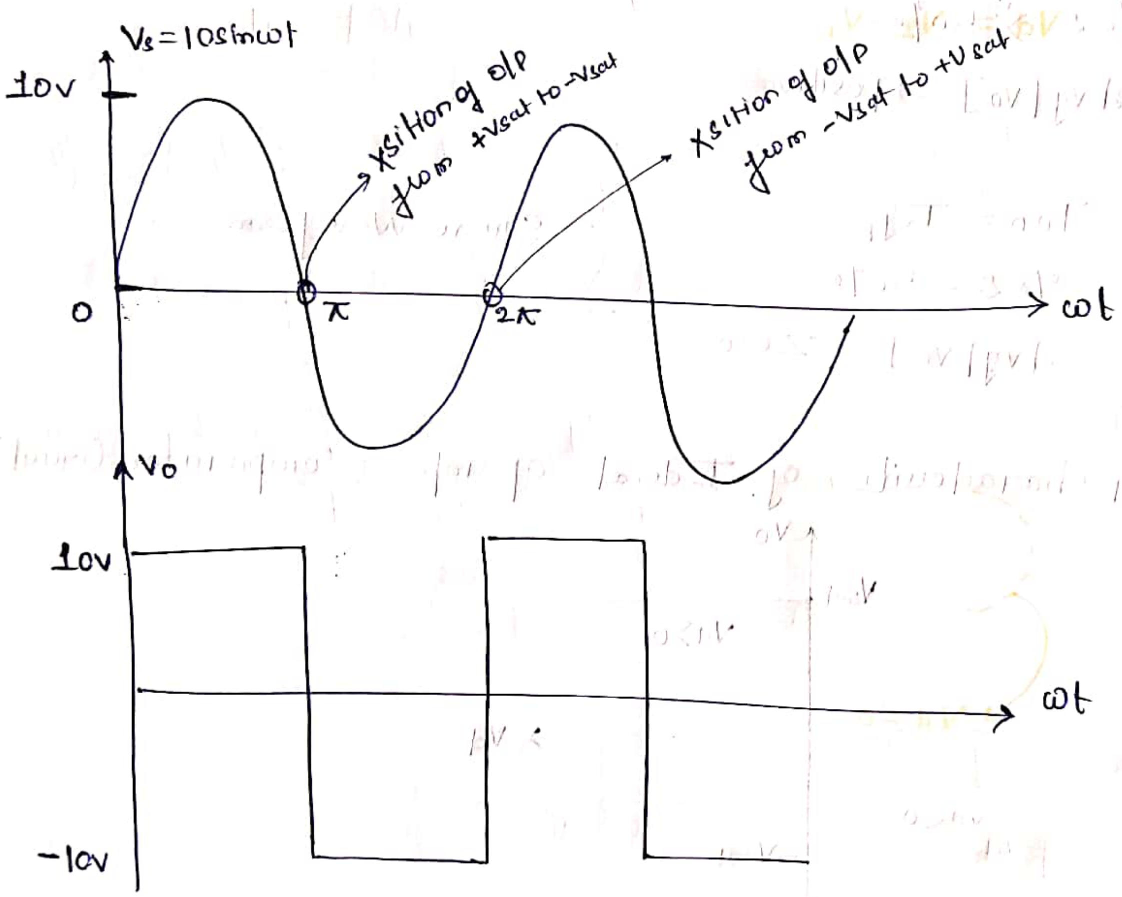
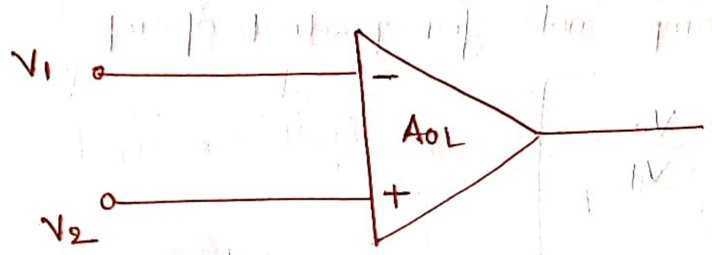


fig. Zero crossing detector



<u>Keypoint</u>: Zero crossing detector ckt is used for generation of square wave form.

* Virtual Ground Concept



$V_o = A_{OL} V_d$

$= A_{OL}[V_2 - V_1]$

$A_{OL} = \frac{V_o}{V_d}$

$V_d = V_2 - V_1$

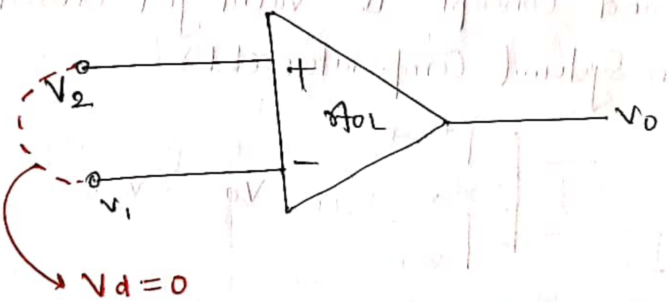
Ideal opamp :- $A_{OL} = \infty$

- $V_o = \infty$ (Not possible)
  $V_o = \pm V_{sat}$
- $V_d = 0$ (possible) ✓

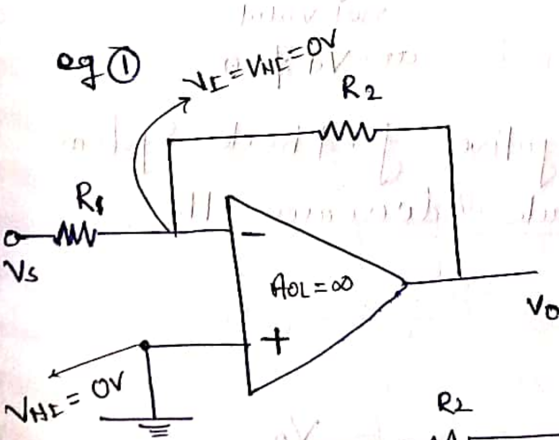
$V_d = 0$

$V_2 - V_1 = 0$

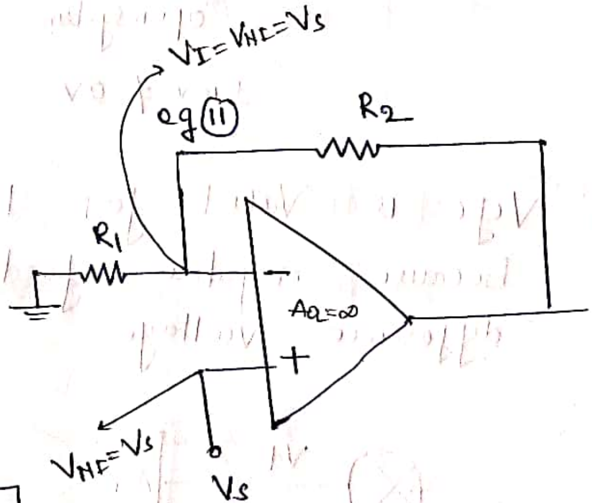
$V_2 = V_1$

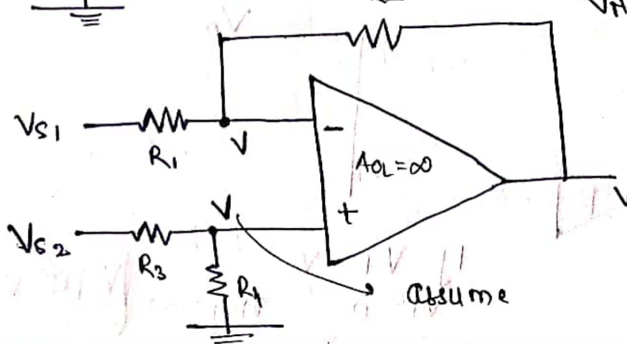


eg (i)



eg (ii)





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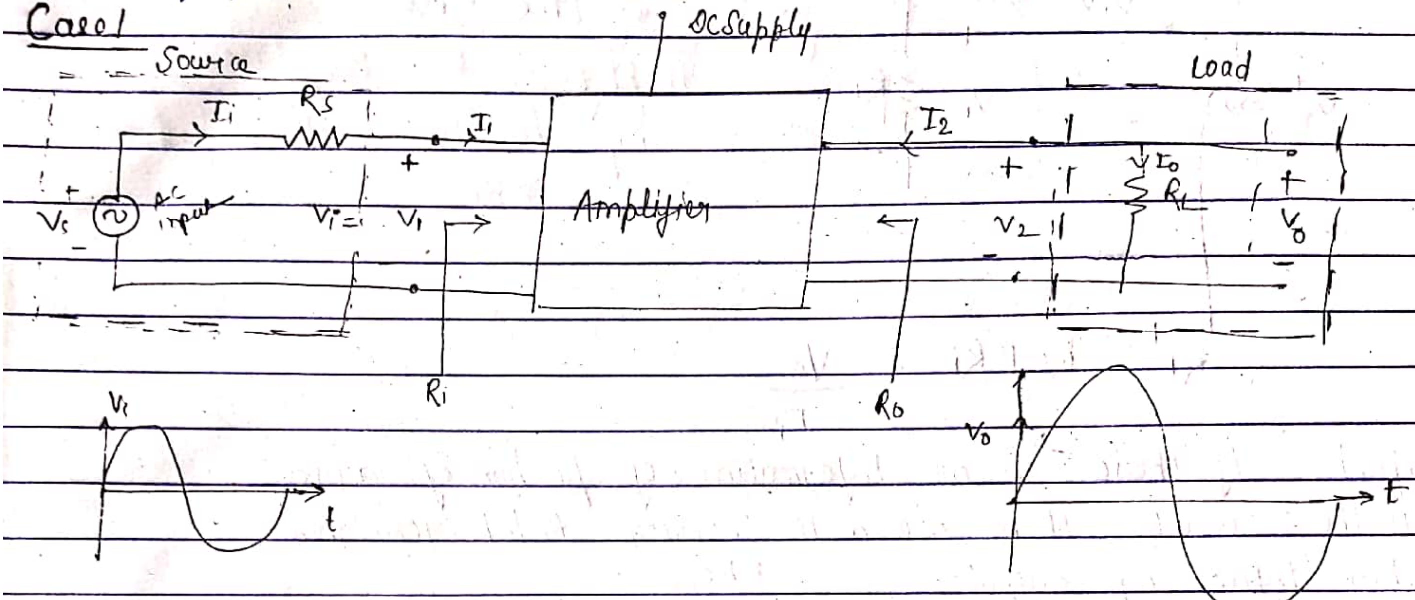
* Amplifier

Case I



- Amplifier is a device which Increases power level of Input Signal i.e. Amplification or Boosting of Input Signal.

- For amplifi^n we use mostly BJT, JFET & MOSFET.
- for amplifi^n device should be in proper region.
- for ampl^n BJT should be in active region.
- For ampl^n JFET & MOSFET should be in Saturation region.
- DC supply maintain the region of device for Ampl^n.
- Internal Input Impedence is given by:

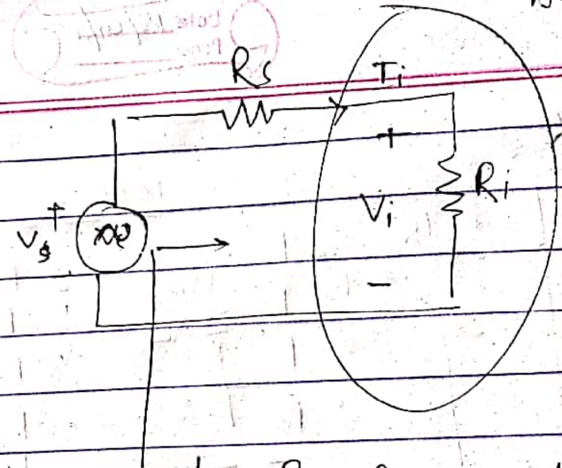
$$\boxed{R_i = \frac{V_1}{I_1}}$$

from fig. $R_i = \frac{V_i}{I_i}$

- Total Input resistance of Amplifier is given by (Input Resistance seen from the Source)

$$R_i' = \frac{V_s}{I_i} = R_s + R_i$$

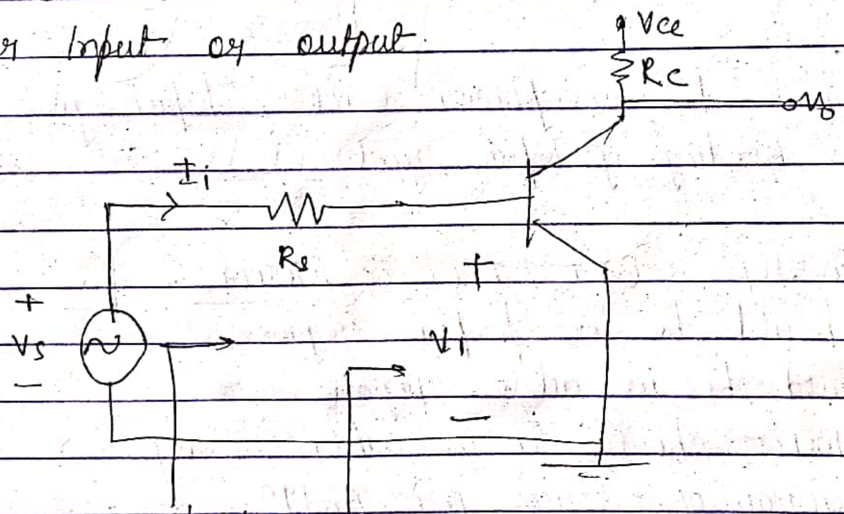
Amplifier



The whole Amplifier is Replaced by its Internal Input Impedence.

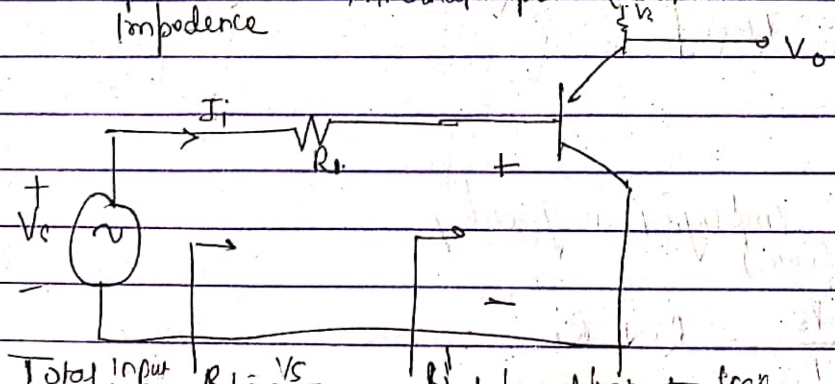
$$R_i' = R_s + R_i = \frac{V_s}{I_i}$$

Keypoint: If there is no Information of position of arrow in the circuit then we will Consider total resistance either Input or output.



$R_i' = \frac{V_s}{I_i}$ Total Input Impedence

$R_i = \frac{V_i}{I_i}$ Internal Input Resistance

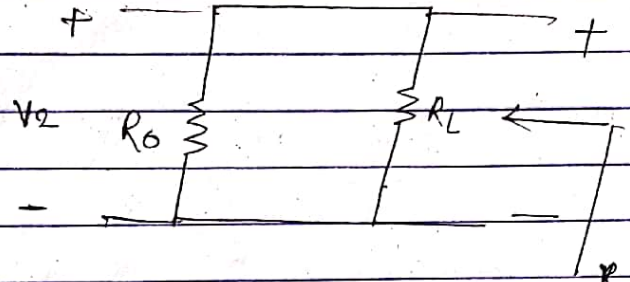


Total Input Imp. $R_i' = \frac{V_s}{I_i}$ R_i Internal Input Imp.

- Internal output resistance is given by

$$R_O = \left.\frac{V_2}{I_2}\right|_{V_s = 0} = R_{th} \text{ Thevenin Resistance}$$

- Total output resistance of Amplifier is given by



$R_O' = R_L \| R_O$

- Internal Voltage gain of Amplifier is given by

$$\boxed{A_V = \frac{V_2}{V_1} = \frac{\text{Internal output Volt}}{\text{Internal Input Volt}}}$$

from figure $V_2 = V_o$, $V_1 = V_i$

$$A_V = \frac{V_o}{V_i}$$

In o/p got case $V_2 = V_o$
(only dual of Miller theo. has $V_2 \neq V_o$)
but it is conventional question

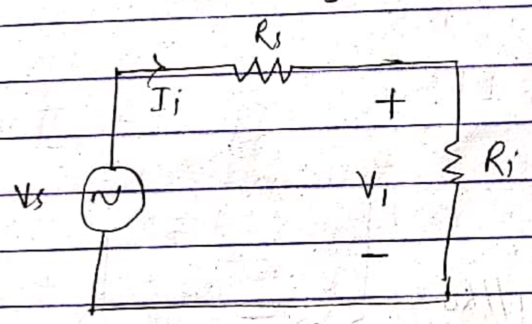
Overall Voltage gain or Total Volt gain of Ampl^r is given by

$$\boxed{A_{Vs} = \frac{V_o}{V_s} = \frac{\text{output Volt}}{\text{source Volt}}}$$

This Voltage gain is also refered as Voltage gain with source resistance.

$$A_{Vs} = \frac{V_o}{V_s} = \frac{V_o}{V_i} \times \frac{V_i}{V_s}$$

$$A_{Vs} = A_V \times \frac{V_i}{V_s}$$



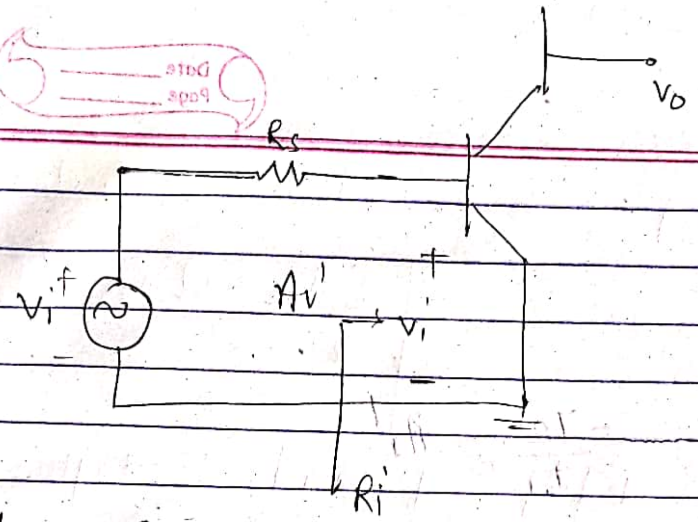
$$V_i = \frac{V_s R_i}{R_i + R_s}$$

$$\Rightarrow \frac{V_i}{V_s} = \frac{R_i}{R_i + R_s}$$

$$A_{Vs} = A_V \frac{R_i}{R_i + R_s}$$

$\boxed{A_{Vs} < A_V}$ $\left\{ \frac{R_i}{R_i + R_s} < 1 \right.$

Overall Voltage gain is always less than Internal Voltage gain.



$A_v = \frac{V_o}{V_i} = ?$ ~~Total internal volt gain~~

$A_v = A_v' \frac{R_i'}{R_i' + R_s}$

Practical Volt Source has Internal Resistance in Series which is Very Small

If $R_s = 0$

then V_s = Ideal Volt Source

$A_{vs} = A_v \frac{R_i}{R_s + R_i}$ $R_s = 0$

$\boxed{A_{vs} = A_v}$

$\boxed{A_{vs} \leq A_v}$

Internal Current gain of Amplifier is given by

$A_i' = \frac{-I_2}{I_1}$ where I_2 = output two port Current

I_1 = Input port Current

Overall Current gain is given by

$A_i = \frac{I_o}{I_i} = \frac{\text{Output Load Current}}{\text{Input Source Current}}$

from figure

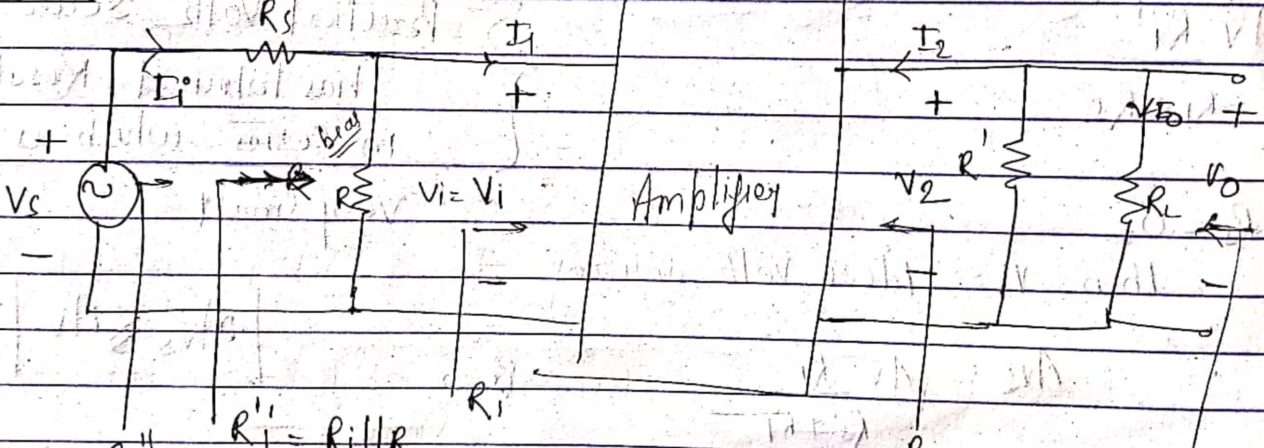
$I_o = -I_2$

$I_1 = I_i$

Overall current gain $= \frac{I_o}{I_1} = \frac{-I_2}{I_1} = A_I'$
A_I

Case II :-

$I_1 \neq I_i$

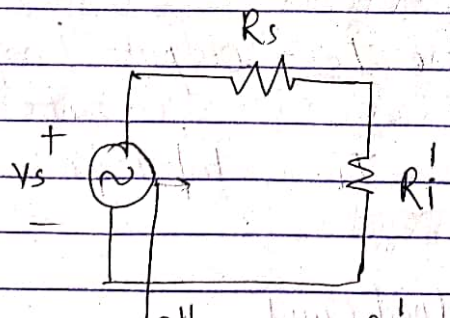


$R_i' = R_i \| R$

$R_i'' = R_i \| R + R_s$

$R_i'' = R_i' + R_s$

$R_o' = R' \| R_o \| R_L$



$R_i'' = R_s + R_i'$.

{There will be no series resistance in output}

- Internal Volt gain $A_V = \frac{V_o}{V_I} = \frac{V_o}{V_i}$

Total Volt gain $A_{VS} = \frac{V_o}{V_s} = \frac{V_o}{V_i} \cdot \frac{V_i}{V_s}$

$$A_{VS} = A_V \frac{V_i}{V_s}$$

$$A_{VS} = A_V \frac{R_i'}{R_i' + R_s}$$

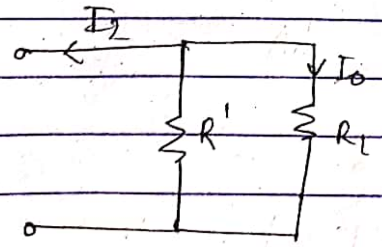
- If $R_s = 0$

$$A_{VS} = A_V = \frac{V_o}{V_i} = \frac{V_o}{V_s}$$

- Internal Current gain $A_I = \frac{-I_2}{I_1}$

Overall Current gain

$$A_{IS} = \frac{I_o}{I_i} = \frac{I_o}{I_2} \times \frac{I_2}{I_1} \times \frac{I_1}{I_i}$$

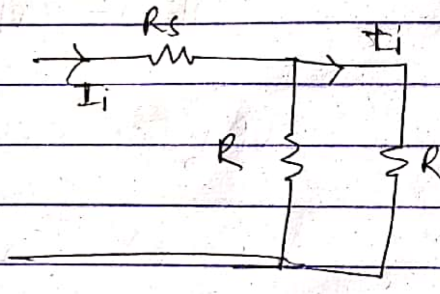


$$I_o = \frac{-I_2 R'}{R' + R_L}$$

$$\frac{I_o}{I_2} = -\frac{R'}{R' + R_L}$$

also $\frac{-I_2}{I_1} = A_I'$

and



$$I_1 = \frac{I_i R}{R + R_i}$$

$$\frac{I_1}{I_i} = \frac{R}{R + R_i}$$

So, total (overall current gain)

$$\boxed{A_{I} = -\left(\frac{R'}{R' + R_L}\right) \times (-A_I') \times \left(\frac{R}{R + R_i}\right)}$$

~~$A_I =$~~

$A_V[dB] = 20 \log_{10} A_V$

$A_I\,[dB] = 20 \log_{10} A_I$

$A_P[dB] = 10 \log_{10} A_P$