

## **GATE ESE 2020 TARGET ECE ENGINEERING**

## **GATE ESE PSU's 2019-20**

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### **105 EDC SYSTEM\_GATEACADEMY**

**TOTAL PAGE EDC SYSTEM-210 PGAE**

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#### **CONTENT COVERED:**

- 1. Theory Notes**
- 2. Explanation**
- 3. Derivation**
- 4. Example**
- 5. Shortcut & Formula Summary**
- 6. Previous year Paper Q. Sol.**

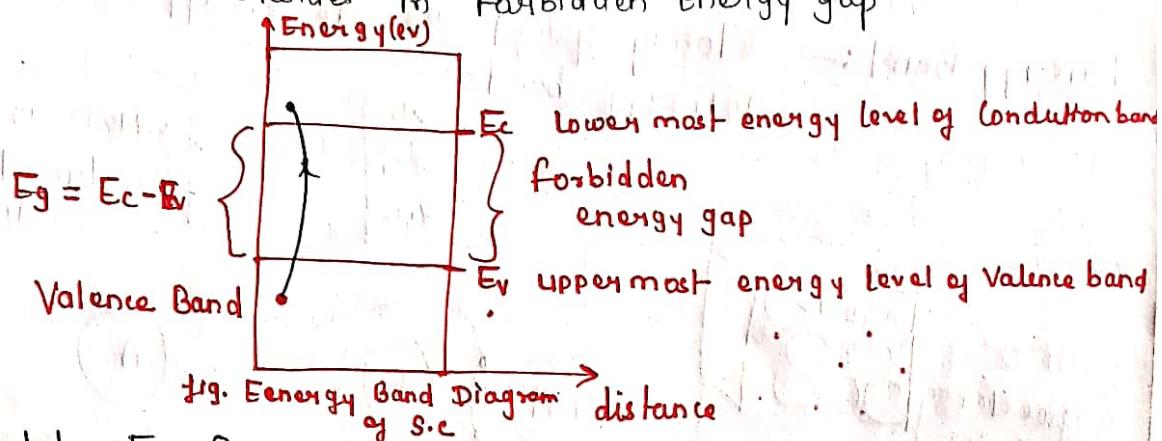
**Noted:- Single Source Follow, Revise**

**Multiple Time Best key of Success**

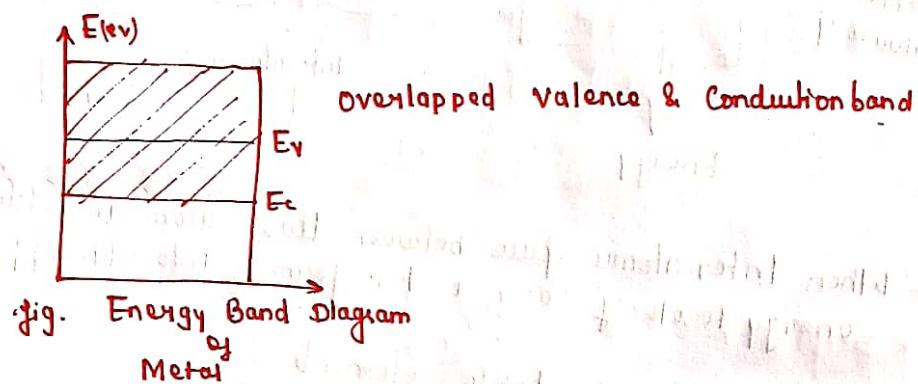
## Unit-1 Semiconductor Theory

①

- There is no allowable energy level in forbidden energy gap thus no electron resides in forbidden Energy gap.



- For Metal  $E_g = 0$



- For Insulator  $E_g = 6\text{ eV}$
- For Semiconductor  $E_g = 1\text{ eV}$  approximately.

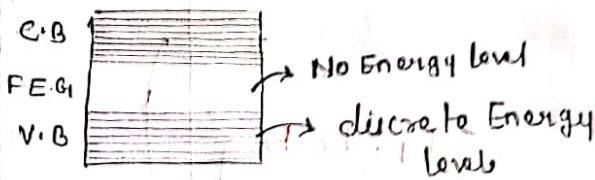
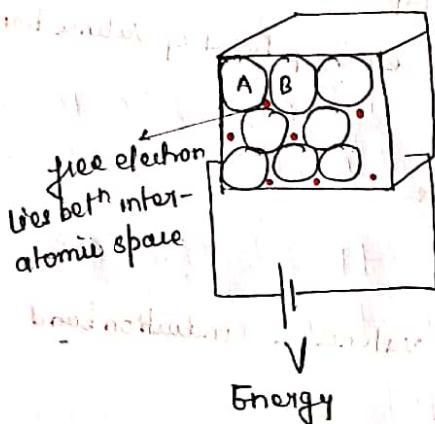
- Energy can be applied to electron by three ways-
  1. Electric field
  2. Temperature
  3. light

So that electron goes to Conduction band.

- In Semiconductor electron in Valence band can also help in conduction. Valence band electron are called bounded electron. when bounded electron left Valence band
- The Vacancy left in Valence band is known as holes.
- The absence of electron in Valence band is hole.

- Current Conduction in Semiconductor is due to free electrons & bounded electrons.

**Energy Band :-** Closely spaced discrete Energy levels is known as Energy band.



- When Inter atomic space between two atom is reduced then the energy levels of each is transformed into Energy band.

- 4th group periodic table elements

C - 6	
Pure S.C {	Si - 14 $1s^2 2s^2 2p^6 [3s^2 3p^2]$
	Ge - 32 $1s^2 2s^2 2p^6 3s^2 3p^6 [3d^{10} 4s^2 4p^2]$
Sn - 50	

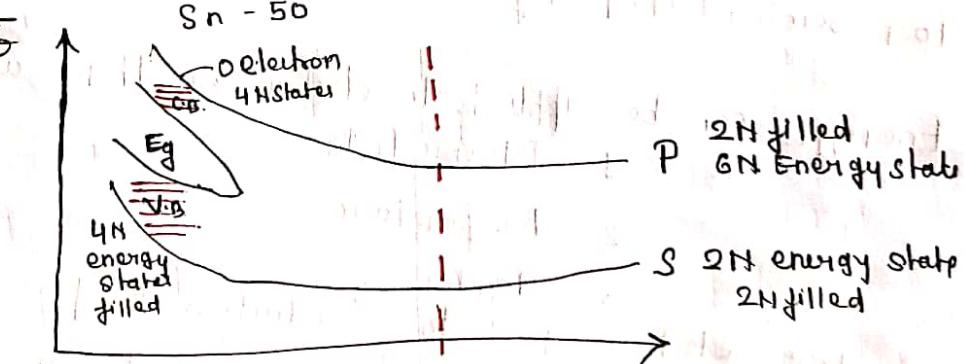
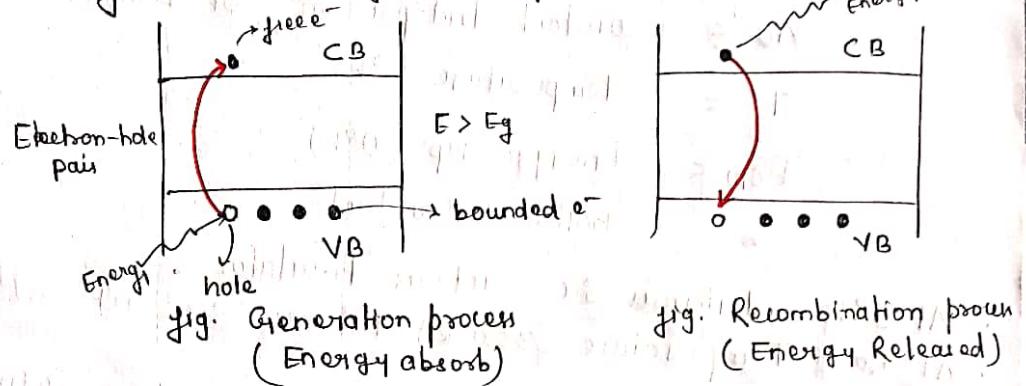


fig. Silicon Energy band diagram  
(4th group)

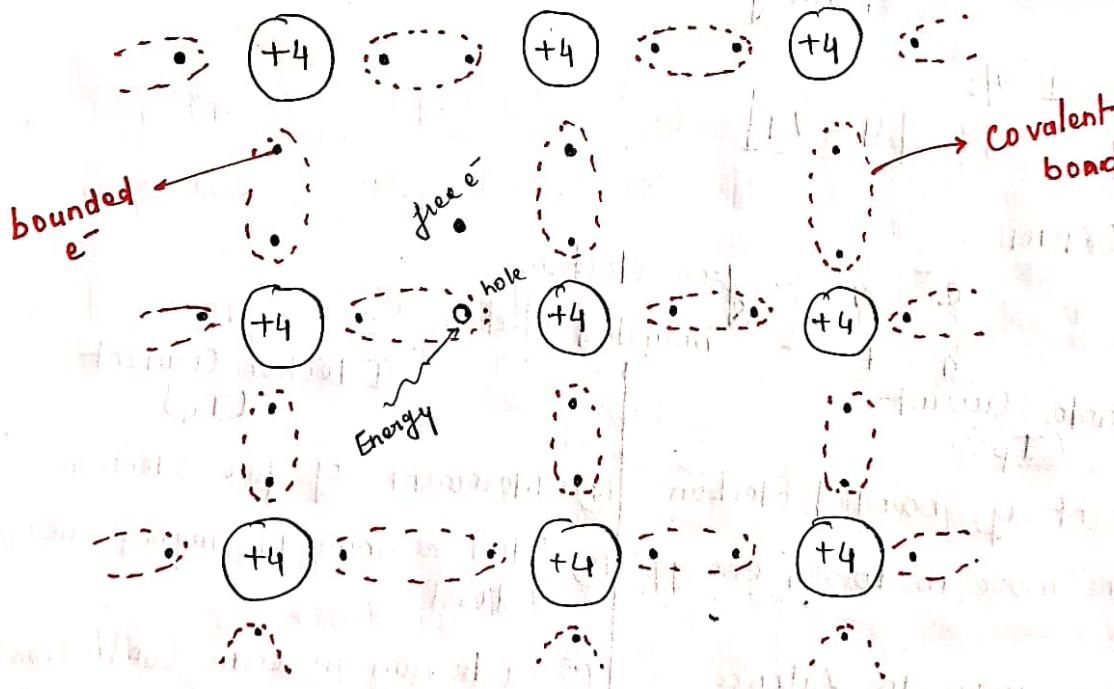
left  
Interatomic distance Reduce.

**Generation :-** Process of generating an electron-hole pair by providing certain amount of energy greater than  $E_g$ . In generation Energy is always absorb.



**Recombination :-** The process in which lose one electron-hole pair. The energy is released in form of heat or light (LEO) ( $\text{Si}, \text{Ge}$ )

\* Intrinsic Semiconductor (Si): A pure semiconductor is without doping



In an Intrinsic Semiconductor

$$\boxed{n = p} = n_i$$

where,  $n$  = no. of free electron

$p$  = no. of hole

$n_i$  = Intrinsic Concentration

$$n_i^2 = A_0 T^3 e^{-E_{GO}/kT}$$

$A_0$  = Constant Independent of temperature

$T$  = Temperature ( $^{\circ}\text{K}$ )

$E_{GO}$  = Energy Gap ( $0^{\circ}\text{K}$ )

$k$  = Boltzman Constant

• At  $0^{\circ}\text{K}$  Intrinsic S.c act as Insulator

• At Room Temperature ( $300^{\circ}\text{K}$ ) Intrinsic S.c act as Conductor.

→ Mobility: It can be defined as the drift velocity ( $V_d$ ) per unit applied electric field.

$$\mu = \frac{V_d}{E} \text{ Group A} \frac{\text{m}^2}{\text{volt}\cdot\text{sec}}$$

• Drift Velocity :- The Velocity of electron when external electric field is applied.

At  $E = \pm 1 \text{ v/s}$

$$\mu = V_d$$

• charge Carrier:

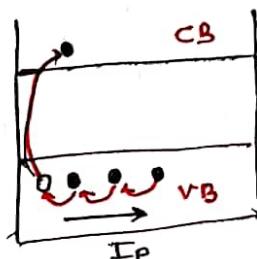
$e^- = n \rightarrow$  free electron

$h = p \rightarrow$  bounded electron

hole current  
( $I_p$ )

Electron Current  
( $I_n$ )

- ① Movement of bounded Electron
- ② Electrons move in lower energy level
- ③ Electrons move in Valence band.



- ① Movement of free electron.
- ② Electrons move in higher energy level.
- ③ Electron moves in Conduction band.

(4) The bounded electron is moving from one covalent bond to another covalent bond.

(4) The free  $e^-$  is moving in interatomic space.

(5)

In Intrinsic S.C

$$\eta = p \\ \text{but } I_n > I_p \quad (I_n \neq I_p)$$

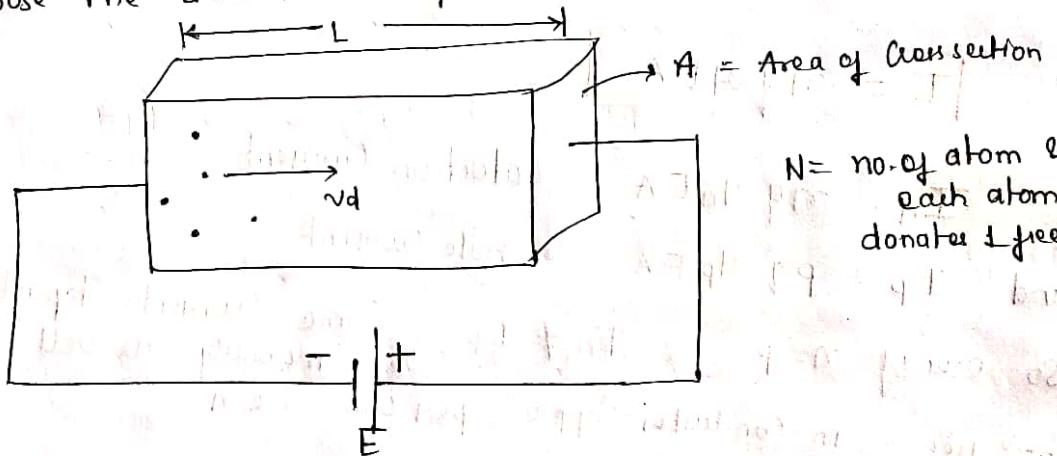
because Mobility of  $e^-$  is always greater than mobility of holes

$$M_n > M_p \\ \downarrow \\ e^- \quad \downarrow \text{due to bounded electron} \\ e^- \quad \downarrow \text{due to free}$$

• bounded  $e^-$  is always under the attraction force of covalent bond. Hence under a unit electric field the Velocity of free  $e^-$  is always greater than Velocity of bounded  $e^-$ .

### + Current Density of a Semiconductor:

Suppose the time taken by the  $e^-$  to cover distance  $L$  is  $T$



$N$  = no. of atom &  
each atom  
donates 1 free  $e^-$

$$I = \frac{Nq}{T}$$

$$\left( \because T = \frac{L}{v_d} \right)$$

$$\Rightarrow I = \frac{Nq v_d}{L}$$

Now, Current Density

$$J = \frac{I}{A} = \frac{Nq v_d}{AL}$$

$$J = nq v_d$$

$$\left\{ \begin{array}{l} \therefore \frac{N}{AL} = e^- \text{-density} \\ \text{or } (n) \\ e^- \text{-concentration} \\ n = \frac{\text{No. of } e^-}{\text{Volume}} = \frac{\text{no. of } e^-}{\text{cm}^3} \end{array} \right.$$

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when  $\eta q = \rho$  = charge density  
Coulomb/cm<sup>3</sup>

$$J = \rho V_d$$

By Ohms Law

$$J = \sigma E$$

$\sigma$  = Conductivity

$$J = \eta q \mu E$$

$$\left\{ \begin{array}{l} \\ \\ \end{array} \right. \quad V_d = \mu E$$

On Comparing.

$$\sigma = \eta q \mu$$

$$J = \frac{I}{A}$$

$$I = \eta q \mu E A$$

$$I_n = \eta q \mu_n E A$$

electron current

$$\text{and } I_p = \rho q \mu_p E A$$

hole current

so, even if  $\eta = \rho$ ,  $I_n \neq I_p$  Since current depends on mobility as well.

•  $10^{28}$  free e<sup>-</sup> in conductor approx per cm<sup>3</sup>. i.e n

•  $10^7$  free e<sup>-</sup> in insulator per cm<sup>3</sup>

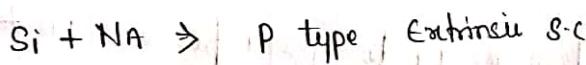
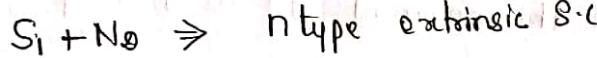
•  $10^{15}$  free e<sup>-</sup> in S.C

• To Increase the Conductivity of a Semiconductor the concentration of free e<sup>-</sup> has to be increased by a process called doping. The material used for doping is known as dopant.

pure Semiconductor + Doping = Extrinsic Semiconductor

\* Extrinsic Semiconductor: Adopted Semiconductor is called Extrinsic S.C.

	hole P	free e-	
	3 <sup>rd</sup>	4 <sup>th</sup>	5 <sup>th</sup>
Boron	B	Si	P
Aluminum	A	Ge	A
Gallium	G		A
Indium	I		B
Acceptor atom		Donor Atom	
Na		No	



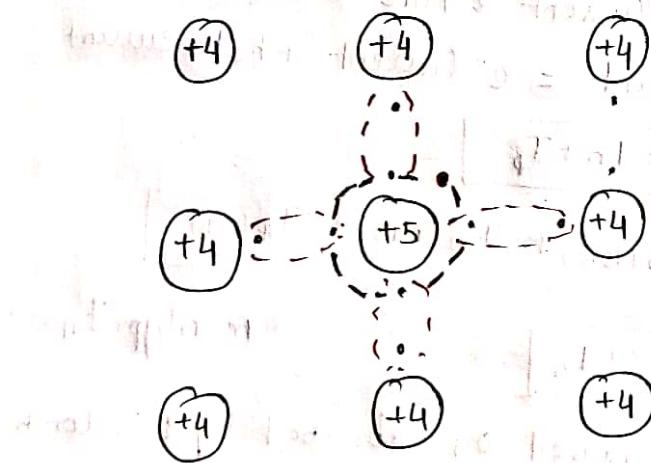
④ : Donor atom

④ : Donor ion

④ → positive ion

Normal Doping: 1 atom in  $10^8$  atoms  
(Dopant) (Si)

\* N type S.C :-



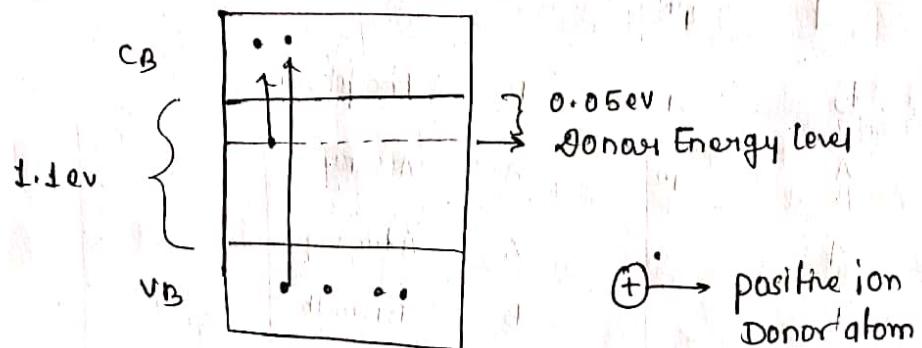
Majority charge carrier e<sup>-</sup>

Minority charge carrier hole

Majority current I<sub>n</sub>

Minority current I<sub>p</sub>

## Energy band diagram



An Intrinsic or Extrinsic S.C both are electrically neutral.

- If  $e^-$  from Donor energy level move to Condn band then no hole is created. and this movement is called Impurity Ionization.
- Impurity Ionization require less energy to give a free  $e^-$  in Val. Condn band.
- Process of movement of  $e^-$  from  $V_B$  to  $C_B$  is called Band to Band transition.
- Band to Band excitation always give LHe pair.

N-type S.C Two type of current & hole current

$$\text{Total Current} = e^- \text{ current} + \text{hole current}$$

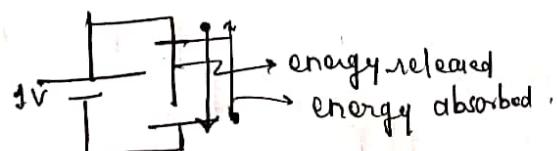
$$I = I_n + I_p$$

$$I = I_{n(BB)} + I_{A(TT)} + I_{p(BB)}$$

$$I \approx I_n$$

n type  $I_n \gg I_p$

Jov- Jov is a energy released or absorbed by 1 Coulomb charge to travel a volth difference of 1V



$$P'(0) = 10^{17} \times 10^{-4} = 10^{13} \text{ cm}^{-1} \quad \text{Eq 1}$$

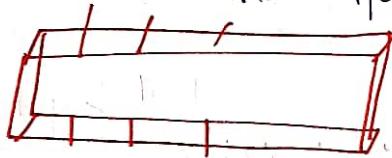
$$L_P = \sqrt{\Delta P Z_P}$$

$$L_P = \sqrt{100 \times 10^{-4}} = 0.1$$

$$J_P = -1.6 \times 10^{-19} \times 100 \times \frac{10^3 - 0}{0 - L}$$

$$= -1.6 \times 10^{-19} \times 100 \times \frac{10^3}{-0.1 \times 10^{-4}}$$

$$= 16 \text{ Amp/cm}^2$$

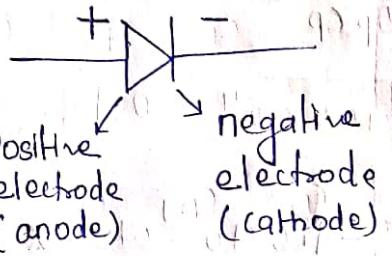


**current & Current density. Same**

## Unit-2

### P-n Junction Semiconductor Diode

Di → Two  
ode → Anode      } electrode  
          Cathode



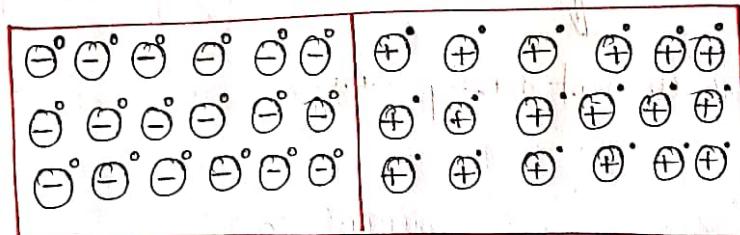
PN Diode Can be used as -

Special Diode  
→ Zener  
→ Tunnel diode  
Voltage Regulator  
Mains

- Switch - ON  
OFF
- VVC Voltage Variable Capacitor

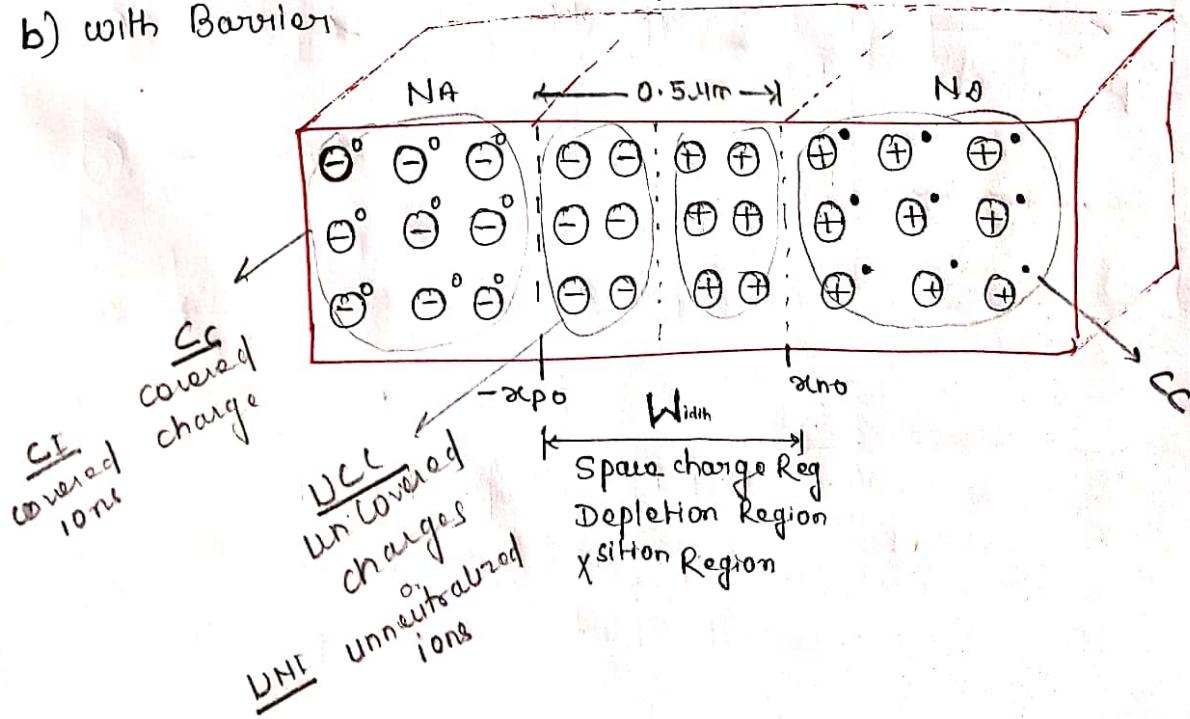
#### \* Open Circuited Diode

a) without Barrier



open circuit  
Electric field  
 $E_0, V_0$   
open circuit  
Voltage

b) with Barrier



$x_{no}$  is penetration of depletion Region into n side.

$x_{po}$  is penetration of depletion Region into p type.

$E_0$  is open circuited electric field

$V_0$  is open circuited potential or voltage (i.e without Biasing)

$$V_0 = kT \ln \left( \frac{N_D N_A}{n_i^2} \right) \quad \text{--- (1)}$$

$$E_0 = -\frac{q N_D x_{no}}{\epsilon} = -\frac{q N_A x_{po}}{\epsilon} \quad \text{--- (2)}$$

$$N_D x_{no} = N_A x_{po} \quad \text{--- (3)}$$

$$W = x_{no} + x_{po} \quad \text{--- (4)}$$

$$x_{no} = \frac{W N_A}{N_A + N_D} \quad \text{--- (5)}$$

$$x_{po} = \frac{W N_D}{N_A + N_D} \quad \text{--- (6)}$$

$$W = \sqrt{\frac{2 \epsilon V_0}{q N_A N_D} \left[ \frac{1}{N_D} + \frac{1}{N_A} \right]} \quad \text{--- (7)}$$

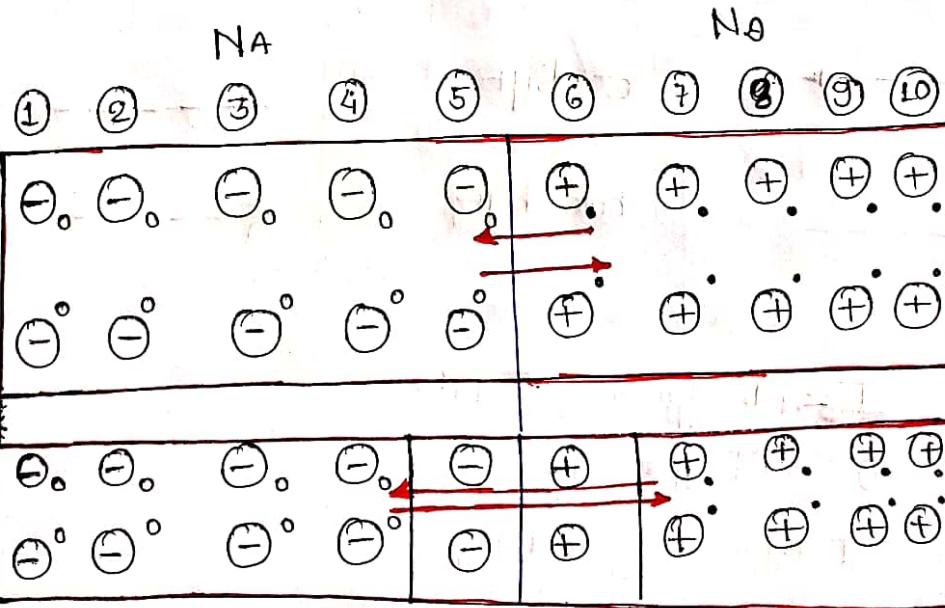
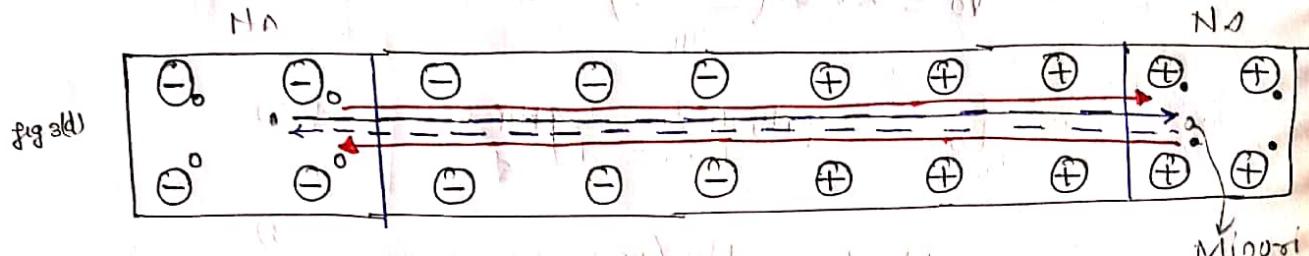
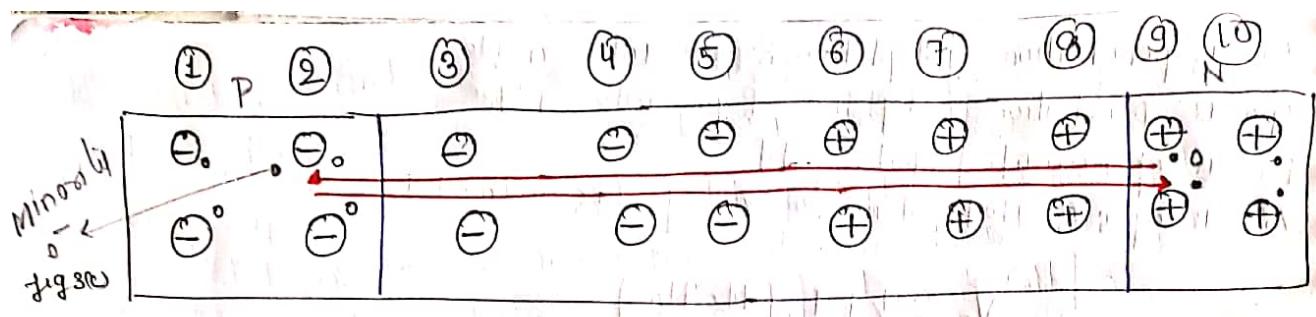


fig 39

fig 3b



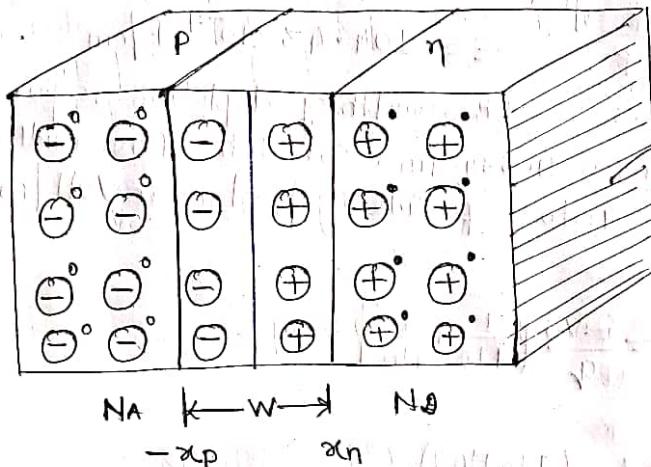
- As diffusion continues opposition to further diffusion increases charge due past diffusion creates ions at the centre which (hole) oppose present diffusion and hence at an instant diffusion stops.
- Barrier opposes the flow of Majority charge carrier but assist the flow of Minority charge carrier.

Direction of flow of charge carrier	Type	Direction of current
① ←	e <sup>-</sup> diffusion	→ { X }
② →	Hole diffusion	→
③ - - - →	e <sup>-</sup> drift	← { Y }
④ ← - - -	hole drift	← - - -

$$I = I_{\text{diffusion}} + I_{\text{drift}}$$

$$0 = I_{\text{diffusion}} + I_{\text{drift}}$$

$$I_{\text{diffusion}} = -I_{\text{drift}}$$



$$W = xn - (-xp)$$

$$W = xn + xp$$

No. of negative charges on p side      = No. of positive charges on inside

$$\rho A \propto p$$

$$\rho A \propto n$$

$$NA \propto A \propto p$$

$$NO \propto A \propto n$$

$$\textcircled{i} \text{ If } NA = NO \Rightarrow xp = xn$$

$$\textcircled{ii} \text{ If } NA > NO \Rightarrow xn > xp$$

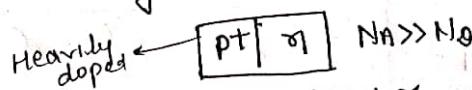
$$\textcircled{iii} \text{ If } NA < NO \Rightarrow xn < xp$$

- Depletion Region penetrates equally into p & n side for equal doping. It penetrates unequally for unequal doping.

(a) P

- Depletion region penetrates more into lightly doped side

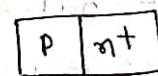
- penetration of Depletion Region into a heavily doped side. Can be neglected in a Single Sided pN Diode.



$$xn_0 \gg xp_0$$

$$W = xp_0 + xn_0$$

$$W \approx xn_0$$



$$NO \gg NA$$

$$xp_0 = \frac{WN_0}{N_A + N_0} \approx \frac{WN_0}{N_0}$$

$$xp_0 \approx W$$

Q1 For a PN diode given

$$N_D = 10^{16} \text{ cm}^{-3}$$

$$\epsilon = 104.43 \times 10^{-4} \text{ F/cm}$$

$N_A = 4 \times 10^{18} \text{ cm}^{-3}$  The width of depletion region under open circuit condition is  $0.334 \mu\text{m}$ . Calculate the width of depletion region into p side. Find  $E_0 \text{ in Volt/m}$ .

Sol

$$W = \sqrt{\frac{2 \epsilon V_0}{q} \left[ \frac{1}{N_D} + \frac{1}{N_A} \right]}$$

$$V_0 = kT \ln \left( \frac{N_D N_A}{n_i^2} \right)$$

$$0.334 \times 10^{-4} = \sqrt{\frac{2 \epsilon V_0}{q} \left[ \frac{1}{N_D} + \frac{1}{N_A} \right]}$$

$$\alpha_{p0} = \frac{N_D W}{N_D + N_A}$$

$$= \frac{10^{16} \times 0.334 \times 10^{-4}}{10^{16} + 4 \times 10^{18}}$$

$$= 8.329 \times 10^{-8} \text{ cm}$$

$$= 8.329 \times 10^{-10} \text{ m}$$

$$= 8.329 \text{ } \textcircled{A}$$

$$E_0 = -q N_A \times 8.329 \times 10^{-8}$$

$$= -5.104 \times 10^{-6} \text{ V/cm}$$

$$= -5.1 \times 10^{-6} \times 10^{+2}$$

$$= -5.1 \times 10^{-4} \text{ N/m}$$

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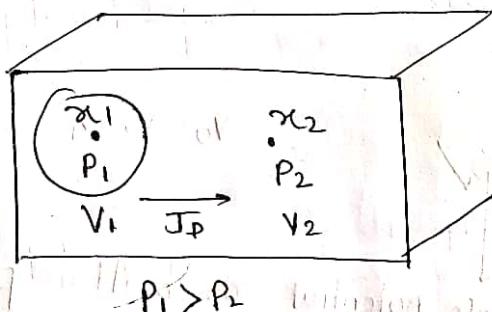
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- \* Consider a non-uniformly doped Semiconductor in which the concentration of holes at  $x_1 = P_1$  and the corresponding voltage is equal to  $V_1$ .
- Similarly at point  $x_2$  the concentration of hole is  $P_2$  and corresponding voltage is  $V_2$ .
- Since the conc. difference between two points in a Semiconductor give rise to diffusion Current between the points ( $x_1 \& x_2$ ) and the net current inside a Semiconductor which is open circuited should be equal to zero. That implies a drift current must be existing between two points  $x_1 \& x_2$ . for drift current to exist there must be a potential difference between the point  $x_1 \& x_2$ . This potential difference must be denoted by  $V_1 \& V_2$  & corresponding electric field represented by  $E$ .



$$I = I_{\text{diff}} + I_{\text{drift}}$$

$$0 = I_{\text{diff}} + I_{\text{drift}}$$

$$I_{\text{diffusion}} = -I_{\text{drift}}$$

$$+ q \frac{\partial p}{\partial x} A = + pq \mu_p E A$$

$$\mu_p E A = \frac{\partial p}{\partial x}$$

$$E = \frac{\partial p}{\mu_p \frac{dP}{dx}} \frac{1}{P}$$

$$E = V + \frac{dP}{dx} \frac{1}{P}$$

$$E = V_T \frac{dP_1}{dx} \cdot \frac{1}{P_1}$$

$$\Rightarrow -\frac{dV}{dx} = V_T \frac{dP}{dx} \cdot \frac{1}{P}$$

Integrating w.r.t Both sides

$$-\int_{V_1}^{V_2} dv = V_T \int_{P_1}^{P_2} \frac{dP}{P}$$

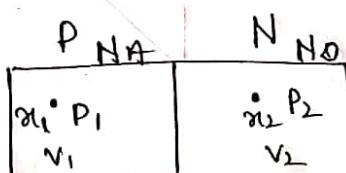
$$\Rightarrow -(V_2 - V_1) = V_T \ln \frac{P_2}{P_1}$$

$$\Rightarrow V_2 - V_1 = V_T \ln \frac{P_1}{P_2}$$

$$V_0 = V_2 - V_1 = V_T \ln \frac{P_1}{P_2}$$

where,  $V_0$  is Contact difference potential or built-in potential  
Built-in  $\rightarrow$  generated inside

Consider a diode



$P_p = P_1 = N_A =$  Majority Carriers

$P_n = P_2 = \frac{n_i^2}{N_D} =$  Minority Carriers

$$V_0 = V_2 - V_1 = V_T \ln \frac{P_1}{P_2}$$

$$V_0 = V_T \ln \frac{N_D N_A}{n_i^2}$$

Q. For a pN diode calculate change in contact potential if doping on n side is increased by factor of 1000 & doping on p side is unaffected.

$$\text{Sol} \quad V_{O1} = V_t \ln \frac{N_0 N_n}{n^2}$$

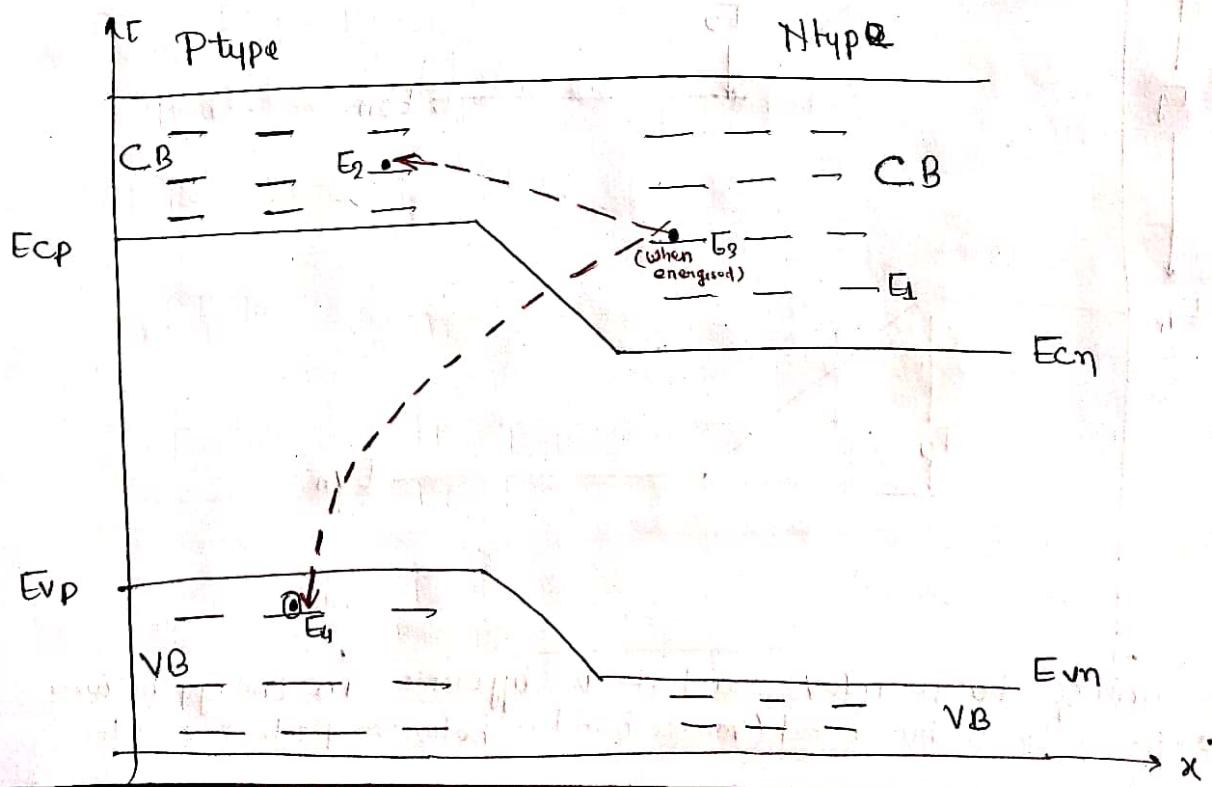
$$\Rightarrow V_{O2} = V_t \ln \frac{1000 N_0 N_n}{n^2} = \text{---}$$

$$\frac{V_{O2}}{V_{O1}} = \ln \left[ \ln 1000 + V_t \ln \frac{N_0 N_n}{n^2} \right] \\ = 0.179 + V_t \ln \frac{N_0 N_n}{n^2}$$

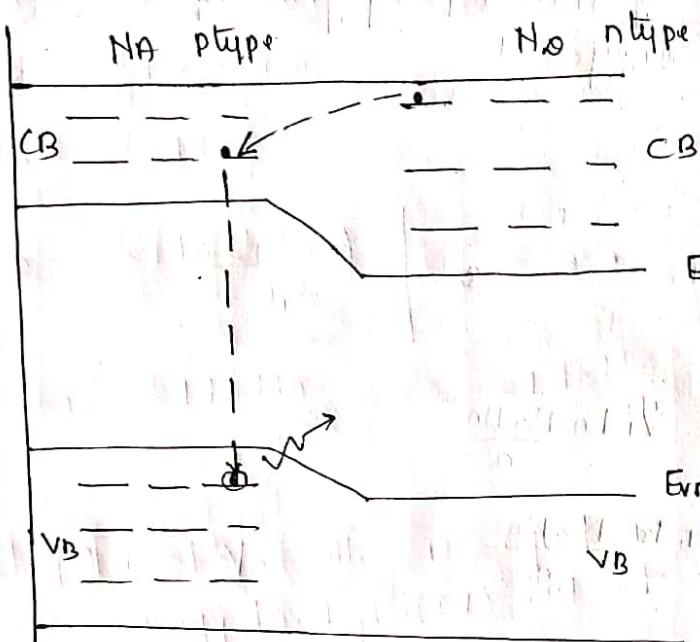
$$\text{change} = 0.179 \text{ volt}$$

### Barrier Potential or Energy Hill

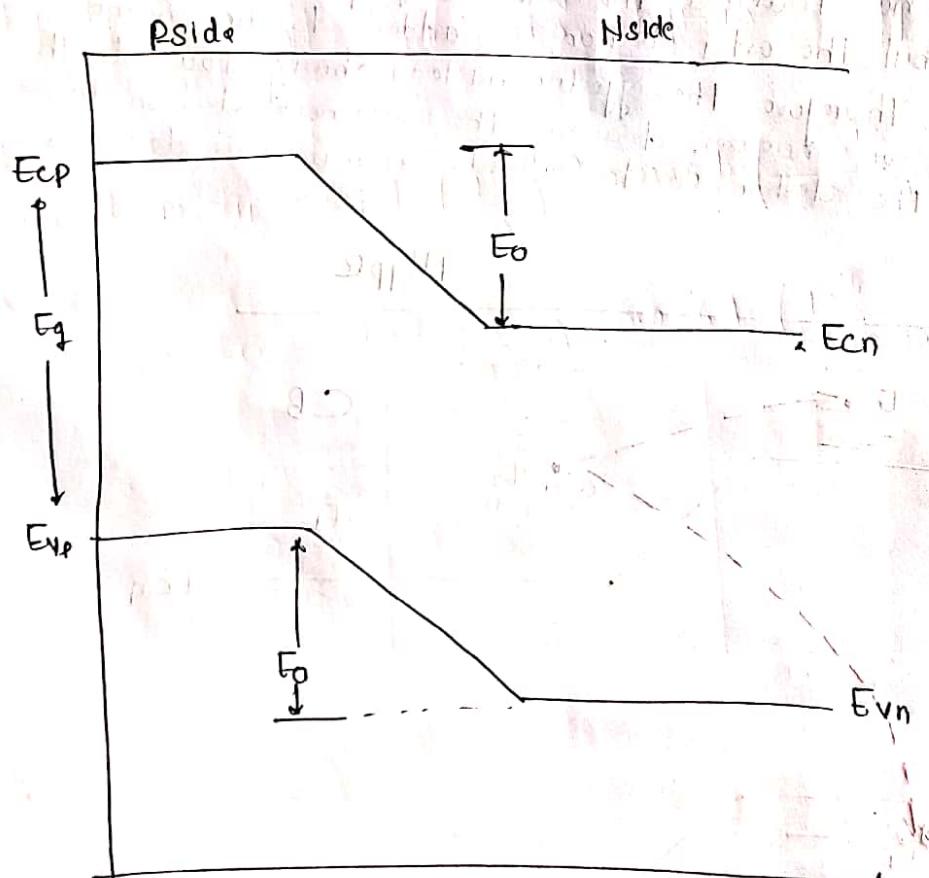
Atomic Radii decreases across the periodic table because as the atomic no. increases the number of proton increases across the period, but the extra electron is added to the same quantum shell. Therefore the effective nuclear charge towards the outermost electron increases, drawing the outermost electron closer. As a result the electron cloud contracts & atomic radii decreases.



a. without Barrier

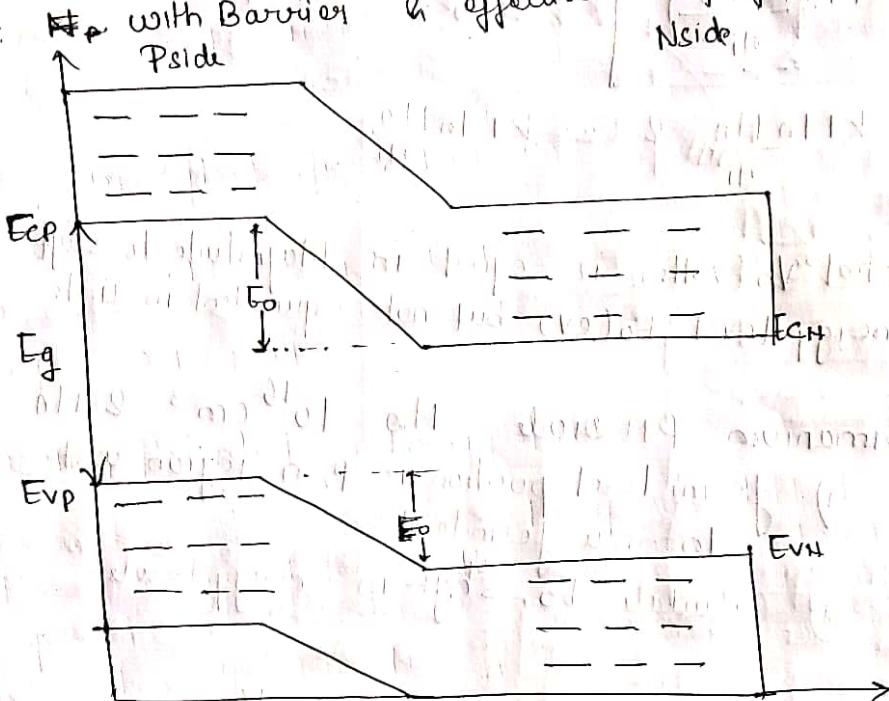


b. with Barrier



The unit of  $E_0$  is m(eV) and it is difference in Energy between edges of conduction band (valence band) between p-side & N-side.

→ If the effective density of energy states in p side & n side are equal then the electron exiting on n side always have to gain energy to move towards p side and the difference of Energy is equal to  $E_0$  eV

Case 1:  with Barrier Potential

a) effective density of states equal on either side

$E_{cp} - E_{cn}$

$E_g$

$E_{vp}$

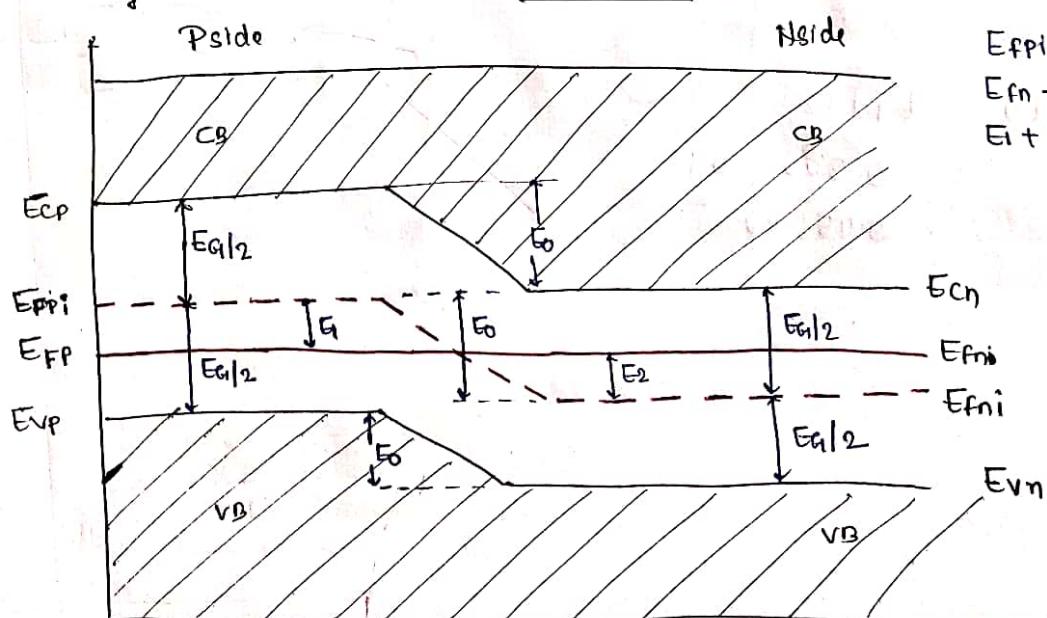
$E_{vn}$

$$E_0 = E_{cp} - E_{cn}$$

$$E_0 = E_{vp} - E_{vn}$$

$$E_g = E_{cp} - E_{vp}$$

open circuit



$$E_{pp} - E_{FPP} = E_1$$

$$E_{nn} - E_{FnN} = E_2$$

$$E_1 + E_2 = E_0$$

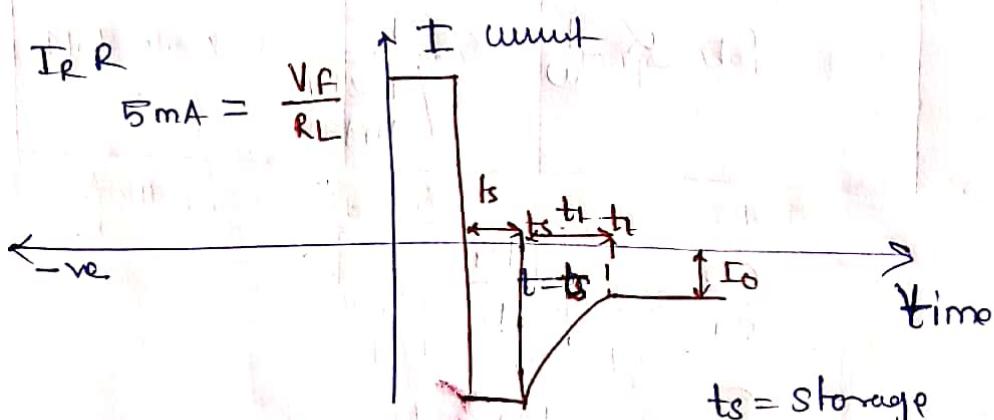
## Reverse Recovery Time

When a diode is reverse biased from forward biased mode, the diode does not show reverse saturation current instantaneously. That means the diode will take some time for full reverse biasing. The time taken by diode for full reverse biasing from Reverse biasing mode is called R.R.T. R.R.T is summation of storage time plus exiton time.

$$R.R.T = \text{Storage time} + \text{Exiton time}$$

$$V_R = I_R R$$

$$5\text{mA} = \frac{V_F}{R_L}$$



$$t_{RR} = t_s + t_r$$

When Reverse bias

$$\frac{-5V}{1k} = \frac{V_R}{R_L}$$

$$V_R = -5\text{mA}$$

$$\text{so } 0 < t < t_s$$

$$V_R = -5\text{V}$$

During  $t < 0$ , in forward bias, the holes are moving from p-type and electrons from n-type. So there are large number of holes on n-side (minority charge carriers) supplied from p-side due to forward current.

Similarly for electron in p side.

- ② At  $t=0$  applied Voltage is reduced to  $-V_r$  due to stored excess minority carrier (holes in n side and e<sup>-</sup> in p side) large reverse current  $I_R$  flows because of higher conc. of stored minority carriers and the diode offers low resistance even in Reverse bias during storage period  $t_s$ . The Reverse Current  $I_R$

$$I_R = \frac{V_r}{R_L}$$

(stored) would

- ③ After time  $t_s$  when all the stored charge carriers have been removed, the reverse current decreases upto reverse saturation current  $I_0$  value during the ~~saturation~~ time.  $I_0$  flow only due to minority charge carrier at equilibrium condition.

- ④ Total time taken by the diode to reach the off state is  $t_{off} = t_s + t_f$   
(Reverse Recovery Time)

Q6.

- sol At  $t=0$  the current flows through diode is the current flow through diode when it is in forward bias.

- \* The Magnitude of Current does not change at  $t=0$  when diode is moved from forward bias mode to reverse bias mode.

note: When the diode changes from Reverse bias mode to forward bias mode the (moved) Magnitude of current depend on mode and application of voltage.

This time taken for this ~~change~~ in forward Recovery time and it is negligible.

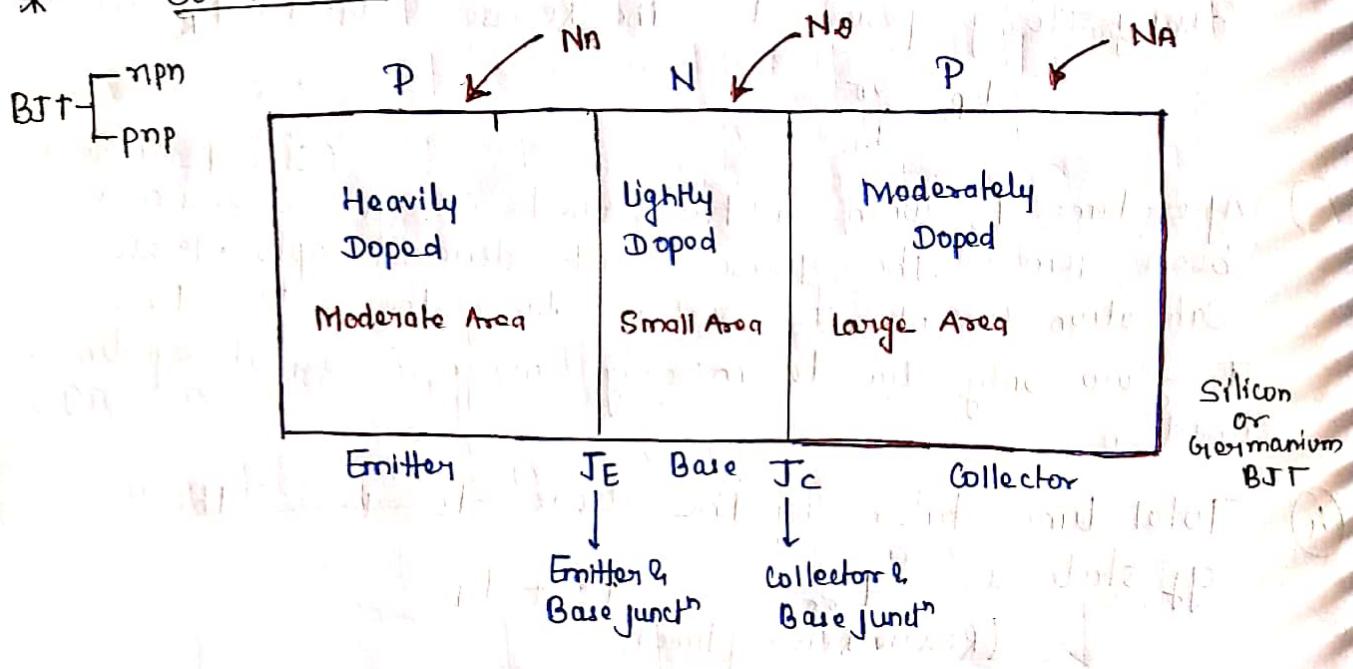
- R.R.T always dominate P.R.T

## Unit-3 Transistor $\rightarrow$ BJT

Tacns fer Resistor

B J T  
Bipolar Junction Transistor

\* Construction :-



Silicon   Germanium BJT	JE	Jc	
doping	Emitter ↑↑↑	Base ↑	Collector ↑↑
Area	↑↑	↑	↑↑↑

\* Biassing :-

Sno.	Mode of operation	JE	Jc	Application
1.	Active	FB	RB	Amplifier
2.	Saturation	FB	FB	Switch-on
3.	Cutoff	RB	RB	Switch-off
4.	Inverse active	RB	FB	Attenuator

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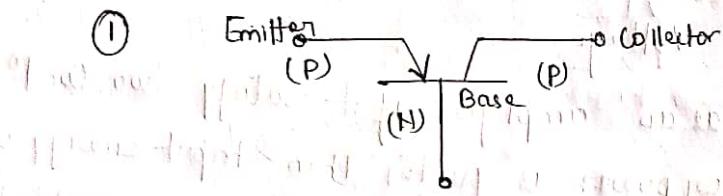
**Noted-: Single Source Follow, Revise**

**Multiple Time Best key of Success**

\* Configuration:

- Common Base CB
- Common Emitter CE
- Common Collector CC

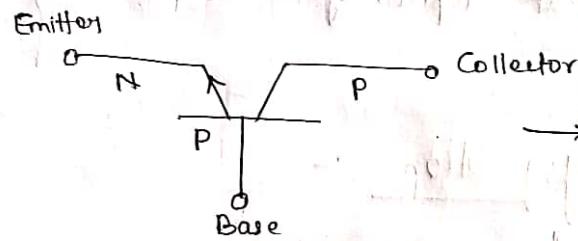
①



→ PNP Xistor

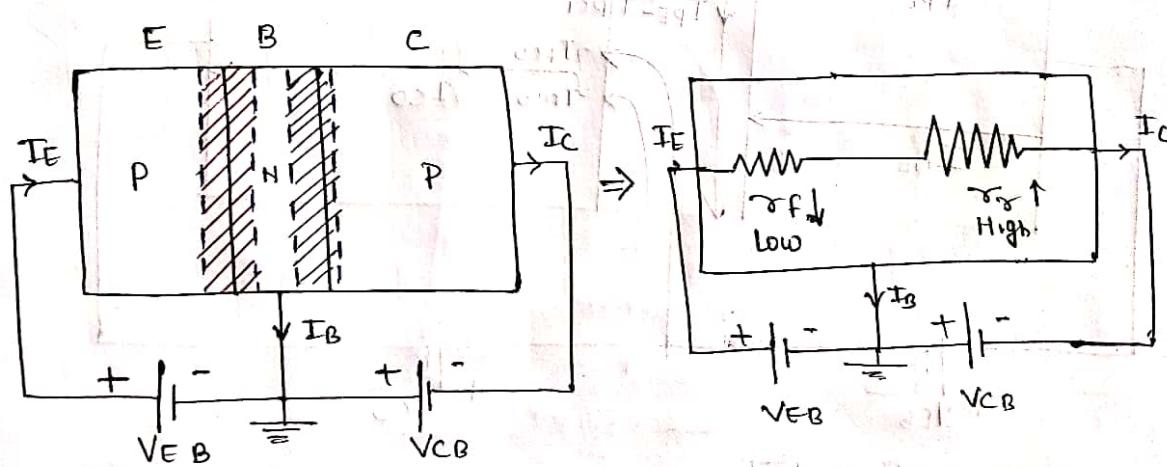
arrow always on Emitter  
shows direction of conventional Current.

②



→ NPN Xtor

Transistor is called xfer of Resistor bcoz when the current Xfer from input terminal to output terminal. It has to pass through from low resistance to high Resistance Value generated at the junction JE & JC.



$$V_j = V_o - V_{eb}$$

w↓

$$V_j = V_o + V_{cb}$$

w↑

$$I_E \rightarrow I_C \rightarrow I_B$$

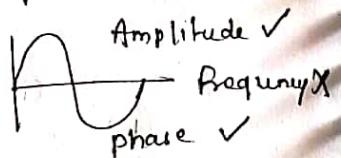
$$I_E = I_C + I_B$$

The Base Region in the  $\text{X}^{\text{ter}}$  is the region of Importance for amplification of Signal that means without base Region we cannot think of Signal Amplification.

An Amplifier is a device which boost up an I/p sig by using a DC Input Voltage.

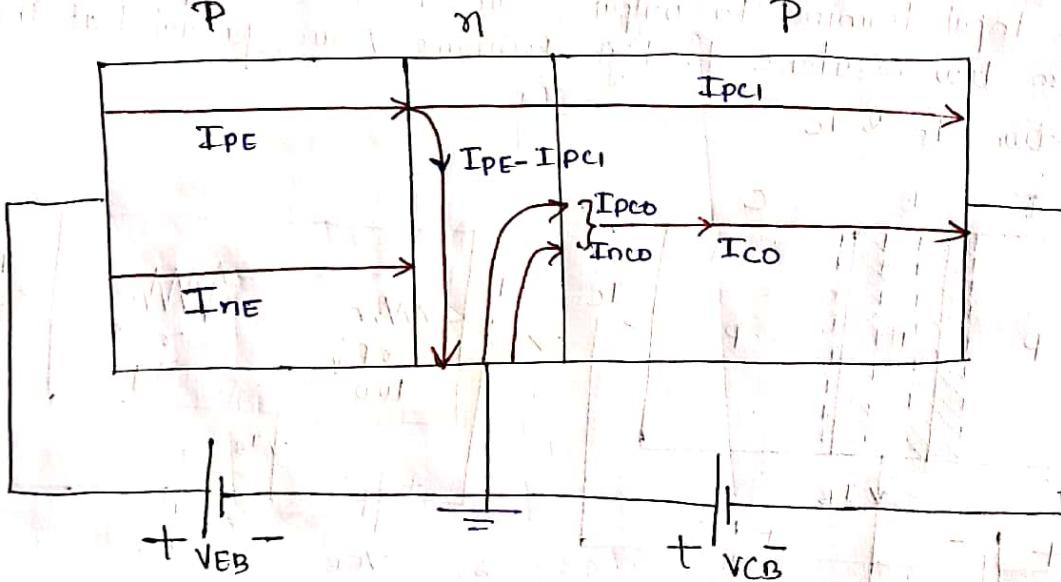
A device is used as an amplifier if it satisfy two cond :-

- 1) The output Energy or power is greater than Input energy or power.
- 2) The output is an exact replica of the input.



### Common Base Configuration :-

#### Current Component in CB Amplifier:



$$I_{CO} = I_{CBO} + I_{CRE}$$

$$I_{CO} = I_{CBO}$$

$I_{PE}$   $\rightarrow$  Current due to hole in Emitter Region

$I_{NE}$   $\rightarrow$  Current due to  $e^-$  in Emitter Region.

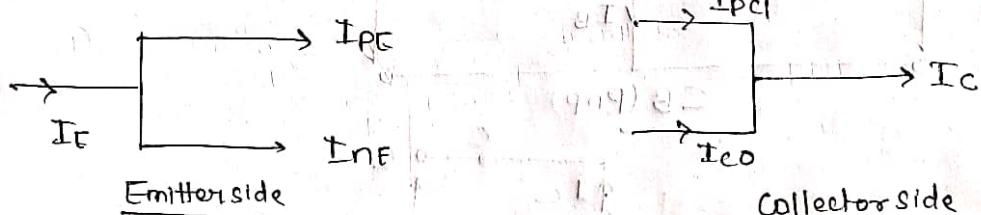
$I_{PCl}$   $\rightarrow$  Current due to hole in Collector Region at thermal equilibrium

$I_{PE} - I_{PCl}$   $\rightarrow$  Recombination Current

$I_{nco}$  → Current due to  $e^-$  (minority) in collector region at thermal equilibrium.

$I_{co}$  → Total reverse saturation current in collector

$$I_{co} = I_{pc} + I_{nco}$$



$$\Rightarrow I_E = I_{pe} + I_{ne} \quad \text{--- (1)}$$

$$I_C = I_{pc} + I_{co} \quad \text{--- (2)}$$

$$I_E = I_B + I_C \quad \text{--- (3)}$$

$$I_{co} = I_{pc} + I_{nco} \quad \text{--- (4)}$$

$$\Rightarrow I_E = I_{pe} + I_{ne}$$

$$I_{ne} \ll I_{pe}$$

$$I_{pc} = \alpha I_E$$

$$\Rightarrow \alpha = \frac{I_{pc}}{I_E} = \frac{I_C - I_{co}}{I_E} \quad \left\{ \begin{array}{l} I_{co} \ll I_E \\ I_{pe} \ll I_E \end{array} \right.$$

$$\boxed{\alpha = \frac{I_C}{I_E}}$$

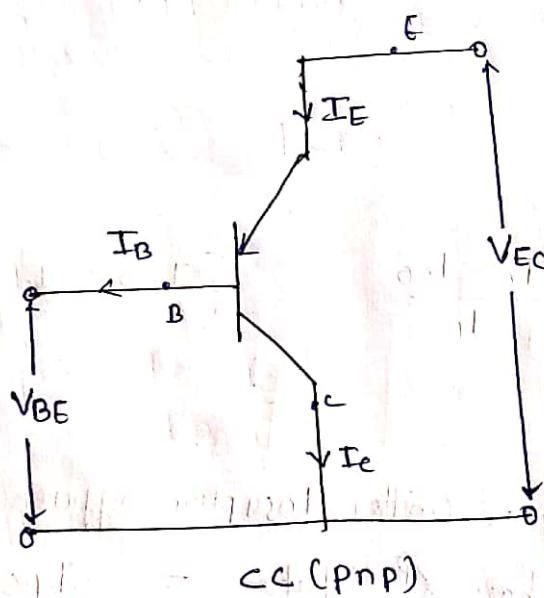
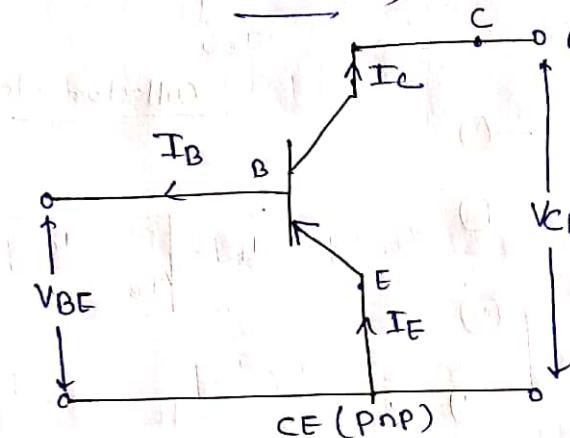
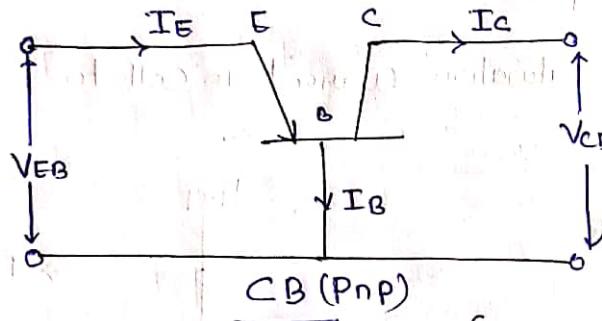
$$\gamma^* = \text{Emitter efficiency or Emitter Inception efficiency} = \frac{I_{pe}}{I_{pe} + I_{ne}}$$

$$\beta^* = X^* \text{ factor or base } X^* \text{ factor} = \frac{I_{pc}}{I_{pe}}$$

$$\gamma^* \beta^* = \frac{I_{pe}}{I_{pe} + I_{ne}} \times \frac{I_{pc}}{I_{pe}} = \frac{I_{pc}}{I_{pe} + I_{ne}}$$

$$\Rightarrow \boxed{\gamma^* \beta^* = \frac{I_{pc}}{I_E} = \alpha}$$

Common Emitter Configuration (NPN)



Common Base Configuration: Base is common in input and output port or otherwise the base is grounded.

$I_E$  = Input Current

$V_{EB}$  = Input Voltage

$I_C$  = Output Current

$V_{CB}$  = Output Voltage

Common Emitter :- Emitter is common between Input and output port or otherwise Emitter is grounded.

$$V_{BE} = \text{Input Voltage}$$

$$I_B = \text{Input Current}$$

$$V_{CE} = \text{Output Voltage}$$

$$I_C = \text{Output Current}$$

Common Collector :- Collector terminal is common between Input & Output port or otherwise it should be grounded.

$$V_{BC} = \text{Input Voltage}$$

$$I_B = \text{Input Current}$$

$$V_{EE} = \text{Output Voltage}$$

$$I_E = \text{Output Current}$$

$$I_C = I_{PC1} + I_{CO}$$

$$= I_{PC1} + I_{CBO}$$

$$\therefore \alpha = \frac{I_{PC1}}{I_E}$$

$$( \because I_{CO} = I_{CBO} )$$

$$I_C = \alpha I_E + I_{CBO}$$

$I_{CBO} \rightarrow$  Reverse Saturation Current between Collector & Base, when Emitter is open circuited.

$$\alpha = \frac{I_C - I_{CBO}}{I_E} = \text{Current gain in Common Base Configuration}$$

$$(\alpha \approx 0.95 \approx 0.985 \approx 1)$$

→ Irrespective of Configuration always Emitter junction  $J_E$  & Collector Junction  $J_C$  has to be biased.

### Common Emitter

$$I_C = \alpha I_E + I_{CBO}$$

$$I_E = I_B + I_C$$

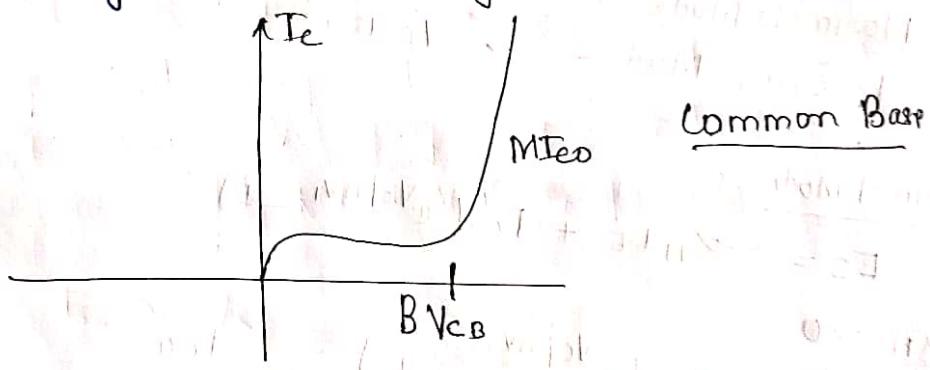
for example, by making Base width much larger than the diffusion length of Minority Carrier in the base, all Minorities will recombine in the base & none will reach collector. For this case, Current gain is zero.

Under this condition  $X_{TO}$  action ceases. In we simply have two diodes placed back-to-back. This discussion shows why it is impossible to construct a  $X_{TO}$  by simply connecting two diode in series opposing.

A cascade of two PN diodes exhibits  $X_{TO}$  properties (the property of Amplification) only if carrier injected across one junction diffuses across the second junction.

### Transistor Breakdown:

1. Avalanche
2. Punch Through or Reach Through



**Avalanche Multiplication**  
which may be applied before breakdown betn Base & Collector terminal under the condition the Emitter terminal is open circuited is represented by symbol  $BV_{CEO}$ .  
This breakdown voltage is the characteristic of transistor  
Breakdown may occur because of Avalanche Multiplication  
the current  $I_{EO}$  that crosses Collector Junction.  
As a result of multiplication the current become  $M I_{EO}$   
where  $M$  is factor by which original current  $I_{EO}$   
is multiplied due to Avalanche effect.

The Avalanche Multiplication depends on Voltage  $V_{CB}$  between Collector & Base.

$$M = \frac{1}{1 - \left( \frac{V_{CB}}{BV_{CBO}} \right)^n}$$

The parameter 'n' is the factor which has range 2 to 10 & it controls the sharpness of the Onset breakdown.

Common Emitter :- In this Case, the Avalanche breakdown voltage is represented by  $BV_{CEO}$  & it is obtained when Collector & Emitter Voltage with open circuited base region are designed. The Relation between  $BV_{CBO}$  &  $BV_{CEO}$  is

$$BV_{CEO} = BV_{CBO} \sqrt[n]{\frac{1}{B}}$$

Que. An n-p-n Ge-xtor is having parameter  $n=6$  &  $B=50$  find the relationship between  $BV_{CEO}$  &  $BV_{CBO}$ . If  $BV_{CBO}$  is 40V then what is  $BV_{CEO}$ .

Sol  $BV_{CEO} = BV_{CBO} \left( \frac{1}{50} \right)^6$

$$BV_{CEO} = 0.52 BV_{CBO} \quad ||$$

$$\text{If } BV_{CBO} = 40V$$

$$BV_{CEO} = 0.52 \times 40$$

$$BV_{CEO} = 20.8 V$$

Ques The Breakdown Voltage of xtor with Base open is  $BV_{CEO}$  & that with Emitter open is  $BV_{CBO}$  then

- Sol
- i)  $BV_{CEO} = BV_{CBO}$
  - ii)  $BV_{CEO} > BV_{CBO}$
  - iii)  $BV_{CEO} < BV_{CBO}$   $\rightarrow$  Always
  - iv)  $BV_{CEO}$  is related with  $BV_{CBO}$ .

Surface leakage Current:

$$I_{CBO} = I_{Co} + I_{\text{surface}} + I_{\text{avalanche breakdown}}$$

or xtor                  leakage                  breakdown

During design of diode across the Surface certain Impurities develop called as Surface Impurity. These Impurities were seen to support leakage current during Reverse bias. The Magnitude of current due to Reverse Voltage called as Surface Leakage Current.

Ques. for a pn diode Surface leakage current is 2nA for a reverse bias Voltage of 25V. what is Surface leakage current for Reverse Voltage of 30V.

Sol  $I_{SL} \propto V_R$

$$\frac{I_{SL1}}{I_{SL2}} = \frac{VR_1}{VR_2}$$

$$\Rightarrow \frac{2}{I_{SL2}} = \frac{25}{30}$$

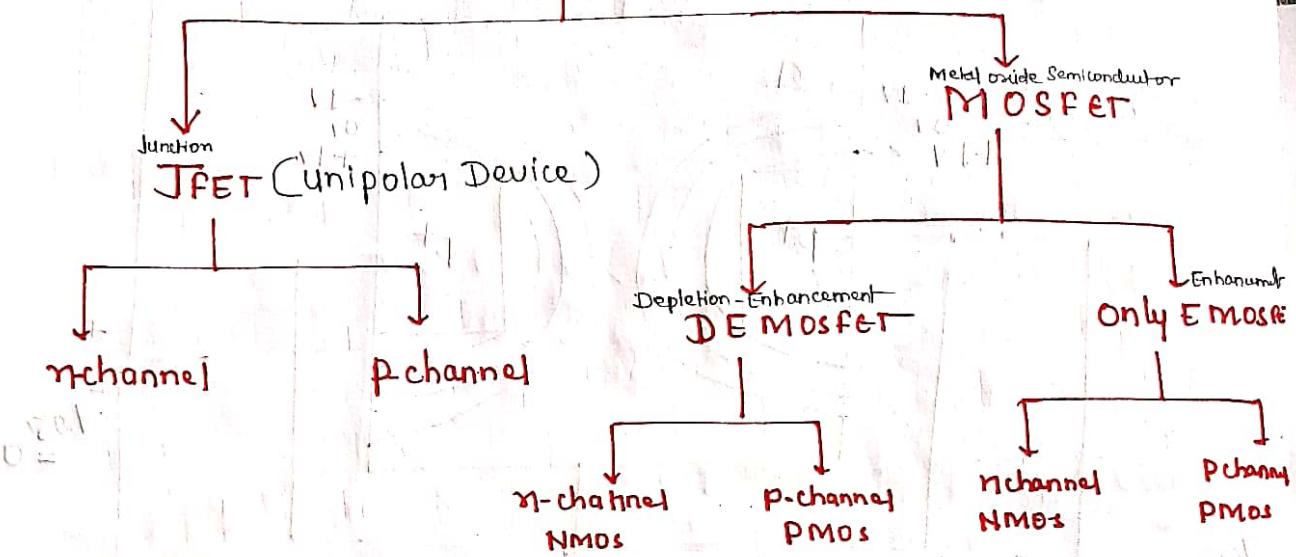
$$\Rightarrow I_{SL2} = \frac{30}{25} \times 2$$

$$= \frac{6 \times 2}{5}$$

$$I_{SL2} = 2.4 \text{nA}$$

## Chapter - 4

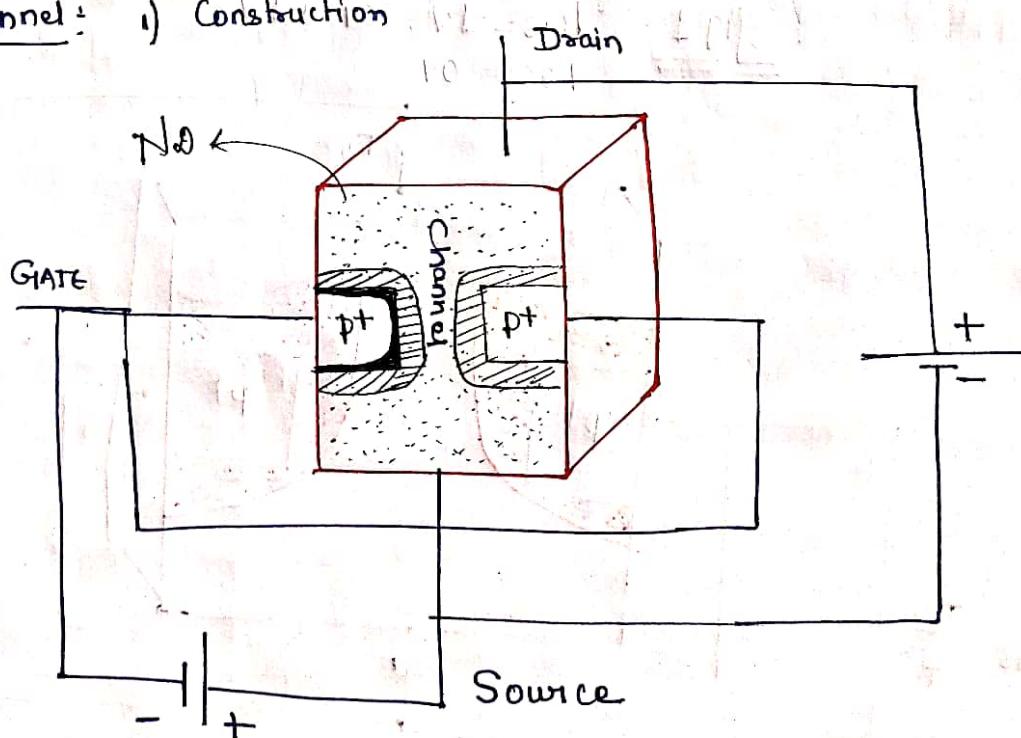
### FIELD EFFECT TRANSISTOR (FET)



In BJT :  $I_C = \alpha I_E$  Current Controlled device

#### JFET

n-channel : i) Construction



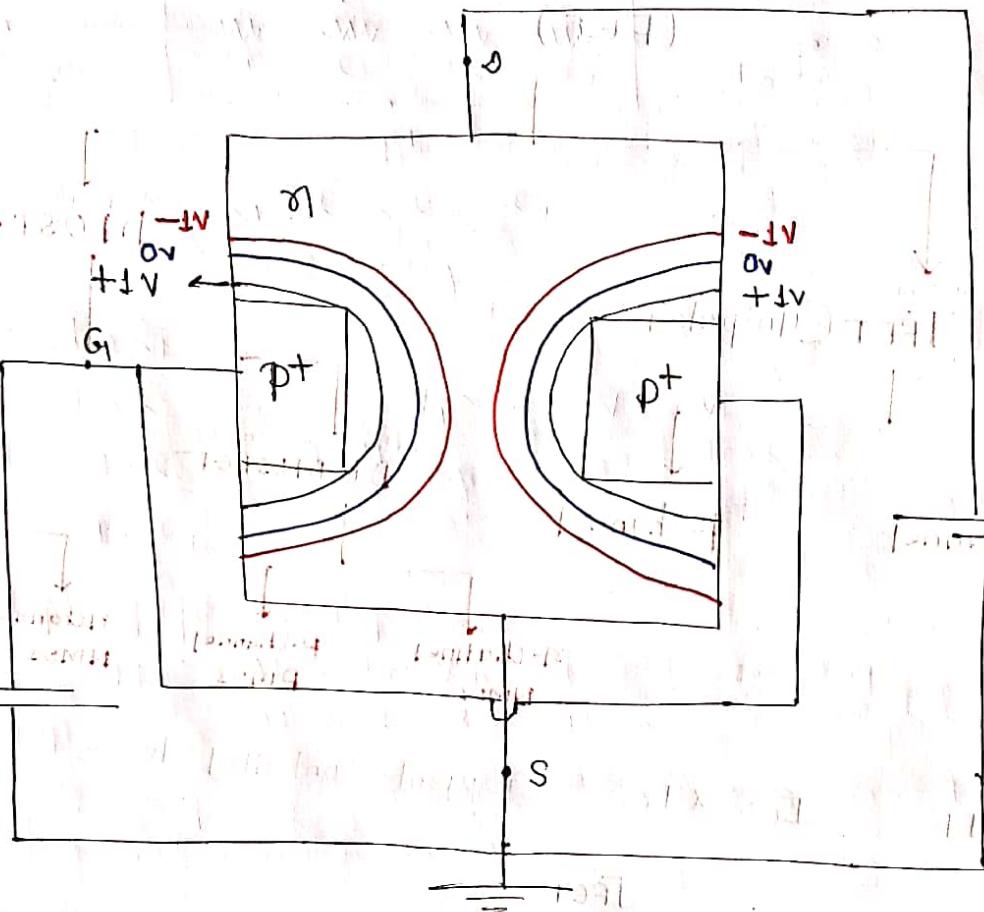


fig. 1  $V_{GS} = -1V$ ,  $DV = +1V$   
 $V_{DS} = 0V$

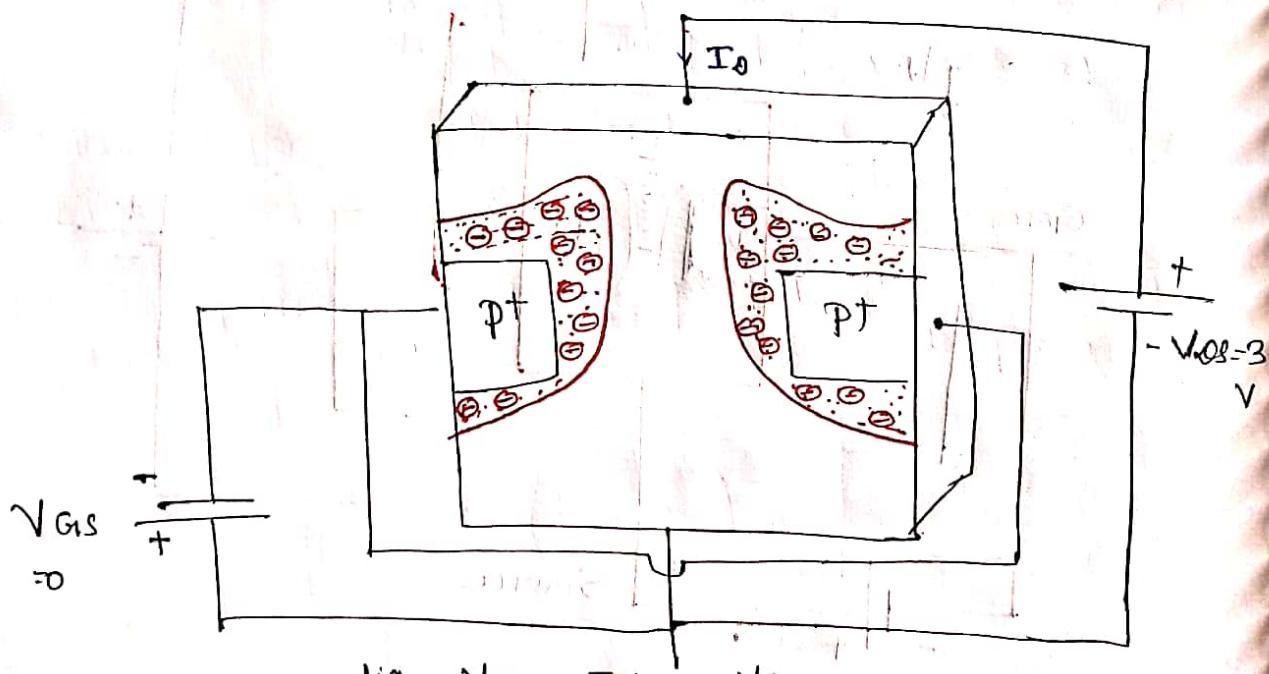


fig.  $V_{DS} = 3V$ ,  $V_{GS} = 0V$

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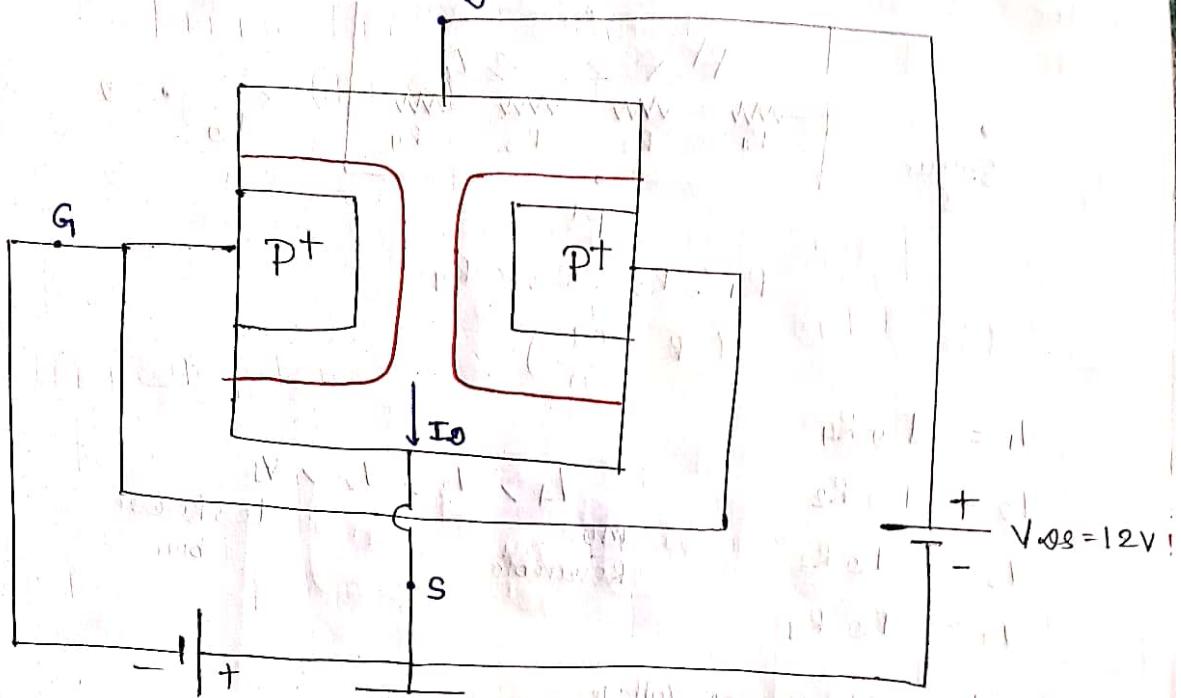


fig :- When  $V_{GS} = 0$  &  $V_{DS} = 12V$

if  $I_D = 0$

$$V_4 = V_3 = V_2 = V_1 = 0$$

\* Cause of depletion region formation = 0

⇒ Results No depletion region

⇒ further Results  $I_D \neq 0$

⇒ Not possible

⇒ This is an unstable state ( $I_D = 0$ )

Transfer characteristic  
or  
Input - output char.

$$V_{GS\text{ off}} = V_{P2} \Rightarrow I_D = 0$$

$V_{GS}$  = Variable

$V_{DS}$  = Const.

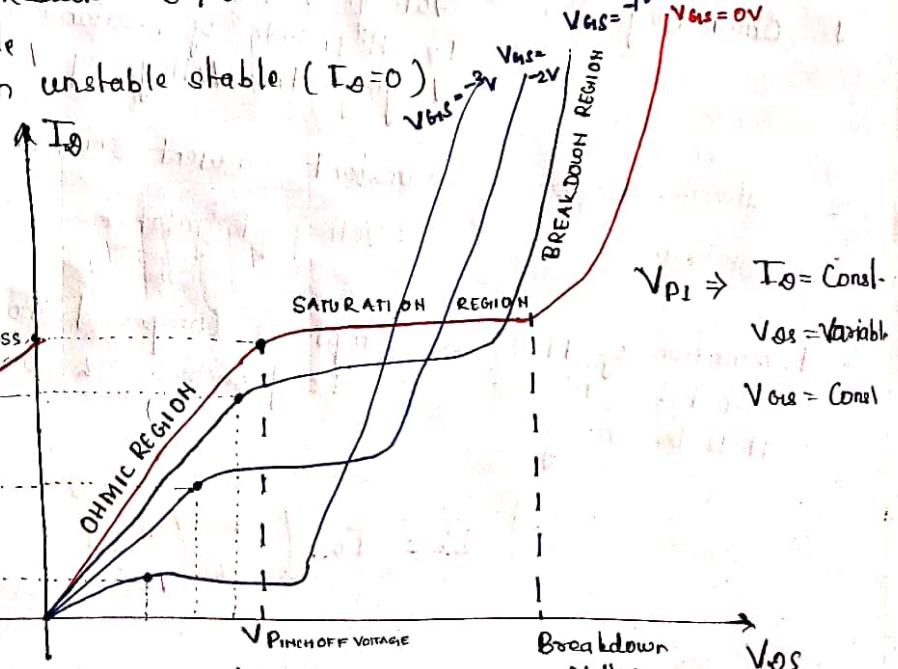
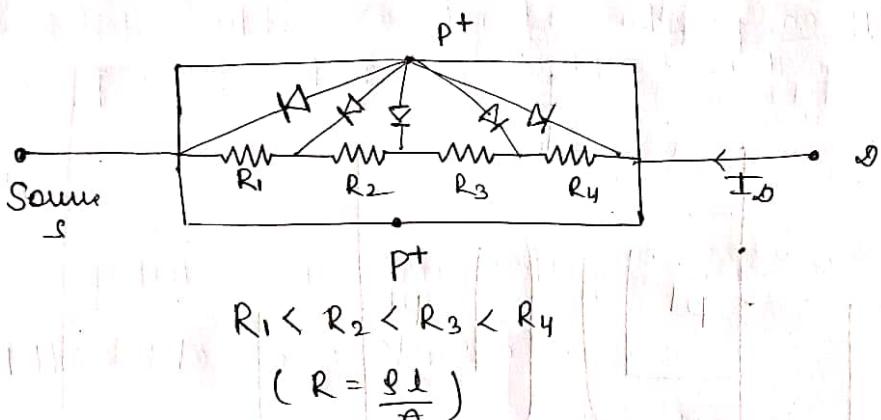


fig :- VI characteristic

output characteristic or drain char.



$$V_1 = I_D R_4$$

$$V_2 = I_D R_2$$

$$V_3 = I_D R_3$$

$$V_4 = I_D R_4$$

$$R_1 < R_2 < R_3 < R_4$$

$$(R = \frac{BL}{A})$$

More Reverse bias

Less Reverse bias

- Two types of pinch-off voltages:-
- $V_{PL}$  :- At constant  $V_{GS}$ ,  $I_D = \text{const.}$ ,  $V_{DS} = \text{change}$
- $(V_{GS\text{off}}) V_{P2}$  :- At constant  $V_{DS}$ ,  $I_D = 0$ ,  $V_{GS} = \text{change}$
- If we change polarity of  $V_{DS}$  then Source & Drain terminal Interchanges. Characteristic remain same.
- Application of JFET
- 1. Ohmic Region :- Voltage Variable Resistor (VVR)  
The Magnitude of Resistance can be controlled by varying the Voltage of  $V_{DS}$ .
- 2. Saturation Region :- Constant Current Source (CCS)
- 3. Breakdown Region :- Voltage Regulator (VR)
- Fabrication of JFET is simple as compared to XTR because it will take less area in IC fabrication. & consume less power. It is less noisy.

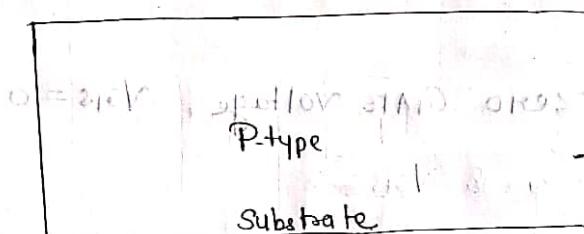
$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$$

$$V_P = V_{P2} \approx V_{GS\text{off}}$$

# METAL OXIDE SEMICONDUCTOR FET

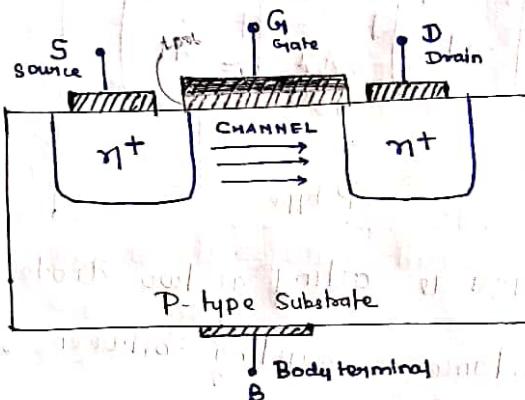
## MOSFET

Construction :- NMOS



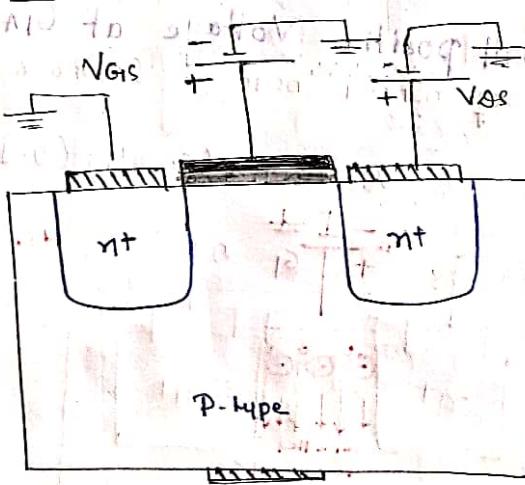
- Intrinsic Semiconductor
- P type Substrate
- Silicon substrate

fig 1 :- Substrate of N type Mosfet or NMOS



- Source / & drain diffusion with No
- Heavily doped
- Source & Drain n+
- $t_{ox} = 2nm \text{ to } 20nm$
- $\text{SiO}_2$  deposit (dielectric / insulator)
- Poly Silicon above  $\text{SiO}_2$
- Metal contact for Source, drain, & Body
- Extrinsic Electrodes to get Source, gate, drain & Body.

fig 2 :- Creation of Source, Gate, Drain & Body



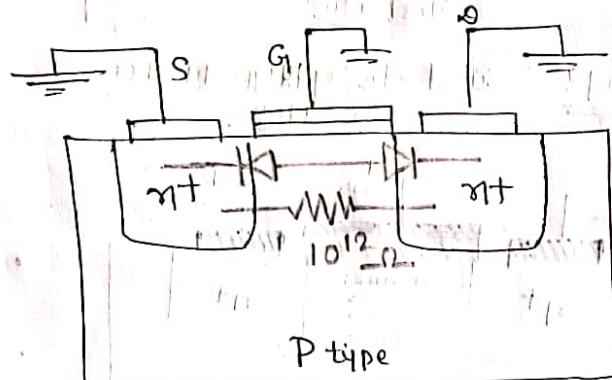
- Observe that the Substrate form a pN junction with Source & Drain region. In normal operation these pN junction are kept Reverse biased all time
- The Drain will be at positive Voltage relative to Source (NMOS). The two PN Junction can be effectively Cut off by Connection Substrate to Source term.

- The Substrate will be Considered as having no effect on device operation and MOSFET will be treated as 3 terminal device.

## Operation :-

Case I :- With zero GATE voltage,  $V_{GS} = 0$

- When  $V_{DS} = 0$  &  $V_{GS} = 0$



- The channel area is acting as two diode connected back-to-back between Source & Drain
- Very high resistance is existing between Source & Drain of order  $10^{12} \Omega$ .

Case II With Small positive Voltage at GATE terminal  $V_{GS} = +ve$  (small)  
i.e Creation of channel between Source & drain

- When  $V_{DS} = 0$  &  $V_{GS} = +ve$  (small) ( $0.1$  to  $0.5V$ )

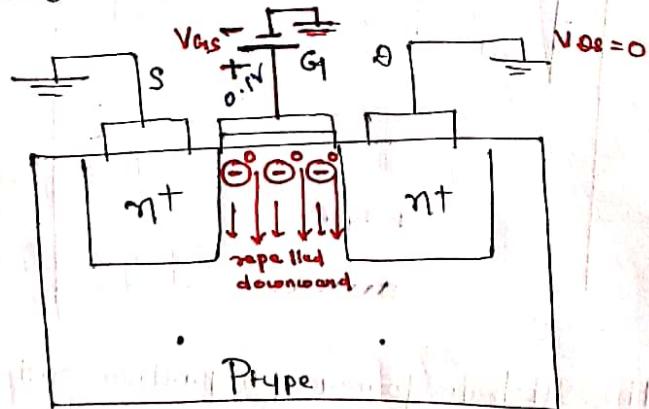
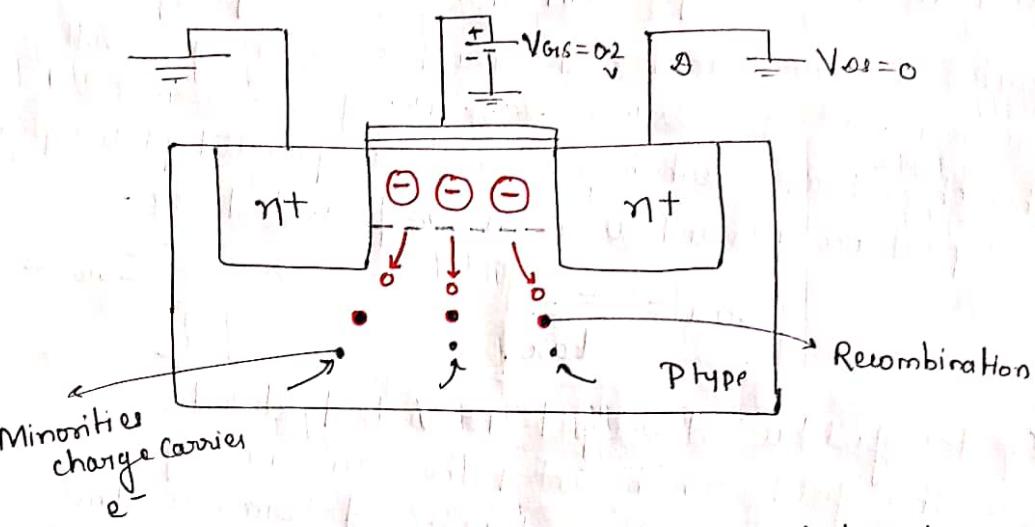


fig:- When  $V_{GS} = \text{small +ve}$   
(say  $0.1V$ )

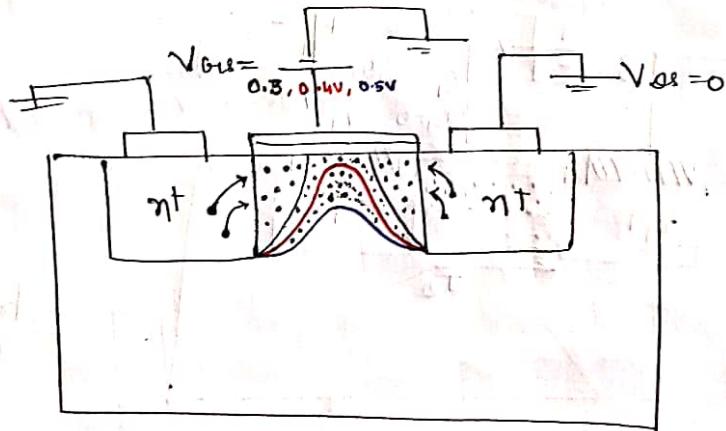
- Small positive Voltage of  $0.1V$  repel the Holes from acceptor atom.

2. When  $V_{DS} = 0$  &  $V_{GS} = 0.2V$



- Increasing  $V_{GS}$  to  $0.2V$  attract minority electron from Substrate.
- Recombination takes place (EHP lost)
- Region of channel is depleted of Mobile charge Carrier.  
i.e. Uncovered charge accumulated.

3.



- Increasing the  $V_{GS}$  Voltage further the  $e^-$  will get attracted from Source & drain toward the channel.
- When sufficient no. of electron are attracted it forms a channel. Hence channel is Induced known as Inversion layer.
- It is called Inversion layer because the polarity of ptype Substrate is inverted by -ve electron.
- The Value of  $V_{GS}$  at which sufficient amount of mobile  $e^-$

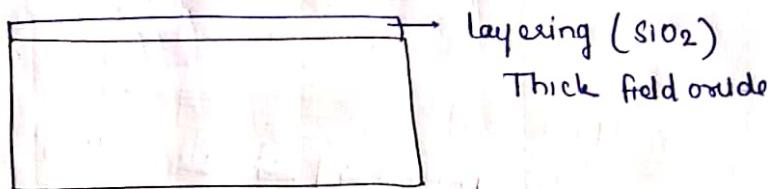
- Finally, the package is sealed using a plastic under vacuum or in inert atmosphere.
- Fine Gold wires are normally used to connect the pins of the package to the metallization pattern on the die.

### Step Involved in MOS Fabrication

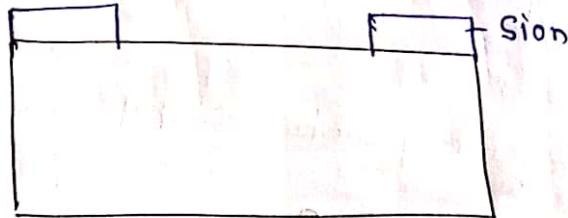
1. Layering
2. Patterning
3. Doping
4. Heat treatment (Annealing)

#### I. Layering:

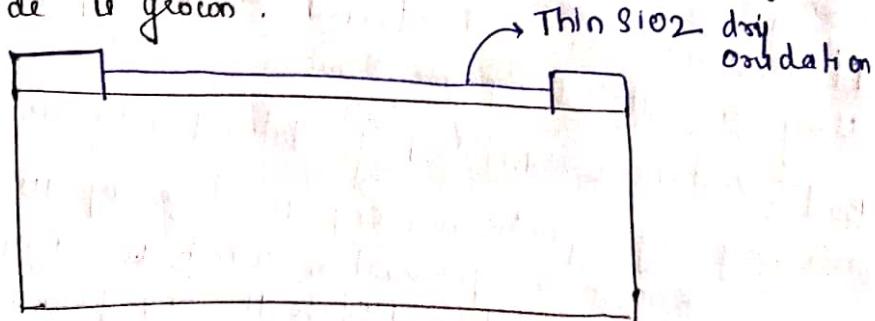
- Growth of the oxide layer (field oxide)
- Field of oxide over the surface of substrate.



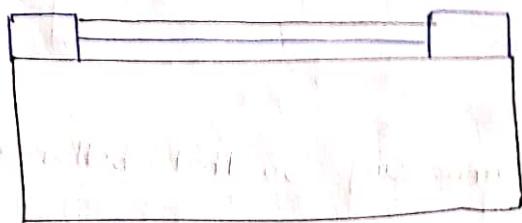
#### 2. Patterning: An opening is created in this step in field oxide for growing source drain & Gate oxide



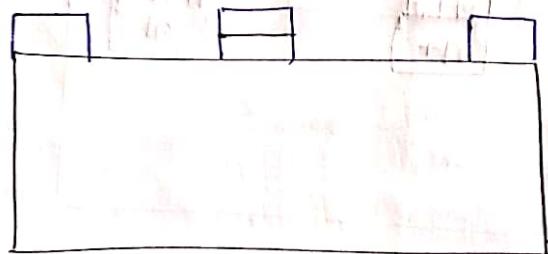
#### 3. Layering: field oxide is removed by etching & gate oxide is grown.



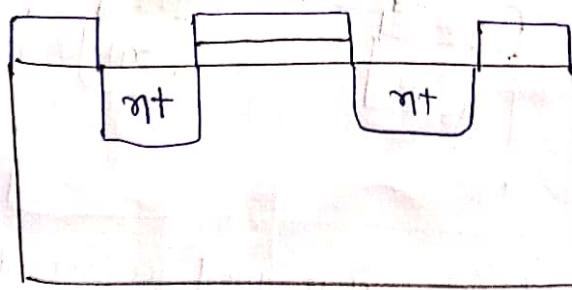
4. Layering: A layer of polysilicon is deposited on the top of gate oxide. This forms the initial step for gate electrode and the polysilicon is grown, by using CVD process. Initially the polysilicon is deposited uniformly.



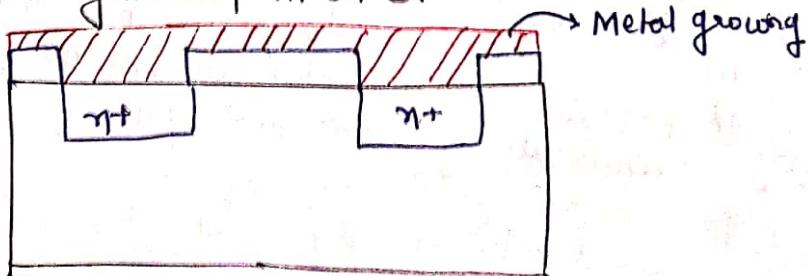
5. Patterning: The opening are created in the gate oxide layer. This is for making the source and drain. The gate region is masked and the material (Polysilicon & SiO<sub>2</sub>) in the remaining region are removed by etching.



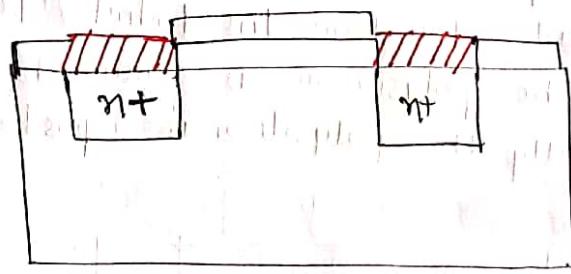
6. Doping: Doping is used to create the n+ region source and drain.



7. Layering: Metal is deposited to make the electrical contact. The metal used is generally Al or Cu.



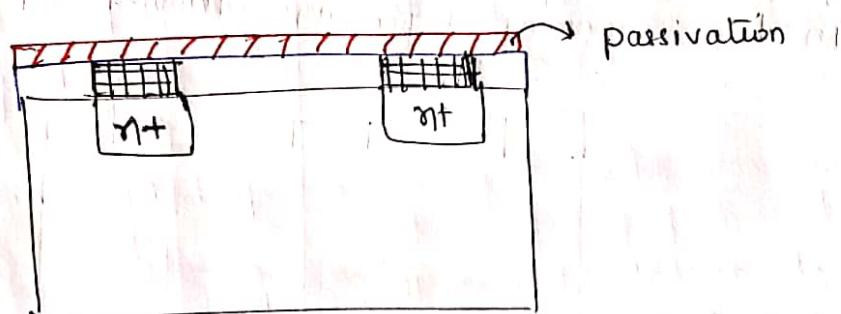
8. Patterning: Excess Metal is removed from the device



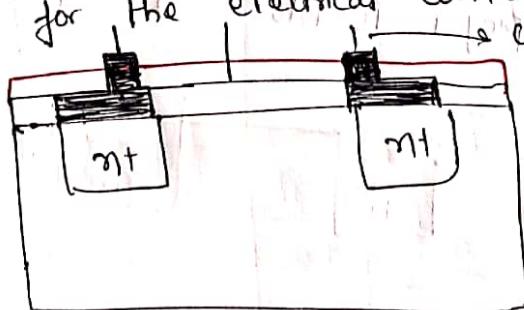
9. Heat treatment:

The MOSFET is annealing so that better electrical contact can be made.

10. Layering: Layering should be done above the fabricated MOSFET and this is said to be passivation. This layer acts as protection layer the device.



11. The last step of patterning is to create holes in the passivation layer for the electrical contact to the external circuit.



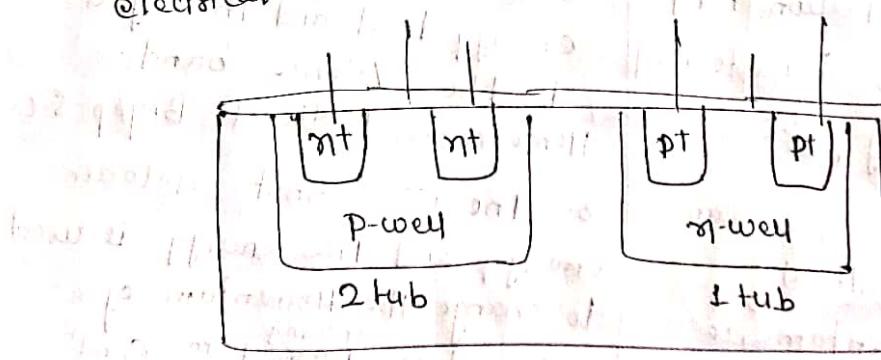
Molecular beam epitaxy: It is used for controlled deposition of very thin layer of compound of Gallium arsenide on the surface of the Silicon Substrate. It is performed in a Molecular beam epitaxy chamber in ultra high vacuum to prevent contamination. In this process controlled beam of projected molecule of Gallium and arsenide is from the opening of the chamber which is deposited on the target surface due to controlled and high speed

Ques. In CMOS Tech. how well & p-well

### Twin-Tub CMOS Process

Different step for fabrication of CMOS using twin-tub is as follows-

- Lightly doped N or P substrate is taken and to protect the latch up epitaxial layer is need.
- A epitaxial layer is very thin layer of P or n type material used to protect the CMOS from electrical connectivity (short circuit).
- High purity controlled thickness of the layer of silicon with p-type or N-type is used to form the twin tub of the CMOS.
- The dopant used used for formation of tub are used to determine electrical properties of CMOS.
- A thin oxide layer is constructed above the Silicon Substrate which is acting as gate oxide.
- Implantation of Source and drain is done by using Ion Implantation technique.
- Next technique is Metalization for and opening for electrical contact.



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3. Test series practice more n more (Try to latest test series 2-3 fully solve then join online test series.)

**Noted-: Single Source Follow, Revise**

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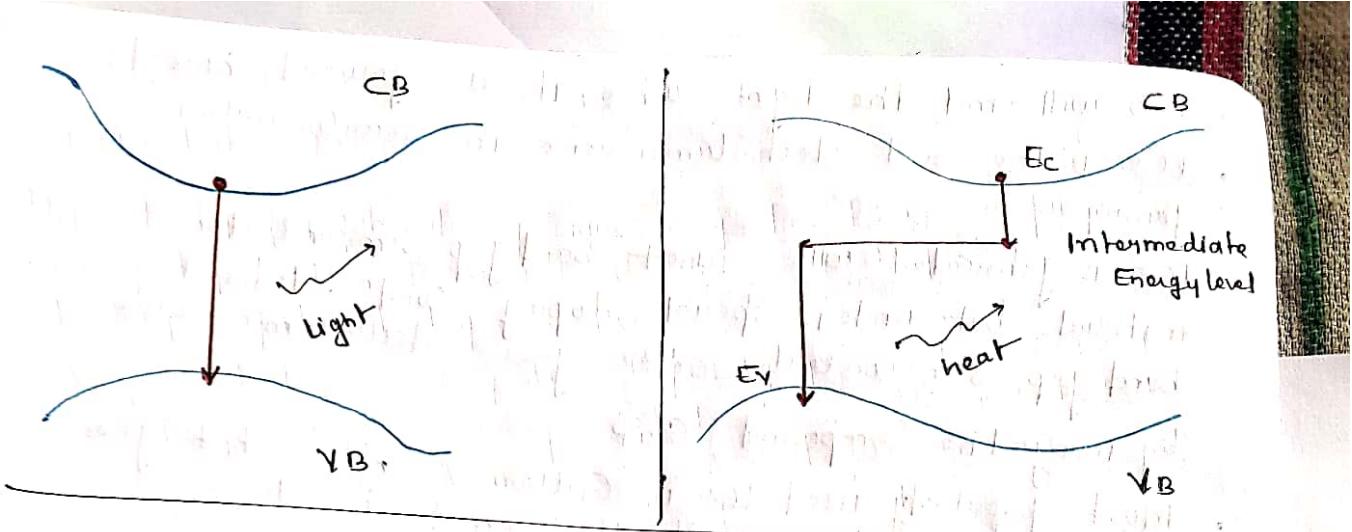
## Unit-5 Special Diodes

1. LED
2. Photodiode
3. Solar Cell

### I. LED :-

1. LED is a direct band gap S.C.  
e.g. GaAs, GaAsP, GaP
2. Si, Ge are Indirect band gap S.C.

Direct Band Gap S.C	Indirect Band Gap S.C
<ol style="list-style-type: none"><li>1. During recombination most of the energy dissipate in the form of light.</li><li>2. During recombination most of the <math>e^-</math> will be directly falling from Conduction band to Valence band hence formed as Direct Band gap S.C.</li><li>3. In direct B.G S.C <math>e^-</math> can release energy without change in Momentum, i.e. the Momentum of electron remains constant.</li><li>4. Example of Direct B.G S.C are GaAsP, GaAsP:N Gallium Arsenide Phosphide      Gallium Arsenide Phosphide Nitrogen.</li></ol>	<ol style="list-style-type: none"><li>1. During recombination most of the energy dissipate in form of heat.</li><li>2. During recombination most of the <math>e^-</math> falling from Conduction band will move to intermediate energy level and then fall to the Valence band. Hence name Indirect B.Gap S.C.</li><li>3. The <math>e^-</math> cannot release energy and the energy is used to change the Momentum of <math>e^-</math> when it is moving from Cond<sup>n</sup> band to Valence band.</li><li>4. Example Si, Ge</li></ol>



- The LED is based on electroluminescence
- The Energy released by an LED can be calculated by using it.

$$E = hf$$

where,  $h$  = Planck's Constant

$$h = 6.626 \times 10^{-34} \text{ J}\cdot\text{s}$$

$$c = \lambda f$$

$$c = 3 \times 10^8 \text{ m/s}$$

$$E = \frac{hc}{\lambda}$$

$$hc = 1.99 \times 10^{-25} \text{ J}\cdot\text{m}$$

$$E = \frac{1.99 \times 10^{-25}}{\lambda \text{ m}}$$

$$1 \text{ eV} = 1.6 \times 10^{-19} \text{ J}$$

$$= \frac{1.99 \times 10^{-25} \times 10^6}{\lambda (\text{nm})} \text{ J nm}$$

$$= \frac{1.99 \times 10^{-19}}{\lambda \times 1.6 \times 10^{-19}} \text{ eV nm}$$

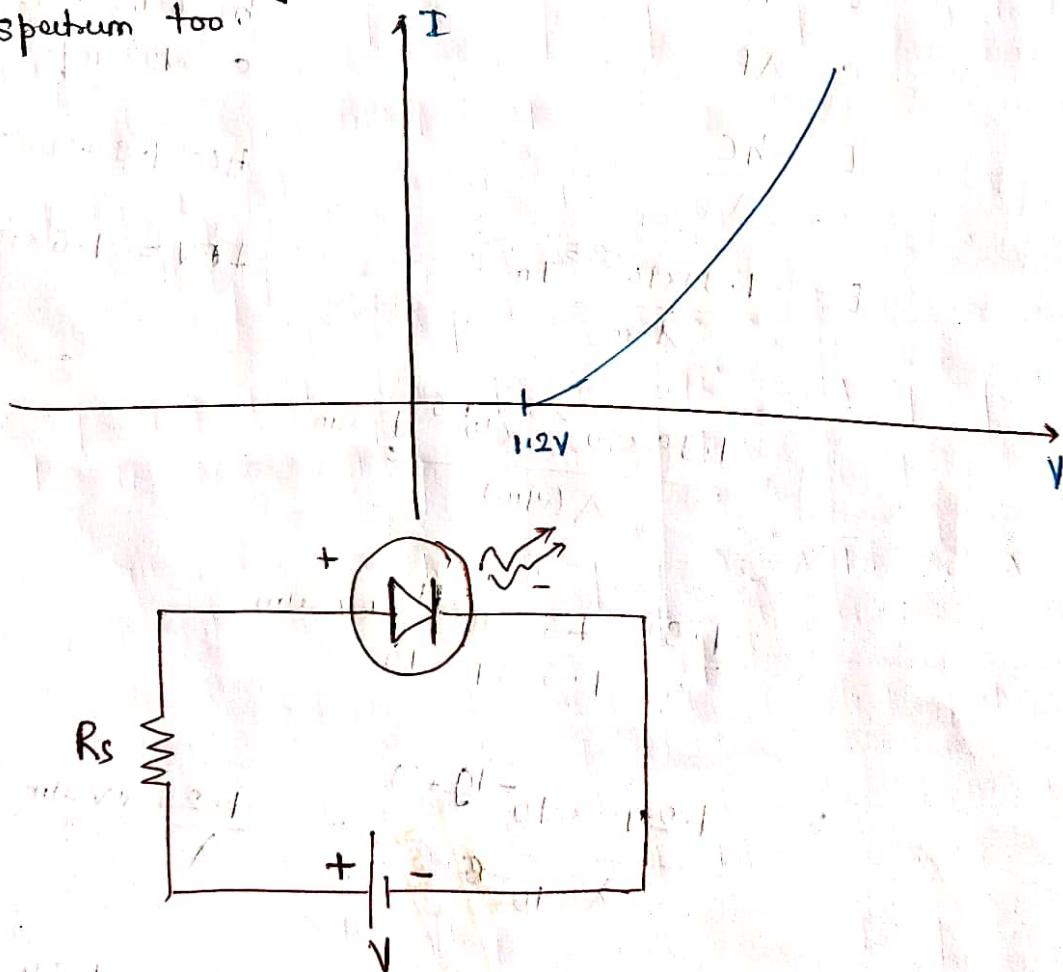
$$\Rightarrow \frac{1.24 \times 10^{-19}}{\lambda \times 10^{-6}} = \frac{1.24 \text{ eV nm}}{\lambda}$$

$$E \Rightarrow \frac{1.24 \times 10^{-6}}{\lambda (\text{nm})} \text{ eV}$$

$$E = \frac{1.24}{\lambda} \text{ eV}$$

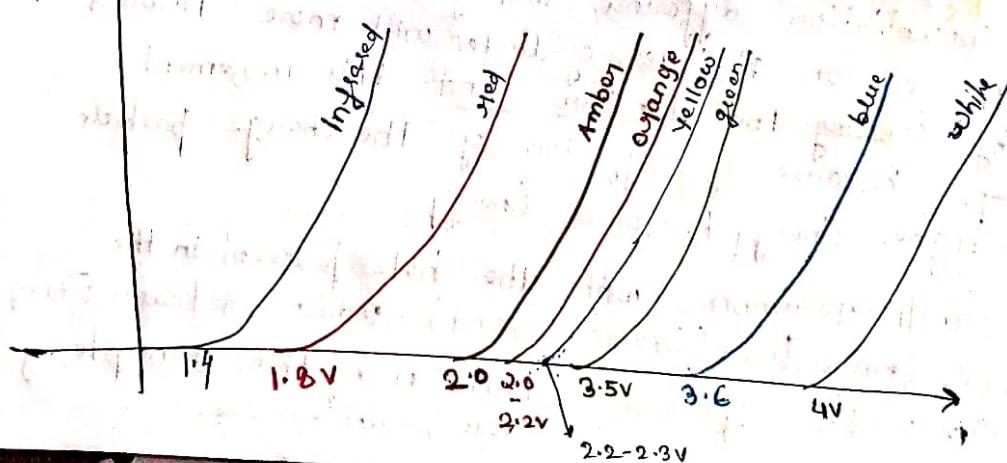
$$E = \frac{1.24 \text{ eV nm}}{\lambda \text{ nm}} \quad (\lambda \text{ is in nm})$$

- LED will emit the light when it is forward biased.
- LED is the best electroluminescence in Semiconductor family
- LED is fabricated with direct band gap Semiconductor material but under special doping condition, Indirect band gap Semiconductor also gives electroluminescence by using the Compound GaP
- Most popularly used LED is Gallium Arsenide which gives infrared radiation when it is forward biased.
- The LED will emit light due to Large no. of recombination of  $e^-$  at the junction of LED diode.
- LED will emit light either in Visible spectrum or in Invisible spectrum too.



- We need a source resistor in series with LEO for the safety of LEO so that if a voltage is applied greater than maximum voltage sustained by LEO then the LEO will get terminate its characteristic.
- The voltage drop across source resistor  $R_s$  will safeguard LEO from getting burnt out.
- If LEO used in remote control then the compound used is GaAs and it radiate Energy in Infrared spectrum.
- For other devices the LEO will radiate Energy in Visible Spectrum and colour are

- Red Green Orange Yellow Blue & Amber White
- i) Red  $\rightarrow$  GaAsP      GaAs  $\rightarrow$  Infrared
  - ii) Yellow  $\rightarrow$  GaAsP:N
  - iii) Orange  $\rightarrow$  GaAsP  
→ Doping conc. of GaAsP when it is radiating orange colour is different due to which the cut-in voltage is approx. 2V
  - iv) Green  $\rightarrow$  AlGaP
  - v) Blue  $\rightarrow$  Silicon Carbide SiC
  - vi) White  $\rightarrow$  GaInN
  - vii) Amber  $\rightarrow$  GaAsP



	<u>Wavelength</u>
Infrared	850 - 940 nm
Red	630 - 660 nm
Amber	605 - 620 nm
Orange	605 - 620 nm
Yellow	585 - 595 nm
Green	550 - 570 nm
Blue	430 - 505 nm
white	450 nm

- The Color of the light depends on four factors of the radiated energy-
  - wavelength of radiated light
  - frequency of the radiated light
  - Dopant (Type of Dopant)
  - Concentration of the dopant
- LED is operated under forward bias with 30mA of forward current. The LED will give maximum Intensity of light.
- The LED will work in the range of 20mA to 30mA (Intensity min at 20mA, Intensity of light Max at 30mA)
- When LED is forward biased, across the Junction of the LED a concentration difference will get rise due to which the e<sup>-</sup> on N Side of diode will move toward P side by crossing the Junction and this movement is b/c because of diffusion of the charge particle from Higher Energy to Lower Energy.

The e<sup>-</sup> will recombine with the hole present in the lower energy level (Valence band) which releases Energy in Visible spectrum. This is by the principle of electroluminescence.