

Paper Id: 110322

Roll No:

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B. TECH.
(SEM-III) THEORY EXAMINATION 2019-20
COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3 Hours

Total Marks: 100

Note: 1. Attempt all Sections. If require any missing data; then choose suitably.

SECTION A1. Attempt *all* questions in brief.

2 x 10 = 20

Qno.	Question	Marks	C O
a.	Define the term Computer Architecture.	2	1
b.	Draw the basic functional units of a computer.	2	1
c.	Perform the 2's complement subtraction of smaller number (101011) from larger number (111001).	2	2
d.	What is the role of Multiplexer and Decoder?	2	2
e.	Write the differences between RISC and CISC.	2	3
f.	What are the types of microinstructions available?	2	3
g.	What is SRAM and DRAM?	2	4
h.	What is the difference between 2D and 2 ^{1/2} D memory organization?	2	4
i.	What is I/O control method?	2	5
j.	What is bus arbitration?	2	5

SECTION B2. Attempt any *three* of the following:

Qno.	Question	Marks	C O
a.	Convert the following arithmetic expressions from infix to reverse polish notation: i. $A*B+C*D+E*F$ ii. $A*[B+C*CD+E]/F*(G+H)$	5+5	1
b.	Design a 4-bit Carry-Look ahead Adder and explain its operation with an example.	10	2
c.	i. Draw the timing diagram for a instruction cycle and explain. ii. Give a note on subroutine.	5+5	3
d.	What do you mean by virtual memory? Discuss how paging helps in implementing virtual memory.	10	4
e.	What is DMA? Describe how DMA is used to transfer data from peripherals.	10	5

SECTION C3. Attempt any *one* part of the following:

Qno.	Question	Marks	C O
a.	Describe in detail the different kinds of addressing modes with an example.	10	1
b.	Discuss stack Organization. Explain the following in details- (i) Register stack (ii) Memory stack	10	1

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4. Attempt any one part of the following:

Qno.	Question	Marks	C O
a.	Represent the following decimal number in IEEE standard floating-point format in a single precision method (32-bit) representation method. i. $(65.175)_{10}$ ii. $(-307.1875)_{10}$	5+5	2
b.	Using Booth algorithm perform the multiplication on the following 6-bit unsigned integer $10110011 * 11010101$	10	2

5. Attempt any one part of the following:

Qno.	Question	Marks	C O
a.	What is parallelism and pipelining in computer Architecture?	10	3
b.	Explain the organization of Microprogrammed control unit in detail.	10	3

6. Attempt any one part of the following:

Qno.	Question	Marks	C O
a.	Discuss the different mapping techniques used in cache memories and their relative merits and demerits.	10	4
b.	RAM chip 4096×8 bits has two enable lines. How many pins are needed for the integrated circuits package? Draw a block diagram and label all input and outputs of the RAM. What is main feature of random-access memory?	5+5	4

7. Attempt any one part of the following:

Qno.	Question	Marks	C O
a.	Write down the difference between isolated I/O and memory mapped I/O. Also discuss advantages and disadvantages of isolated I/O and memory mapped I/O.	10	5
b.	i. Discuss the design of a typical input or output interface. ii. What are interrupts? How are they handled?	10	5

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B. TECH.
(SEM III) THEORY EXAMINATION 2022-23
COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3 Hours**Total Marks: 100****Note:** Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt all questions in brief.**2 x 10 = 20**

- (a) List the steps involved in an instruction cycle.
- (b) How memory read and write operations are performed in computer system?
- (c) Define bus and memory transfer?
- (d) Define HIT and MISS ratio in memory with an example.
- (e) Define instruction cycle.
- (f) Differentiate between RISC and CISC.
- (g) List the difference between static RAM and dynamic RAM.
- (h) Define Virtual memory.
- (i) List down the functions performed by an Input/Output unit.
- (j) Why does the DMA get priority over CPU when both request memory transfer?

SECTION B

2. Attempt any three of the following:**10x3=30**

- (a) Explain functional units of computer system in detail.
- (b) Explain IEEE-754 standard for floating point representation. Express $(314.175)_{10}$ in all the IEEE-754 models.
- (c) Explain the concept of pipelining and also explain types of pipelining.
- (d) Consider a cache consisting of 256 blocks of 16 words each for a total of 4096 words and assume that the main memory is addressable by a 16 bits address and it consists of 4K blocks. How many bits are there in each of TAG, SET, WORD field for 2-way set associative technique?
- (e) Define interrupt. Also discuss different types of interrupt.

SECTION C

3. Attempt any one part of the following:**10x1=10**

- (a) Explain about stack organization used in processors. What do you understand by register stack?
- (b) What is an effective address? How it is calculated in different types of addressing modes? Explain.

4. Attempt any *one* part of the following: 10x1=10

- (a) Describe the derivation procedure of look ahead carry adder by an example with the help of block diagram.
- (b) Show the systematic multiplication process of $(-15) \times (-16)$ using Booth's Algorithm.

5. Attempt any *one* part of the following: 10x1=10

- (a) Write a program to evaluate the arithmetic statement.
$$P = ((X - Y + Z) * (A \wedge B)) / (C \wedge D * E)$$

By using (i) Two address instructions (ii) One address instructions (iii) Zero address instructions
- (b) What are the differences between hardwired and micro-programmed control unit?

6. Attempt any *one* part of the following: 10x1=10

- (a) Discuss the Memory Hierarchy in computer system with regard to Speed, Size and Cost.
- (b) Write a short notes on magnetic disk, magnetic tape and optical disk.

7. Attempt any *one* part of the following: 10x1=10

- (a) With a neat schematic diagram, explain about DMA controller and its mode of data transfer.
- (b) Discuss the design of a typical input or output interface.



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B TECH
(SEM-III) THEORY EXAMINATION 2020-21
COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3 Hours**Total Marks: 100****Note: 1.** Attempt all Sections. If require any missing data; then choose suitably.**SECTION A****1. Attempt all questions in brief.****2 x 10 = 20**

Q no.	Question	Marks	CO
a.	Define the term Computer architecture and Computer organization.	2	1
b.	What is mean by bus arbitration? List different types of bus arbitration.	2	1
c.	Discuss biasing with reference to floating point representation.	2	2
d.	What is restoring method in division algorithm?	2	2
e.	Define micro operation and micro code.	2	3
f.	Write short note on RISC.	2	3
g.	Define hit ratio.	2	4
h.	What do you mean by page fault?	2	4
i.	Explain the term cycle stealing.	2	5
j.	What do you mean by vector interrupt? Explain.	2	5

SECTION B**2. Attempt any three of the following:****3 x 10 = 30**

Q no.	Question	Marks	CO
a.	i. Draw a diagram of bus system using MUX which has four registers of size 4 bits each. ii. Evaluate the arithmetic statement. $X = A + B * [C * D + E * (F + G)]$ using a stack organized computer with zero address operation instructions.	10	1
b.	Explain in detail the principle of carry look ahead adder and design 4-bit CLA adder.	10	2
c.	Draw the flowchart for instruction cycle with neat diagram and explain.	10	3
d.	Discuss 2 D RAM and 2.5D RAM with suitable diagram.	10	4
e.	Draw and explain the block diagram of typical DMA controller.	10	5

SECTION C**3. Attempt any one part of the following:**

Q no.	Question	Marks	CO
a.	An instruction is stored at location 400 with its address field at location 401. The address field has the value 500. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is (i) direct (ii) immediate (iii) relative (iv) register indirect (v) index with R1 as index register	10	1
b.	What do you mean by processor organization? Explain various types of processor organization.	10	1

4. Attempt any one part of the following:

Q no.	Question	Marks	CO
a.	Show the systemic multiplication process of (20) X (-19) using Booth's algorithm	10	2
b.	Explain IEEE standard for floating point representation. Represent the number $(-1460.125)_{10}$ in single precision and double precision format.	10	2



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5. Attempt any one part of the following:

Q no.	Question	Marks	CO
a.	What is a micro program sequencer? With block diagram, explain the working of micro program sequencer.	10	3
b.	Differentiate between hardwired and micro programmed control unit. Explain each component of hardwired control unit organization.	10	3

6. Attempt any one part of the following:

Q no.	Question	Marks	CO
a.	Calculate the page fault for a given string with the help of LRU & FIFO page replacement algorithm, Size of frames = 4 and string 1 2 3 4 2 1 5 6 2 1 2 3 7 6 3 2 1 2 3 6	10	4
b.	A computer uses RAM chips of 1024*1 capacity. i) How many chips are needed & how should their address lines be connected to provide a memory capacity of 1024*8? ii) How many chips are needed to provide a memory capacity of 16 KB?	10	4

7. Attempt any one part of the following:

Q no.	Question	Marks	CO
a.	What do you mean by asynchronous data transfer? Explain strobe control and hand shaking mechanism.	10	5
b.	Discuss the different modes of data transfer.	10	5



BTECH
(SEM III) THEORY EXAMINATION 2021-22
COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3 Hours**Total Marks: 100****Note:** Attempt all Sections. If you require any missing data, then choose suitably.**SECTION A****1. Attempt all questions in brief. 2x10 = 20**

Qno	Questions	CO
(a)	List and briefly define the main structural components of a computer.	CO1
(b)	Differentiate between horizontal and vertical microprogramming.	CO3
(c)	Represent the following conditional control statements by two register transfer statements with control functions. If(P=1) then (R1 ← R2) else if (Q=1) then (R1 ← R3)	CO1
(d)	Design a 4-bit combinational incremental circuit using four full adder circuits.	CO2
(e)	Differentiate between Daisy chaining and centralized parallel arbitration.	CO5
(f)	What is the transfer rate of an eight-track magnetic tape whose speed is 120 inches per second and whose density is 1600 bits per inch?	CO5
(g)	Register A holds the binary values 10011101. What is the register value after arithmetic shift right? Starting from the initial number 10011101, determine the register value after arithmetic shift left, and state whether there is an overflow.	CO2
(h)	What is an Associative memory? What are its advantages and disadvantages?	CO4
(i)	Differentiate between static RAM and Dynamic RAM.	CO4
(j)	What are the different types of instruction formats?	CO3

SECTION B**2. Attempt any three of the following: 10x3 = 30**

Qno	Questions	CO
(a)	A digital computer has a common bus system for 8 registers of 16 bit each. The bus is constructed using multiplexers. I. How many select input are there in each multiplexer? II. What is the size of multiplexers needed? III. How many multiplexers are there in the bus?	CO1
(b)	Explain destination-initiated transfer using handshaking method.	CO5
(c)	Explain 2-bit by 2-bit Array multiplier. Draw the flowchart for divide operation of two numbers in signed magnitude form.	CO2
(d)	A digital computer has a memory unit of 64K X 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words. I. How many bits are there in the tag, index, block, and word fields of the address format? II. How many bits are there in each word of cache, and how they are divided into functions? Include a valid bit. III. How many blocks can the cache accommodate?	CO4
(e)	Explain with neat diagram, the address selection for control memory.	CO3

**BTECH**
(SEM III) THEORY EXAMINATION 2021-22
COMPUTER ORGANIZATION AND ARCHITECTURE**SECTION C**

- 3. Attempt any one part of the following: 10x1 = 10**

Qno	Questions	CO
(a)	A binary floating-point number has seven bits for a biased exponent. The constant used for the bias is 64. I. List the biased representation of all exponents from -64 to +63. II. Show that after addition of two biased exponents, it is necessary to subtract 64 in order to have a biased exponent's sum. III. Show that after subtraction of two biased exponents, it is necessary to add 64 in order to have a biased exponent's difference.	CO2
(b)	Show the multiplication process using Booth algorithm, when the following binary numbers, (+13) x (-15) are multiplied.	CO2

- 4. Attempt any one part of the following: 10x1 = 10**

Qno	Questions	CO
(a)	Draw a diagram of a Bus system in which it uses 3 state buffers and a decoder instead of the multiplexers.	CO1
(b)	Explain in detail multiple bus organization with the help of a diagram.	CO1

- 5. Attempt any one part of the following: 10x1 = 10**

Qno	Questions	CO
(a)	The logical address space in a computer system consists of 128 segments. Each segment can have up to 32 pages of 4K words each. Physical memory consists of 4K blocks of 4K words each. Formulate the logical and physical address formats.	CO4
(b)	How is the Virtual address mapped into physical address? What are the different methods of writing into cache?	CO4

- 6. Attempt any one part of the following: 10x1 = 10**

Qno	Questions	CO
(a)	Explain how the computer buses can be used to communicate with memory and I/O. Also draw the block diagram for CPU-IOP communication.	CO5
(b)	What are the different methods of asynchronous data transfer? Explain in detail.	CO5

- 7. Attempt any one part of the following: 10x1 = 10**

Qno	Questions	CO
(a)	Write a program to evaluate arithmetic expression using stack organized computer with 0-address instructions. $X = (A-B) * (((C - D * E) / F) / G)$	CO3
(b)	List the differences between hardwired and micro programmed control in tabular format. Write the sequence of control steps for the following instruction for single bus architecture. $R1 \leftarrow R2 * (R3)$	CO3

BTECH
(SEM III) THEORY EXAMINATION 2018-19
COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3 Hours

Total Marks: 70

Note: 1. Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt all questions in brief.

2 x 7 = 14

- a. What do you understand by Locality of Reference?
- b. Which of the following architecture is/are not suitable for realizing SIMD?
- c. What is the difference between RAM and DRAM?
- d. What are the difference between Horizontal and vertical micro codes?
- e. Describe cycle stealing in DMA.
- f. List three types of control signals.
- g. Define the role of MIMD in computer architecture.

SECTION B

2. Attempt any three of the following:

7 x 3 = 21

- a. Evaluate the arithmetic statement $X = (A+B) * (C+D)$ using a general register computer with three address, two address and one address instruction format a program to evaluate the expression
- b. Perform the division process of 00001111 by 0011 (use a dividend of 8 bits).
- c. A two way set associative cache memory uses blocks of 4 words. The cache can accommodate a total of 2048 words from memory. The main memory size is 128K X 32.
 - i. Formulate all pertinent information required to construct the cache memory.
 - ii. What is the size of cache memory?
- d. What is associative memory? Explain with the help of a block diagram. Also mention the situation in which associative memory can be effectively utilized.
- e. A Computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers and an address part.
 - (i) How many bits are there in the operation code, the register code part and the address part?
 - (ii) Draw the instruction word format and indicate the number of bits in each part.
 - (iii) How many bits are there in the data and address inputs of the memory?

SECTION C

3. Attempt any **one** part of the following:

7 x 1 = 10

- (a) Write short notes on :
 - (i) Instruction pipeline.
 - (ii) DMA based data transfer.
- (b) Explain the difference between vectored and non-vectored interrupt. Explain stating examples of each.

4. Attempt any **one** part of the following:

7 x 1 = 10

- (a) Draw the flow chart of Booth's Algorithm for multiplication and show the multiplication process using Booth's Algorithm for $(-7) \times (+3)$.
- (b) Write short notes on:
 - (i) Amdahl's Law
 - (ii) Pipelining

5. Attempt any **one** part of the following:

7 x 1 = 10

- (a) What is a microprogram sequencer? With block diagram, explain the working of microprogram sequencer.
- (b) Draw a flowchart for adding and subtracting two fixed point binary numbers where negative numbers are signed 1's complement presentation.

6. Attempt any **one** part of the following:

7 x 1 = 10

- (a) Give the block diagram of DMA controller. Why are the read and write control lines in a DMA controller bidirectional?
- (b) Explain all the phases of instruction cycle.

7. Attempt any **one** part of the following:

7 x 1 = 10

- (a) Explain the basic concept of Hardwired and Software control unit with neat diagrams.

(b)

	1	2	3	4	5	6
S1	X					X
S2		X			X	
S3			X			
S4				X		
S5		X				X

For the following Reservation table:

- i. Calculate the set of the forbidden latencies and collision vector.
- ii. Draw a state diagram, showing all possible initial sequences (cycles) without a collision in the pipeline.
- iii. Simple cycles (SC)
- iv. Greedy cycles among simple the cycles
- v. MAL (minimum average latency)
- vi. What is the minimum allowed constant cycles
- vii. Maxi. Throughput
- viii. Throughput if the minimum constant cycle is used.

B.Tech.
(SEM III) THEORY EXAMINATION 2017-18
COMPUTER ORGANIZATION & ARCHITECTURE

Time: 3 Hours**Total Marks: 70****Note: 1.** Attempt all Sections. If require any missing data; then choose suitably.**SECTION A****1. Attempt all questions in brief. 2 x 7 = 14**

- a. Draw the circuit diagram of D Flip Flop.
- b. Write the difference between RAM & ROM.
- c. Write short note on pipelining process.
- d. Write the difference between serial & parallel communication.
- e. Perform the following operation on signed numbers using 2's compliment method: $(56)_{10} + (-27)_{10}$
- f. Write speed up performance laws.
- g. Differentiate between Horizontal & Vertical microprogramming.

SECTION B**2. Attempt any three of the following: 7 x 3 = 21**

- a. What is programmable logic device? List various techniques to program PLD. Explain any one technique with example.
- b.
 - (i) Draw the block diagram for a small Accumulator based CPU
 - (ii) How floating point numbers are represented in computer, also give IEEE 754 standard 32-bit floating point number format.
- c. Draw the data path of sequential n bit binary divider. Give the non restoring division algorithm for unsigned integers. Also illustrate algorithm for unsigned integer with a suitable example.
- d. What is micro programmed control unit? Give the basic structure of micro programmed control unit. Also discuss the microinstruction format and the control unit organization for a typical micro programmed controllers using suitable diagram.
- e. What do you mean by locality of reference? Explain with suitable example.

SECTION C**3. Attempt any one part of the following: 7 x 1 = 7**

- (a) Differentiate between RISC & CISC based microprocessor.
- (b) Explain Booths multiplication algorithm in detail.

4. Attempt any one part of the following: 7 x 1 = 7

- (a) Draw the Data path of 2's compliment multiplier. Give the Robertson multiplication algorithm for 2's compliment fractions. Also illustrate the algorithm for 2's compliment fraction by a suitable example.
- (b) Describe Sequential Arithmetic & Logic unit (ALU) using proper diagram

5. Attempt any one part of the following: 7 x 1 = 7

- (a) Give the structure of commercial 8MX 8 bit DRAM chip.
- (b) Explain the working of DMA controller with help of suitable diagrams.

6. Attempt any *one* part of the following: **7 x 1 = 7**

- (a) What is hardwired control? List various design methods for hardwired control. Discuss in detail using diagram any one of the method for designing GCD processor.
- (b) How pipeline performance can be measured? Discuss. Give a space time diagram for visualizing the pipeline behavior for a four stage pipeline.

7. Attempt any *one* part of the following: **7 x 1 = 7**

- (a) Discuss the various types of address mapping used in cache memory.
- (b) A moving arm disc storage device has the following specifications:

Number of Tracks per recording surface	200
Disc rotation speed	2400 revolution/minute
Track-storage capacity	62500 bits

Estimate the average latency and data transfer rate of this device.