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SAHIL AGARWAL

Degree	Major	University	Graduation
Master of Science	Computer Science	University of California San Diego	2017 (expected)
Bachelor, Master of Technology	Electrical Engineering	Indian Institute of Technology Bombay	2015

- Obtained **All India Rank** of **176** in **IIT-Joint Entrance Exam** out of 450,000 students ['10]
- One among **35 out of over 35,000 participants** selected for Orientation cum Selection Camp for the **International Physics Olympiad** ['10]

INTERNSHIP EXPERIENCE

Clock Distribution in Integrated Circuits | University of California, San Diego [May'13-July'13]
Research Intern; Guide- Prof Andrew Kahng, CSE

- Performed **worst-case analyses of zero- skew clock trees** (ZSTs) in VLSI Circuits
- Explored and compared the upper bound of ZSTs and other functionals of a geometric point sets
- Showed ZSTs exhibit different growth rates compared to functionals of geometric point sets like Steiner trees.

KEY PROJECTS

Implementation of a Parallel SAT Solver | Master's Thesis [July'14-June'14]

- Developed parallel algorithm using decomposition based technique based on MiniSat 2.2 and GNU parallel
- Obtained **comparable performance** to modern parallel solvers for unsatisfiable instances

Fall Detector and Perimeter Monitoring Unit | Electronics Design Lab [Jan'13-Apr'13]

*Developed a **cheap, wearable prototype** to detect and report if wearer suffers a fall or exits a safe perimeter*

- Implemented using PIC micro-controller, GSM module, GPS module, accelerometer along with a user display
- Received the **Akshay Dhoke Memorial Award** for prototype developed

Elevator Group Control System | Course: VLSI Design Lab [Spring'14]

- Designed a controller to manage a group of 3 elevators in a 7 floor building in **synthesizable VHDL**
- Objective: **Minimize** the waiting time for the user by system optimization

TECHNICAL SKILLS

- **Programming languages**: C/C++, Python (lib: NetworkX, Matplotlib)
- **Tools**: Matlab, Latex, Git
- **Hardware Description**: Verilog HDL, VHDL, Bluespec System Verilog

TEACHING, LEADERSHIP ROLES

Teaching Assistant [July'14-Apr'15]

- (Undergraduate) Digital Systems, (Graduate) Microelectronics Simulation Lab

Tutor in Practical English Training Program [Aug'13-Nov'13]

- Part of a 7 member team to improve practical English knowledge in freshmen weak in the language
- Organized the curriculum of 30 hours of classes; tutored a class of 20 students

Institute Student Mentor [Apr'14-Apr'15]

- Mentoring 12 freshmen; providing guidance in achieving personal, social and academic goals
- Active in dissemination of information through the Freshmen Forum and Practical English Training Program

Department Academic Mentor [Mar'14-Mar'15]

- Guiding, motivating and tutoring two academically underperforming undergraduate students

EXTRA-CURRICULAR ACTIVITIES

- Part of the **IIT Bombay Football Team:** Inter-IIT Camp (Dec'10), MDFA (Mumbai District Football Association) tournament (Aug-Sep'11)
- Declared the **Best Defender** in the Institute Football League among 200 players ['11]
- Awarded **A Grade** in **Basic Mountaineering Course** at ABVIMAS, Manali [May'11]