EE 352 Homework 4
Spring 2010 Nazarian

Name: ______________________ Score:______

Assigned: March 11

Due: Tuesday, March 30 at 9:30am (in class)

1) (12 pts.) A certain memory controller connects a processor with a 32-bit address bus (A31-A0) and **64-bit** data bus to a memory system consisting of 2 SIMM's (ranks). Each SIMM consists of (8) 64M x 8-bit chips (i.e. each addressable unit/column grouping is 8-bits). Each of these chips has 2 banks with 8K rows each. In the table below, show the address bit ranges that will be used for each portion. Do so by writing in An – Am where n and m are the most and least significant bit indexes for that range (e.g. A5-A2).

Unused MSBs	Rank	Row	Bank	Column	Unused (64-bit data bus)

2) (12 pts.) A certain memory controller connects a processor with a 36-bit address bus (A35-A0) and **32-bit** data bus to a memory system consisting of 2 DIMM's (4 ranks). Each DIMM consists of (8) 128M x 4-bit chips (i.e. each addressable unit/column grouping is 4-bits). Each of these chips has 4 banks with 1024 (1K) rows each. In the table below, show the address bit ranges that will be used for each portion. Do so by writing in An – Am where n and m are the most and least significant bit indexes for that range (e.g. A5-A2).

Unused MSBs	Rank	Row	Bank	Column	Unused (32-bit data bus)

3) (18 pts.) A processor has a 32-bit memory address space (i.e. 32-bit addresses). The memory is broken into blocks of 32 **bytes** each (you need to convert to 4-byte words to calculate the word field bits). The computer also has a cache capable of storing 16K **bytes**.

a) How many blocks can the cache store?

b) Assuming the cache uses **direct-mapping**, break the address into TAG, BLOCK, and WORD fields (show which address bits correspond to which field). Show your calculations.

Tag	Block	Word	Unused LSB's

c) Assuming the cache uses a **4-way set-associative mapping**, break the address into TAG, SET, and WORD fields (show which address bits correspond to which field). Show your calculations.

Tag	Set	Word	Unused LSB's

4) (18 pts.) A processor has a 36-bit memory address space (i.e. 36-bit addresses). The memory is broken into blocks of 64 **bytes** each (you need to convert to 4-byte words to calculate the word field bits). The computer also has a cache capable of storing **1 Megabyte**.

a) How many blocks can the cache store?

b) Assuming the cache uses **direct-mapping**, break the address into TAG, BLOCK, and WORD fields (show which address bits correspond to which field). Show your calculations.

c) Assuming the cache uses a **8-way set-associative mapping**, break the address into TAG, SET, and WORD fields (show which address bits correspond to which field). Show your calculations.

5) (20 pts.) Exercises 5.3.5 in CO&D, 4th Ed. page 551. Consider a direct-mapped cache of 64 KB and a block size of 2 words. Generate a series of read requests (address sequence) that will have a lower miss rate on a 2 KB 2-way set associative cache with the same block size than this 64 KB direct mapped cache? Then generate a series of read requests (address sequence) that will have a lower or equal miss rate in the 64KB direct-mapped cache. To make answers more standard, use address that are as small as possible to make your case (i.e. make unneeded tag bits of your address 0 [you should just need to change a few of the LS tag bits] and make the word portion [i.e. LSB] 0 wherever possible).

First do the address breakdown for each cache:

Cache	Tag (A19-A?)	Block or Set	Word	Unused
64 KB, direct, 2 w/block				A1-A0
2 KB, 2-way SA, 2 w/block				A1-A0

For the first question, find a 3 address sequence. Write out your address to **20-bits**. (i.e. 0x00800)

	20-bit address in hex.
1	
2	
3	

For the second question, find a 4 address sequence. Write out your address to **<u>20-bits</u>**. (i.e. 0x00800)

	20-bit address in hex.
1	
2	
3	
4	

6) (20 pts.) Exercises 5.3.3 in CO&D, 4th Ed. page 550. You are asked to optimize a cache design for the given references. There are three direct-mapped cache designs possible, all with a total of eight words of data: C1 has one-word blocks, C2 has two-word blocks, and C3 has four-word blocks. In terms of miss rate, which cache design is best? If the miss stall time is 25 cycles, and C1 has an access time of 2 cycles, C2 takes 3 cycles, and C3 takes 5 cycles, which is the best cache design? (Every access, hit or miss, requires an access to the cache)

Do this exercise only for access pattern **a** below. To make this easier for you, the address sequence has been converted to binary below. NOTE: THESE ADDRESSES are WORD ADDRESSES not BYTE ADDRESSES (i.e. you don't need to leave A1 and A0 unused. First do the address bit breakdown, then complete the table to answer the question.

Address Sequence **a** (Word Addresses)	LS 8-bits of address	C1 Block Answer [0-7] H/M	C2 Block Answer [0-3] H/M	C3 Block Answer [0-1] H/M
1	0000 0001			
134	1000 0110			
212	1101 0100			
1	0000 0001			
135	1000 0111			
213	1101 0101			
162	1010 0010			
161	1010 0001			
2	0000 0010			
44	0010 1100			
41	0010 1001			
221	1101 1101			
Miss Rate		____/12	____/12	___/12
Time		2*12 + ______ = _____	3*12+____ = _____	5*12+____ = _____