Individual Report – Anthony Nguyen

1 Name and Group Members:

- Name: Anthony Nguyen
- Group Members: Sahil Palnitkar, Simon Yao

2 Parts of Design I did Alone:

- Register file
- Half of main
- Decode logic
- ROM to RAM
- Half of Memory Control
- ISA Layout

3 Advantages/Disadvantages

- Advantage: This accurately shows effort required for a CPU architecture design, as different members contribute different parts. It was a great learning experience to figure out how Turing complete machines function.
- Disadvantage: The division of some parts of this project necessitated source control to allow for collaboration on various parts at the same time. However, GitHub proved, only barely sufficient, as the file structure for Logisim files makes it very hard to see what changes were made, to what parts, and where.

4 Design Preference/Improvements

- Superior: I do not believe that any one part was superior for this project. However, after making bugfixes to the hardware logic, it was clear that using multiplexers was superior to other combinatorial logic using basic gates, as it was clearer to see why different inputs were used and how.
- Improvements: Using tunnels was useful in maintaining clarity, however, was not implemented everywhere to show various busses in a more open manner. Using more would clean up the overall look of the circuitry. Furthermore, the processor is relatively slow; relying on no-ops to synchronize each phase. This could be improved with a pipelined architecture.