Final Project Report

Problem 1)

ISA Description and OPcodes

ISA

Instruction	OPcode	Description	Format
`add` `sub` `mul` `div`	`00` `01` `02` `03`	Adds rA to rB Subtracts rA from rB Multiplies rB by rA Divides rB by rA	`00 rA rB` `01 rA rB` `02 rA rB` `03 rA rB`
`mrmov` `rmmov` `rrmov` `irmov`	 `40` `50` `60` `70`	Moves D(rB) to rA Moves rA to D(rB) Moves rB to rA Moves V to rA	 `40 rA rB D` (1 byte) `50 rA rB D` (1 byte) `60 rA rB` `70 rA F V` (1 byte)
`jmp` `jle` `jl` `je` `jne` `jg` `jge`	 `90` `91` `92` `93` `94` `95` `96`	Unconditional jump to Dest Jump <= to Dest Jump < to Dest Jump == to Dest Jump != to Dest Jump > to Dest Jump <= to Dest	`90 FF Dest` (1 byte) `91 FF Dest` (1 byte) `92 FF Dest` (1 byte) `93 FF Dest` (1 byte) `94 FF Dest` (1 byte) `95 FF Dest` (1 byte) `96 FF Dest` (1 byte)
`halt` Maybe `push` `pop`	 `A0` `B0` `C0`	Stops execution Push rA to stack Pop rA from stack	`A0`

Registers

Register	Code
%eax	0
%ebx	1
%ecx	2
%edx	3
%rsp	4
%rbp	5

Flags

Flag	Code
No Flag	00
Neg Flag	01
Zero Flag	10

Problem 2)

The assumptions for Matrix A, B, and C are that they are all 2x2 matrices. The corresponding values from the first value in matrix A and B should be added to produce the first value in matrix C. Continue this for the other 3 values. This produces matrix C. Eax holds the value of matrix A and is added to ebx which holds the matrix B value. The resulting ebx value is pushed for the corresponding matrix C value.

Main:

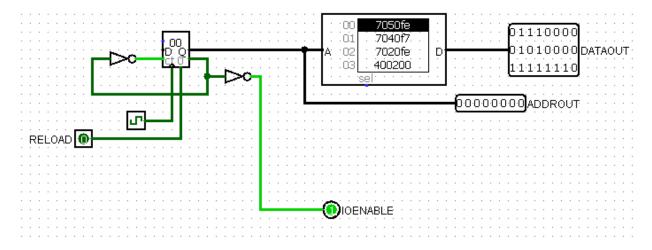
```
#******Setting up base and stack pointer, filling stack
               with matrix values ******
#
irmovl $0xFC, %esp
irmovl $0xFE, %ebp
irmovl $0x05, %eax
pushl %eax
irmovl $0x02, %eax
pushl %eax
irmovl $0x04, %eax
pushl %eax
irmovl $0x03, %eax
pushl %eax
irmovl $0x01, %eax
pushl %eax
irmovl $0x07, %eax
pushl %eax
irmovl $0x09, %eax
pushl %eax
irmovl $0x02, %eax
pushl %eax
#Add first element and push to stack
irmovl $0xF8, %ecx
mrmovl (%ecx), %eax
irmovl $0xe8, %ecx
mrmovl (%ecx), %ebx
addl %eax, %ebx
pushl %ebx
#Add second element and push to stack
irmovl $0xF4, %ecx
mrmovl (%ecx), %eax
irmovl $0xe4, %ecx
mrmovl (%ecx), %ebx
addl %eax, %ebx
pushl %ebx
#Add third element and push to stack
irmovl $0xF0, %ecx
mrmovl (%ecx), %eax
irmovl $0xe0, %ecx
mrmovl (%ecx), %ebx
addl %eax, %ebx
pushl %ebx
#Add fourth element and push to stack
irmovl $0xec, %ecx
mrmovl (%ecx), %eax
irmovl $0xdc, %ecx
mrmovl (%ecx), %ebx
addl %eax, %ebx
pushl %ebx
```

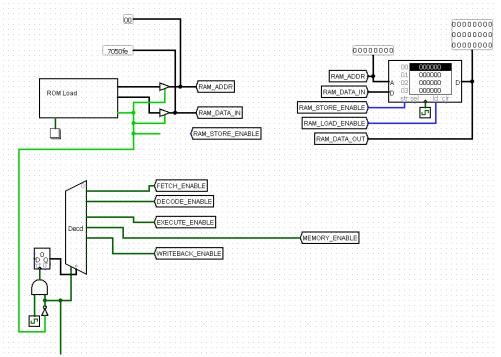
```
[simonyao]@compute ~/CSCE312/Lab5/sim/y86-code> (18:00:51 04/23/19)
:: ../misc/yis finalproject.yo
Stopped in 43 steps at PC = 0xbc. Status 'HLT', CC Z=0 S=0 O=0
Changes to registers:
%eax:
      0x00000000
                       0x00000003
%ecx: 0x00000000
                       0x000000dc
%ebx: 0x00000000
                       0x00000005
%esp: 0x00000000
                       0x000000cc
%ebp: 0x00000000
                       0x000000fe
Changes to memory:
0x00cc: 0x00000000
                       0x00000005
0x00d0: 0x00000000
                       0x0000000d
0x00d4: 0x00000000
                       0x00000009
0x00d8: 0x00000000
                       0x00000006
0x00dc: 0x00000000
                       0x00000002
0x00e0: 0x00000000
                        0x00000009
0x00e4: 0x00000000
                        0x00000007
0x00e8: 0x00000000
                       0x00000001
0x00ec: 0x00000000
                        0x00000003
0x00f0: 0x00000000
                        0x00000004
0x00f4: 0x00000000
                        0x00000002
                       0x00000005
0x00f8: 0x00000000
```

Our ISA program:

irmov irmov irmov mrmov irmov mrmov add	FE -> %ebp F7 -> %esp FE -> %ecx %ecx -> %eax FA -> %ecx %ecx -> %ebx %eax + %ebx	70 70 40 70 40	4 2 0 2 1	0 0 2 0 2	FE F7 FE 00 FA 00
push	%ebx	B1	1	0	01
irmov mrmov irmov mrmov add push	FD -> %ecx %ecx -> %eax F9 -> %ecx %ecx -> %ebx %eax + %ebx %ebx	40 70 40 00	0 2 1 0	2 0 2 1	FD 00 F9 00 00
irmov	FC -> %ecx	70	2	0	FC
mrmov	%ecx -> %eax	40	0	2	00
irmov	F8 -> %ecx	70	2	0	F8
mrmov	%ecx -> %ebx	40	_	_	
add	%eax + %ebx				00
push	%ebx	B1	1	0	01
irmov	FB -> %ecx	70	2	a	FB
mrmov	%ecx -> %eax	40			
irmov	F7 -> %ecx		_		F7
mrmov	%ecx -> %ebx	40			
add	%eax + %ebx	00	0	1	00
push	%ebx	B1	1	0	01

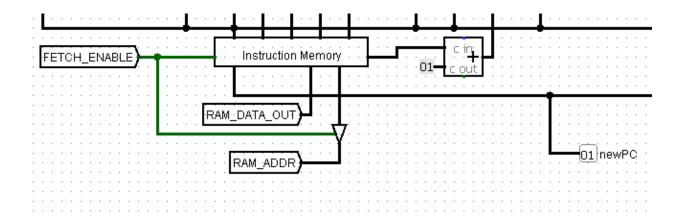
The architecture is divided based upon the Y86 sequential architecture implementation shown in class with the 5 sections fetch, decode, execute, memory, and write back. The PC is then updated. The first step is to load instructions and data from the ROM to the RAM. This is performed in a sub circuit known as the ROM loader. The ROM loader is shown:



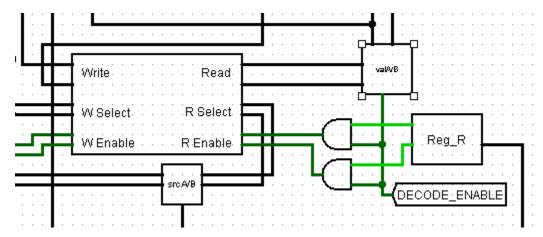


The processor then begins evaluating instructions sequentially based on the 5 steps with implemented no-OP's to compensate for register delay.

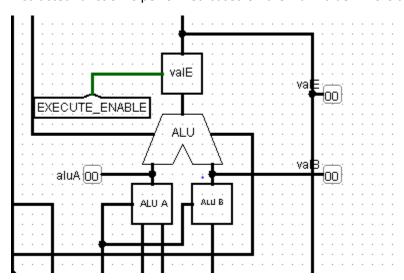
Fetch: For the fetch step, the processor starts at an address of 00. It reads the instructions located at that memory location into the instruction memory register and is used to feed busses that hold the iCode, iFun, rA, rB, and valC.



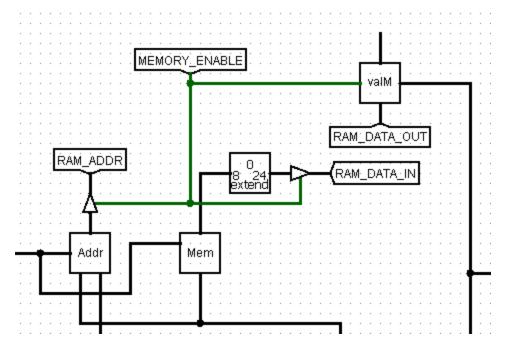
Decode: The decode step is then initiated by using the OP code to decide which sources to read from for the valA and valB busses.



Execute: Next, the execute stage begins where the values at ALU A and B are passed into the ALU. The instructed function is performed based on the iFun value. This is then stored into valE.



Memory: Next, the memory stage is initiated depending on the iCode. It either stores or loads data to/from the RAM. Fetched values are stored in valM.



Write back: Finally, the program writes back data values from valE and/or valM into the register file at the location specified by the instruction. The PC is then incremented based on whether or not a jump was encountered. The processor then loops into the same set of steps.

