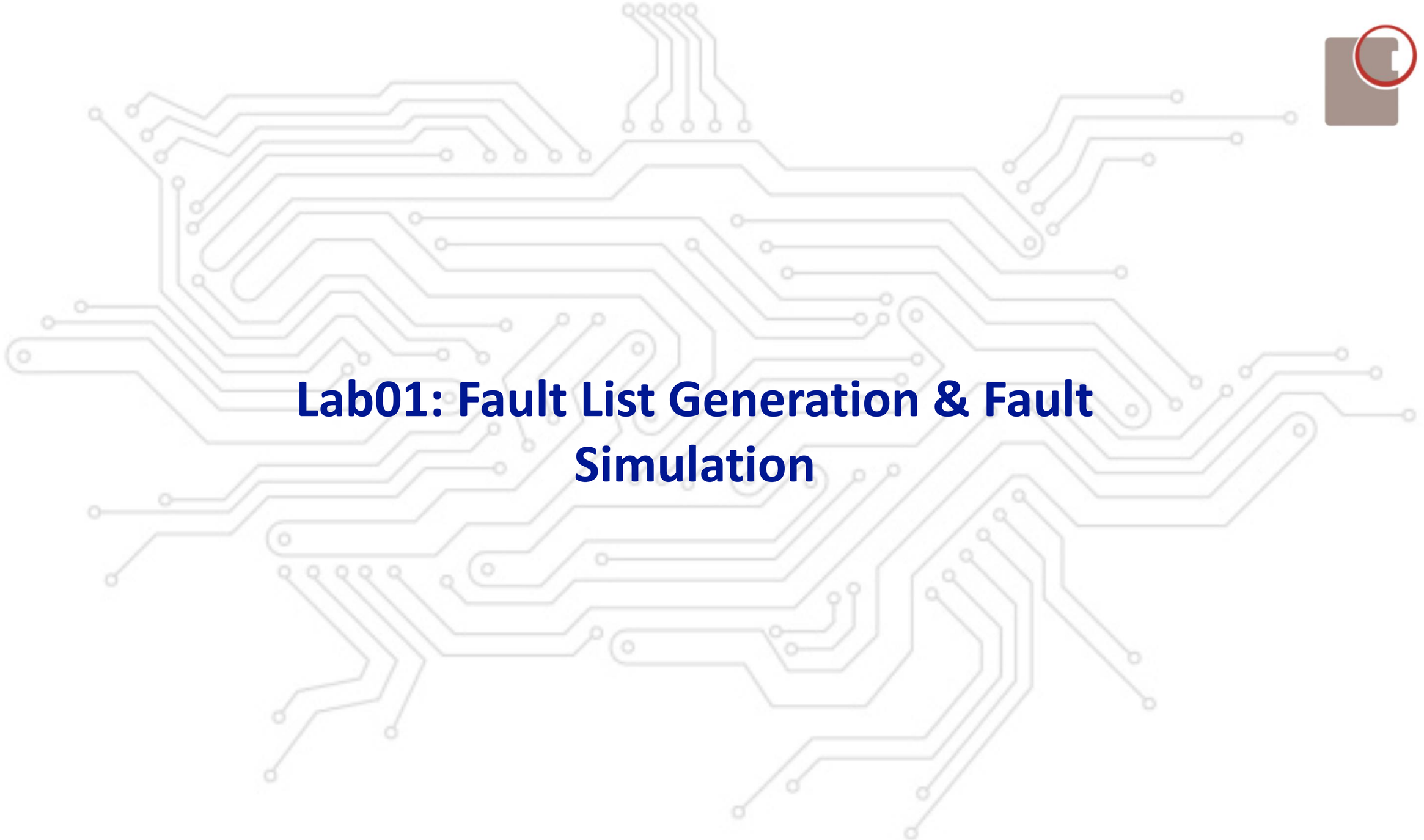


Lab01: Fault List Generation & Fault Simulation

Lab01

Write a script to do the following for a given scan inserted sequential circuit.

- Generate the launch-on capture transition delay fault list and the corresponding fully specified and partially specified test pattern set. (10%)
  - Each fault and test pattern are indexed according to the order in which it appears in the fault list and test pattern file.

Plot the following 4 pictures.

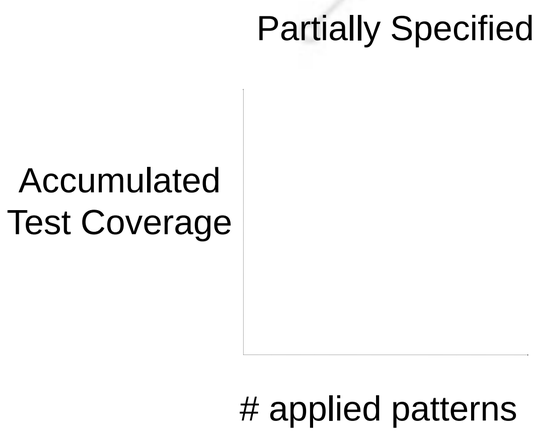
- Accumulated fault coverage vs. the number of applied test patterns (fully/partially specified) (40%)
- A histogram that shows the distribution of the numbers of detected faults (fully/partially specified) (40%)

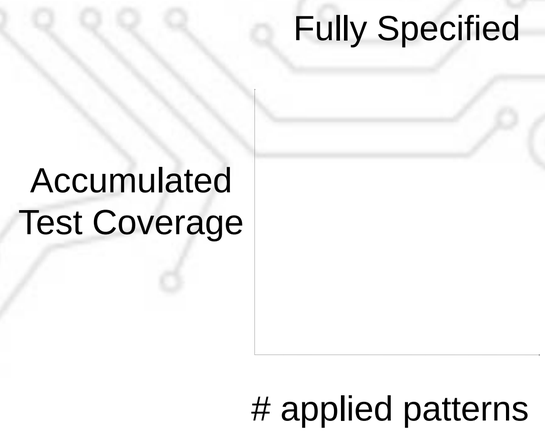
Lab01

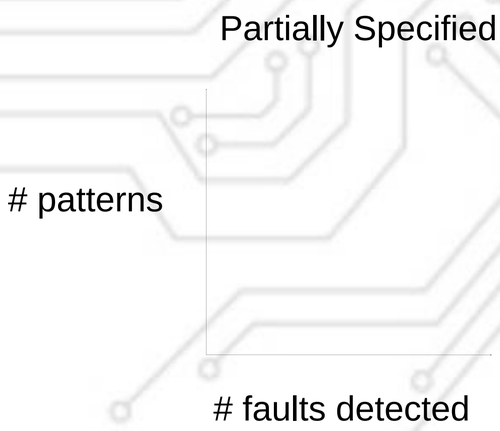
What do you observe from the plots? Try to explain them in report. (10%)

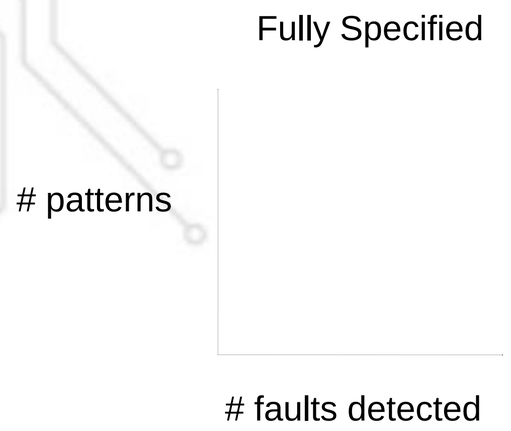
Your script or code submitted will be tested

Tetramax user guideline link: https://reurl.cc/ka90An



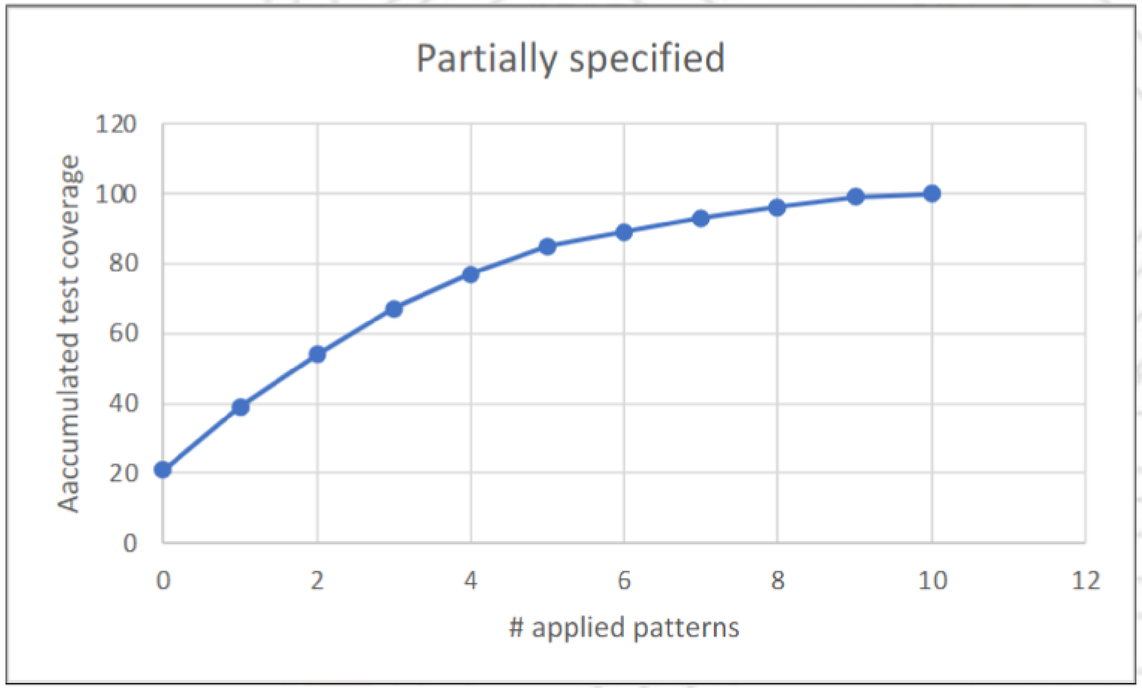


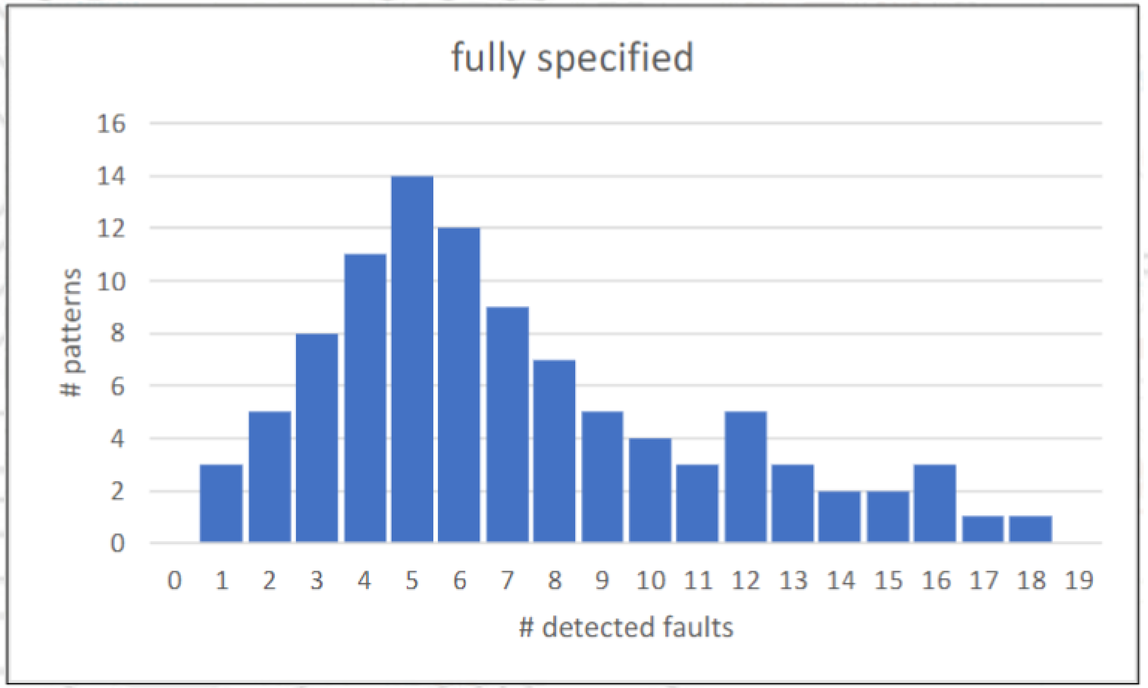




Lab01

Example of pictures





Submission

- Due: November 8, 2024
- Submission via NTU COOL
- Place all your files in a folder (named after your student ID), zip it, and submit the zip file.
- Ex: R13943001_lab1.zip

Submission

- /R13943001_lab1
  - report.pdf (put your pictures in the report)
  - s1238_LOCTDF_fully.fault
  - s1238_LOCTDF_partial.fault
  - s1238_LOCTDF_fully.stil
  - s1238_LOCTDF_partial.stil
  - Tcl script or code to generate your result
  - README.md (explain how to run your script or code)