Logic Synthesis & Verification, Fall 2024

National Taiwan University

Problem Set 5

Due on 2024/12/15 by 23:59.

1 [Technology Mapping]

(24%)

(a) (8%) Given the subject graph of Figure 1, perform SAT based technology mapping to find a legal mapping solution using the library of Figure 2. Show the CNF formula and give a legal mapping solution.

(b) (8%) Given the subject graph of Figure 1, explore different tree partitioning options of the subject graph and perform the DAGON (dynamic programming) algorithm on each tree to find an area-minimum mapping solution using the library of Figure 2 assuming the cost specified in Figure 2 corresponds to gate area. Show all intermediate costs and the final optimum covering.

(c) (8%) Find a minimum-area technology mapping for the subject graph of Figure 1 without tree decomposition.

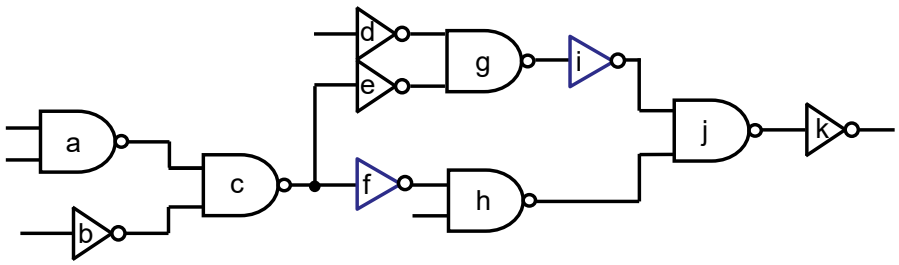

Fig. 1. Subject graph under technology mapping.

2 [Timing Critical Region Property]

(8%) Consider static timing analysis of a circuit. Prove that the critical region in which the slack values are less than or equal to some constant c must consist of paths connecting primary inputs and primary outputs.

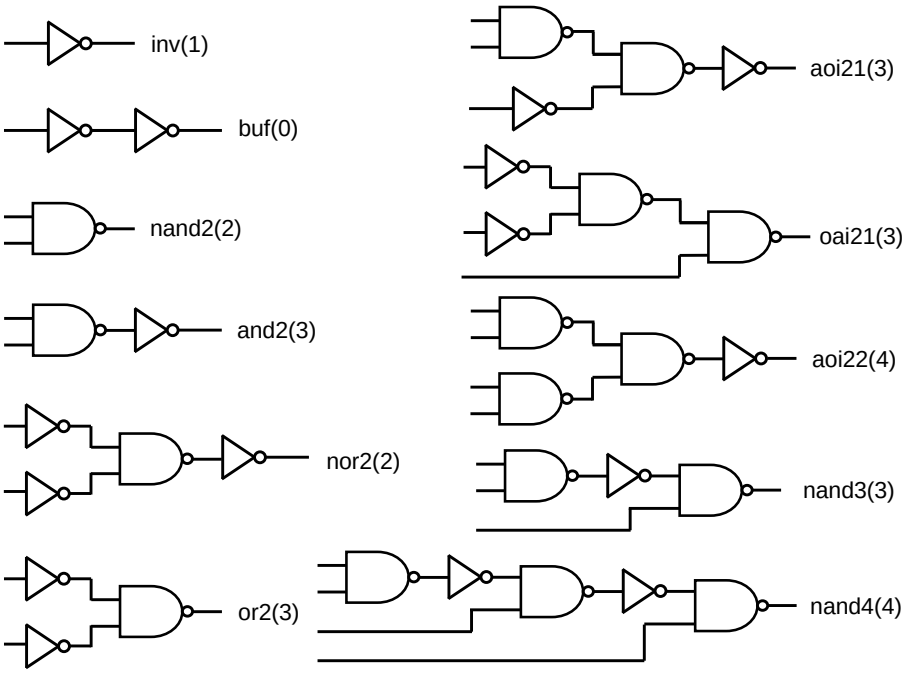

Fig. 2. Pattern graphs.

3 [Static Timing Analysis]

(18%) Consider the circuit of Figure 3.

(a) (14%) Compute the *arrival time*, *required time*, and *slack* of every net.
(b) (4%) Identify the critical region (consisting of gates and wires) with negative slacks in Figure 3. Justify the property stated in Problem 2.

4 [Functional Timing Analysis]

(20%) Consider the circuit of Figure 3.

(a) (4%) Perform X-valued simulation on the circuit to determine the signal steady time for every net under the initial assignment $x_1 = x_2 = x_3 = x_4 = s = 0$ at time 0.
(b) (6%) Perform the SAT-based functional timing analysis on the circuit to determine the longest true delay.
(c) (6%) Given the satisfying assignment in (b) establishing the longest true delay, identify the corresponding longest true delay path. (Hint: You may need the *exact sensitization criterion*, that is, the delay at a gate is determined by

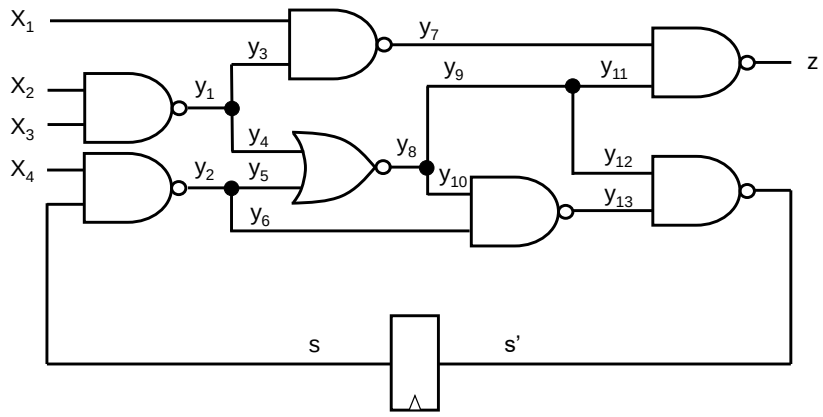

Fig. 3. A circuit under timing analysis, where the clock period is set to 10 ns, the propagation delay and the setup time of the flip-flop are both 1 ns, arrival times for all of the primary inputs are 0, the gate delay of a NAND gate is 2 ns, and the gate delay of a NOR gate is 3 ns.

1) the earliest arrival input with a controlling value, or 2) the latest arrival input when all inputs are of non-controlling values.)

(d) (4%) Continuing (b), determine the minimum clock cycle of the circuit.

5 [Clock Skew Scheduling]

(10%) Consider the circuit of Figure 4. What is the minimum clock period achievable by clock skew scheduling? What are the corresponding skews of r_2, r_3, and r_4 (with respect to the clock edge of r_1)?

6 [Retiming]

(20%) Consider the circuit of Figure 4.

(a) (4%) Draw the corresponding retiming graph. (You may need to create a dummy node for every fanout point.)

(b) (4%) What are the corresponding W and D matrices?

(c) (4%) Write down the inequality constraints of the integer linear program for a retime function r satisfying the condition that the clock period $c \leq 4$ns.

(d) (4%) Draw the corresponding constraint graph for the set of inequality constraints in (c).

(e) (4%) Is there a negative-weighted cycle in the constraint graph? Derive a feasible retime function if it exists.

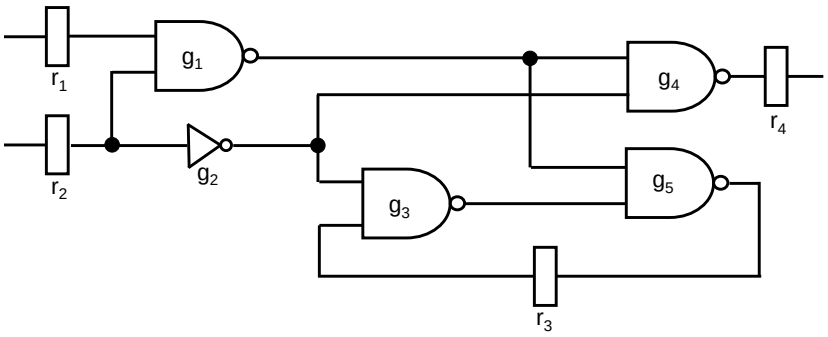

Fig. 4. A circuit under timing optimization, where NAND2 and INV are of gate delays 2ns and 1ns, respectively. Assume the setup and hold times of the registers are 0.