Volume Diagnosis

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Agenda

Central Limit Theorem

Why volume diagnosis

Challenges of Physical Failure Analysis

Layout Aware Diagnosis

Other info used for volume diagnosis

The intent of this lecture is to give an overview of volume diagnosis. Further details can be found in journals, conference papers, or EDA company application notes

Central Limit Theorem

The reason Why many manufacturing process control w/ sampling work

*In many situations, for independent and identically distributed random variables, the sampling distribution of the standardized sample mean tends towards the **standard normal distribution** even if the original variables themselves are not normally distributed.

… It implies that probabilistic and statistical methods that work for normal distributions can be applicable to many problems involving other types of distributions.

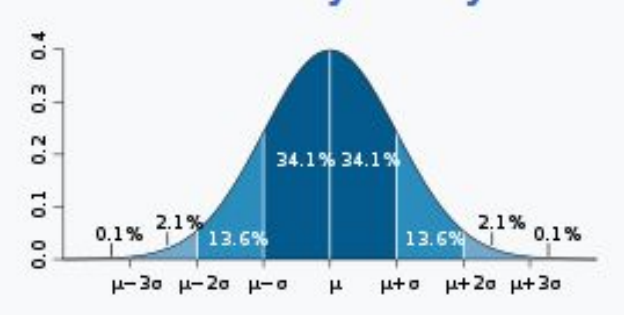
*https://en.wikipedia.org/wiki/Central_limit_theorem

Central Limit Theorem v.s. Normal Distribution

An elementary form of the theorem states the following. Let $X_1, X_2, \ldots, X_n$ denote a random sample of n independent observations from a population with overall expected value (average) μ and finite variance σ^2, and let $\bar{X}_n$ denote the sample mean of that sample (which is itself a random variable). Then the limit as $n \to \infty$ of the distribution of $\frac{\bar{X}_n - \mu}{\sigma_{\bar{X}_n}}$, where $\sigma_{\bar{X}_n} = \frac{\sigma}{\sqrt{n}}$, is the standard normal distribution.[2]

Suppose that a large sample of observations is obtained, each observation being randomly produced in a way that does not depend on the values of the other observations, and that the average (arithmetic mean) of the observed values is computed. If this procedure is performed many times, resulting in a collection of observed averages, the central limit theorem says that if **the sample size was large enough**, the probability distribution of these averages will closely approximate a **normal distribution**

Normal Distribution



The distribution of sample means approximates a **normal distribution** as the sample size gets **larger**, regardless of the population's distribution

2 tail distributions: Mean+-1*stddev ~68.2%, Mean +- 2*stddev ~95.4%, Mean+-3*stddev ~99.7%

Foundry Process Control -> large enough samples -> lots of data collection and data become very useful

Statistical Process Control (SPC)-> take measurements on certain critical parameters of golden samples to monitor machine performance

Why Volume Diagnosis

To improve production yield, solving the “systematic” issues leads to the most significant yield recovery

Systematic test failures could result from a systematic issue as

- Manufacturing defectivity -> modifying process parameters
- Design marginalities -> methodologies to correct the failure-prone design features
- Test overkill -> correcting an error in the test patterns or refining the test conditions

“Volume” diagnosis and debug are therefore critical for yield learning

Mu-Ting Wu, etc. “Improving Volume Diagnosis and Debug with Test Failure Clustering and Reorganization”, ITC 2021

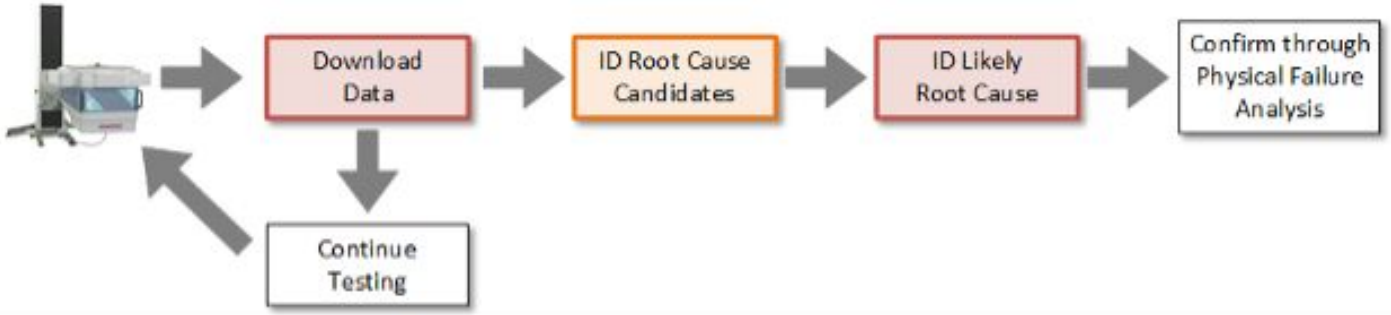
Analysis Process

Extracting information from the tester after the device has failed

Running automated software tools to narrow down the likely root-cause candidates

Further analysis to identify one or two most likely causes

Physical failure analysis to confirm the failure on known-failing devices.



Why Volume Diagnosis

During the New Product Initiative (NPI) stages, failures need to be logged and evaluated to determine which ones are most critical to improving yield. This typically can be done using a Pareto chart to identify **priorities** -> enough volume to see the clear signals.

There are analytics and learning tools that can look at this large volume of data and tell us that there's **a systemic issue**.

https://semiengineering.com/speeding-up-scan-based-volume-diagnosis/

Physical Failure Analysis

Prior to physical failure analysis, the causes are only considered to be likely. It's through physical confirmation that a root cause can be firmly established

Physical analysis process is time-consuming and uses expensive equipment. Ideally, only one candidate would be submitted for verification. Failing that, one must narrow down the candidates to the absolute fewest possible

Poor diagnosis resolution usually originates from

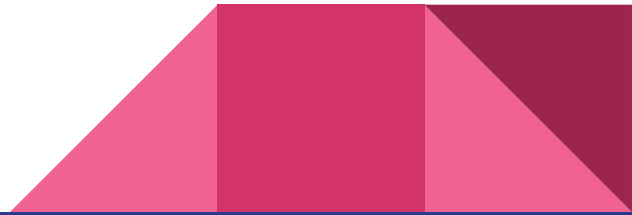
- Test pass simulation fail (TPSF)
- Multiple defect diagnosis
- Compression aliasing

Test Pass Simulation Fail

TPSF (false negative) happens when a defective device passes a test pattern where the fault simulation of the culprit (the actual defect location) produces simulation failure

TPSF makes multiple failing devices with the same defect produce different test failures depending on the severity of defectivity due to process variation

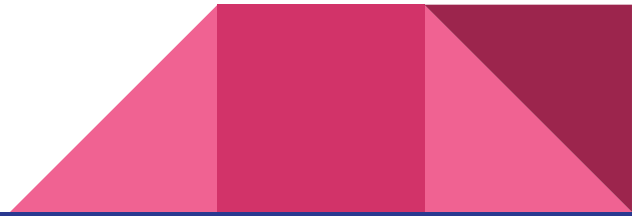
- No failing signature for analysis
- Become Probability or Statistics in nature



Multiple Defects

Multiple defect diagnosis can result in poor diagnosis resolution due to immense search space -> simulation time will be very long

Multiple defects should be the norm



Test Compression Aliasing

Compression aliasing results in many suspects on the fan-in cones of multiple possible failing scan cells -> which one is the good pFA candidate?

How to resolve aliasing

- Apply adaptive diagnosis -> diagnostic ATPG patterns
- Bypassed or Masked patterns (can generate these contents beforehand and add them into fail flow to minimize the test time impact)
- Ranking on the candidates with heuristics

High cost & time overheads

Layout Aware Diagnosis

Layout-aware diagnosis is the process that analyzes scan failures observed on the tester for a defective die to produce a list of suspects that potentially contain the real defect

If a die contains multiple defects, diagnosis arranges the suspects into multiple symptoms, each symptom corresponding to one defect in the die, and each suspect within that symptom representing a potential location and type for the defect

“Logic-based” diagnosis tool faces a fundamental barrier that cannot be overcome by algorithms: It cannot assume where defects are physically possible or not

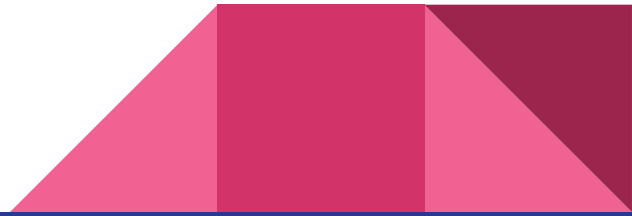
J. D’Souza, “Improving PFA Accuracy and Defect Localization with Volume Scan Diagnosis”, IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits, 2018

Layout Aware Diagnosis

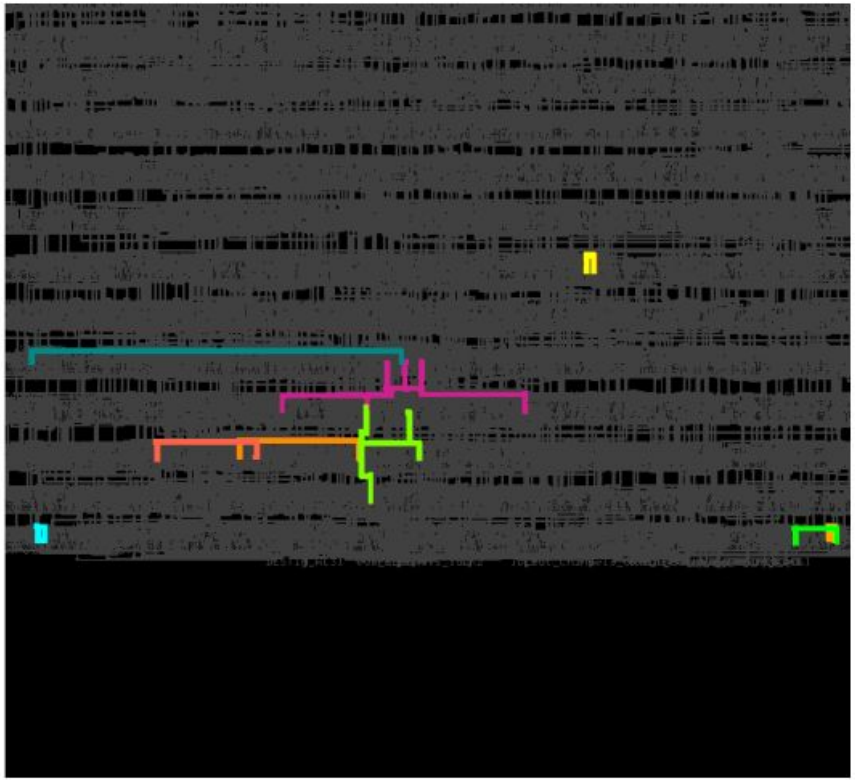
Layout data provides information that can improve the accuracy and resolution of a diagnosis tool

- x-y locations of library cell instances
- polygon shapes
- locations for each polygon of a net, pin, or cell
- the layout hierarchy

Design data must be present in the layout files so that the diagnosis tool can link entities such as net names or cell instances from the design to the layout



Layout Aware Diagnosis



Each of the nets is a valid candidate for a bridge, based on the simulated logic values

With layout info, the reported result would be more meaningful if the candidates can be narrowed down to a most likely net

Three basic types of suspects:

- Opens
- Bridges
- Cell internal (defects inside library cell boundaries)

https://sst.semiconductor-digest.com/wp-content/uploads/whitepapers/mentorpaper_44405.pdf

Cell Aware Diagnosis

The characterization information includes cell input conditions that trigger defect behavior, layout information, defect probability and its related critical area information

Cell characterization is done once per technology library and uses extracted SPICE and GDSII of the cell to simulate all the pertinent information about the cell and its defects called the user-defined fault model (UDFM) format

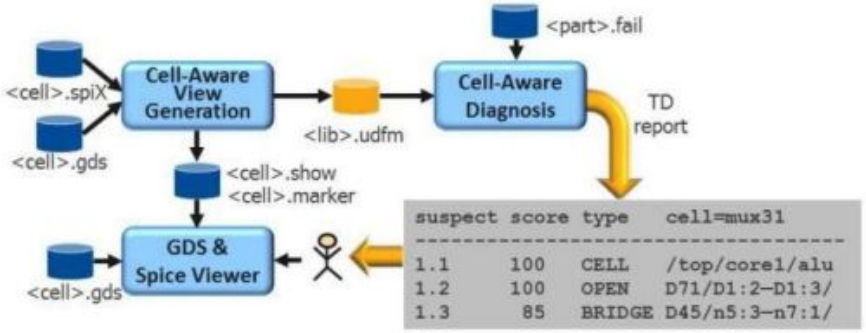
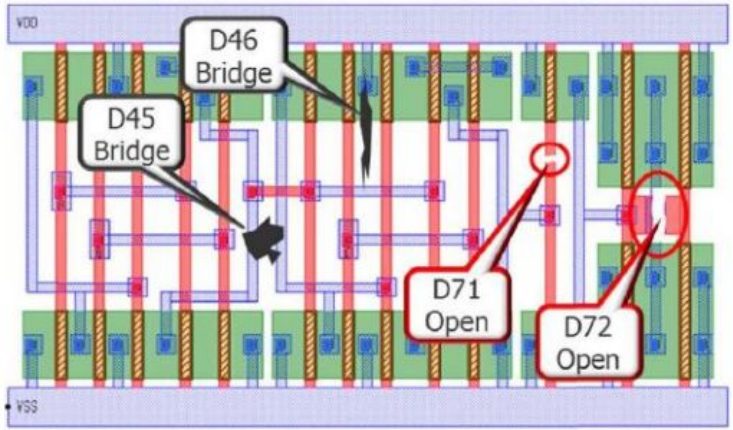
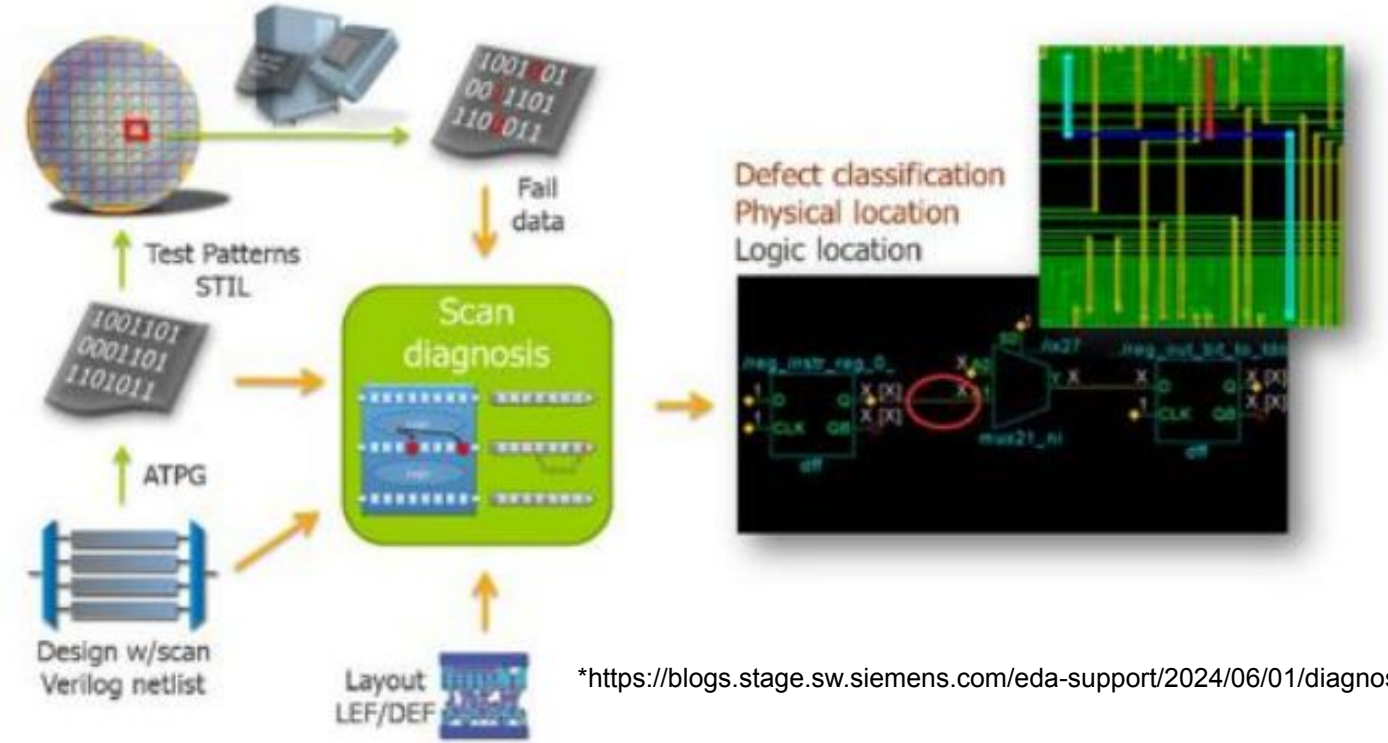


Figure 4: Characterization of cell defects



Layout Aware Diagnosis



*https://blogs.stage.sw.siemens.com/eda-support/2024/06/01/diagnosis-driven-yield-analysis/

LEF DEF Files

LEF (Library Exchange Format) and DEF (Design Exchange Format) files contain all layout and design information required by a diagnosis tool, and usually no translation process is required

Library Exchange Format (LEF): LEF file can be categorized into two parts i.e. Technology LEF and Cell LEF

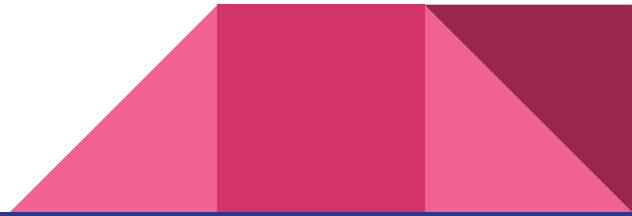
Technology LEF: contains information about technology site, available layers for routing, layer's physical information (pitch, width, spacing, mask, direction etc.), DRC rules, VIA definition, Non-Default Rules (NDR).This file is provided by foundry

Cell LEF: contains information about abstract view of macro and standard cells. There is separate LEF files for macros and standard cells. Standard cell LEF file is provided by foundry, macro LEF file will be provided by foundry or third party vendor

DEF File

Design Exchange Format (DEF): contains placement data of all the physical objects present in the design

As netlist includes logical connectivity, hierarchy information and physical constraints, similarly DEF file contains placement locations, orientation, routing geometry information



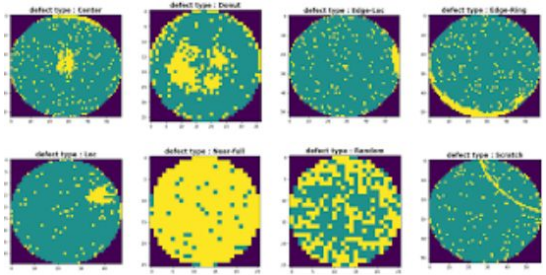
Other Info

Many statistics can use to set the priority of pFA

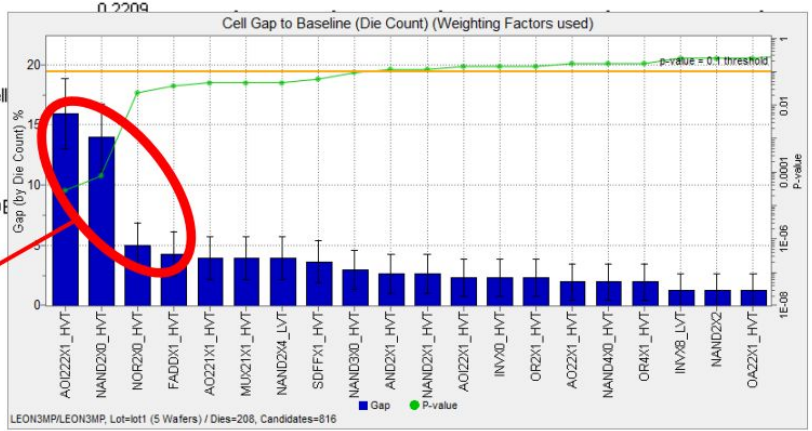
Systematic failure modes with the most yield impact (yield pareto)

The wafer map of the failures

Check for commonality between failures



Control Factor	P-value	Gap %	Count	Percentage	FA Candidate (Ideal)	Strength
DesignBlock	0.0001	89.5	17	5.6	6	4.1
Cell	0.0001	16.8	90	29.9	2	5.0
OpenLayer	0.0602	11.5	59	19.6	6	1.7
Cell + Component	0.0012	5.3	82	27.2	12	3.6
Cell + Placement	0.0012	3.2	33	11.0	0	3.5
DiagClass	0.0315	3.0	81	26.9	11	1.9
ViaLayer	0.0278	2.8	50	16.6	3	2.6
Layer	0.0086	2.0	276	91.7	617	2.3
Instance	0.0001	1.3	37	12.3	2	10.9
Net	0.0001	1.3	34	11.3	10	7.2
Net + Subnet	0.0002	1.0	11	3.7	0	4.6
Placement (Cell)	0.1402	-	-	-	-	-
BridgeLayer	0.2209	-	-	-	-	-
Via						
FaultType						
Component (Cell						
FaultModel						
Diagnosable						
Equipment						
DesignBlock (DE						
CellGroup						



The p-value approach to hypothesis testing uses the calculated probability to determine whether there is evidence to reject the null hypothesis. The null hypothesis is the initial claim about a population. If p value is small (<0.05), the null hypothesis is rejected, i.e. the alternate hypothesis should be true with high confidence

https://www.synopsys.com/solutions/silicon-lifecycle-management/yield-explorer.html

What Else

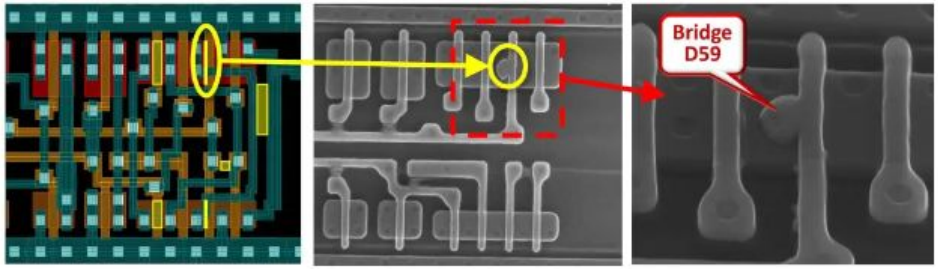
Overlay failed patterns with scan cell switching activity

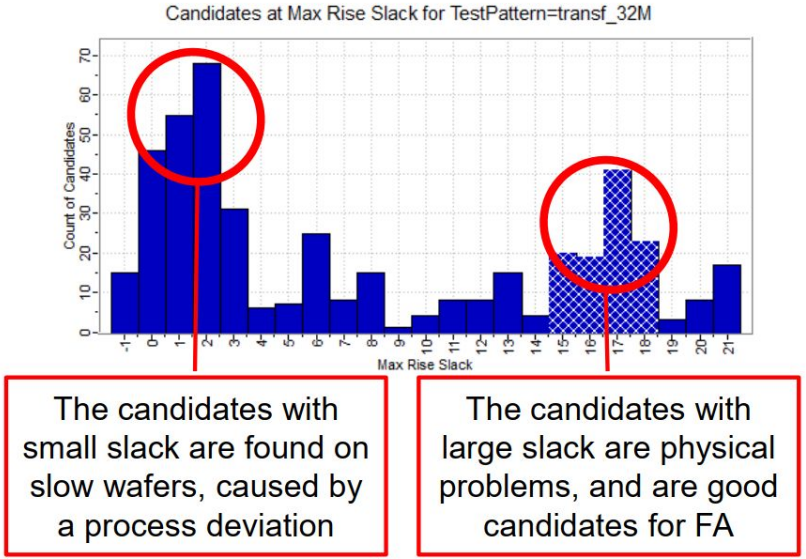
Gross failures caused by power loss

Speedpath info with STA slacks/margins

Hotspot info from DFM/DRC rules - correlated failures from diagnosis results

suspect	score	type	cell=adder
1.1	100	CELL	/top/core1/alu
...	...	...	...
1.6	100	BRIDGE	D59/MP8:G–MN8:D/1.0





"Volume Diagnostics with Static Timing Analysis to improve Yield on Transition Fault test patterns," 8th IEEE International Workshop on Silicon Debug and Diagnosis ITC 2012