Logic Synthesis & Verification, Fall 2024

National Taiwan University

Reference Solution for Problem Set 5

1 [Technology Mapping]

(a) Let the inputs be x_1, x_2, x_3, x_4, x_5 respectively, as shown in figure 1.

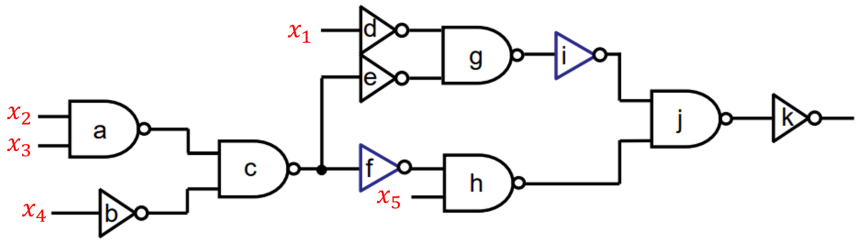


Fig. 1. The subject graph with named input.

The possible matches for all nodes are as shown in table 1.
First, we generate the clauses for the constraint that every node must be covered by one or more pattern graphs.

$$
\begin{aligned}
C_1 = &(m_1 + m_7 + m_{10}) \\
&(m_2 + m_7 + m_{10}) \\
&(m_3 + m_6 + m_7 + m_9 + m_{10} + m_{13} + m_{15} + m_{21}) \\
&(m_4 + m_{12} + m_{18}) \\
&(m_5 + m_6 + m_7 + m_{12} + m_{13} + m_{18} + m_{21}) \\
&(m_8 + m_9 + m_{10} + m_{15}) \\
&(m_{11} + m_{12} + m_{13} + m_{17} + m_{18} + m_{20} + m_{21}) \\
&(m_{14} + m_{15} + m_{24}) \\
&(m_{16} + m_{17} + m_{18} + m_{20} + m_{21} + m_{24}) \\
&(m_{19} + m_{20} + m_{21} + m_{23} + m_{24}) \\
&(m_{22} + m_{23} + m_{24})
\end{aligned}
$$

Table 1. The possible matches for all nodes.

Match	Gate	Cost	Inputs	Root	Covers
m_1	nand2	2	x_2, x_3	a	a
m_2	inv	1	x_4	b	b
m_3	nand2	2	a, b	c	c
m_4	inv	1	x_1	d	d
m_5	inv	1	c	e	e
m_6	and2	3	a, b	e	c, e
m_7	aoi21	3	x_2, x_3, x_4	e	a, b, c, e
m_8	inv	1	c	f	f
m_9	and2	3	a, b	f	c, f
m_{10}	aoi21	3	x_2, x_3, x_4	f	a, b, c, f
m_{11}	nand2	2	d, e	g	g
m_{12}	or2	3	x_1, c	g	d, e, g
m_{13}	nand3	3	a, b, d	g	c, e, g
m_{14}	nand2	2	x_5, f	h	h
m_{15}	nand3	3	x_5, a, b	h	c, f, h
m_{16}	inv	1	g	i	i
m_{17}	and2	3	d, e	i	g, i
m_{18}	nor2	2	x_1, c	i	d, e, g, i
m_{19}	nand2	2	h, i	j	j
m_{20}	nand3	3	d, e, h	j	g, i, j
m_{21}	nand4	4	a, b, d, h	j	c, e, g, i, j
m_{22}	inv	1	j	k	k
m_{23}	and2	3	h, i	k	j, k
m_{24}	aoi21	3	x_5, f, g	k	h, i, j, k

Then, we generate the clauses for constraint (2).

$$
\begin{aligned}
C_2 =&(m'_3 + m_1)(m'_3 + m_2)\\
&(m'_5 + m_3)\\
&(m'_6 + m_1)(m'_6 + m_2)\\
&(m'_8 + m_3)\\
&(m'_9 + m_1)(m'_9 + m_2)\\
&(m'_{11} + m_4)(m'_{11} + m_5 + m_6 + m_7)\\
&(m'_{12} + m_3)\\
&(m'_{13} + m_1)(m'_{13} + m_2)(m'_{13} + m_4)\\
&(m'_{14} + m_8 + m_9 + m_{10})\\
&(m'_{15} + m_1)(m'_{15} + m_2)\\
&(m'_{16} + m_{11} + m_{12} + m_{13})\\
&(m'_{17} + m_4)(m'_{17} + m_5 + m_6 + m_7)\\
&(m'_{18} + m_3)\\
&(m'_{19} + m_{14} + m_{15})(m'_{19} + m_{16} + m_{17} + m_{18})\\
&(m'_{20} + m_4)(m'_{20} + m_5 + m_6 + m_7)(m'_{20} + m_{14} + m_{15})\\
&(m'_{21} + m_1)(m'_{21} + m_2)(m'_{21} + m_4)(m'_{21} + m_{14} + m_{15})\\
&(m'_{22} + m_{19} + m_{20})\\
&(m'_{23} + m_{14} + m_{15})(m'_{23} + m_{16} + m_{17} + m_{18})\\
&(m'_{24} + m_8 + m_9 + m_{10})(m'_{24} + m_{11} + m_{12} + m_{13})
\end{aligned}
$$

The whole CNF formula is $C_1 \wedge C_2$. A satisfying solution is $\{m_1, m_2, m_3, m_8, m_{12}, m_{24}\}$ assigned to 1, and other variables assigned to 0.

(b) The results of two different tree partitioning options are shown in figure 2 and figure 3, respectively. The pattern graphs in red text are selected.

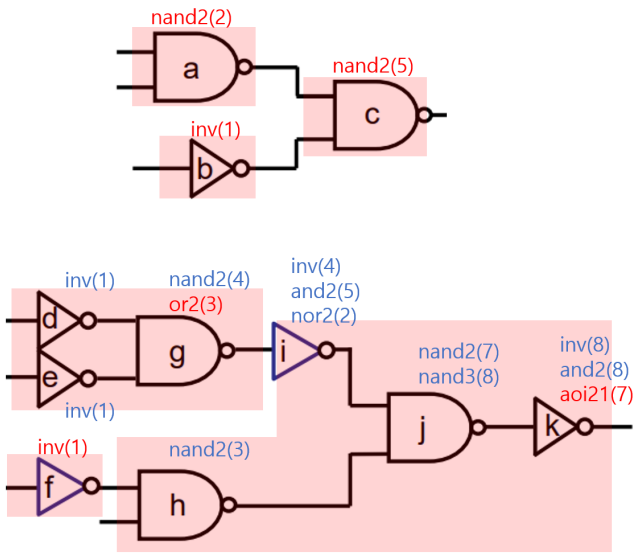


Fig. 2. Performing DAGON with trivial partition (two trees.) The resulting optimum covering has an area of $5 + 7 = 12$.

(c) The results in (b) with an area of 12 are already optimal.
In addition, if we merge node e and node f (share the same pattern graph), an area-minimum cover can be derived as shown in fig. 4. Both answers are acceptable.

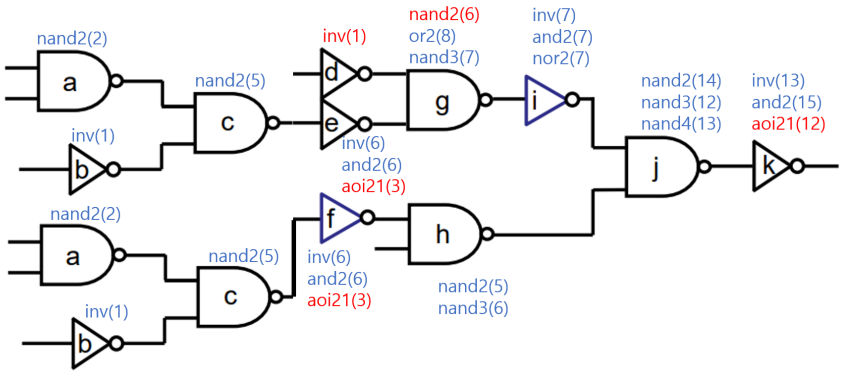


Fig. 3. Performing DAGON with single-cone partition. The resulting optimum covering has an area of 12.

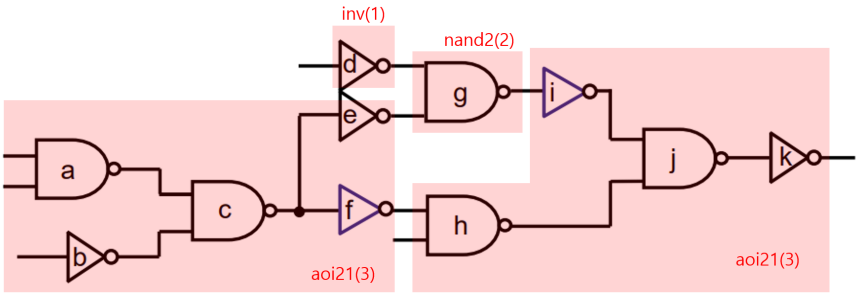


Fig. 4. An area-minimum cover with an area of 9. Node e and f share the same pattern graph.

2 [Timing Critical Region Property]

Let e be an edge (wire segment) from node X to node Y with slack value $S(e) \leq c$. Note that a node can be a gate, primary output (PI), primary input (PO), or a connection between a fanout stem and fanout branches. Let the fanin edges of X be $x_1, \cdots, x_n$, and the fanout edges of Y be $y_1, \cdots, y_m$. Let $D(X)$ denotes the delay of node X. Let $A(e), R(e), S(e)$ denote the arrival time, required time, and slack value respectively.

Lemma 1. *If X is not a PI, there exists a fanin edge x_i such that $S(x_i) \leq S(e)$.*

Proof: $R(x_i) \leq R(e) - D(X)$ for all x_i. Also, since $A(e) = \max\{A(x_1), \cdots, A(x_n)\} + D(X)$, there exists x_i s.t. $A(x_i) = A(e) - D(X)$. Therefore,

$$S(x_i) = R(x_i) - A(x_i) \leq (R(e) - D(e)) - (A(e) - D(e)) = S(e).$$

Lemma 2. *If Y is not a PO, there exists a fanout edge y_i such that $S(y_i) \leq S(e)$.*

Proof: $A(y_i) \geq R(e) + D(Y)$ for all y_i. Also, since $R(e) = \min\{R(y_1), \cdots, R(y_m)\} - D(X)$, there exists y_i s.t. $R(y_i) = R(e) + D(Y)$. Therefore,

$$S(y_i) = R(y_i) - A(y_i) \leq (R(e) + D(e)) - (A(e) + D(e)) = S(e).$$

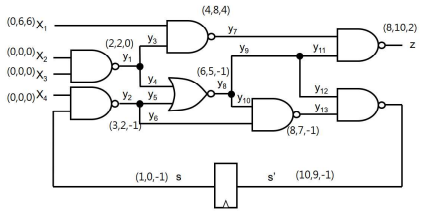
As a result, for any edge e with slack $S(e) \leq c$ in the critical region, a path P from PI to PO containing e s.t.

$$S(x) \leq S(e) \leq c \quad \forall x \in P$$

must exist according to lemma 1 and lemma 2. Thus, all the edges in the region belong to some paths in this region from PIs to POs. Therefore, the region must consist of paths from PI to PO.

Problem 3: Static Timing Analysis

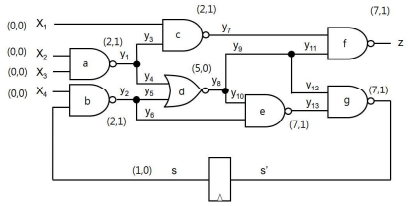
(a) (20%) We denote the arrival time, required time and slack of each node as a 3-tuple (a, r, s). The result is shown below.



(b) (4%) The timing critical region is s, y_2, y_6, y_{13}, s' and the 3 NAND gates in between. This is indeed a path from (pseudo) PI to (pseudo) PO, i.e. the property stated in Problem 2 is satisfied.

Problem 4: Functional Timing Analysis

(a) (5%) We annotate each signal with a 2-tuple (t, x), where t denotes the time where the value stables, and x denotes the stable value. The result is shown below.



(b) (12%) We shall also take the setup time and propagation time of the flip-flop into consideration. Based on the result from static timing analysis, we set $L = 11$, and based on the result from Problem 4, we may set $L_{\text{old}} = 7$. We shall refer to each gate as labeled in Problem 4.

Thus, we first check the case where $L = 9$. We start by computing the onset for z, which is

$$\begin{aligned} f(1, t = 9) &= c(0, t = 7) \cup d(0, t = 7) \\ &= (x_1(1, t = 5) \cap a(1, t = 5)) \cup (a(1, t = 4) \cup b(1, t = 4)) \\ &= (x_1(x_2(0, t = 3) \cup x_3(0, t = 3))) \cup ((x_2(0, t = 2) \cup x_3(0, t = 2)) \cup (x_4(0, t = 2) \cup s(0, t = \\ &= x_1(\neg x_2 + \neg x_3) + (\neg x_2 + \neg x_3) + (\neg x_4 + \neg s) \\ &= \neg x_2 + \neg x_3 + \neg x_4 + \neg s\,. \end{aligned}$$

Note that no timing related simplification occurred, hence z is always stable within 9ns, and we don't need to compute its offset.

Next compute the onset for s', which is

$$\begin{aligned} g(1, t = 8) &= d(0, t = 6) \cup e(0, t = 6) \\ &= (a(1, t = 3) \cup b(1, t = 3)) \cup (d(1, t = 4) \cap b(1, t = 4)) \\ &= ((x_2(0, t = 1) \cup x_3(0, t = 1)) \cup (x_4(0, t = 1) \cup s(0, t = 1))) \\ &\quad \cup ((a(0, t = 1) \cap b(0, t = 1)) \cap (x_4(0, t = 2) \cup s(0, t = 2))) \\ &= ((\neg x_2 + \neg x_3) \cup (\neg x_4 + \neg s)) \cup ((\varnothing) \cap (\neg x_4 + \neg s)) \\ &= \neg x_2 + \neg x_3 + \neg x_4 + \neg s\,. \end{aligned}$$

Note that $L - 1 = 8$ is used due to the setup time condition.

The onset of s' is also

$$\begin{aligned} g &= \neg d + \neg e \\ &= (a + b) + bd \\ &= a + b \\ &= \neg x_2 + \neg x_3 + \neg x_4 + \neg s\,. \end{aligned}$$

Next compute the offset for s', which is

$$\begin{aligned} g(0, t = 8) &= d(1, t = 6) \cap e(1, t = 6) \\ &= (a(0, t = 3) \cap b(0, t = 3)) \cap (d(0, t = 4) \cup b(0, t = 4)) \\ &= ((x_2(1, t = 1) \cap x_3(1, t = 1)) \cap (x_4(1, t = 1) \cap s(1, t = 1))) \\ &\quad \cap ((a(1, t = 1) \cup b(1, t = 1)) \cup (x_4(1, t = 2) \cap s(1, t = 2))) \\ &= (x_2x_3x_4 \cap s) \cap ((\varnothing) \cup (x_4s)) \\ &= x_2x_3x_4 \cap s \\ &= \neg g\,. \end{aligned}$$

We can thus update $L_{\text{old}} = 9$ and $L = 8$.

We start by computing the onset for z, which is

$$\begin{aligned} f(1, t = 8) &= c(0, t = 6) \cup d(0, t = 6) \\ &= (x_1(1, t = 4) \cap a(1, t = 4)) \cup (a(1, t = 3) \cup b(1, t = 3)) \\ &= (x_1(x_2(0, t = 2) \cup x_3(0, t = 2))) \cup ((x_2(0, t = 1) \cup x_3(0, t = 1)) \cup (x_4(0, t = 1) \cup s(0, t = \\ &= x_1(\neg x_2 + \neg x_3) + (\neg x_2 + \neg x_3) + (\neg x_4 + \neg s) \\ &= \neg x_2 + \neg x_3 + \neg x_4 + \neg s\,. \end{aligned}$$

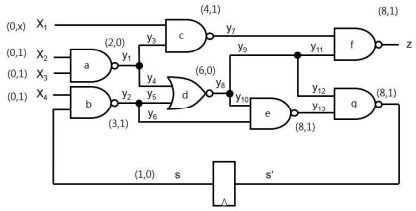
Again, as no timing related simplification occurred, z is always stable within 8ns, and we don't need to compute its offset.

Next compute the onset for s', which is

$$\begin{aligned} g(1, t = 7) &= d(0, t = 5) \cup e(0, t = 5) \\ &= (a(1, t = 2) \cup b(1, t = 2)) \cup (d(1, t = 3) \cap b(1, t = 3)) \\ &= ((x_2(0, t = 0) \cup x_3(0, t = 0)) \cup (x_4(0, t = 0) \cup s(0, t = 0))) \\ &\quad \cup ((a(0, t = 0) \cap b(0, t = 0)) \cap (x_4(0, t = 1) \cup s(0, t = 1))) \\ &= ((\neg x_2 + \neg x_3) + \neg x_4) \cup (\varnothing \cap (\neg x_4 + \neg s)) \\ &= \neg x_2 + \neg x_3 + \neg x_4 \\ &\neq g\,. \end{aligned}$$

We conclude that there is an input vector under which an output gets stable after 8ns, namely $x_2 x_3 x_4 \neg s$ (x_1 don't care).

(c) (8%) We first perform x-value simulation with the input. The result is shown below.



Clearly, the critical path is the one that feed from g to s'. Tracing back, we can see that $d = 0$ is g's controlling value, $b = 1$ is d's controlling value, and $s = 0$ is b's controlling value.

Hence, the longest true delay path is $s, b, y_5, d, y_{12}, g, s'$.

(d) (5%) The minimum clock cycle is 9ns.

5 [Clock Skew Scheduling]

By performing static timing analysis assuming there is no clock skew, we can compute the maximum and minimum delay between registers as shown in fig. 1.

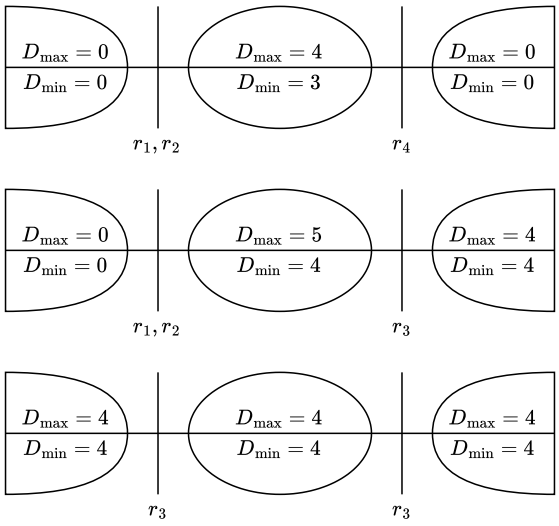


Fig. 1. Maximum and minimum delay between transistors when skew= 0.

From fig. 1, we can see that the minimum achievable clock period must be at least 4ns since the skew from r_3 to r_3 must be 0. By changing the clock delay of r_3 to 1ns, we can achieve $D_{\max} = 4$ as shown in fig. 2. The minimum achievable clock period is thus 4ns. Note that the output register of r_3 is itself.

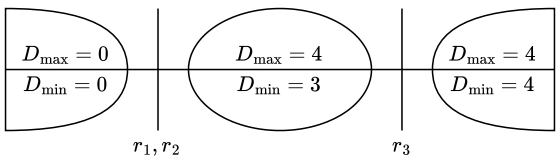


Fig. 2. Maximum and minimum delay when r_3 has a clock delay of 1ns.

Alternatively, by changing the clock delay of r_1 and r_2 to -1ns, we can also achieve $D_{\max} = 4$ as shown in fig. 3. The minimum achievable clock period is thus 4ns.

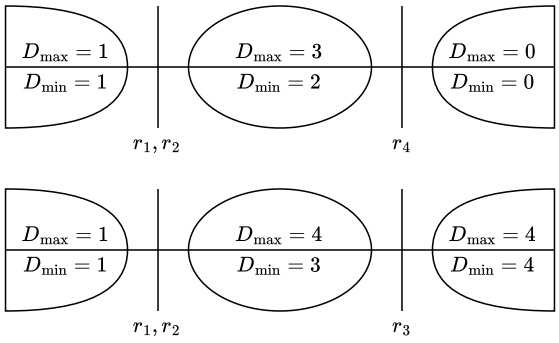


Fig. 3. Maximum and minimum delay when r_1 and r_2 have a clock delay of -1ns.

The clock delay of $(r2, r3, r4)$ with respect to $r1$ can be $(0, 1, 0)$ or $(0, 1, 1)$.

6 [Retiming]

(a) The retiming graph is shown in fig. 4.

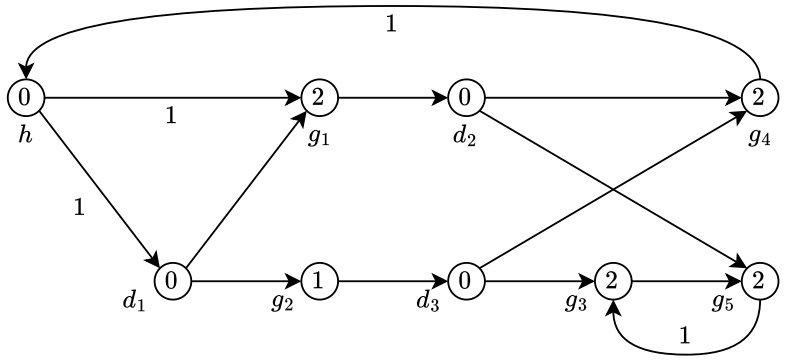


Fig. 4. The retiming graph where d_i are dummy nodes and h is the primary inputs and outputs. The weight (number of registers) of each edge is zero if not specifed.

Table 1. The W matrix in problem 6(b). The elements in red text are included in the delay constraints.

	h	d1	g1	d2	g2	d3	g3	g4	g5
h	0	1	1	1	1	1	1	1	1
d1	1	0	0	0	0	0	0	0	0
g1	1	$\perp$	0	0	$\perp$	$\perp$	1	0	0
d2	1	$\perp$	$\perp$	0	$\perp$	$\perp$	1	0	0
g2	1	$\perp$	$\perp$	$\perp$	0	0	0	0	0
d3	1	$\perp$	$\perp$	$\perp$	$\perp$	0	0	0	0
g3	$\perp$	$\perp$	$\perp$	$\perp$	$\perp$	$\perp$	0	$\perp$	0
g4	1	$\perp$	$\perp$	$\perp$	$\perp$	$\perp$	$\perp$	0	$\perp$
g5	$\perp$	$\perp$	$\perp$	$\perp$	$\perp$	$\perp$	1	$\perp$	0

Table 2. The D matrix in problem 6(b). The elements in red text are included in the delay constraints.

	h	d1	g1	d2	g2	d3	g3	g4	g5
h	0	0	2	2	1	1	3	4	5
d1	4	0	2	2	1	1	3	4	5
g1	4	$\perp$	2	2	$\perp$	$\perp$	6	4	4
d2	2	$\perp$	$\perp$	0	$\perp$	$\perp$	4	2	2
g2	3	$\perp$	$\perp$	$\perp$	1	1	3	3	5
d3	2	$\perp$	$\perp$	$\perp$	$\perp$	0	2	2	4
g3	$\perp$	$\perp$	$\perp$	$\perp$	$\perp$	$\perp$	2	$\perp$	4
g4	2	$\perp$	$\perp$	$\perp$	$\perp$	$\perp$	$\perp$	2	$\perp$
g5	$\perp$	$\perp$	$\perp$	$\perp$	$\perp$	$\perp$	4	$\perp$	2

(b) The W matrix is table 1, and the D matrix is shown in table 2.
(c) The constraints for legality:

$$\begin{aligned}
r(h) - r(d_1) &\leq 1 \\
r(h) - r(g_1) &\leq 1 \\
r(d_1) - r(g_1) &\leq 0 \\
r(d_1) - r(g_2) &\leq 0 \\
r(g_1) - r(d_2) &\leq 0 \\
r(d_2) - r(g_4) &\leq 0 \\
r(d_2) - r(g_5) &\leq 0 \\
r(g_2) - r(d_3) &\leq 0 \\
r(d_3) - r(g_4) &\leq 0 \\
r(d_3) - r(g_3) &\leq 0 \\
r(g_3) - r(g_5) &\leq 0 \\
r(g_4) - r(h) &\leq 1 \\
r(g_5) - r(g_3) &\leq 1
\end{aligned}$$

The constraints for delay ≤ 4:

$$\begin{aligned}
r(g_1) - r(g_3) &\leq 0 \\
r(h) - r(g_5) &\leq 0 \\
r(d_1) - r(g_5) &\leq -1 \\
r(g_2) - r(g_5) &\leq -1
\end{aligned}$$

(d) The constraint graph are shown in fig. 5.
(e) There is no negative-weighted cycle. A feasible retime function is

$$r(v) = \begin{cases} -1\,, v \in \{d_1, g_1\} \\ 0\,, \text{otherwise} \end{cases}$$

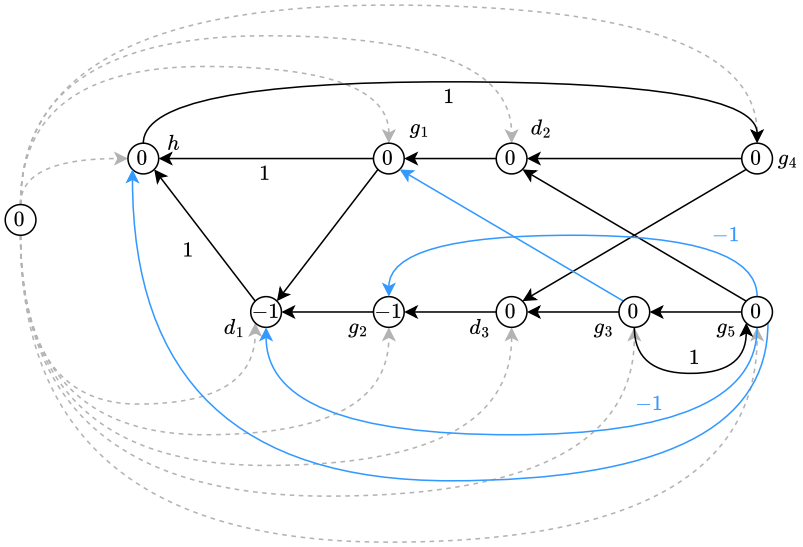


Fig. 5. The constraint graph and a feasible solution in problem 5. The black edges, blue edges, and gray dotted edgges are legality constraints, delay constraints, and the edges from the additional source vertex, respectively. The weight of each edge is zero if not specifed.