LaDS
Laboratory of Dependable Systems

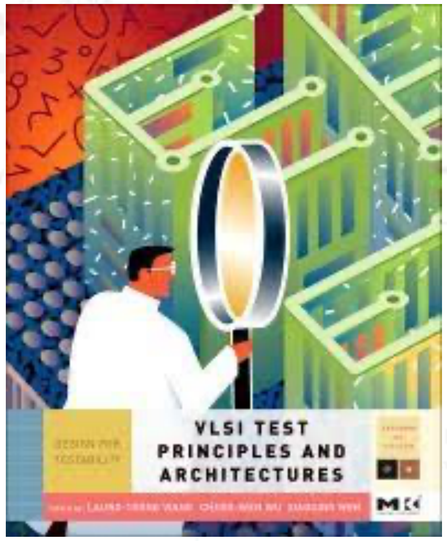
VLSI System Testing, F24

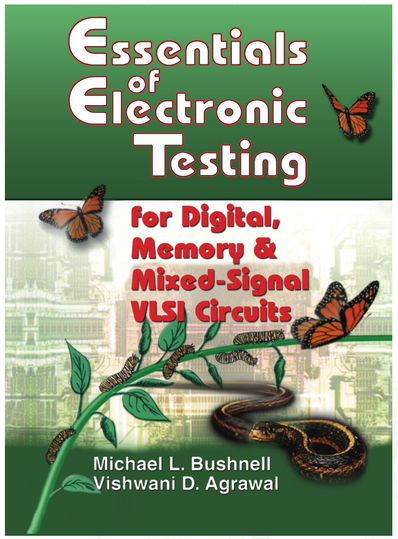
Jiun-Lang Huang & Yi-Shing Chang

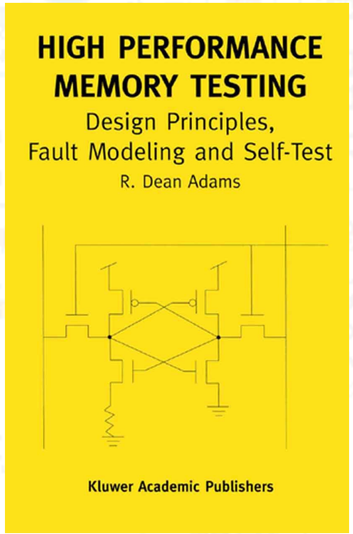
GIEE/ICDA, National Taiwan University

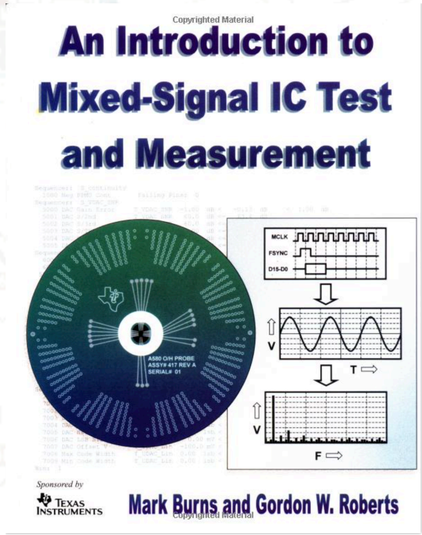
General Information

Lecture Hours	Friday, 2:20 PM - 5:10 PM
Classroom	MK-117
Instructor	Jiun-Lang Huang （黃俊郎） / BL-623 / jlhuang@ntu.edu.tw Yi-Shing Chang （張益興） / yishingc@ntu.edu.tw
TA	Kuan-Ming Liu（劉冠明） / （r12943167@ntu.edu.tw） Chia-Cheng Wu（吳佳政） / （r13943070@ntu.edu.tw）
Textbook	* "***VLSI Test Principles and Architectures***" L.-T. Wang, C.-W. Wu, and X. Wen Morgan Kaufmann Publishers, 2006
Reference books	* "***Essentials of Electronic Testing***" Michael L. Bushnell, Vishwani D. Agrawal Kluwer Academic Publishers, 2002 * "***High Performance Memory Testing***" R. Dean Adams Kluwer Academic Publishers, 2003 * "***An Introduction to Mixed-Signal IC Test and Measurement***" M. Burns and G. W. Roberts Oxford University Press, 2001 Morgan Kaufmann Publishers


VLSI TEST
PRINCIPLES AND
ARCHITECTURES


Essentials
of
Electronic
Testing
for Digital,
Memory &
Mixed-Signal
VLSI Circuits
Michael L. Bushnell
Vishwani D. Agrawal


HIGH PERFORMANCE
MEMORY TESTING
Design Principles,
Fault Modeling and Self-Test
R. Dean Adams
Kluwer Academic Publishers


Copyrighted Material
An Introduction to
Mixed-Signal IC Test
and Measurement
Sponsored by
Texas Instruments
Mark Burns and Gordon W. Roberts
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Syllabus

basics

- a crash course
- fault modeling
- design-for-test built-in-self-test

domain/ application specific

- memory, AMS, interconnect
- low power
- test compression

advanced topics

- scan/memory diagnosis
- test program and binning
- adaptive testing
- SCA vulnerability

Evaluation

- Homework: 50%
- Term project: 30%
- Participation: 20%