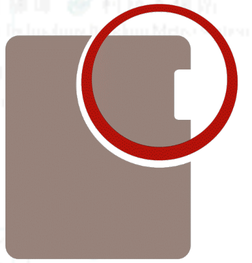
Fault Simulation

Logic Simulation

- Logic simulation may be utilized to
  (1) verify the correctness of the design or
  (2) predict the behavior of the design.
- Simulation accuracy and complexity depend on the circuit model.
  - Functional level description down to transistor level.
  - Two-valued (0 or 1), three-valued (0, 1, or u), *or more complicated signal models*.
  - *Inclusion of timing model, types of timing models*.

Fault Simulation



- A fault simulator is used to evaluate the quality of tests.
  - It can simulate the circuit response in the presence of faults.
  - Fault dropping—test pattern generator utilizes fault simulation to remove faults detected by newly generated test patterns from the fault list.
  - Utilize fault-parallelism or pattern-parallelism to speed up the process.
- Inputs:
  - The design under test, the fault list
- Outputs:
  - Detected faults, fault coverage, fault detection dictionary

Test Pattern Generation

Why?

- Fault simulation with user-given patterns is insufficient and inefficient.
- ATPG aims to generate a high-quality test pattern set (high fault coverage with few patterns) to detect the target faults.
- Modern ATPGs consider not only fault coverage and the pattern count but also test power, compressibility, and diagnosability.

Sequential ATPG?

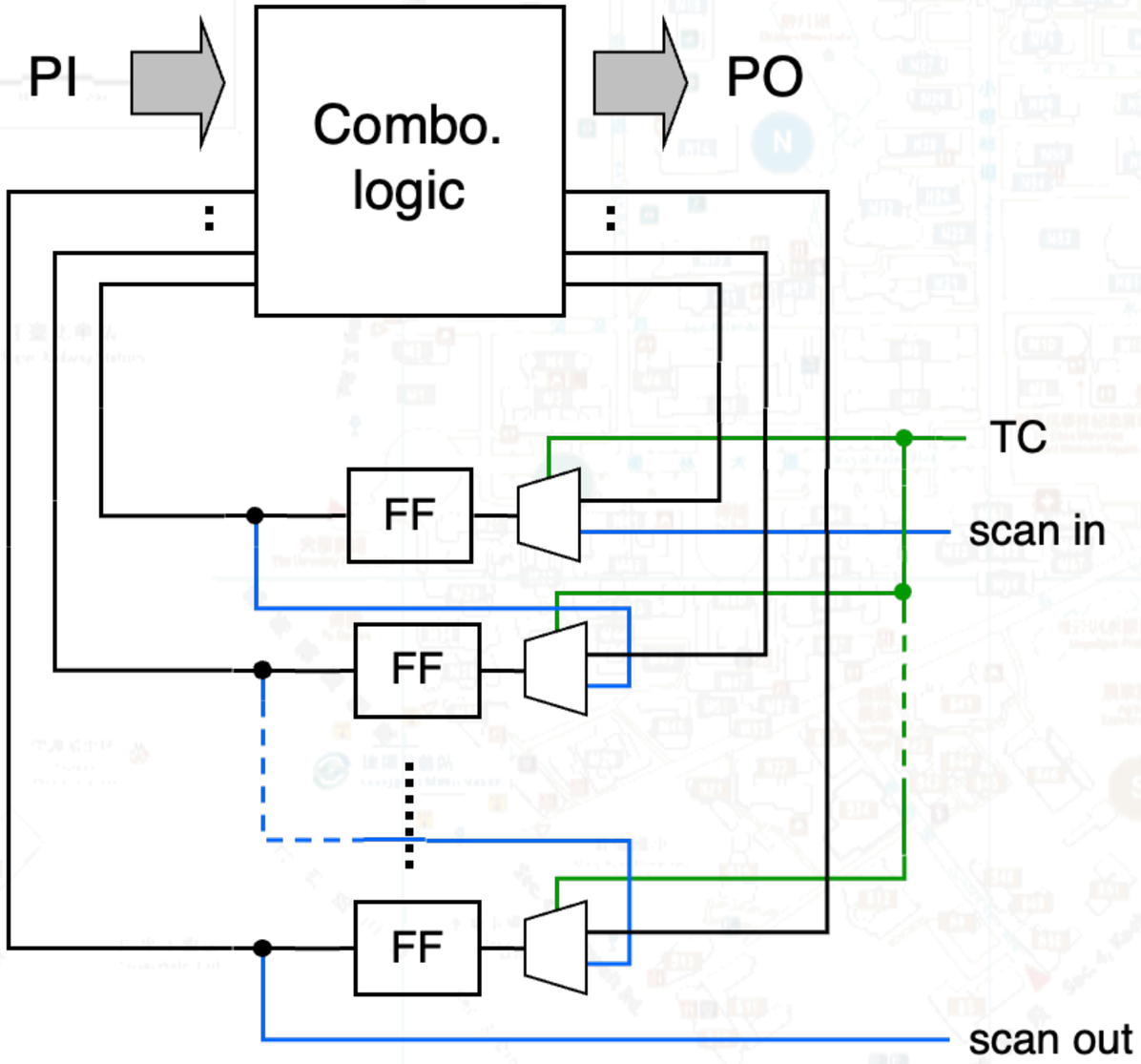
- Very low efficiency.
- With full-scan design, sequential ATPG is no longer needed.

Some Facts about ATPG

- Random pattern generation
  - Use random patterns to detect easy-to-detect faults—fault simulation is cheaper than pattern generation.
  - Stop when fault coverage saturates.
- X-ratio
  - Most ATPG patterns are sparsely specified.
  - The ratio of unspecified bits (at PI and PPI), i.e., X-ratio, is generally higher than 90%.
  - Test power reduction and test compression techniques rely heavily on X-bits.

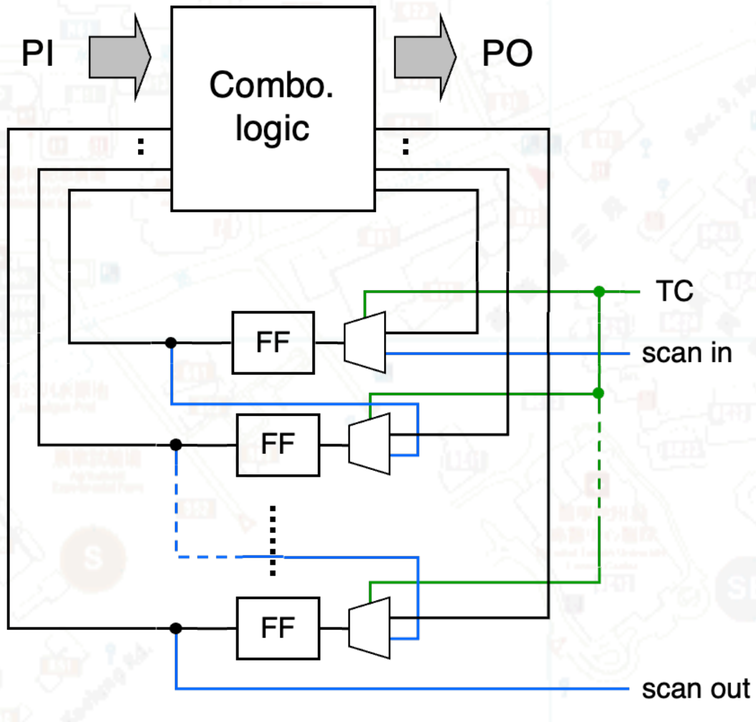
Full-Scan Design

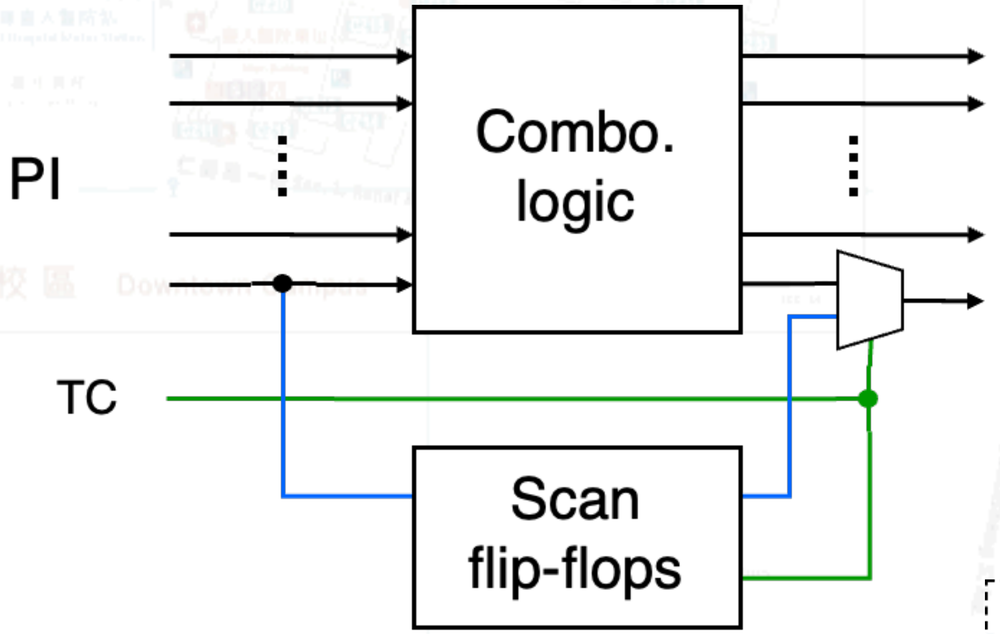
The Scan Concept

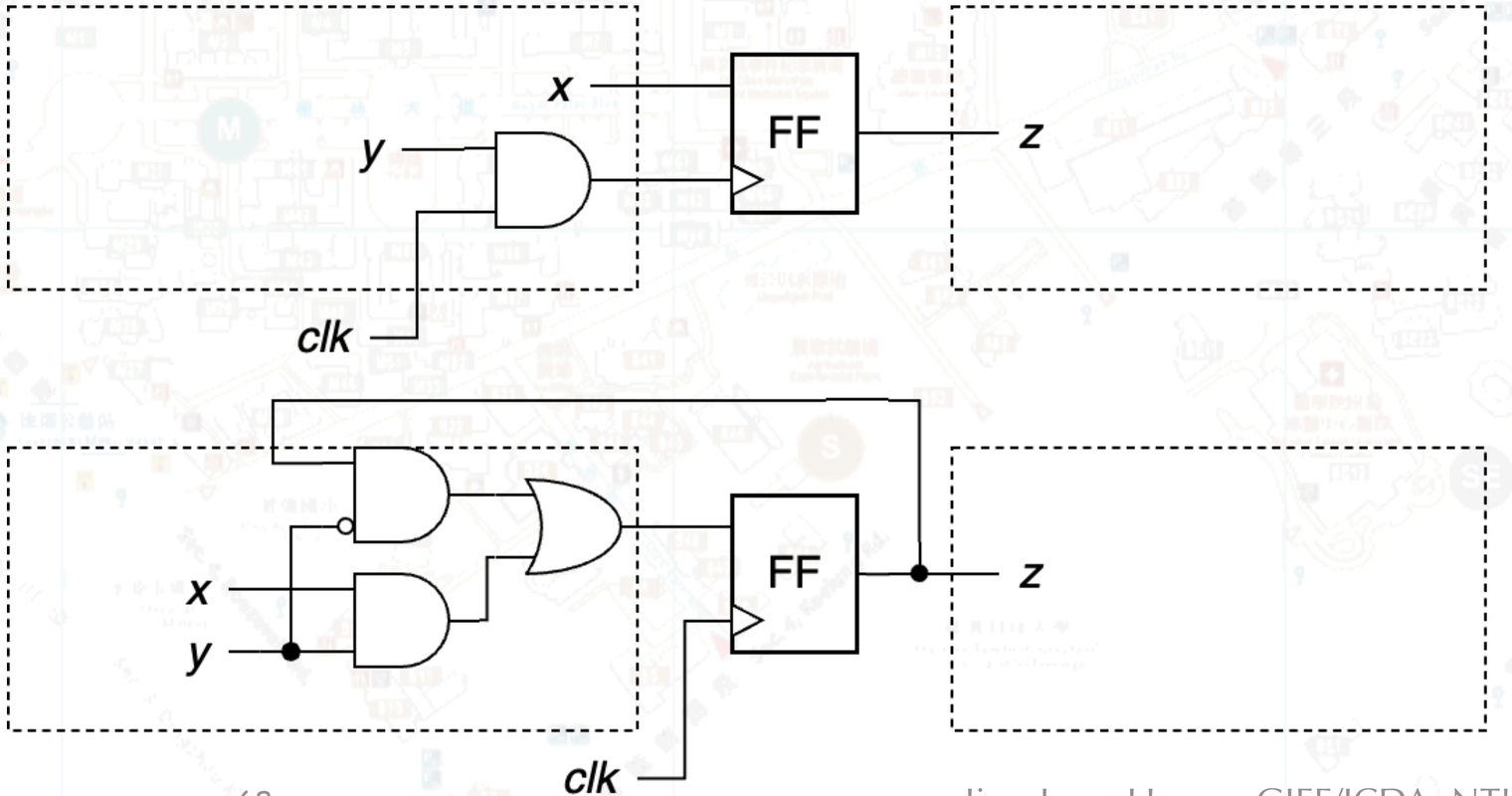


The Scan-Design Rules

- The designers must adhere to the rules so that the design is scan-testable.
- Rule I: Use only D-type master-slave FFs.
- Rule II: At least one PI pin must be available for TC.
  - Scan-in and out can be shared (using MUX) with functional PI and PO.
- Rule III: All FF clocks must be controllable from PI.
  - This is necessary for FFs to function as a scan register.
- Rule IV: Clock must NOT feed the data inputs of FFs.
  - To avoid potential race conditions in the normal mode.




PI
Combo.
logic
PO
TC
Scan
flip-flops


x
y
FF
z
clk
x
y
FF
z
clk

Tests for Scan Circuits

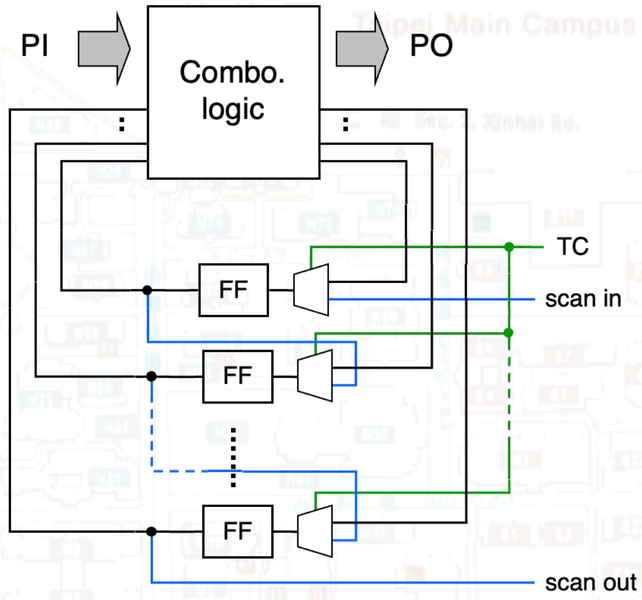
- Phase I:
  - Shift test
  - Targets the scan flip-flops.
- Phase II:
  - Combinational test
  - Target the faults in the combinational circuit.

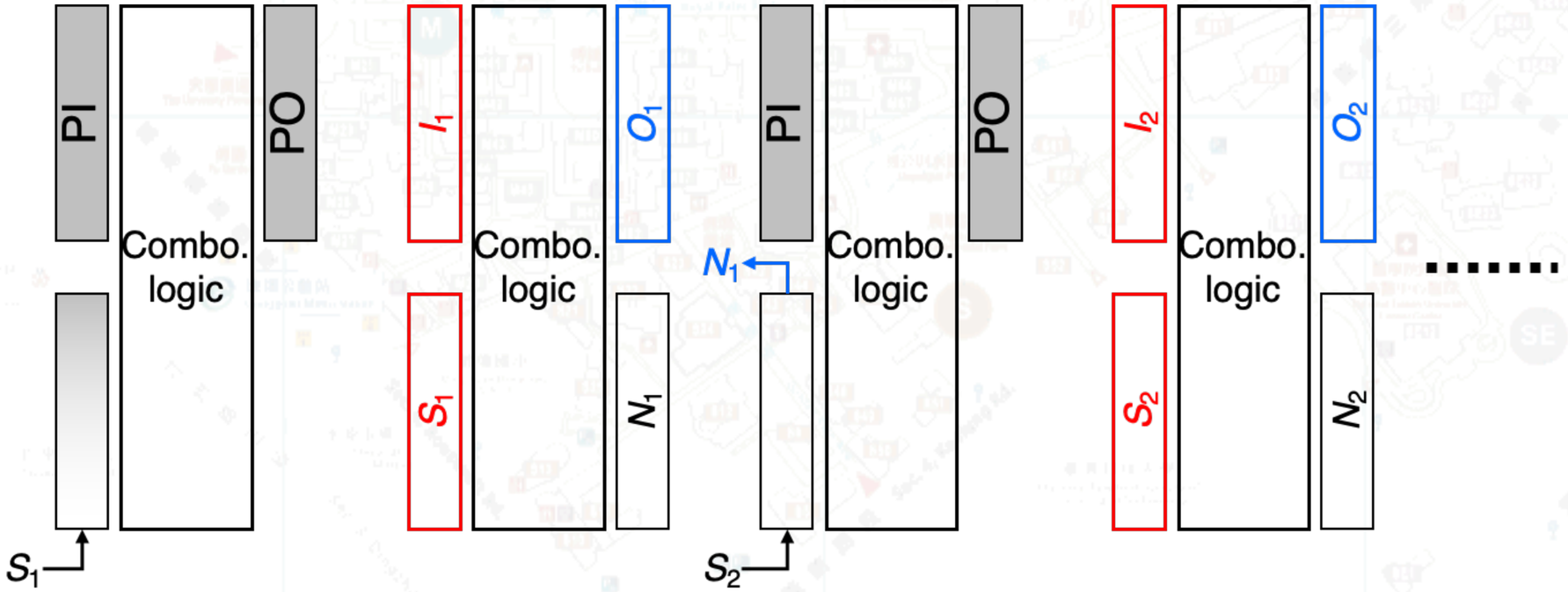
Phase I: Shift Test

- A toggle sequence
  - 00110011… of length n+4 is scanned in.
  - n is the maximum number of FFs in a scan chain.
- Each SFF experiences all four transitions: 0→1, 0→0, 1→1, 1→0.
- The shift test covers most single stuck-at faults in the FFs.
- The shift test also verifies the correctness of the shift operation.

Phase II: Combinational Test

- Each test vector consists of I_i and S_i
- Scan-test length
  - $n_{comb}(n + 1) + n$
  - n_{comb}: number of combinational tests





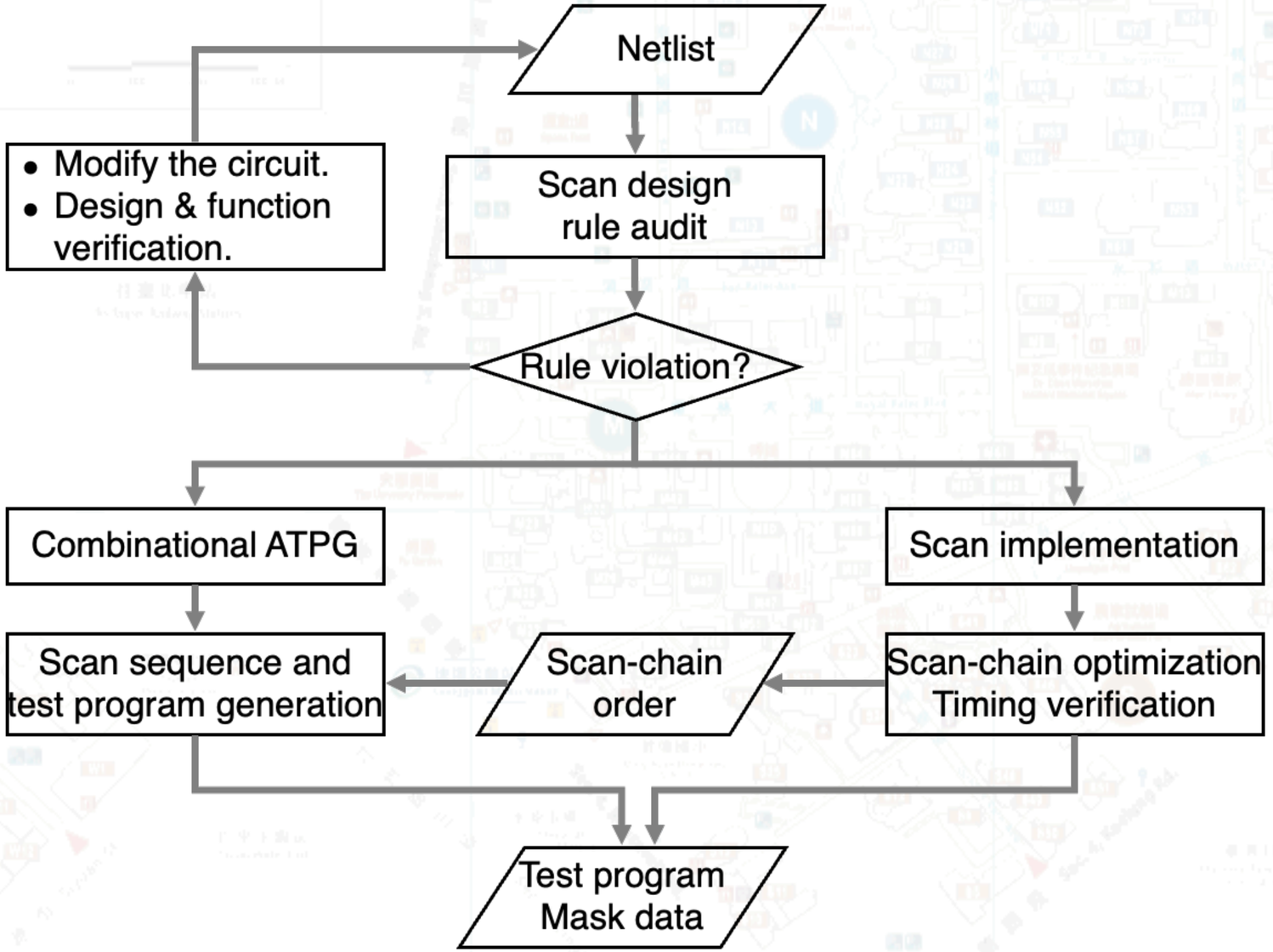
Multiple Scan Chains

- To reduce test time.
  - However, each scan register has its own scan-in and scan-out.
- The scan registers may differ in length.
  - Test time determined by the longest one.

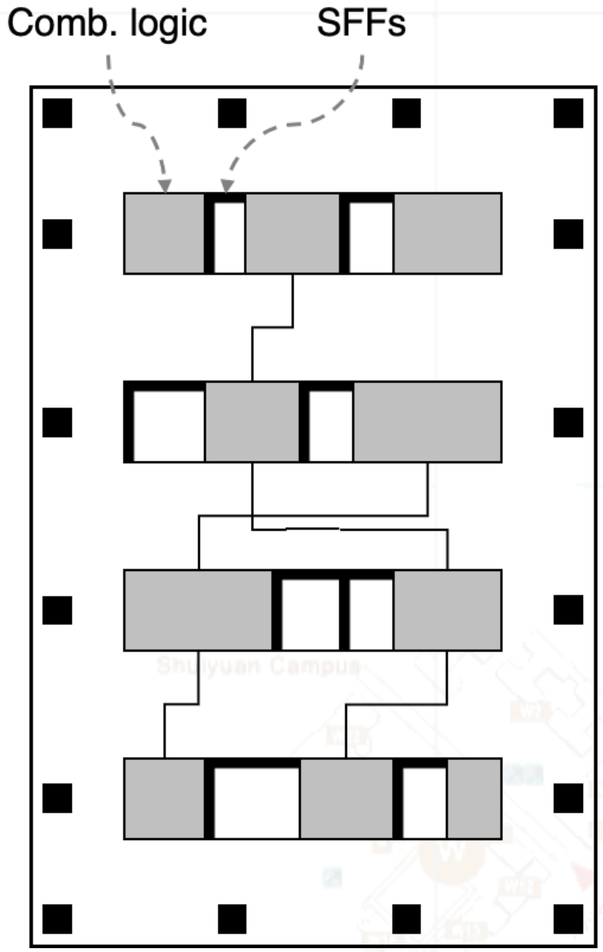
Problem w/ Scan Design

- Area/performance overhead
  - Increased gate count and routing area
  - MUXed input (in single-clock SFF design)
  - Extra load capacitance at FF output.
- Long test application time.
- Not applicable to all designs.
  - Must follow the scan design rules.
- High power dissipation during testing.

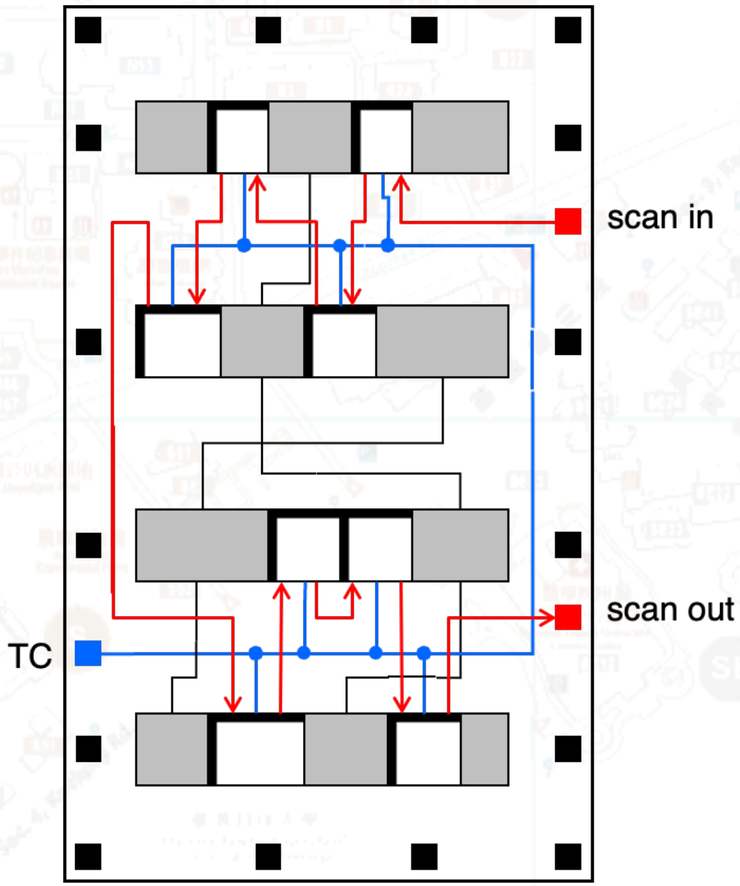
Design Automation



Physical Design of Scan w/ Standard Cells



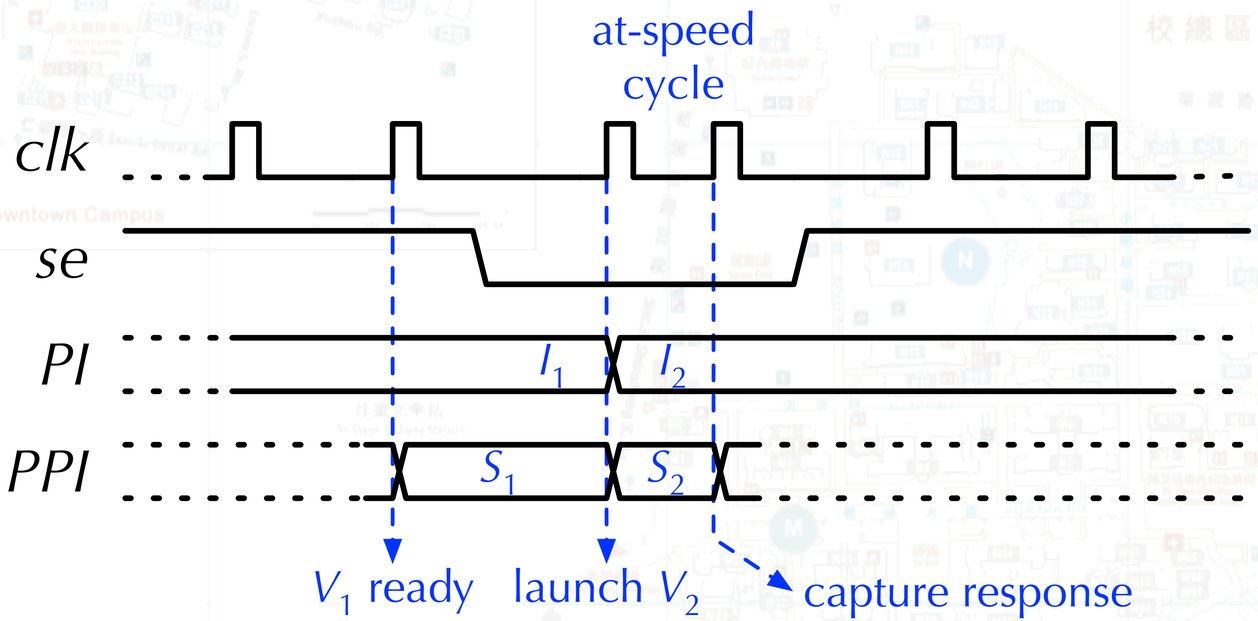
- Placing the cells without scan wiring.
- Replace FFs with SFFs.
  - Wider than original.
- Add TC control line.
  - At most one track in every alternate routing channel.
- Scan path routing.
  - One track in every alternate routing channel is possible.

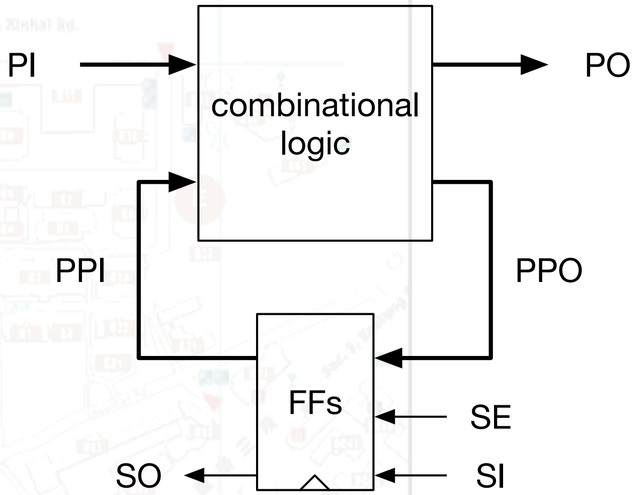


At-Speed Test Application

- For timing-related faults, need two-vector patterns.
- However, a scan cell only stores one vector.
- LoC (Launch-on-Capture) or LoS (Launch-on-Shift).

Scan-Based LoC Test Pattern Application

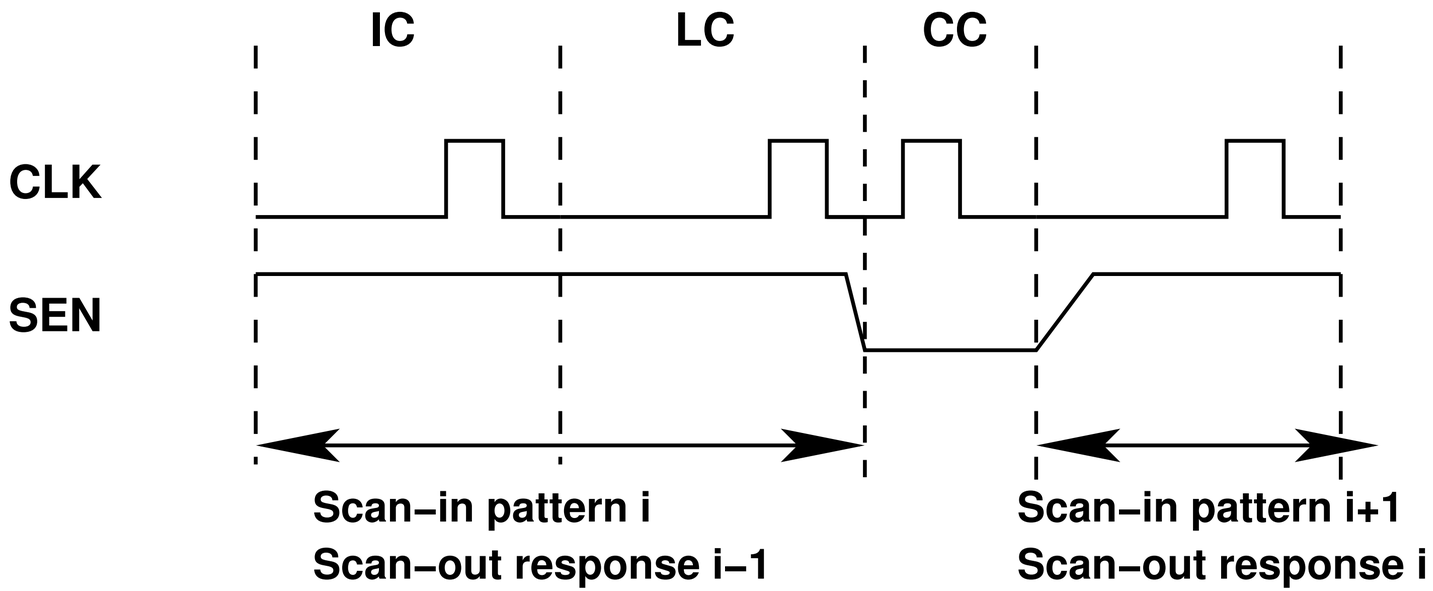




- An LoC pattern consists of two vectors.
  - $V_1 = < I_1, S_1 >$, $V_2 = < I_2, S_2 >$ where *I*/*S* corresponds to PI/PPI.
  - S_2 is generated by CUT.
- ***At-speed cycle is identical or similar to functional operation.***

LAUNCH-ON-SHIFT (LOS)

- Skewed-load



LOW COST TESTER LIMITATIONS

- PI hold constant from launch to capture
- PO masked

LOC VS. LOS

- Fault coverage
- Hardware requirement
- Test power