EC203 DSD BACKLOG EXAM, Date: 29/12/20, Time: 10:00-12:00, MO-2020

EC203 Digital System Design

1

Which is not the shadow or folded back memory of ROM in minimum system with 8085? *
(2 Points)

- 2200H-22FFH
- 8000H – 87FFH
- 8800H – 8FFFH
- 9000H – 97FFH.

2

A 4-stage ripple carry adder is composed of three 1-bit full adders and one half adder (for its 1st stage). Find out the propagation delay of the final CO (carry out), if each gate, be it a OR gate or AND, has a propagation delay of 10 ns. *
(2 Points)

- 50 ns
- 40 ns

- [x] 70 ns.
- [ ] 60 ns

3

When CLR_bar goes LOW and return back to HIGH, the initial o/p word of ring counter is Q3Q2Q1Q0=0001 and subsequent clock pulses make the Qs as follows: *
(2 Points)

- [ ] 4th clock Q3Q2Q1Q0 = 0001.
- [ ] 3rd clock Q3Q2Q1Q0 = 0100
- [x] 1st clock Q3Q2Q1Q0 = 0001
- [ ] 2nd clock Q3Q2Q1Q0 = 0010

4

How many MOSFETs are required to realize Sum (S) function of a 1-bit full adder in static CMOS logic family? *
(2 Points)

- [x] 24
- [ ] 32.
- [ ] 20
- [ ] 28

5

Which is the design metrics that decides the speed or performance of a digital system? *
(2 Points)

- [x] Propagation delay (tp)
- [ ] power dissipation
- [ ] none of these
- [ ] noise margin

6

The ring oscillator will oscillate only if *
(2 Points)

- [ ] 2Ntp ≠ tf + tr.
- [ ] 2Ntp << tf + tr
- [x] 2Ntp = tf + tr
- [ ] 2Ntp >> tf + tr

7

To implement a 1-bit full subtractor using 1:8 Demultiplexer we need *
(2 Points)

- [ ] 1 OR gate and 1 inverter.
- [ ] 1 OR gate
- [x] two OR gates
- [ ] 3 OR gates

8

In a Johnson-counter arrangement it is possible to construct a MOD-N counter (where N is an even number) by connecting *
(2 Points)

- [x] N/2 flip-flops
- [ ] 2N flip-flops
- [ ] N/4 flip-flops.
- [ ] N flip-flops

9

The POS form is also called *
(2 Points)

- [x] Conjunctive Normal Form (CNF)
- [ ] none of these.
- [ ] Disjunctive Normal Form (DNF)
- [ ] Disjunctive Canonical Form (DCF)

10

In a 4-bit BCD adder, when the sum of two BCD numbers is smaller than decimal 9, the binary number to be added to the 2nd binary adder at the bottom is *
(2 Points)

- [ ] 1001
- [ ] 0000
- [x] 0110
- [ ] 0011

11

Convert decimal 0.85 to binary up to the accuracy of six binary digits. *
(2 Points)

- 0.111110
- 0.110111
- 0.100110
- 0.110110

12

The duty cycle of clock generated by 555 timer and its associated elements in SAP-1 is *
(2 Points)

- 75%.
- 45%
- 65%
- 50%

13

How many microinstructions are required to form a macroinstruction of SAP-1 *
(2 Points)

- 5
- 2
- 12.
- 3

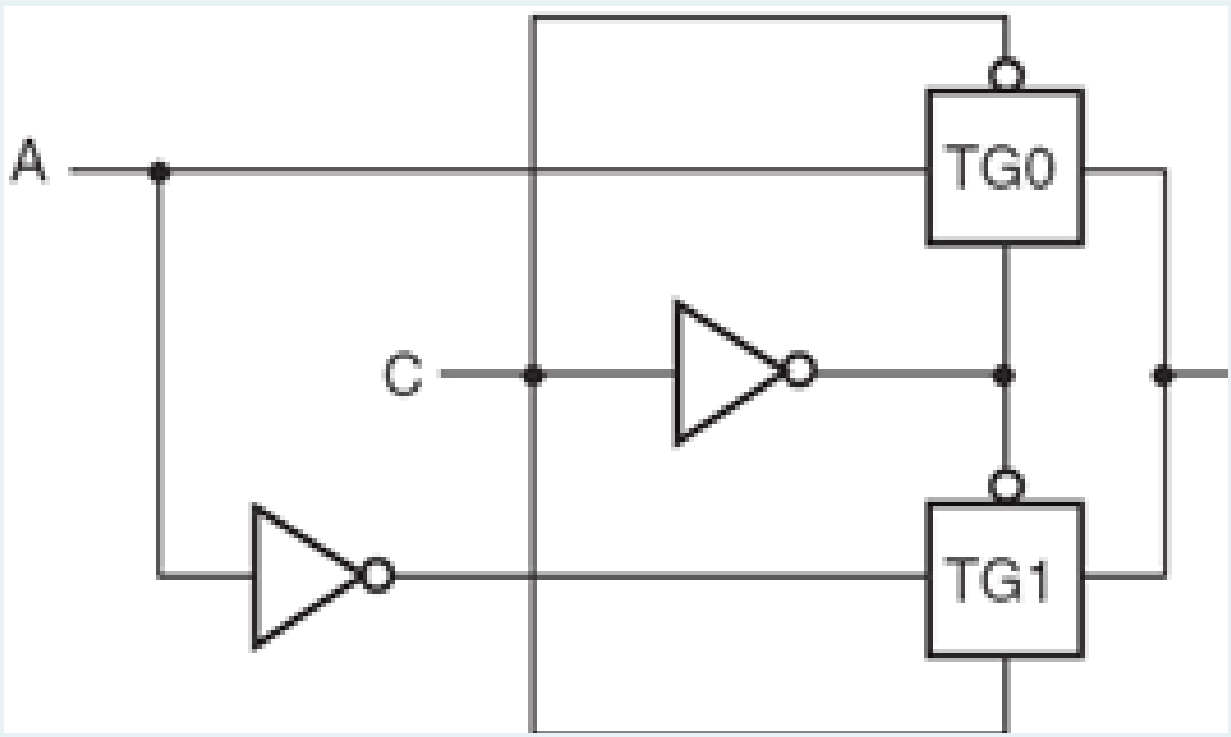
14

The 12-bit control word generated by the controller/sequencer during T5 state of ADD is *
(2 Points)

- 3E3H
- 2C3H
- 2E1H
- 1A3H.

15

The Boolean function F in the following fig. equals to *
(2 Points)



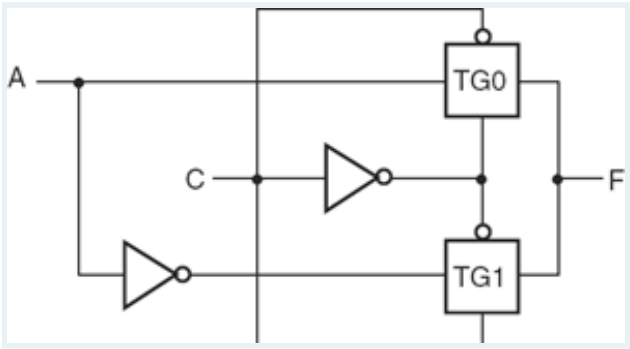
- $X\bar{Y}^{-}+XY$.
- F= XY
- $F= XY+XY^{-}$
- $F= X\bar{Y}+X(Y)^{-}$

16

A 3-stage ripple carry adder is composed of two 1-bit full adders and one half adder (for its 1st stage). Its sum output bits are S0, S1, S2. Find out the propagation delay of the S2 if each gate, be it an OR gate, AND gate or XOR gate has a propagation delay of 10 ns. *
(2 Points)

- 50 ns
- 60 ns
- 40 ns ns
- 70 ns.

17



The Boolean function F in the following fig. equals to *
(2 Points)

- $F=X\bar{Y}+X\bar{Y}$
- $X\bar{Y}+XY$.
- $F= XY+X\bar{Y}$
- F= XY

18

What is the control word corresponding to increment state? *
(2 Points)

- 263H
- BE3H
- 3E3H.
- 5E3H

19

The minimum number of 2-input NAND gates required to realize an Exclusive-NOR gate is *
(2 Points)

- 7.
- 5
- 6
- 4

20

The basic SR flip-flop realized only with two NAND gates has a quiescent state of *
(2 Points)

- SR = 00
- SR = 10.
- SR = 01
- SR = 11

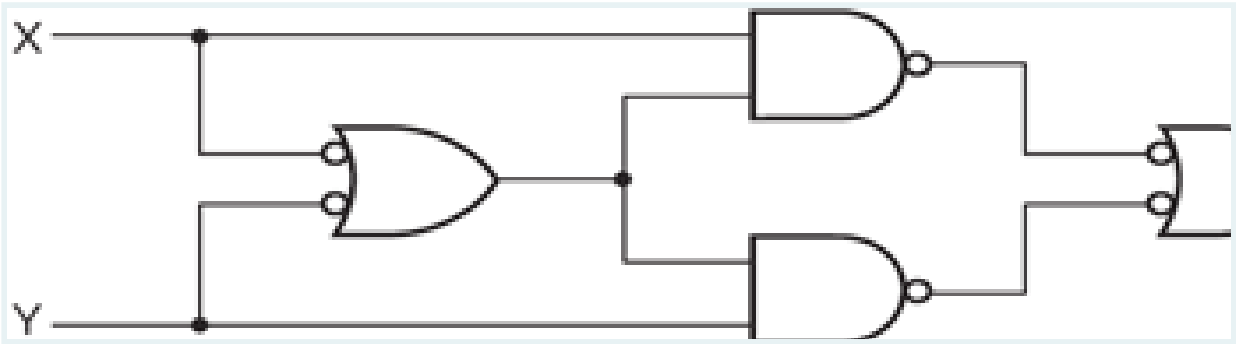
21

In Verilog, registers are described with an always @(posedge clk) statement with nonblocking assignment *
(2 Points)

- :=
- =
- =>
- <=

22

The Boolean function F in the following fig. equals to *
(2 Points)



- $X\bar{Y}^{-}+XY$.
- F= XY
- $F= X\bar{Y}+X(Y)^{-}$
- $F= XY+XY^{-}$

23

What modulus counters can be constructed with the use of four flip-flops? *
(2 Points)

- [x] a modulus between 16 and 2.
- [ ] a modulus of 4
- [ ] a modulus of 8
- [ ] a modulus of 16

24

Each microinstruction of SAP-1 has *
(2 Points)

- [ ] 3 bits
- [x] 12 bits.
- [ ] 1 bit
- [ ] 2 bits

25

In VHDL, variable assignment is done with the symbol *
(2 Points)

- [ ] <=
- [ ] =>
- [x] :=
- [ ] =