END EXAMINATION EC303 Microprocessors & Microcontrollers (EC303 Microprocessor and Microcontroller)

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* Required

1. _____ has application in data acquisition. *
(1 Point)

- [x] ADC 0801
- [ ] DAC0808
- [ ] RS232
- [ ] LF398

2. The _____ is designed as the mixture of Both RISC and CISC technologies. *
(1 Point)

- [ ] 80586
- [ ] Pentium
- [ ] None of above
- [x] Both of above

3. Which out of the following supports Harvard architecture? *
(1 Point)

- ( ) ARM7
- ( ) Pentium
- (•) SHARC
- ( ) All of the above

4. What is TEST instruction? *
(1 Point)

- ( ) Contents of AC is not changed
- (•) All of the above
- ( ) It is mainly AND operation
- ( ) Only flags are changed

5. Find out the correct missing instruction for performing multiplication of 71D and -67D
MOV AX, 71D
MOV CX, -67D *
(1 Point)

- ( ) MUL CX
- ( ) AAM AX
- ( ) AAM CX
- (•) IMUL CX

6. Data Pointer (DPL & DPH) of 8051 can represent the value from *
(1 Point)

- ( ) 0000H to 7FFFH

- ○ 00H to FFH
- ○ 8000H to FFFFH
- ◉ None of the above

7. After resetting of 8051, SP register is initialized to address_____. *
(1 Point)

- ○ 9H
- ○ 6H
- ◉ 7H
- ○ 8H

8. Graphic display controller is an example of? *
(1 Point)

- ◉ Input/Output Processor
- ○ DSP
- ○ Transputer
- ○ Coprocessor

9. The 80286 has 24- bit address bus which is *
(1 Point)

- ○ Multiplexed
- ◉ Nonmultiplexed
- ○ None
- ○ Having dual functions

10. What is the content of accumulator and flag register of the program written below
XRA A; ADI 01H; STA 2400H; HLT *
(1 Point)

- ○ 0FH and F0H
- ○ 00H and 01H
- ○ 00H and FFH
- ◉ 01H and 00H

11. Which of the following are correct characteristics of RISC? *
(1 Point)

- ○ It consists of simple instructions.
- ○ It supports various data-type formats.
- ○ It supports register to use in any context.
- ◉ All of the above

12. In 8086 microprocessor the following has the highest priority among all type interrupts. *
(1 Point)

- ○ OVER FLOW
- ○ DIV 0
- ○ TYPE 255
- ◉ NMI

13. The FIFO RAM of 8279 acts as_____ bit memory matrix. *
(1 Point)

- ○ 16x16

- ○ 16x8
- ○ 8x4
- ◉ None of the above

14. Instruction DAA adjust as *
(1 Point)

- ○ 06 with the accumulator if the value of bits 0-3 exceed 9
- ○ 60 with the accumulator if the carry bit is set
- ○ 60 with the accumulator or if 06 was added to the accumulator in the first step
- ◉ All of the above is correct

15. In 8086, writing a byte to an address location 0004H means *
(1 Point)

- ○ A0 will be HIGH and BHE' will be HIGH
- ○ A0 will be HIGH and BHE' will be LOW
- ◉ A0 will be LOW and BHE' will be HIGH
- ○ None

16. Instruction LDAX D indicates which types of addressing mode. *
(1 Point)

- ○ Direct addressing mode
- ◉ Indirect addressing mode
- ○ Immediate addressing mode
- ○ Implied addressing mode

17. When 8051 wakes up then 0x00 is loaded to which register? *
(1 Point)

- ○ SP
- ○ PSW
- ◉ PC
- ○ None of the mentioned

18. Which pin of 8086 enables the data onto the most significant half of the data bus, D8-D15? *
(1 Point)

- ○ ALE
- ◉ BHE
- ○ TEST
- ○ DEN

19. The _____ bus controller device decodes the signals to produce the control bus signal *
(1 Point)

- ○ Data
- ○ Address
- ○ Internal
- ◉ External

20. If the Address of Port B of 8255 is A1, then the address of Control Register will be *
(1 Point)

- ○ A2

- ○ A5
- ◉ A3
- ○ A0

21. If 8086 trap flag is set, the 8086 will automatically do a *
(1 Point)

- ◉ Type 1 Interrupt
- ○ Type 0 Interrupt
- ○ Type 2 Interrupt
- ○ None

22. Fetching the next instruction while the current instruction executes is called _____ *
(1 Point)

- ◉ Pipelining
- ○ Offset
- ○ Segmentation
- ○ Queue

23. _____8051 Instruction copy data from external 8-bit address in R0 to accumulator is *
(1 Point)

- ○ MOV A, @R0
- ◉ MOVX A, @R0
- ○ MOV @R0, A
- ○ MOVC A, @R0

24. ROLL NO *

betch/10475/18

25. The number of Register Bank available within the 8051 is *
(1 Point)

- [ ] 3
- [ ] 8
- [x] 4
- [ ] 6

26. With larger instruction sets, the control matrix becomes very complicated. This is why hardwired control is being replaced by _____. The basic idea is to store the _____ in a control ROM. *
(1 Point)

- [x] Microprogramming, microinstruction
- [ ] Control ROM, Look up table
- [ ] Microprogramming, Look up table
- [ ] All above are true

27. Which characteristic/s of accumulator is /are of greater significance in terms of its functionality? *
(1 Point)

- [ ] Ability to store one of the operands before the execution of an instruction
- [ ] Ability to store the result after the execution of an instruction
- [x] Both a & b
- [ ] None of the above

28. MOV AL, 55H; NOT AL; MOV BL, 03H; ADD AL, BL; END;
After the execution of the above ALP in 8086, the content of the Accumulator will be *
(1 Point)

- ○ FA
- ○ FD
- ◉ AD
- ○ 03

29. The number of Data Registers in the ARM processor is *
(1 Point)

- ○ 24
- ○ 20
- ◉ 16
- ○ 18

30. The HOLD PIN of 8085 becomes high when an instruction is executing. The microprocessor finishes the _____ before going to serve it. *
(1 Point)

- ◉ The current machine cycle
- ○ None
- ○ The whole program
- ○ The current instruction

31. How many address lines a 2Kx8 RAM IC required? *
(1 Point)

- ○ 14

- ○ 16
- ○ 8
- ◉ 11

32. In 8086 _____ handles transfers of data and addresses on the buses. *
(1 Point)

- ◉ Bus Interface unit
- ○ Segment Register
- ○ Instruction queue
- ○ Execution unit

33. In 8051 SP is ___ wide register. And this may be defined anywhere in the _____. *
(1 Point)

- ○ 16 bit, on-chip 128 byte ROM
- ○ 8 byte, on-chip 128 byte RAM.
- ◉ 8 bit, on chip 128 byte RAM.
- ○ 8 bit, on chip 256 byte RAM.

34. An 8253, working in Mode-3 (Square Wave Generator) and having clock frequency of 2MHz, what count needs to be loaded into the timer to generate a square wave of 50KHz. *
(1 Point)

- ◉ 0028H
- ○ 0040H
- ○ None
- ○ 0032H

35. The contents of a register (B) and Accumulator(A) of 8085 microprocessor are 49H and 3AH respectively. The contents of A and the status of carry flag(CY) and sign flag (S) after executing SUB B instruction are *
(1 Point)

- ○ A = 1F, CY = 1, S = 1
- ○ A = F0, CY = 0, S = 0
- ○ A = 0F, CY = 1, S = 1
- ◉ A = F1, CY = 1, S = 1

36. If the stack of 8051 is beginning at 60H, what is the size of the stack? *
(1 Point)

- ◉ 32 byte
- ○ 64 byte
- ○ 128 byte
- ○ None

37. ARM stands for *
(1 Point)

- ○ Advanced Reduced Machine
- ○ Advanced RISC methodology
- ◉ Advanced RISC Machine
- ○ Advanced Reduced methodology

38. Find the control word of the 8255 for resetting BIT 7 of Port C. *
(1 Point)

- ◉ 00001110

- ○ 10001110
- ○ 00001111
- ○ 10001111

39. Assuming that R = 5K, Iref = 2mA, find the Iout , Vout for the input 10011001 for DAC 0808. *
(1 Point)

- ○ Iout =1.813 mA,Vout =9.0625 mA.
- ○ Iout =1.875 mA,Vout =9.375 mA.
- ○ Iout =1.34375 mA, Vout =6.71875 mA.
- ◉ Iout =1.195 mA,Vout =5.975 V.

40. If Register C contains FFH, then INR A will *
(1 Point)

- ◉ None
- ○ Will make the Zero Flag 1
- ○ Will make the AC Flag 0
- ○ Make the Carry flag 1

41. If any change in sensor value is detected at the end of a sensor matrix scan, then the IRQ line *
(1 Point)

- ○ remains unchanged
- ○ none
- ○ goes low
- ◉ goes high

42. I/O Mapped I/O scheme is _____ but _____ than Memory mapped I/O scheme. *
(1 Point)

- ○ Slower, Simpler
- ○ Faster, Costlier
- ◉ Complex, Cheap
- ○ Cheap, Slower

43. The result of MOV AL, 65 is to store *
(1 Point)

- ○ store 0100 0010 in AL
- ◉ store 0100 0001 in AL
- ○ store 40H in AL
- ○ store 42H in AL

44. CISC systems shorten execution time by reducing the number of _____ per program. *
(1 Point)

- ○ Machine cycles
- ○ Clock cycles
- ◉ Instructions
- ○ All of above

45. In RISC architecture, a method that increases the maximum size for a program is *
(1 Point)

- ○ ROM

- ○ Overlapping Memory
- ◉ Virtual Memory
- ○ Cache Memory

46. _____ 8051 instruction interchange the nibbles of register A. *
(1 Point)

- ○ XCHG A
- ○ XCHD A
- ◉ SWAP A
- ○ None of above

47. If Register C contains FFH, then INR A will *
(1 Point)

- ○ Make the Carry flag 1
- ◉ None
- ○ Will make the Zero Flag 1
- ○ Will make the AC Flag 0

48. In which of the following modes of the 8255 PPI, only port C is taken into consideration? *
(1 Point)

- ○ Mode 2 of I/O mode
- ○ Mode 0 of I/O mode
- ○ Mode 1 of I/O mode
- ◉ BSR mode

49. Determine the Mode 0 Control Word of 8255 to configure port A and Port CU as input port and port B and Port CL as output ports *
(1 Point)

- (●) 98H
- ( ) 83 H
- ( ) 84 H
- ( ) None

50. CAMPUS *

- (●) MESRA-Section A
- ( ) MESRA-Section B
- ( ) DEOGHAR
- ( ) JAIPUR
- ( ) PATNA

51. The instruction sequence shown below has been written for 8051. Identify the logical
operation it performs
MOV C, BIT1
JNB BIT2, SKIP
CPL C
SKIP: Continue *
(1 Point)

- ( ) AND
- ( ) OR
- (●) EX-OR
- ( ) None

52. 80486 introduced concept of _____ memory. *
(1 Point)

- ○ Virtual
- ○ Segmented
- ◉ Cache
- ○ All of above

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