ASSIGNMENT-7

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Question-1:

What are the various inherent issues with the vector architecture? Give the name of the technique that can solve each problem.

answer:

Inherent Issue with Vector Architecture:

* Vector processor cannot handle programs in which the vector length is not same as length of vector register. Technique: Most application vector won’t match architecture vector length. Hence in need for efficient solution.
* The vector processor cannot execute single vector which can be faster than 1 element/ per clock cycle. Technique: Using Multiple elements per clock cycle will improve the performance.
* Having IF statement inside code which is to be vectorized. Technique: Handling Conditional Statement helps more code to vectorize.
* Vector processor cannot handle sparse matrices. Technique: Popular data structure must vectorize.
* Vector processor cannot handle multiple dimensional matrices. Technique: For vector architecture to do well, data structure must vectorized.

Question–2:

Provide Similarities and differences between MIPS and VMIPS architecture.

answer:

DIFFERENCES: -

|  |  |
| --- | --- |
| MIPS | VMIPS |
| 1. MIPS stand as Microprocessor without Interlocked Pipeline Stages. 2. MIPS code, every ADD.D must wait for a MUL.D, and every S.D must wait for the ADD.D. 3. It is power efficient – so less number of instructions. 4. It executes 600 instruction. 5. For faster execution of the code, Loop unrolling and loop scheduling. | 1. VMIPS Stand as Vector Microprocessor without interlocked pipeline stage. 2. each vector instruction will only stall for the first element in each vector, and then subsequent elements will flow smoothly down the pipeline. 3. Loads or stores a vector to or from memory. The VMIPS vector loads and stores are fully pipelined, so that words can be moved between the vector registers and memory with a bandwidth of one word per clock cycle, after an initial latency. 4. For faster Execution of code, convey and chaining is used. |

SIMILARITY

1. VMIPS has scalar architecture just like MIPS.
2. In VMIPS, vector operations use the same names as scalar MIPS instructions, but with the letters “VV” appended.
3. There are also eight 64-element vector registers, and all the functional units are vector functional units.

Question-3: Use the VMIPS instructions to convert following code into VMIPS code.

             for ( i = 0; i < 64; i++)

X[i] = X[i] + 4;

                 if ( X[i] < Y[i] ) { Y[i] = Y[i] -X  }

              else{ Y[i] = 0; }

          }

answer:

L.D F0, 4

L.D F1, 0

L.V V1, Rx

L.V V2,Ry

ADDVS.D V1,V1,F0

S.V. Rx,V1

SLTVV.D V1,V2, Else

SUBVV.D V2,V2,V1

Else: L.D V2, F1

S.V. Ry,V2

Question-4:

For the VMIPS code in  above answer, find how many Convoys you should have for maximum performance.

Ensuring each convoy has no structural or data dependencies. If each convoy finishes in one clk count the total number of clks it takes to finish the whole code.

Assume normal Cray -1 VMIPS architecture, one LOAD/STORE unit, one  Floating FP Add/Sub, One Integer Add/Sub, One FP Multiplier , one FM Decider.

answer:

- I will be needing 5 Convoys to execute the code and hence 5 clock cycles if one convoy takes one clock cycle to execute.

1. L.D F0, 4

L.V V1,Rx

2. ADDVS.D V1,V1,F0

L.V V2,Ry

3. SLTVV.D V1,V2, Else

S.V. Rx,V1

4. L.D F1, 0

SUBVV.D V2,V2,V1

5. Else: L.D V2, F1

S.V Ry, V2