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Laboratory Module 1: Operational Amplifiers – Integrators, Bandwidth, DC biasing

Introduction:

This lab will cover the expected values as compared to the real values of an op amp. We will explore the DC bias characteristics of real op amps. We will analyze the low pass characteristics of the op amp itself. By testing extreme values we will also determine some of the spec sheet values of the specified op amp.

Exercise 1.1: Integrators

For exercise 1.1 an integrator was built with a .1 microfarad capacitor, a 10k ohm resistor and the op 27 op amp. The op amp was powered by +/- 5V from the discovery board.

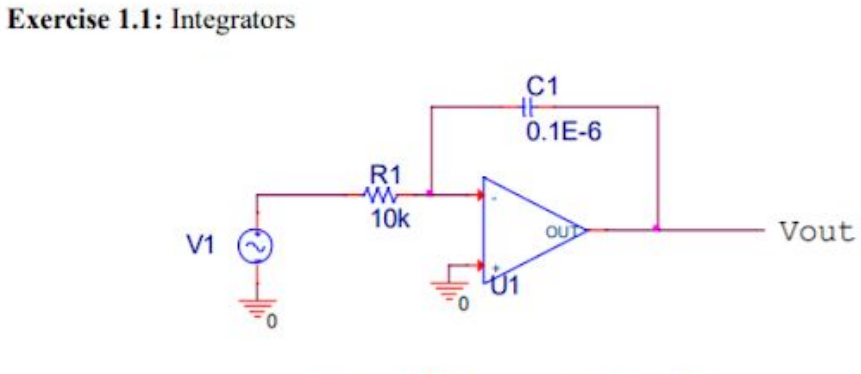

Figure 1.1 Integrating Amplifier Circuit for 1.1

a) For part a, the input voltage was set to a 30 Hz square wave with a 1Vpp signal and 0V DC offset, with Vmax = 0.5V and Vmin = -0.5V. The output voltage is shown below.

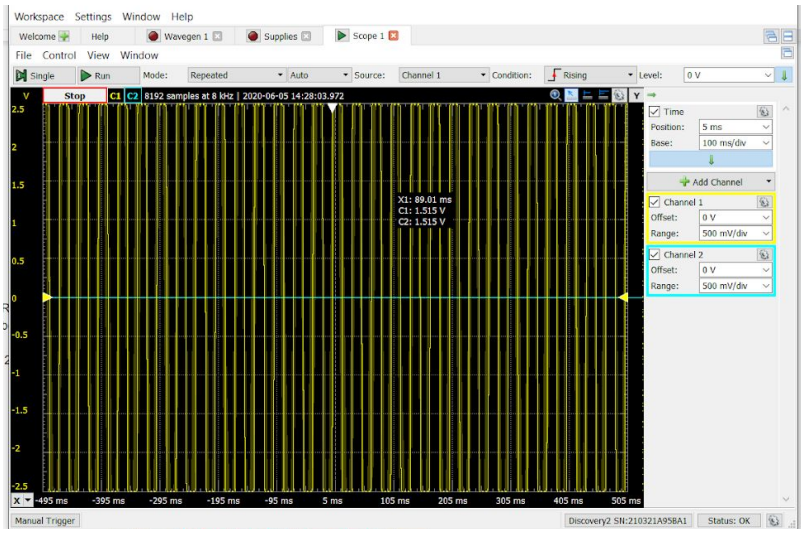

Figure 1.2 Output Voltage for Op-Amp in Part A

b) For part b, the frequency was lowered to 1Hz, giving the output voltage below.

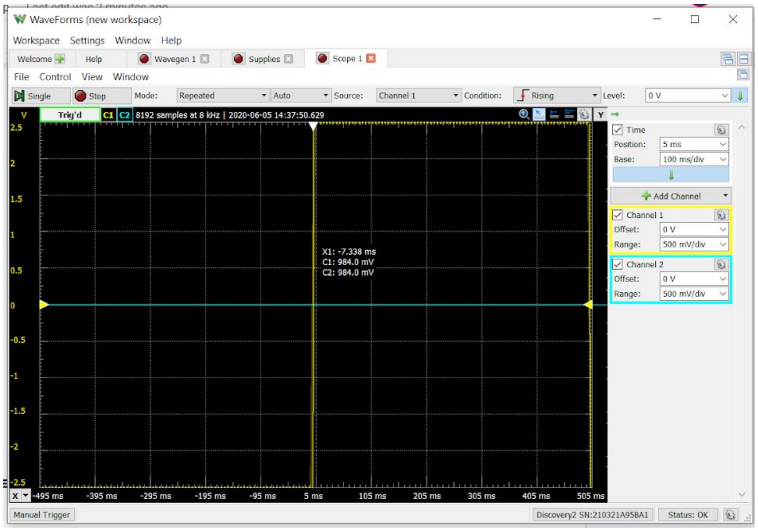

Figure 1.3 Output Voltage of Op-Amp in part B

c) For part c the frequency was again changed to 1 KHz yielding the following output.

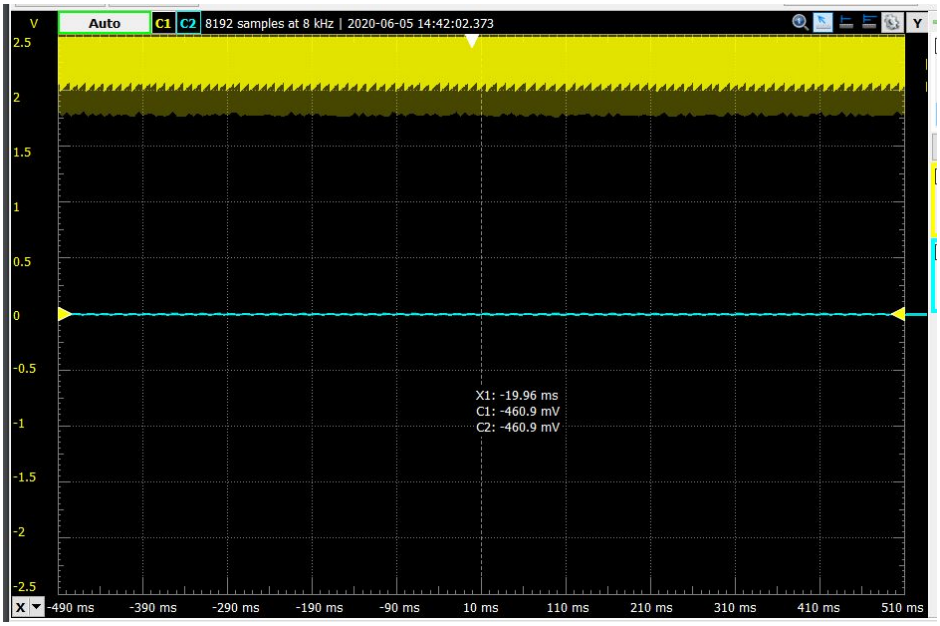

Figure 1.4 Output Voltage of Op-Amp in part C

The output is different from the first two parts because the frequency is so much higher that as the capacitor reaches saturation, the voltage remains constant.

d)For part d, a DC offset was added, toggling between 10V and -10V.

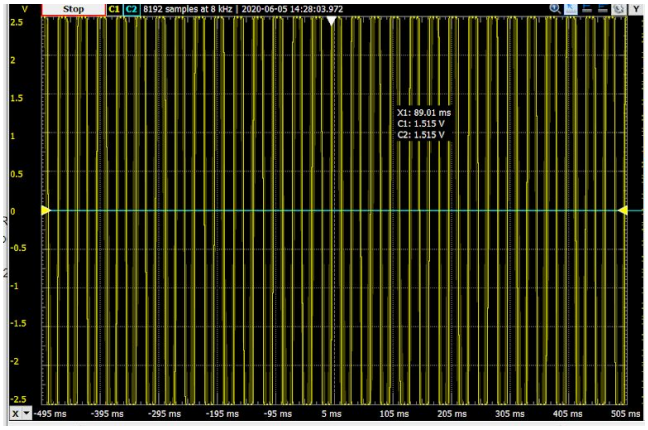

Figure 1.5 Output Voltage of Op-Amp in part D

The DC offset made the output back into a square wave, instead of reaching saturation.

A 4.7k resistor was added to the circuit in parallel with the capacitor giving the circuit below. Vin was also set to a 1V amplitude sinusoidal signal with 0 DC offset.

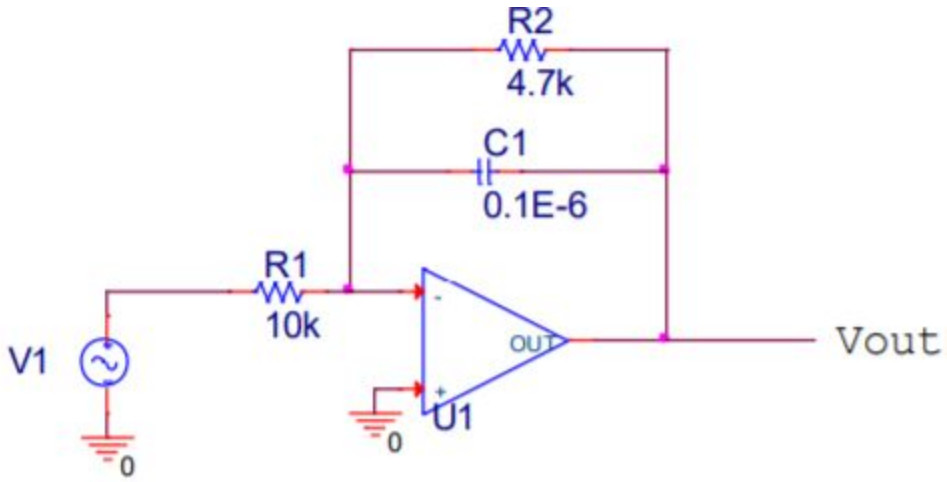

Figure 1.6 Integrating Amplifier circuit used for rest of exercise 1.1

1.) The transfer function for this circuit is H(s) = -(1/(.1E-6s + 2.12E-4)/10000 . The bode plot is shown below.

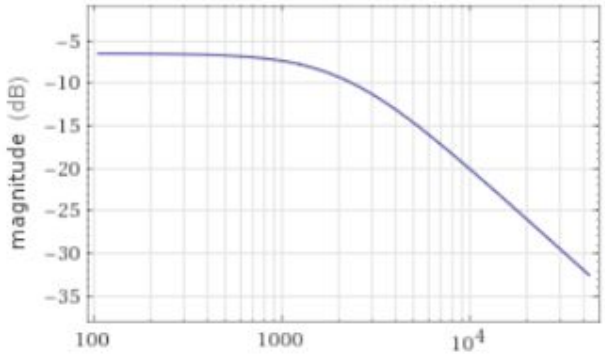

Figure 1.7 Bode Plot of Transfer Function

2.) There is a pole at 2120.
3.) On the discovery board, the frequency was swept from 10 Hz to 100 kHz, yielded the following output:

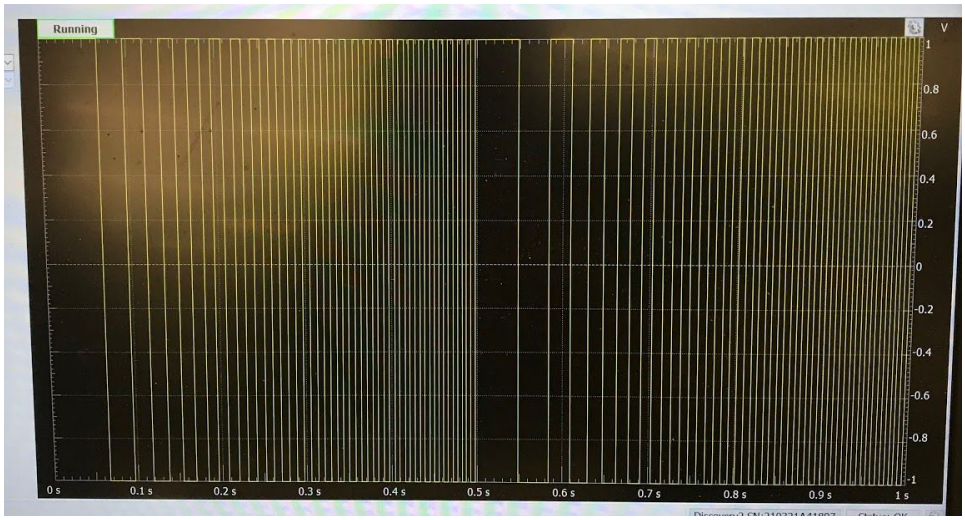

Figure 1.8 Output from Sweep on discovery board

4.) There seems to be a pole around 2000 which would be consistent with the analysis above , but it is hard to tell with this graph.

Exercise 1.2: Common mode gain, Differential gain

1.2) In exercise 1.2 a Difference amplifier was built according to the schematic below.

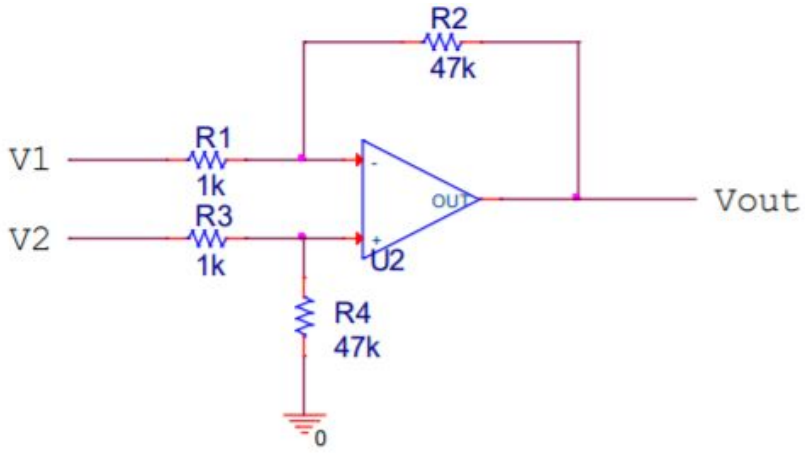

Figure 2.1 Difference Amplifier Circuit

The op amp was then fed the input shown below in figure 2.2, and resulted in the output shown in figure 2.3.

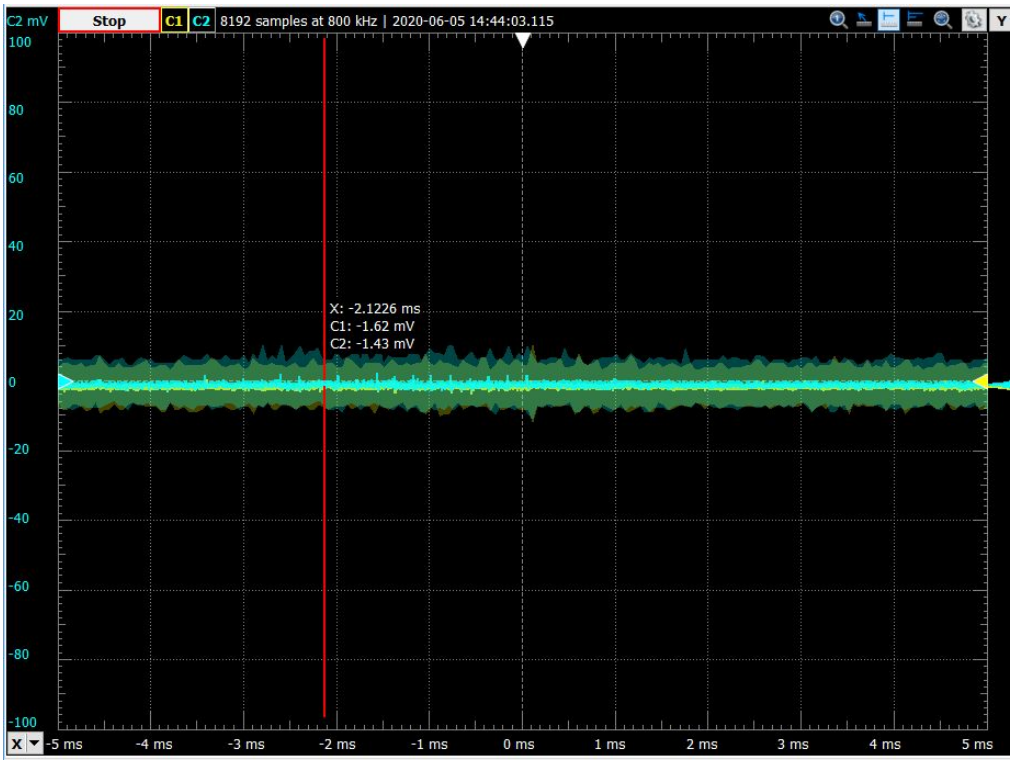

Figure 2.2 input voltage for the Op-Amp for part 2.1

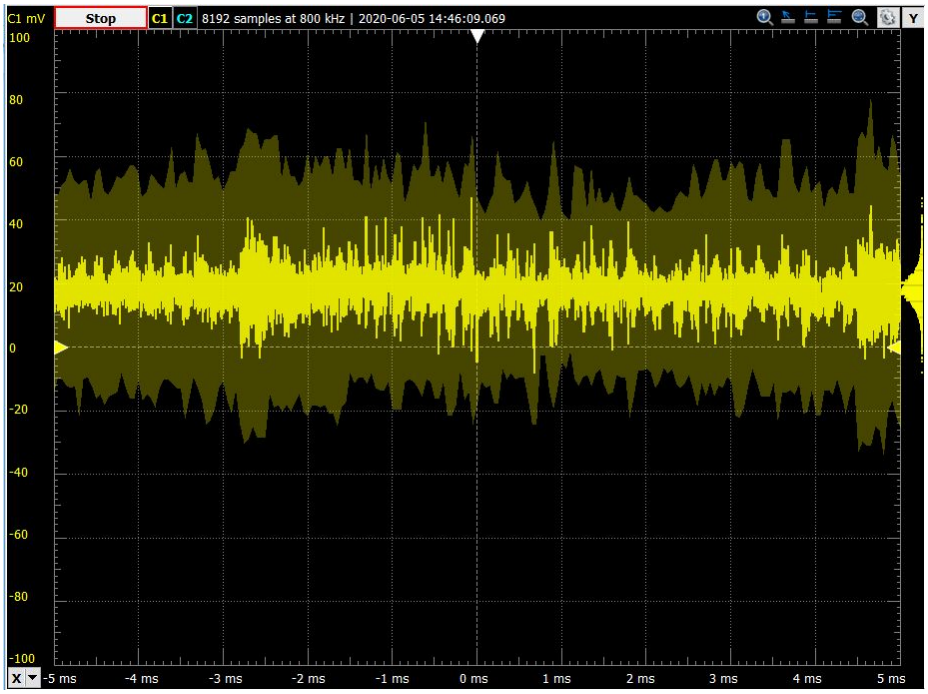

Figure 2.3 Output Voltage of Op-Amp for Part 2.1

The output voltage is roughly 10mV when V1=V2=0V. Thus we use 10mV as the ground

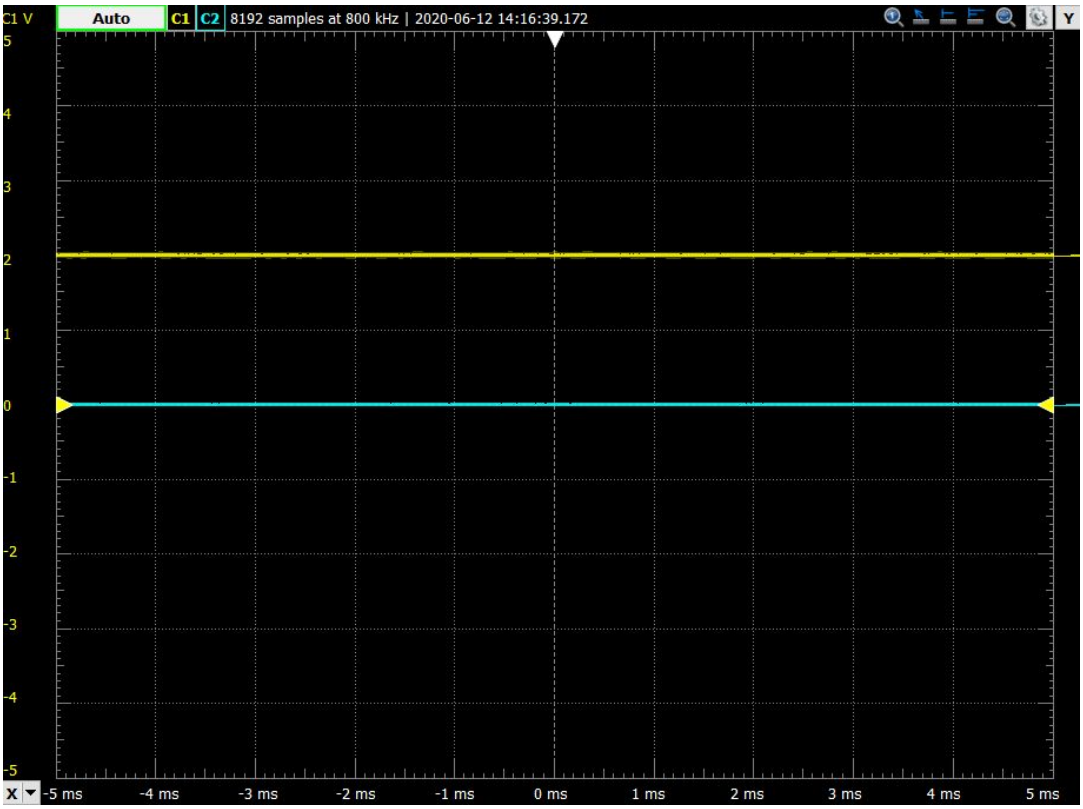

Figure 2.4 Input Voltage of Op-Amp for Part 2.2

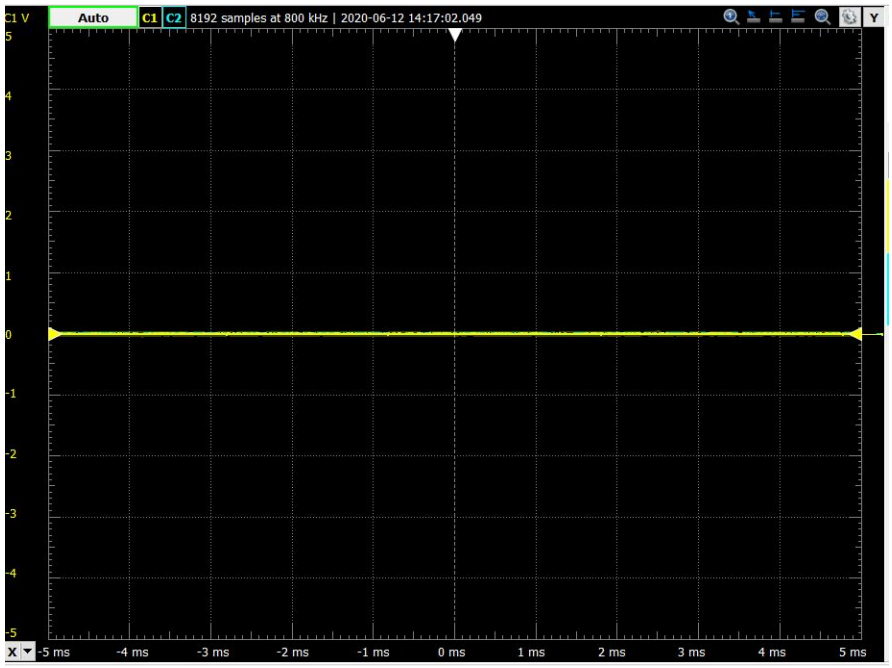

Figure 2.5 Output Voltage of Op-Amp for Part 2.2

The output when V1=V2=2V is roughly 0V.

We estimate common mode gain by the formula:

$$A_{CM} = \left(\frac{R4}{R3+R4}\right)\left(\frac{R1+R2}{R1}\right) - \frac{R2}{R1}$$

$$A_{CM} = \left(\frac{47k}{1k+47k}\right)\left(\frac{1k+47k}{1k}\right) - \frac{47k}{1k} = 0.$$

This is also seen in our measurements which has a gain of approximately 7mV / 2V = 0.0035 or practically 0V.

Figure 2.6 Input Voltage of Op-Amp for Part 2.3

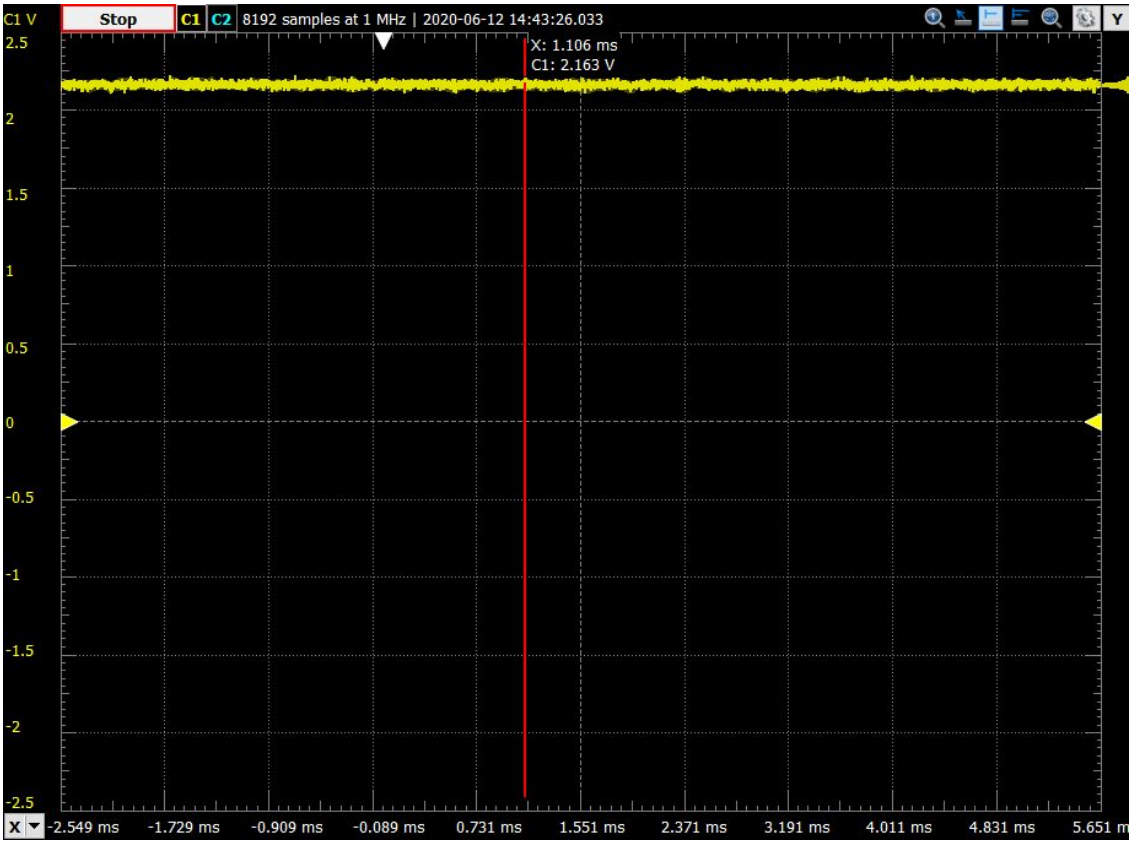

Figure 2.7 Output Voltage of Op-Amp for Part 2.3

The output is 2.163V which if we consider the DC offset will be 2.162V

We estimate common mode gain by the formula:

$$A_{DM} = 0.5 * ((\frac{R4}{R3+R4})(\frac{R1+R2}{R1}) + \frac{R2}{R1})$$

$$A_{DM} = 0.5 * ((\frac{47k}{1k+47k})(\frac{1k+47k}{1k}) + \frac{47k}{1k}) = 47$$

This is nearly consistent with the expected value. Resistor tolerances are affecting what the true resistance, and thus was the true differential gain is. It is within resistor tolerance though.

CMRR = 20log(Adm/Acm) = 82.56

1. Results were different due to resistor tolerances. Assuming that the Acm is kept the same, the Adm can change drastically. It's the luck of the draw with resistors and their tolerances. For example when I measured the resistance of my resistors. The supposed 47k was more around 46k. This can change the Adm values.

Exercise 1.3: DC Bias Characteristics

a. Offset voltage is around $10\ \mu V$. Bias Current is $10nA$. Bias current creates an offset proportional to the value of the resistors. Given that the circuit shown below in figure 3.1 has virtually no resistance in a practical application, the offset created is negligible.

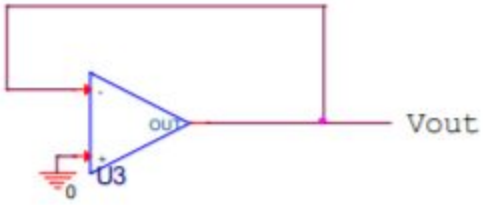

Figure 3.1 Circuit For Part 3 of Lab

b.

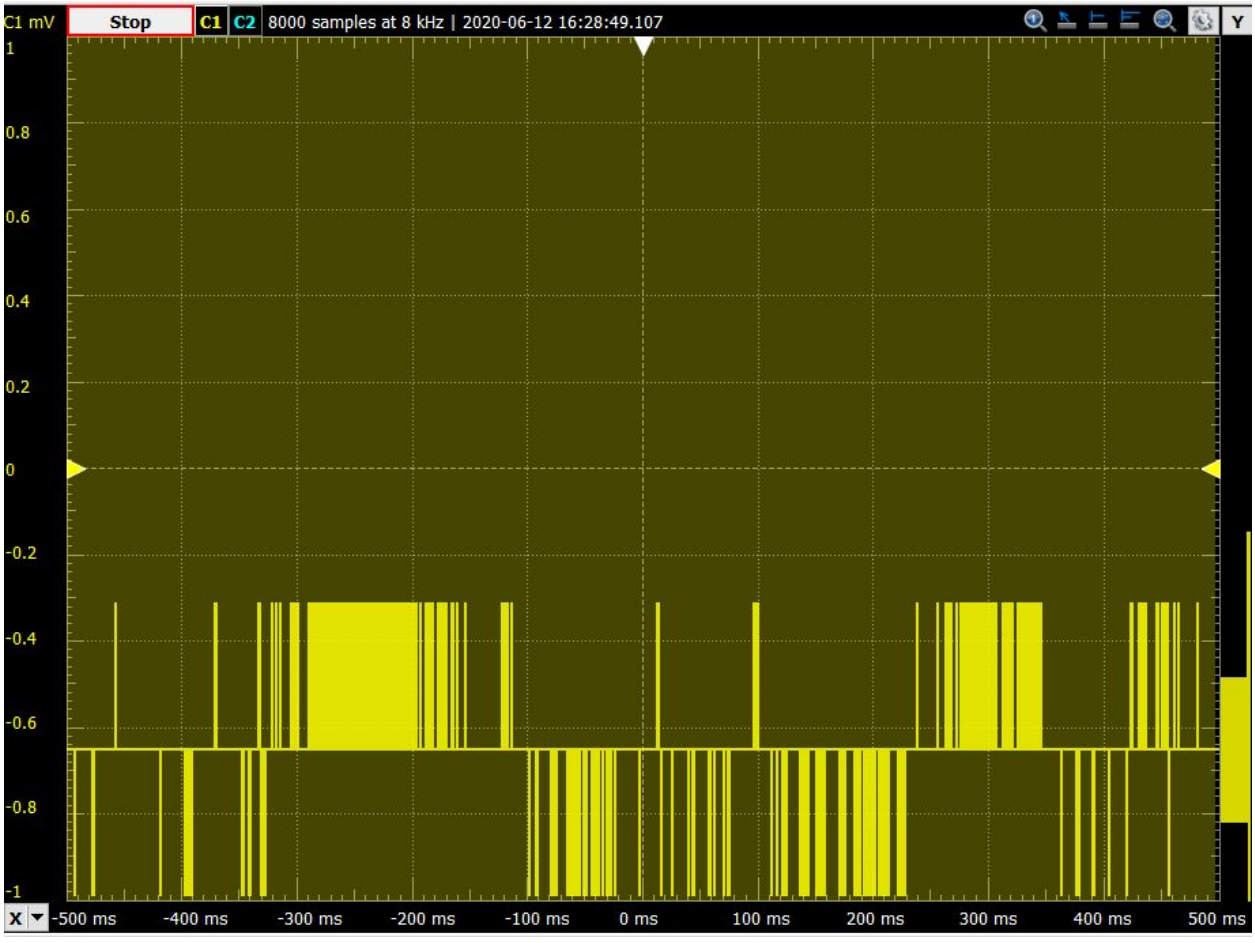

Figure 3.2 Output Voltage of Op-Amp for Part 3.1

The output is around -7mV. Analytically the output will be mostly due to DC Offset bias. Practically it is negative due to the Ground of the Discovery board not being a true 0V. This noise is larger than the DC bias of the amp which is listed on the MicroVolt range.

c. The Analog Discovery will cause most of the output. DC bias output from the op amp will matter. As resistances get larger the bias current will affect the circuit,shown below in figure 3.3, output.

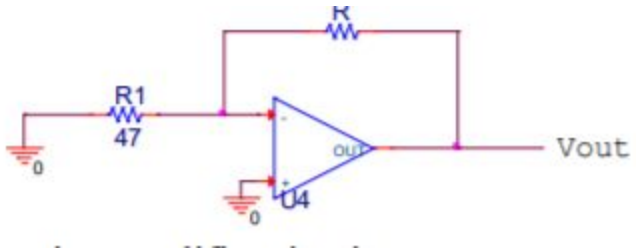

Figure 3.3 Circuit with added Resistor R1 for part C and D

For R = 47k

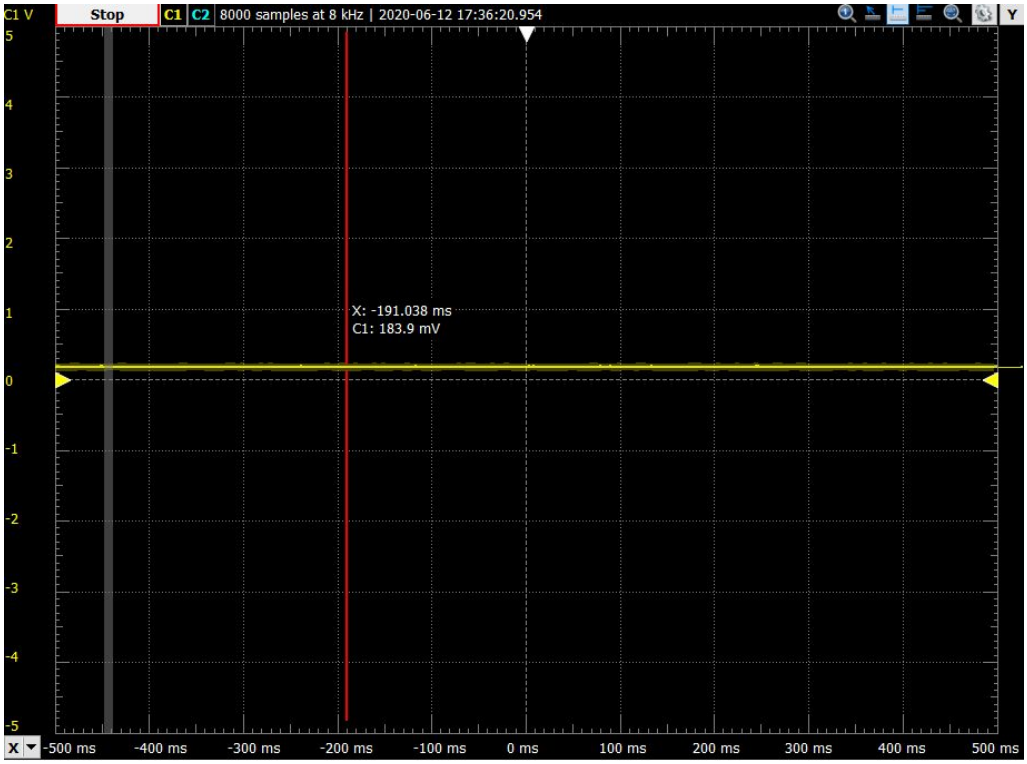

Figure 3.4 Output Voltage of Op-Amp with a 47k ohm resistor

For R = 470k

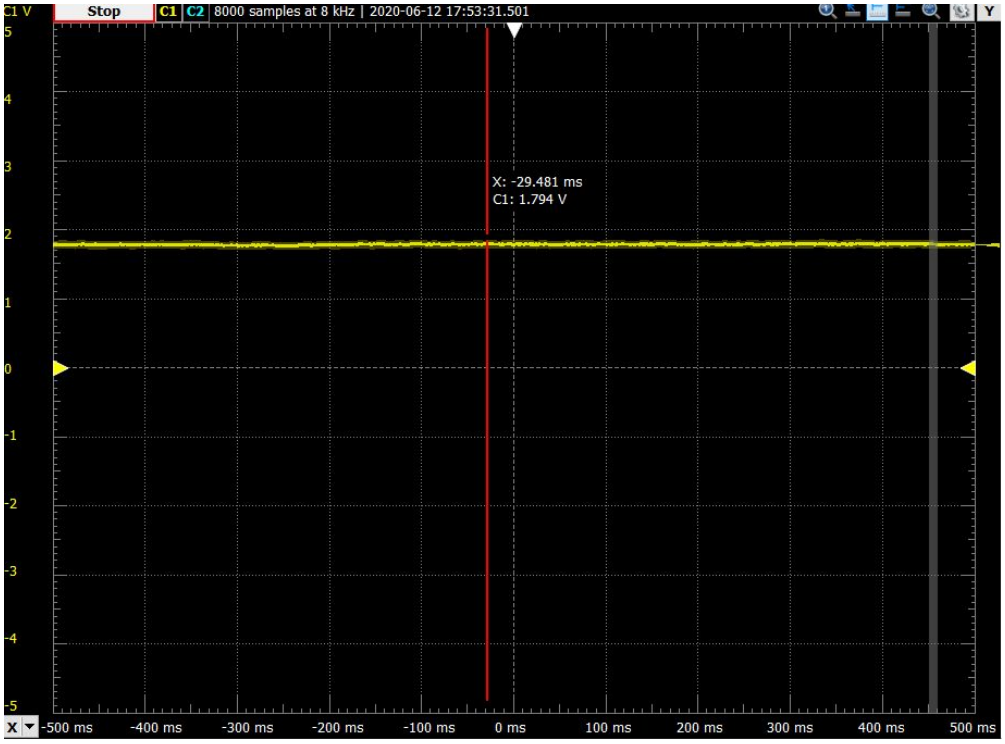

Figure 3.5 Output Voltage of Op-Amp with a 470k ohm resistor

For 1Meg

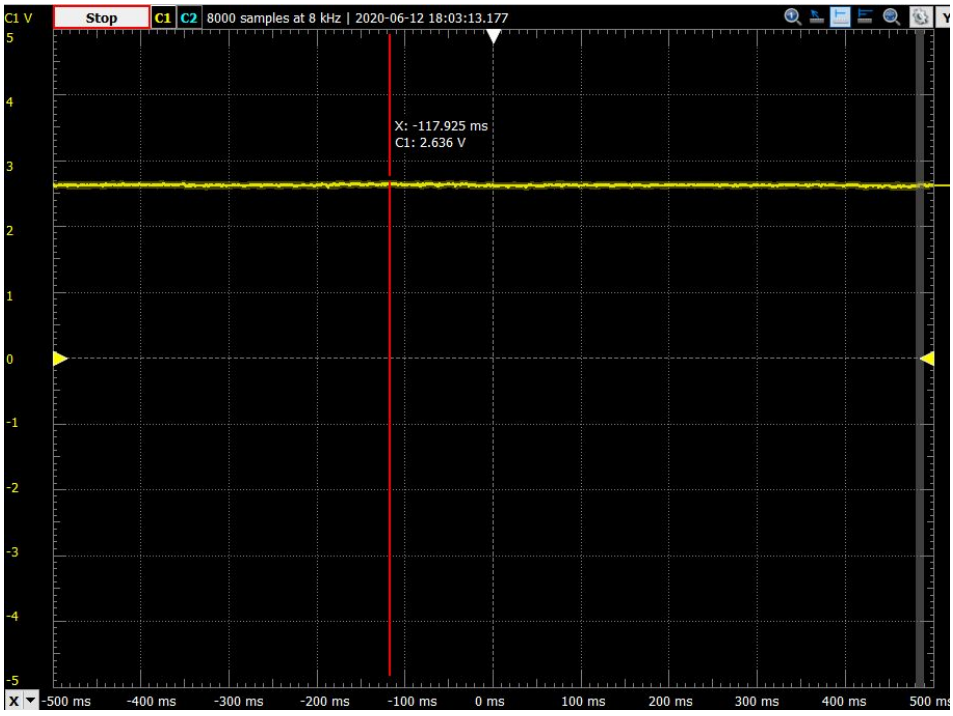

Figure 3.6 Output Voltage of Op-Amp with a 1 Megohm resistor

For 5 Meg

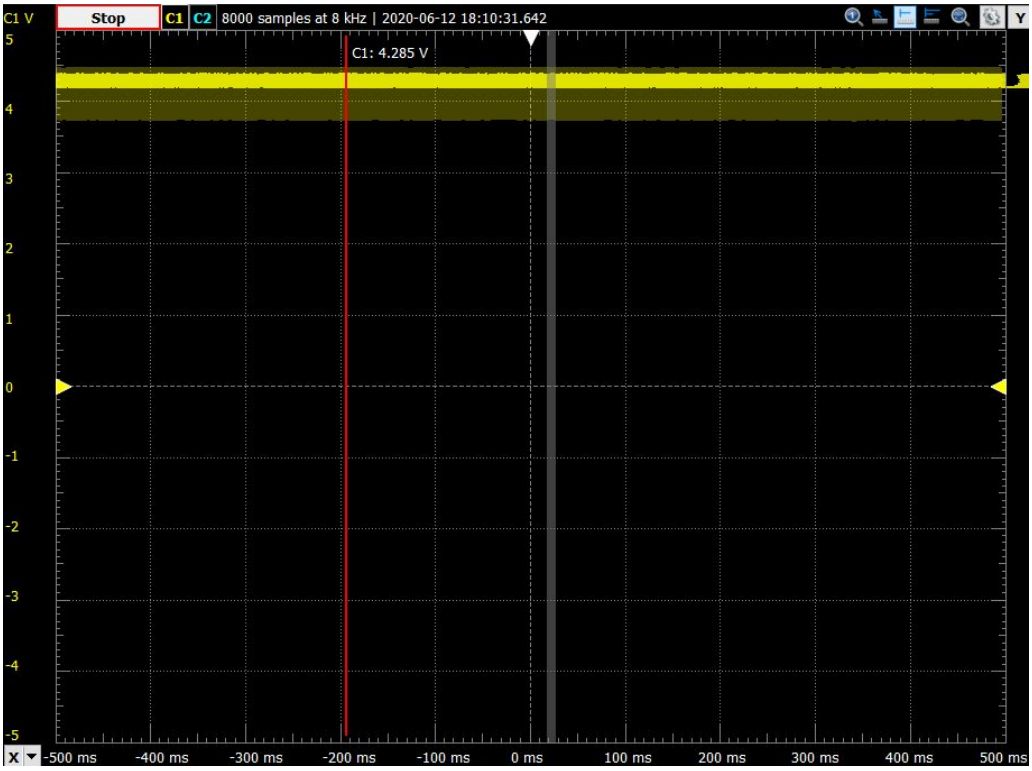

Figure 3.7 Output Voltage of Op-Amp with a 5 Megaohm resistor

We will ignore the 5 meg because it hit saturation.

$$183.9mV = \frac{-47k}{47}(7mV) + (1 + \frac{47k}{47})V_{DC} + 47k(I^{-}_{bias})$$

$$1.794V = \frac{-470k}{47}(7mV) + (1 + \frac{470k}{47})V_{DC} + 470k(I^{-}_{bias})$$

Solving the system of equations we get $V_{DC} = 0.005V \; ; \; I^{-}_{bias} = 4 * 10^{-5}A$

As compared to the spec sheet this is off by almost a factor of 1000. However as compared to part B these are quite close, well within the order of magnitude.

Exercise 1.4: Gain-Bandwidth product, Slew rate, Current Saturation

For part 1.4 the following circuit was built, using resistor values such that |R2/R1| = 5, 10, 50, 100.

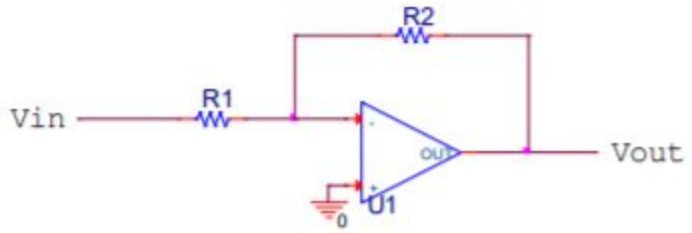

Figure 4.1 Inverting Amplifier Circuit used for part 4 of the lab

a.)

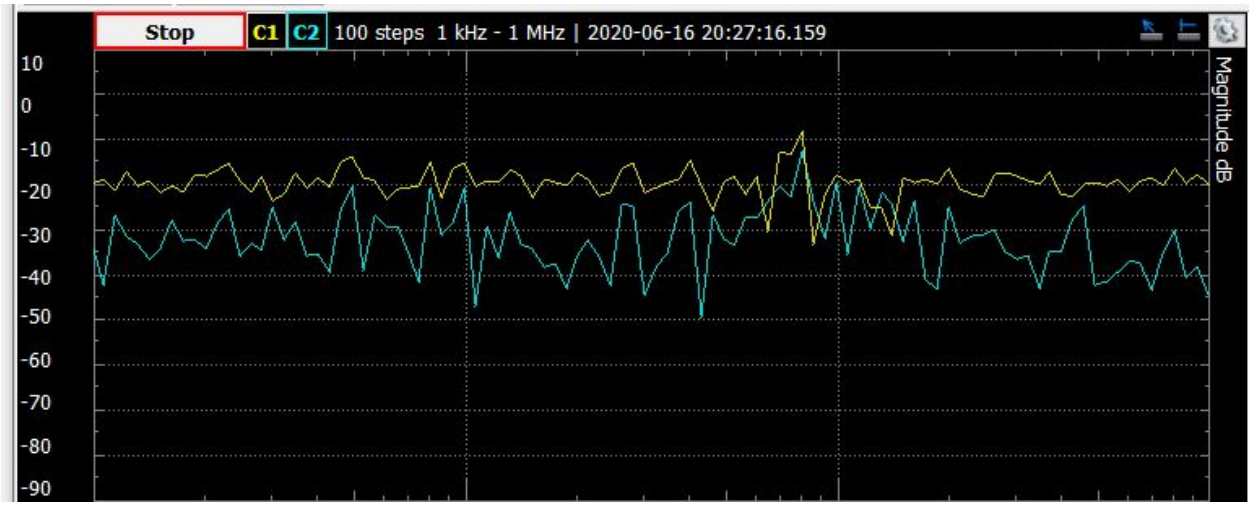

Figure 4.2 Output Voltage across Op-Amp when R2/R1 = 10

Shown above is the output for when R2/R1 is 10. The 3 dB cutoff frequency for the op-amp is estimated to be 4 MHz. The bode plots are active lowpass and are consistent with expectations.
b.) For the above values, the gain bandwidth product that was calculated was 3.8, 4.1, 4.2, and 3.9 MHz, according to the spec sheet the gain bandwidth product is 4 MHz consistent with our analysis.

c.) Output voltage when vin is set to a 4V peak to peak square wave, and R1 and R2 are both 1k.

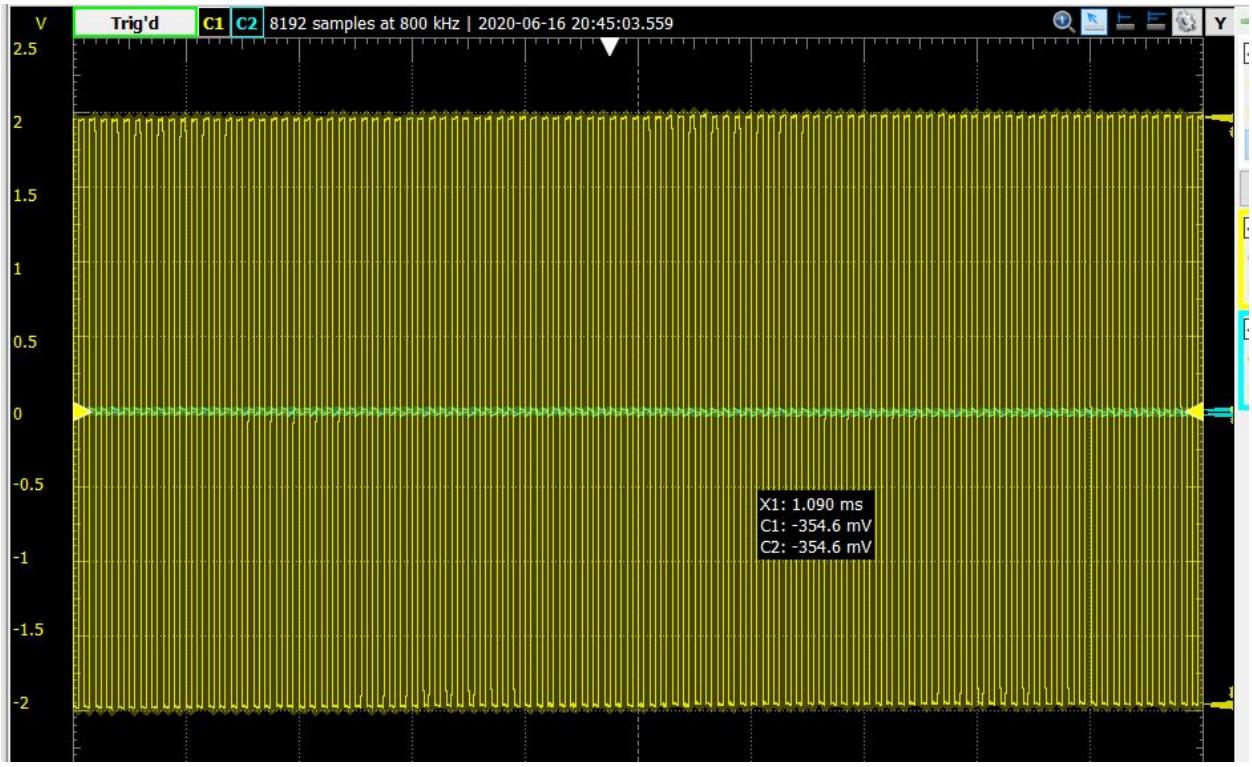

Figure 4.3 Output Voltage of Op-Amp when frequency is increased

d.) For the slope of the line, it is calculated to be 12.8 V/microsecond, the value for slew rate on the spec sheet is 13V/microsecond.

e.)The output when the frequency is increased to form a 2v peak to peak triangle wave.

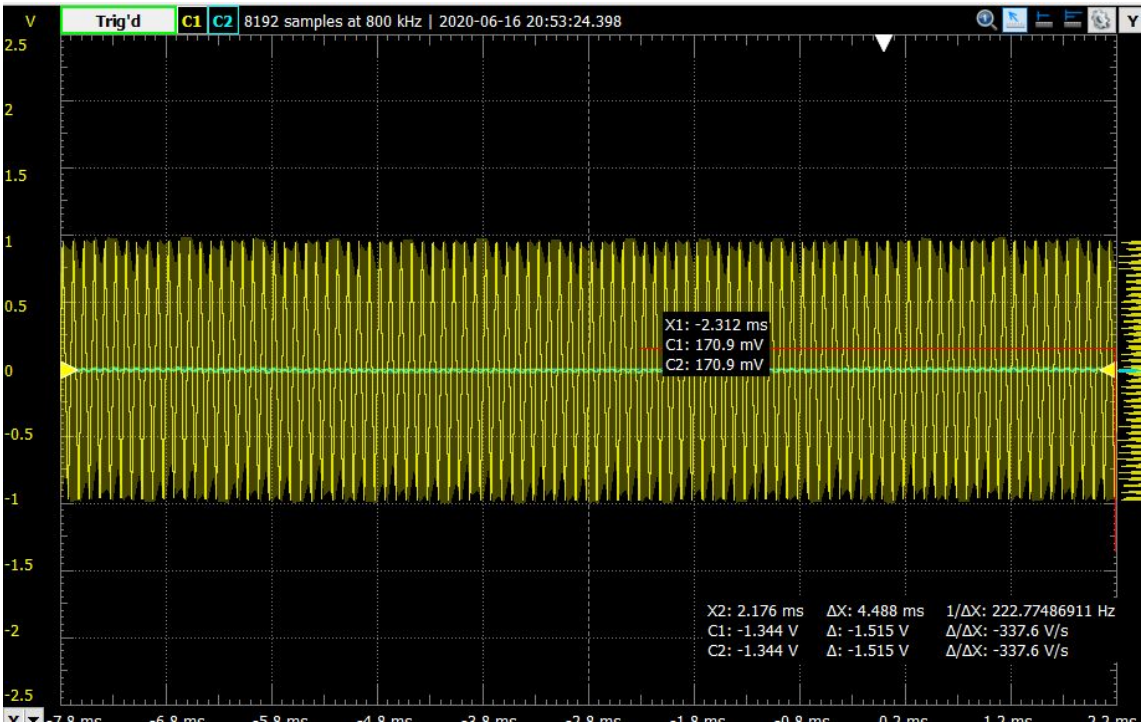

Figure 4.4 Output Voltage of Op-Amp when frequency is increased until a triangle wave is formed

g.) The following output is when a load resistor of 1k was added to the circuit as shown below.

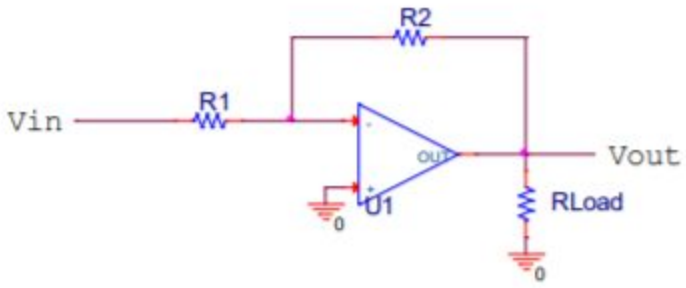

Figure 4.5 Inverting Amplifier Circuit with added load resistor used for part f and g

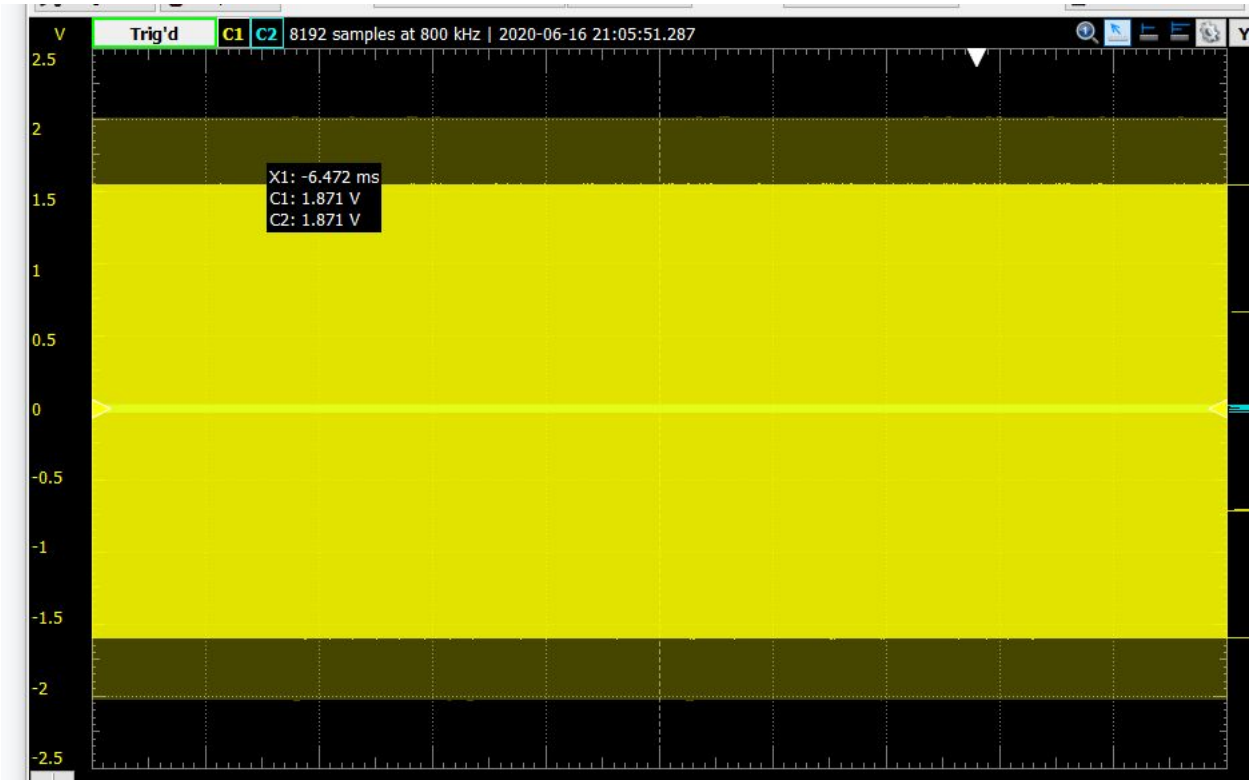

Figure 4.6 Output Voltage of the Op-Amp with added load resistor

The maximum output current is 1.5V/1000 ohms or .0015 A.

Conclusion:

For most normal conditions that the OP 27 was engineered for, it works quite well. The largest problems that can be experienced in a normal setting are, saturation voltage, and resistor tolerances. These become quite obvious when trying to perform some rigorous applications of op amps like voltage following. However when you try to push the precision of the op amp, it's real characteristics show. At high frequencies and at small voltage inputs the outputs begin to shift, which is computable.