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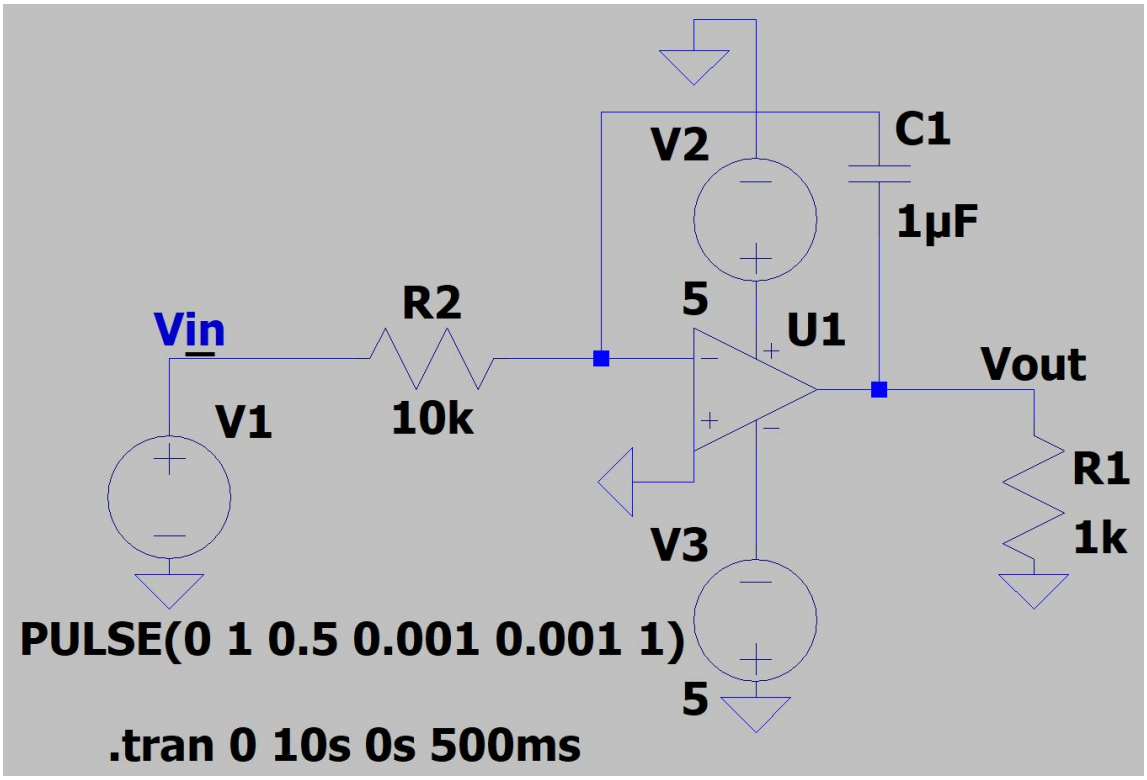
1: Prove Op Amp with Capacitive/Inductive Feedback Network

WE ARE OPTIMIZING OMEGA LABS PROOF OF CONCEPTS 3

Building Block: (Changed schematic node label from V1 to Vin)

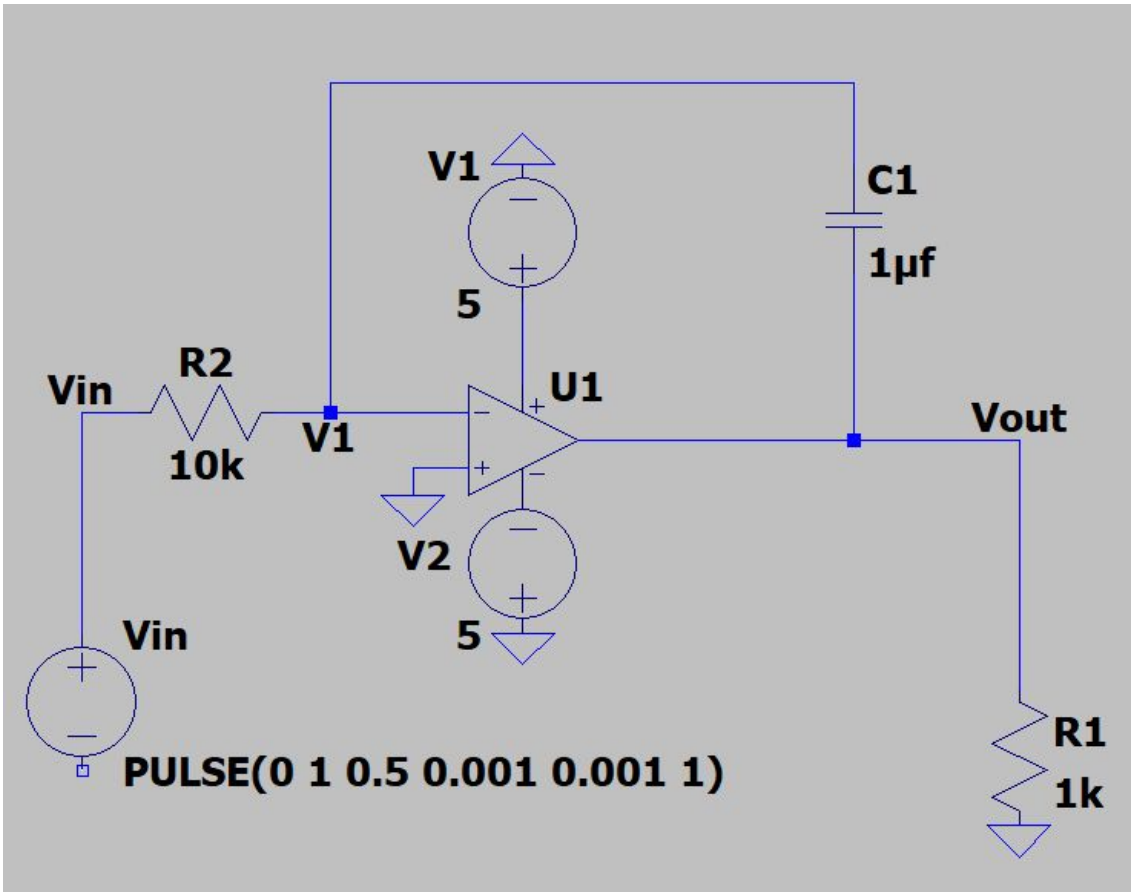
Description: An Integrator Circuit (first order). The positive op amp input is tied to ground and the input voltage to the negative input terminal is a square wave, where the amplitude is 1 volt. The resistor on the negative input is 1Meg ohm, The capacitor on the negative feedback loop is 1uf, and the resistor on the output terminal is 1k ohm. The power supply to the op amp is 5 volt.

(OLD)



Nodes to be analyzed: Vout and Vin

(NEW)



Nodes to be analyzed: Vout, Vin, and V1

Analysis:

Doing KCL at node V1:

Since the positive input terminal of the op amp is tied to ground and using the fact that voltage at positive terminal equals the voltage at the negative terminal when there is a feedback loop in the op amp, we know at node V1 at the negative input of the op amp is 0V. Hence V1=0. Doing KCL at that point, we get:

$\frac{0-Vin}{R_2} + c\frac{dv}{dt} + 0 = 0$

$c\frac{dv}{dt} = \frac{Vin}{R_2}$

$c\int \frac{dv}{dt} = \int \frac{Vin}{R_2}$ integrate both side

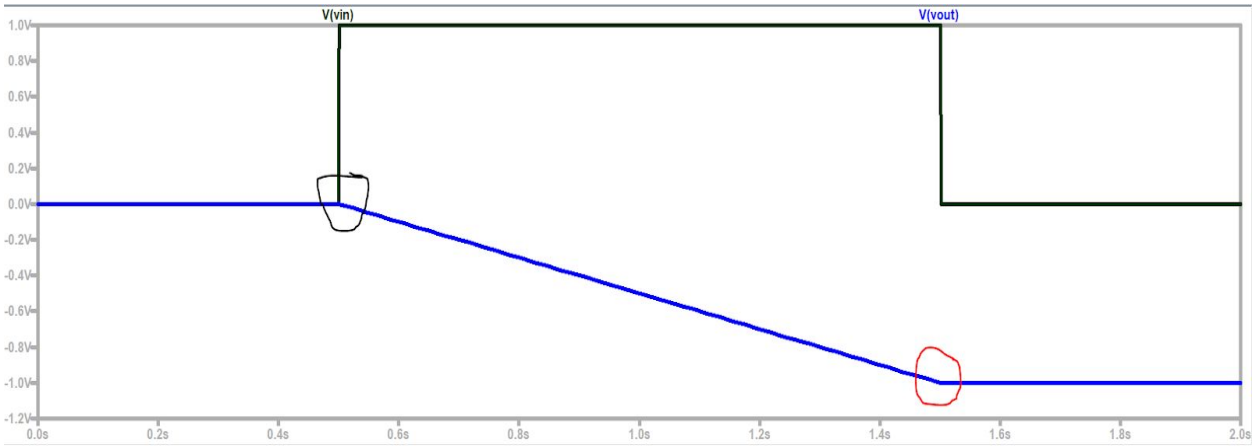
We know the change of voltage over the capacitor at node V1 is $\triangle V$ which is 0-vout

C (-vout)= $\frac{1}{R_2}\int$ Vin dt

vout=- $\frac{1}{CR_2}\int Vin\, dt$

Result from analysis is that vout is integral of the Vin signal over a specified time period divided by the product of the capacitance value on the feedback loop and the resistor value on the negative input of the op amp.

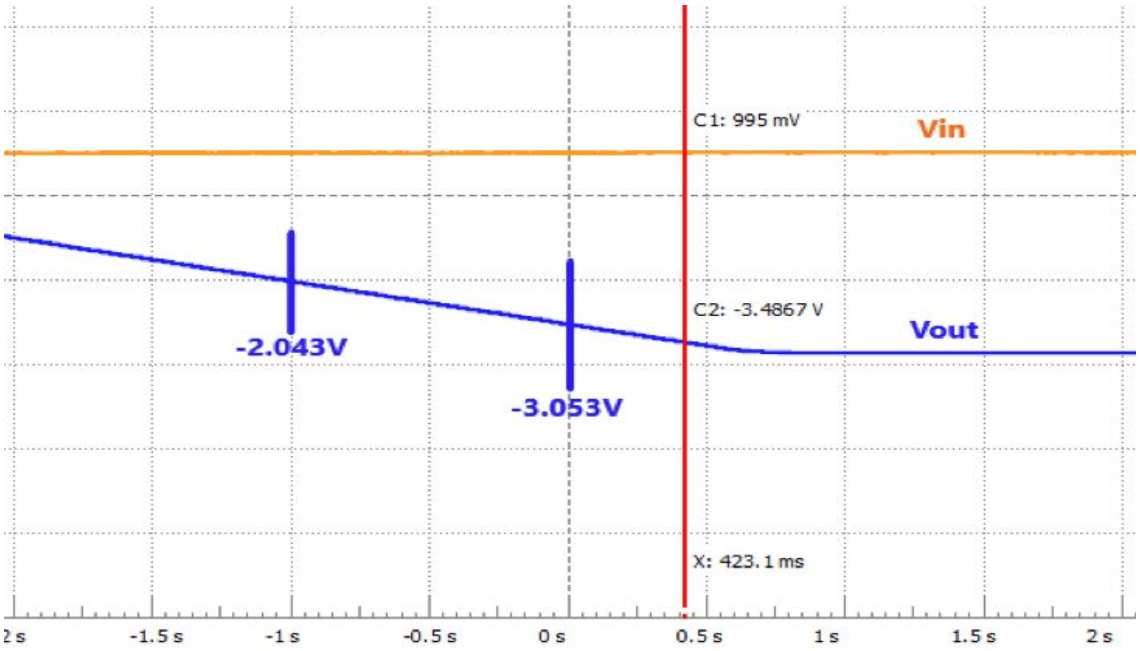
Simulation:



The black curve is the input signal. The integral or area under the curve is $1V * 1s = 1t$. The blue line is the output of the integrator op-amp. Because we chose $R * C = 1$, the output should be $-\int V_{in}$. We know that the integral is $1t$ so the output is $= -1t$. We can verify this be calculating the slope of the blue line which is -1. Thus our simulation matches our analysis.

Measurement:

Build the circuit with the resistance of 10^6 ohm and capacitor of $1\mu C$



Just like in Simulation we verify by finding the slope. $\frac{-3.053+2.043}{0+1} \approx -1$. There is some difference due to non-ideal components

Discussion:

From the result from the analysis portion, an integrator op amp integrates the given Vin voltage signal over a given time divided by the product of the capacitance value on the feedback loop and the resistor value on the negative input of the op amp. The simulation from LTSPICE and the measurement from

analog discovery backs up the analysis. We selected a resistor value and capacitance that yield a value of 1 and an input is a square wave on the LTSPICE simulation and a constant voltage signal for analog discovery. It can be seen that in both scenarios the result is a negative, linear voltage signal that saturates to the power supply of the op amp. From basic calculus, the integral of a constant V is V(t) which is a linear function which matches the output of the simulation and measurement. In both simulation and measurement since $\frac{1}{RC}$ is 1 and Vin is 1V. Our integration yields a slope of 1V. From analog discovery measurement the slope calculation is $\frac{-3.053--2.043}{-1}$ = $\frac{-1}{-1}$ = 1V and from the LT splice simulation graph, the
slope calculation is $\frac{1-0}{1.5-0.5}$ = $\frac{-1}{-1}$ = 1V. The slope from measurement and simulation matches the math from the analysis.

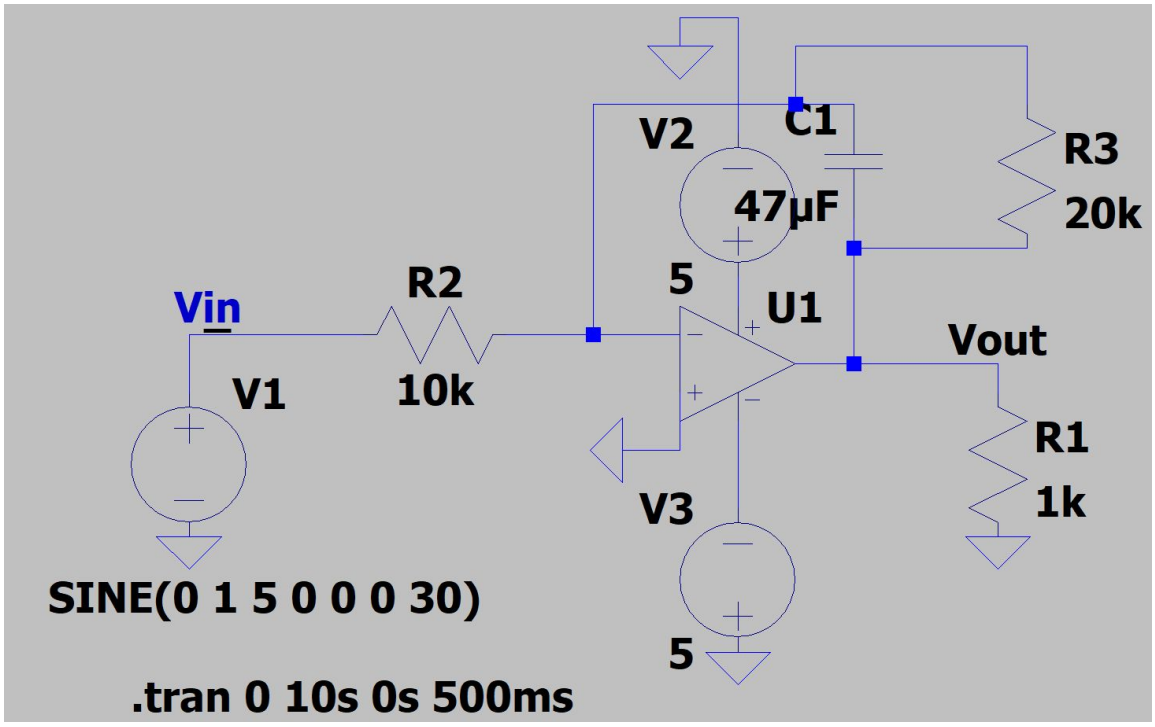
We will use the integrator in our final circuit to take in the AC output from MQ9 sensors and outputs the negative summation over a period of time. We could easily just compare the MQ9 sensors at instantaneous values, but it's a much more rigorous reading if we actually compare over a longer period of time. The sensor outputs a higher signal if the area is polluted and a low signal if there is no pollution. Thus when we take the negative integral of the signal we see that the lesser value will represent more pollution. We can use this in further comparisons. Thus the inverting integrators allows us to take the summation of a signal and allows us to compare two signals over a period of time.

2: Proving Equivalent Impedance

Building Block: (Changed schematic node label from V1 to Vin)

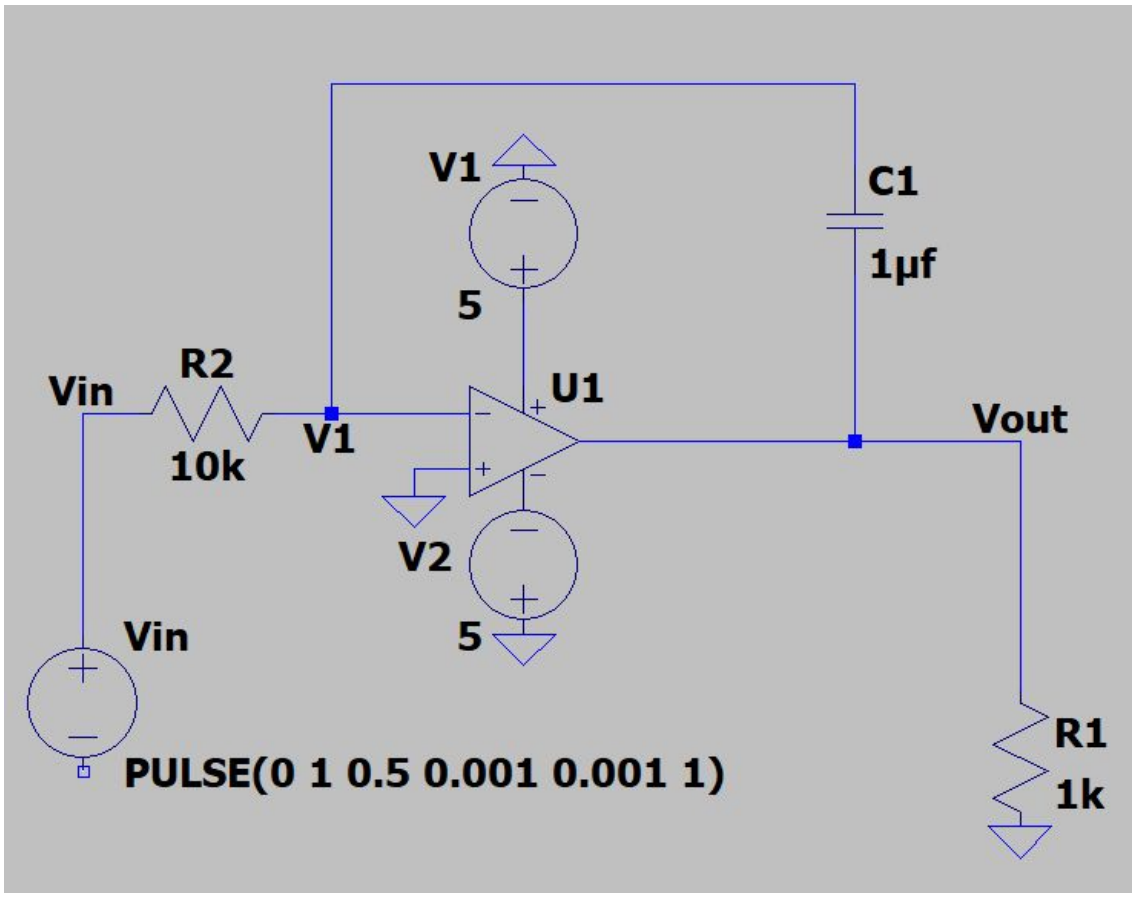
Description: The circuit is an op-amp with a feedback loop of a capacitor and resistor in parallel. We use this to analyze the AC steady state equivalent impedance. We input a sine wave with 1V amplitude with frequency of 5 hertz. The resistor to the negative input of the op amp is 10k, the capacitor (47uf) on the feedback is parallel to a resistor (20k). The op amp is powered by 5V.

(old)



Nodes to Be Analyzed: Vin, Vout, C1, R3, R2

(New)



Nodes to Be Analyzed: Vin and Vout

Analysis:

In AC steady state the impedance of a capacitor is equal to $1/j\omega C$. Thus in our circuit, we can analyze the AC steady state impedance of the resistor in parallel with the capacitor to generate an inverting amplifier circuit.

The inverting amplifier formula is: $V_{out} = V_{in} - Z_f/Z_1$. We define our impedance values:

$$Z_f = (\frac{1}{Z_c} + \frac{1}{Z_R})^{-1} = (j\omega C + \frac{1}{20*10^3})$$

$$Z_1 = R_2 = 10k\,\Omega$$

Other values we will use: $\omega = 10\pi$; $C = 47 * 10^{-6} F$

Because this is in AC steady state we are only interested in the gain this equivalent impedance provides us. Our sin wave amplitude = 1. Plugging in our values to the equation for V_{out}

$$V_{out} = -(j(10\pi * 47 * 10^{-6}) + \frac{1}{20*10^3}) * \frac{1}{10^4}$$

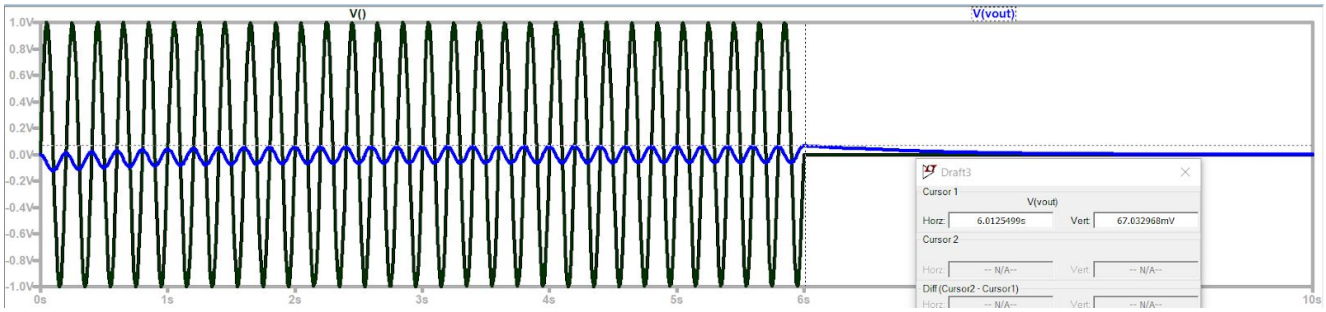
$$V_{out} = \frac{-50}{25+2209\pi^2} + j\frac{470\pi}{25+2209\pi^2}$$

While in the form $V_{out} = aj + b$, the gain will be equal to $\sqrt{a^2 + b^2}$. We calculate this.

$$\sqrt{\left(\frac{-50}{25+2209\pi^2}\right)^2 + \left(\frac{470\pi}{25+2209\pi^2}\right)} = 0.067$$

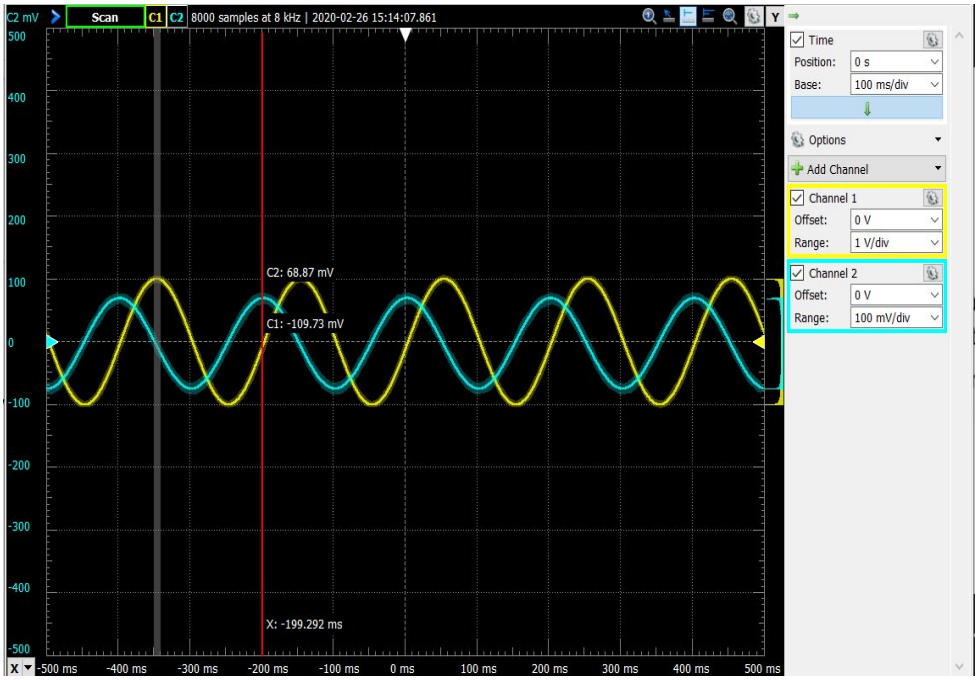
Thus with an input amplitude of 1V we expect the output to be $1V * 0.067 = 67mV$

Simulation:(ADDED Y AXIS)



Based on our predefined definition of AC steady state ($5 * \tau$), from our circuit, after roughly 5 seconds it reached AC steady state. We measure the vertical height of Vout at the cursor location and find that it is roughly 67mV. This matches our predictions from analysis

Measurement:



Blue is the output and yellow is the input.
We input 1V sine wave with a frequency of 5 hertz.
The peak on the yellow since wave is 1V and the peak on the yellow is ~68.87mV
The measurement gain is:
input*gain=output
1*gain_measurement=0.06887
gain_measurement= $\frac{0.06887}{1}$

gain_measurement=0.06887

Discussion:

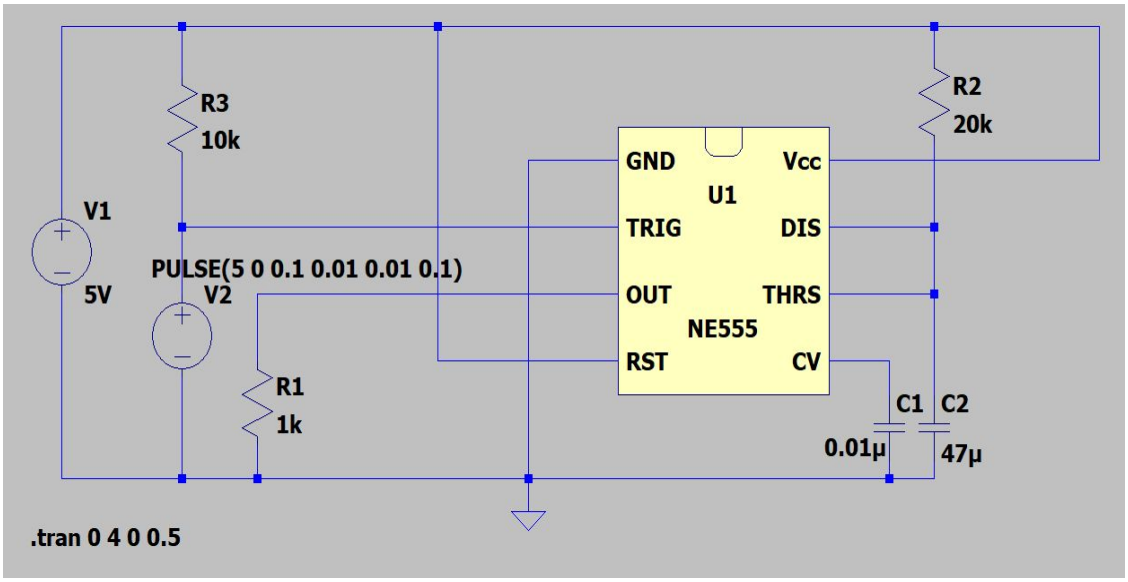
With a resistor in parallel with the capacitor in the feedback loop, we get an amplifier integrator when we input a sine wave. From the analysis, we $V_{out} = \sqrt{a^2 + b^2} \angle$ tan(b/a) where **b** is the real part and **a** is the imaginary part. In our measurement, we got a gain of 0.06887 and in our simulation, the gain is 0.067 and our analysis, the gain is 0.067. The simulation and analysis match while the gain from analog discovery differs by 0.00187 due to resistor tolerance. Applying 5% tolerance, 0.06887+0.05(0.06887) and 0.06887-0.05(0.06887). The bound is [0.0654265,0.0723135], the expected result is within the 5% tolerance.This shows that with a resistor in parallel with the capacitor, we can use impedance to analyze the output voltage.

We use this design, having the resistor in parallel with the capacitor, to allow the capacitor to be discharged after each use of integration when we have our results from the current reading over a time period to compare. This makes the inverting integrators ready for the next usage in the next time period by removing charge from the capacitor from current reading when the sensors are turned off in their down time. When a trigger turns on the sensor again, we can get a clean integration result that was not influenced by previous reading. In the future if we have a large capacitor for our op amp, it can hold charge for quite some time, depending on the level we charge it to. We don't want that to affect the next reading.

3: Proving First Order Circuit with Differential Equations

Building Block:

Description: We have a 555 timer wired as a monostable multivibrator. The input voltage is 5 voltage, the switch “pulse” source goes from 5V to 0V and serves as a negative edge trigger for the 555 timer. We chose resistor and capacitor values so that the output holds for 1 second.



Nodes to be Analyzed: V1, R2, C2

Analysis:

The Output of the 555 timer is exclusively controlled by an RC circuit consisting of R2 and C2. This circuit becomes “active” when the input to the 555 timer is given a negative edge, as shown by the V2 Pulse component. This creates a circuit of V1 series with R2, series with C2. The output is then turned off when the $V_{C2} = V_{CC} * 2/3$.

We analyze the RC Circuit using differential equations to solve for the voltage across C2 in time.

KVL around the circuit: $-V1 + iR + Vc = 0$

$i = i_R = i_c = C\frac{dV_c}{dt} \longrightarrow RC\frac{dV_c}{dt} + V_c = V1 \longrightarrow \frac{dV_c}{dt} + \frac{1}{RC}V_c = \frac{V1}{RC}$

Guess that $V_c(t) = Ae^{\frac{-t}{\tau}} + A_2$. Initial conditions: $V_c(0) = A_1 + A_2 = 0$

$V_c(\infty) = A_2 = 5$. $A_1 = -A_2 = -5$ thus $V_c(t) = -5e^{\frac{-t}{.94}} + 5$

From our analysis we must find the t that makes $V_c(t) = \frac{2}{3} * V_{CC} = \frac{10}{3}$

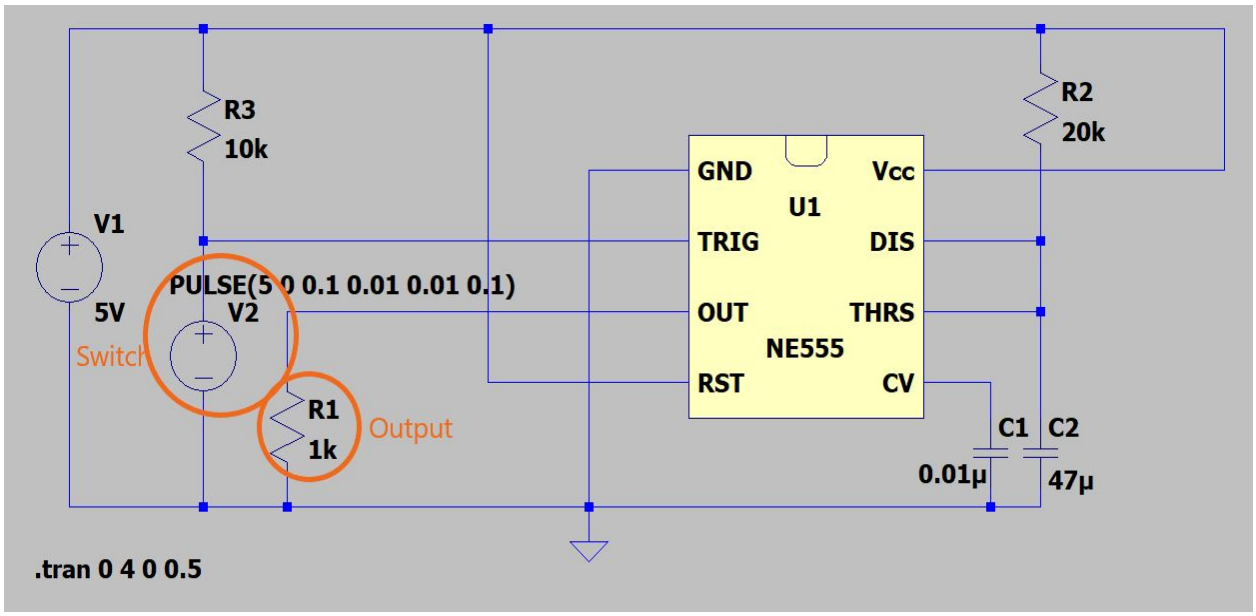
$V_c(t) = -5e^{\frac{-t}{.94}} + 5 = \frac{10}{3}$

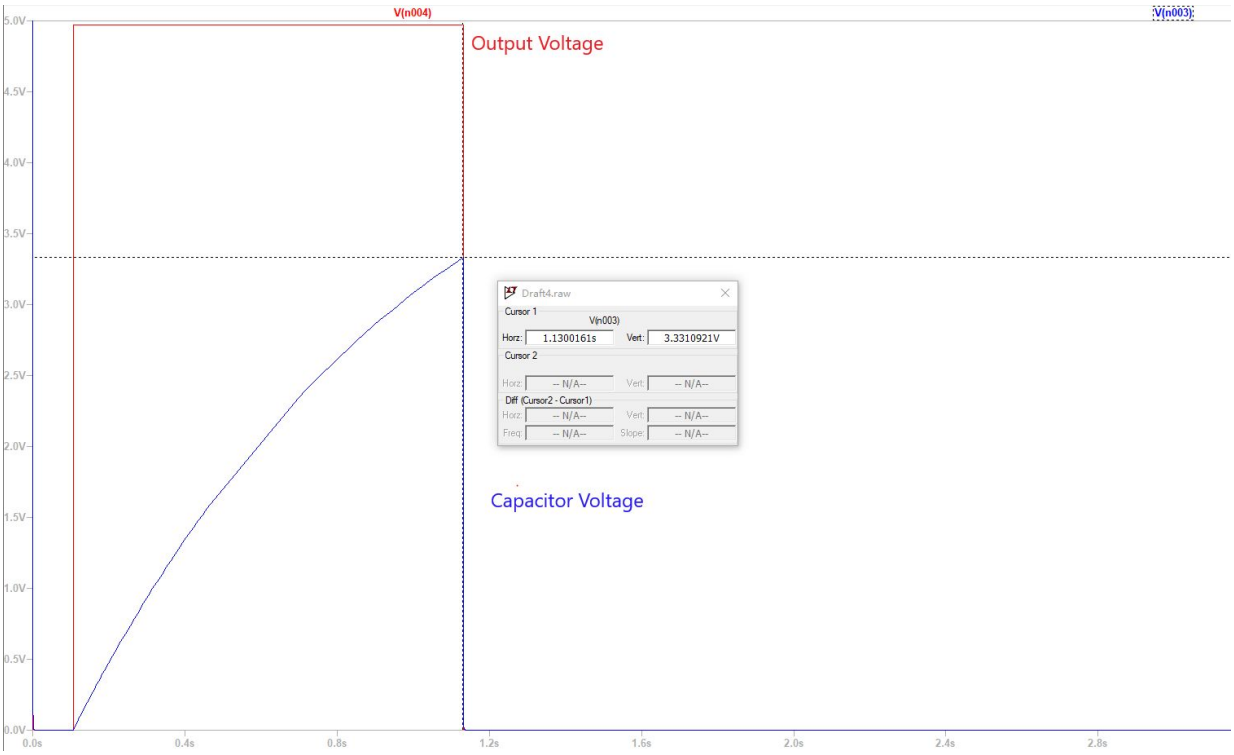
$t = -.94(\ln(\frac{-2}{3} + 1))$

$t = 1.03$

Thus our analysis predicts our output should hold for roughly 1 second.

Simulation:

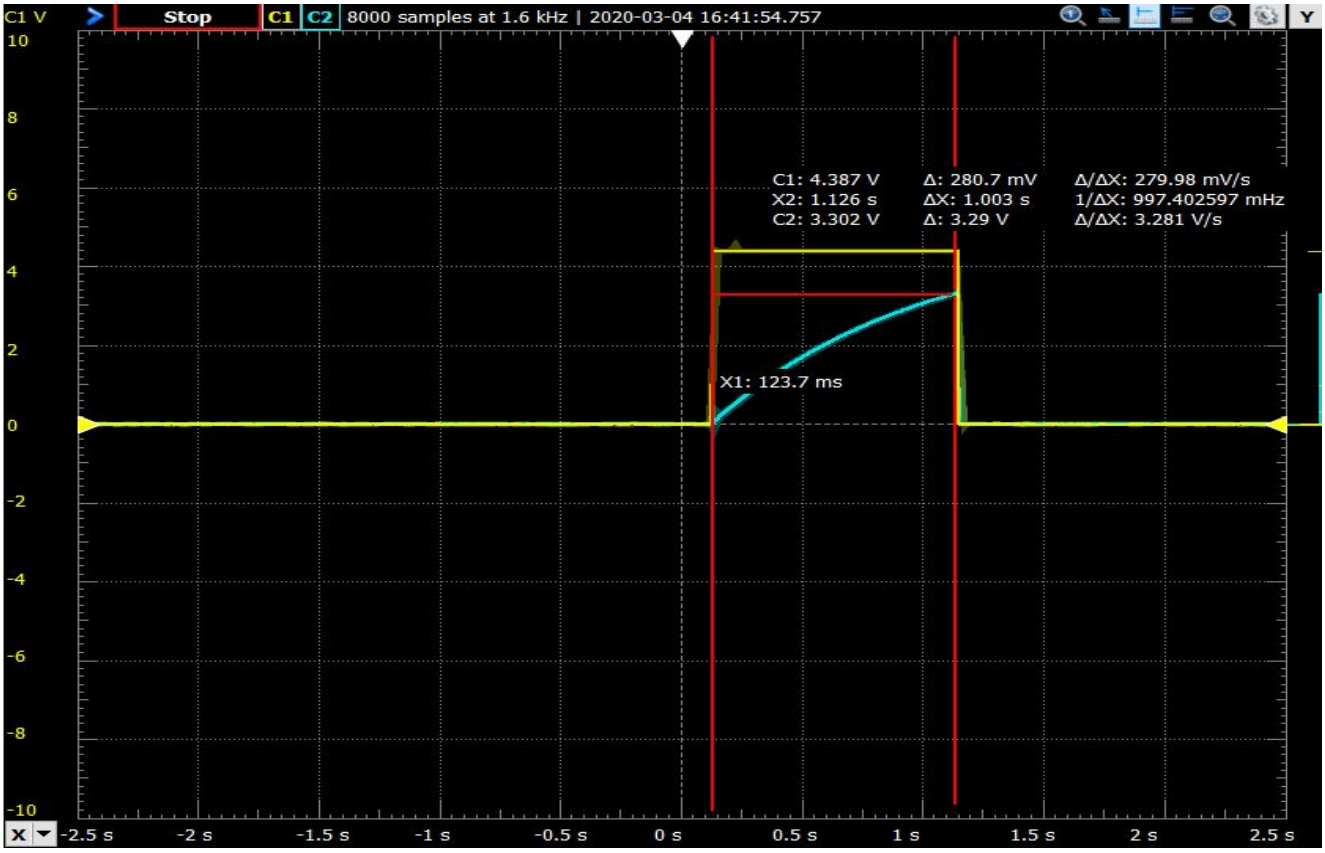




Consistent with the analysis, the Capacitor Voltage (Blue) reaches ⅔ of Input Voltage (3.33V) in 1 second causing the output voltage (red) to turn off.

Measurement:

The time on for the pulse is 1.029 seconds



When the capacitor voltage reaches 3.302V (⅔ of the reference 5V) the output of the 555 timer is low. It reaches that time in roughly 1 second which is consistent with analysis.

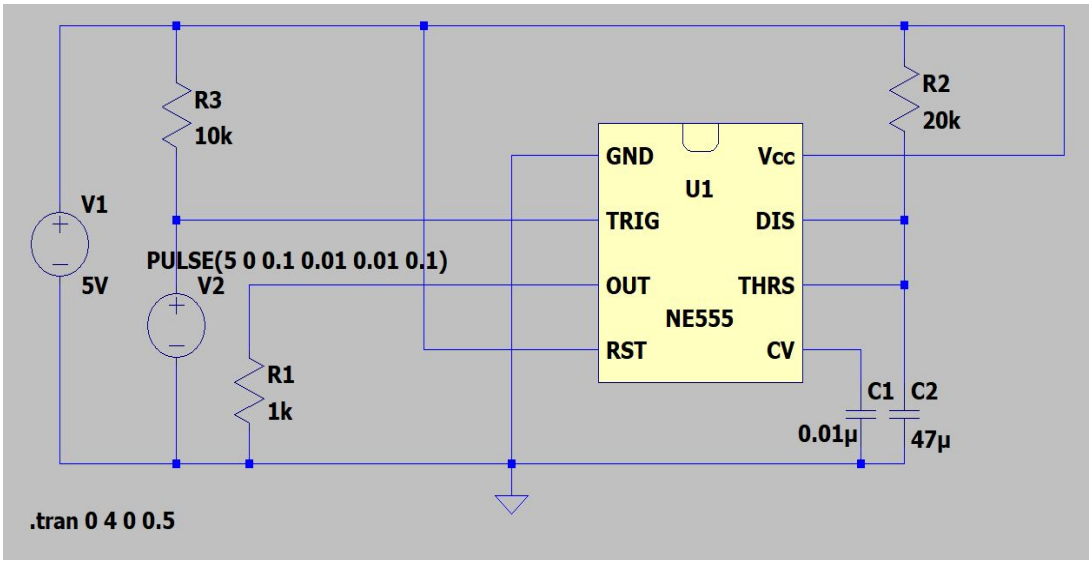
Discussion:

The 555 timer sends a high pulse when the trigger is high (5V) and matches with Vcc(5V). The comparator sends a high signal to the Flip Flop which is controlled by the comparator from Threshold pin and Vcc and the Reset pin. The reset pin is always 5 V because it is connected to Vcc and the comparator is between the capacitor voltage and 5V. The Flip flop is a negative trigger so when the capacitor voltage is equal to ⅔ of 5V, the comparator sends a high signal which turns the Flip Flop off. The analysis of the 555 timer on time matches with the simulation and measurement. The output is then turned off when the $V_{C2} = V_{CC} * 2/3$. The capacitor, as shown in the analysis part takes roughly 1 second to charge up to $2/3$ of 5V, the time matches with the simulation and measurement result which both shows that the width of the pulse is ~1 second. The slight differences between 1.029 second (measurement result) and 1.03 second (analysis result) is due to rounding error and non-ideal components.

4: Proving First-Order Circuit (RC or RL) with Laplace/S-Domain Analysis:

Building Block:

Description: We have a 555 timer wired as a monostable multivibrator. The input voltage is 5 voltage, the switch “pulse” source goes from 5V to 0V and serves as a negative edge trigger for the 555 timer. We chose resistor and capacitor values so that the output holds for 1 second.



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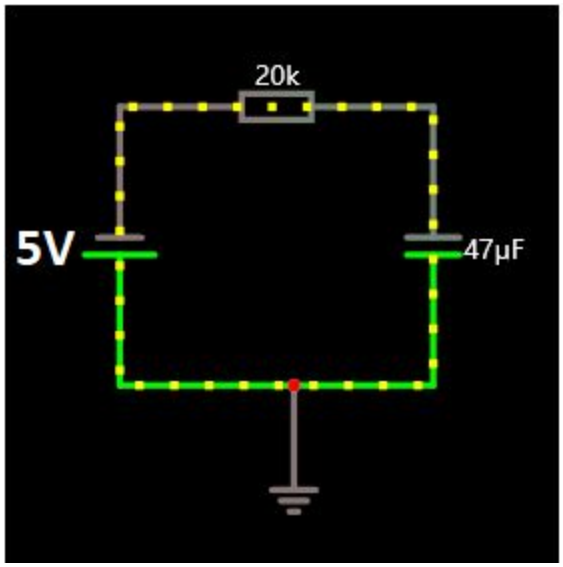


We analyze the circuit using S-Domain analysis. Resistors stay as resistors, our voltage source is a step function of $5u(t)$, and the cap in S-Domain is equal to $\frac{1}{sC}$.

Voltage across the cap will be a voltage divider which we solve in S-Domain.

$$V_C = \frac{V_{in} Z_2}{Z_1 + Z_2} = \frac{5}{s} * \frac{1}{sC(\frac{1}{sC} + R)}$$

$$V_c = \frac{5}{s(1 + sRC)} = \frac{5}{s(1 + 0.94s)}$$ expand using partial fractions

$$\frac{A}{s} + \frac{B}{1 + 0.94s} = \frac{5}{s(1 + 0.94s)}$$ zeros: none, poles: 0, -1.06383

Cover up rule using $s = 0 \rightarrow A = 5$

Cover up rule using $s = \frac{-1}{0.94} \rightarrow B = \frac{5}{\frac{-1}{0.94}} = -4.7$

Inverse Laplace on $V_c(s) = \frac{5}{s} + \frac{-4.7}{1 + 0.94s}$

$$\frac{-4.7}{0.94(\frac{1}{0.94} + s)} = \frac{-5}{\frac{1}{0.94} + s}$$ $V_C(t) = 5u(t) - 5e^{-1.0638t}$ u(t)

From our analysis we must find the t that makes $V_c(t) = \frac{2}{3} * V_{CC} = \frac{10}{3}$

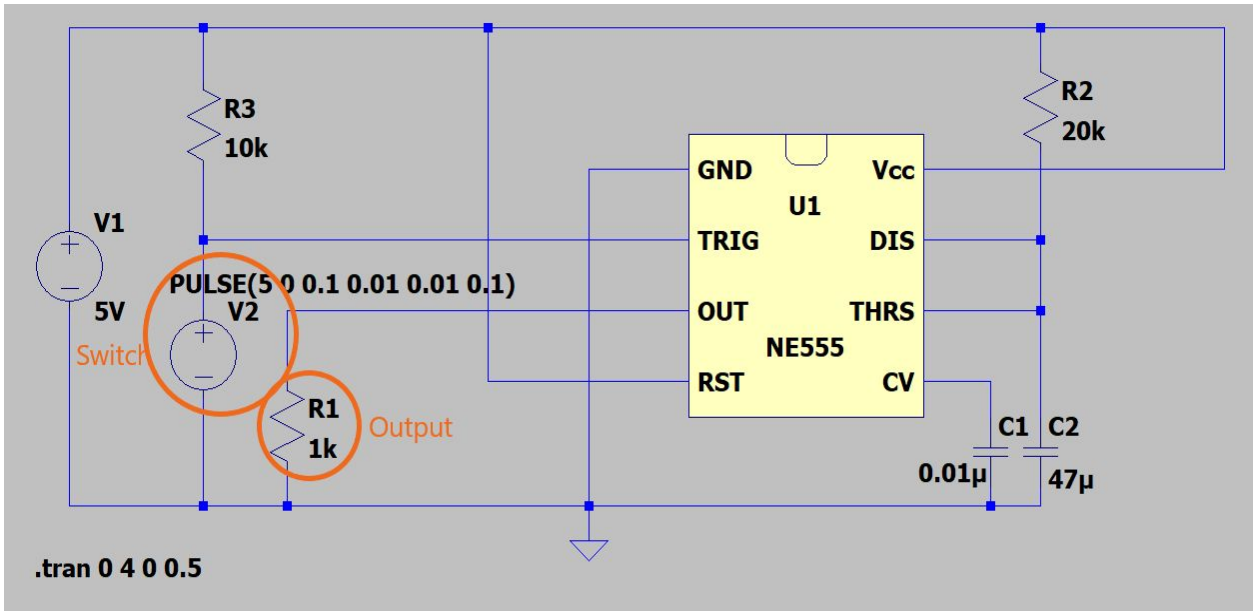
$$V_c(t) = -5e^{-1.0638t} + 5 = \frac{10}{3}$$

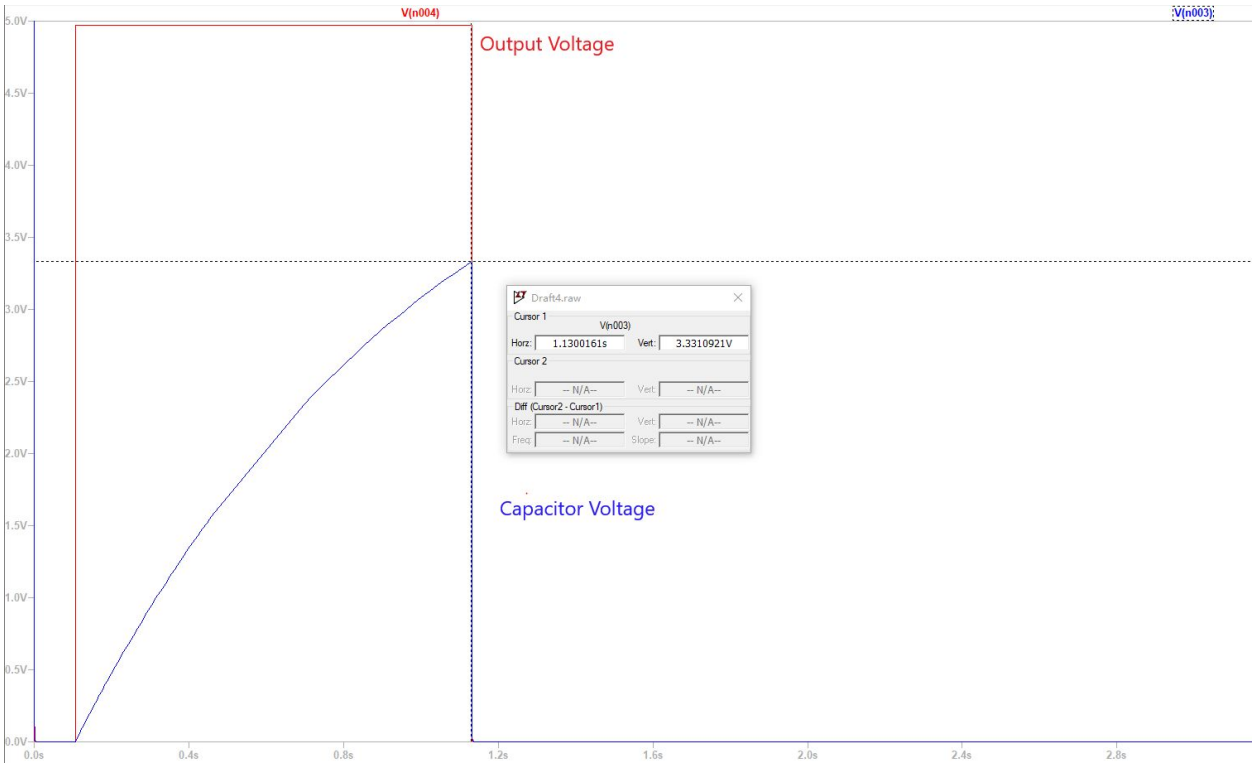
$$t = -.94(\ln(\frac{-2}{3} + 1))$$

$$t = 1.03$$

Thus our analysis predicts our output should hold for roughly 1 second.

Simulation:





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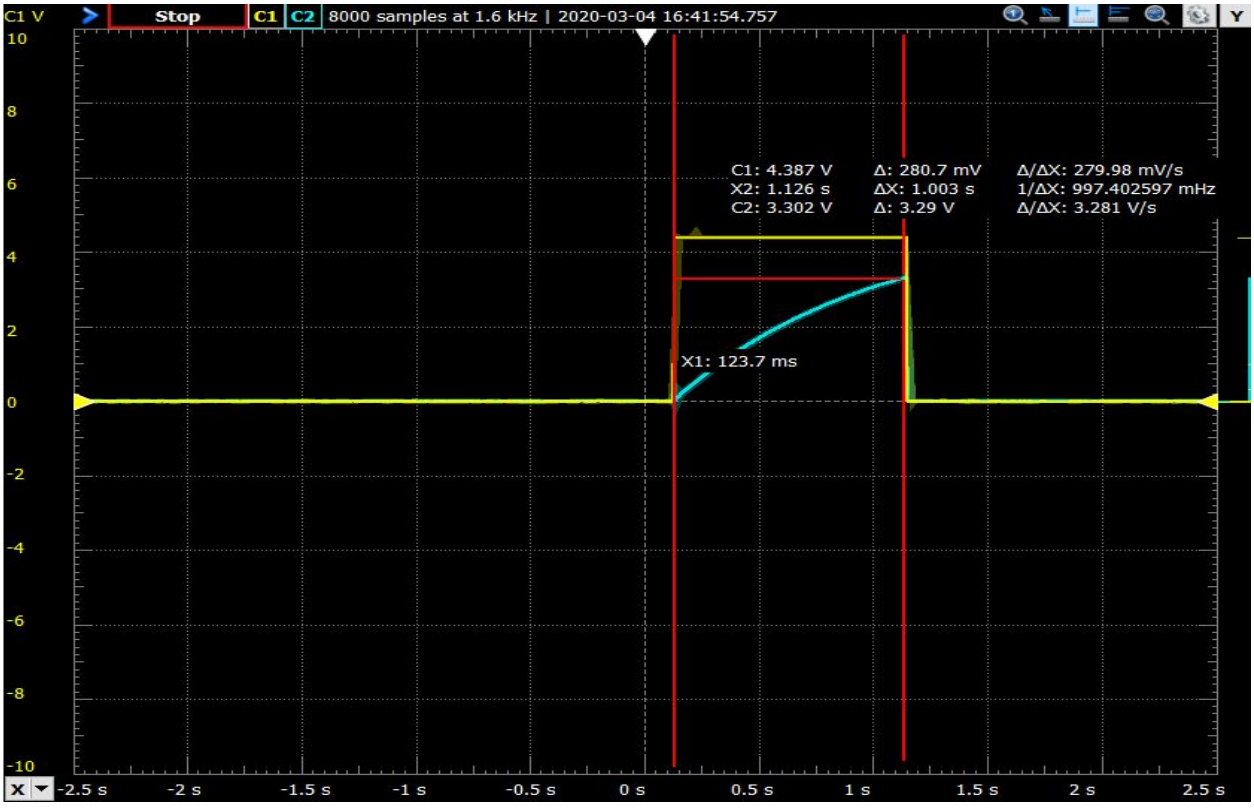

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