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10/21/14
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Cole HW #7

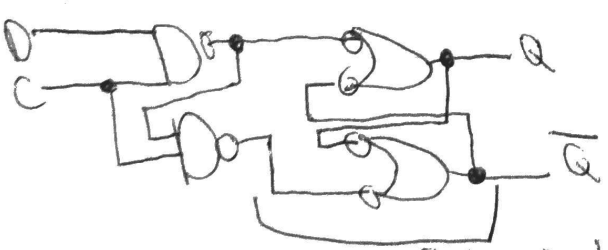
7.4: Intervals are 10ns

Interval	Q	$\overline{Q}$
1:	0	0
2:	1	0
3:	1	0
4:	1	0
5:	1	0
6:	1	0
7:	1	0
8:	1	0
9:	0	1
10:	0	1
11:	0	0
12:	0	0
13:	0	1
14:	0	1
15:	0	1

7.5: Intervals are 10ns

Interval	Q	$\overline{Q}$
1:	0	0
2:	1	0
3:	1	0
4:	0	0
5:	0	1
6:	0	1
7:	0	1
8:	0	1
9:	0	0
10:	0	0
11:	0	0
12:	0	0
13:	0	0
14:	0	0
15:	0	0

7.41:



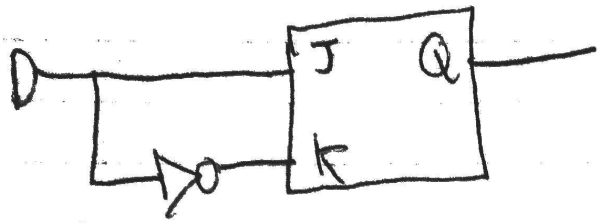
This section is the same.

NAND Truth Table

D	C	Z
0	0	1
0	1	1
1	0	1
1	1	0

D is mostly inverted by the NAND gate and the scenario if it is not is irrelevant overall. This design is better because it save a NOT gate which saves on large scale manufacturing on wires and space.

4.



D Latch Truth Table

C	D	Q	$\overline{Q}$
1	0	0	1
1	1	1	0
0	X	last Q	last $\overline{Q}$

Truth Table for Above

D	J	K	Q
0	0	1	0
1	1	0	1

→ This matches the D latch truth table.

5.

A	B	C	D	Q
0	0	0	X	0
0	1	1	0	0
1	0	1	1	0
1	1	1	0	0

I believe it is an ~~SR latch where~~ JK latch where the output is Q as the output Q matches $\overline{B}$. A seems to be an enable input.

HW #7 Re-sub

2: S

R

Q

$\bar{Q}$

2 gate delay

Q ignores set because R = 1

1 gate delay

$\bar{Q}$ reacts but transitions back because R = 1

* I didn't realize what the original question was asking so I drew a truth table. I realize now how signals actually affect the circuit with delay and labeled how some elements interact.

2. S.

R

q

$\bar{Q}$

q acts the resets because R=1

* Same reason as before, I think the outputs oscillate because both the set and reset fall at the same time and there is equal delay on the chips.