Saaif Ahmed
661925946

9/23/19
ahmeds7

CoCo HW #3

1) A: $\Sigma_{xyz}(1,3,5,6,7)$

z \ xy	00	01	11	10
0	0	1	1	0
1	1	0	1	1

$= \boxed{\bar{Y}Z + XY + \bar{Z}Y}$

B: $\Sigma_{wxyz}(0,1,6,7,8,9,14,15)$

yz \ wx	00	01	11	10
00	1	0	0	1
01	1	0	0	1
11	0	1	1	0
10	0	1	1	0

$= \boxed{XY + \bar{W}\bar{Y}}$

C: $\Sigma_{xyz}(0,1,2,4)$

z \ xy	00	01	11	10
0	1	1	0	1
1	1	0	0	0

$= \boxed{\bar{X}\bar{Y} + \bar{X}\bar{Z} + \bar{Y}\bar{Z}}$

D: $\Pi_{xyz}(1,4,5,6,7)$

z \ xy	00	01	11	10
0	1	1	0	0
1	0	1	0	0

$= \bar{x}\bar{z} + \bar{x}y$

E: $\Pi_{w,x,y,z}(1,3,4,5,6,7,9,12,13,14)$

yz \ wx	00	01	11	10
00	1	0	0	1
01	0	0	0	0
11	0	0	1	1
10	1	0	0	1

$= wyz + \bar{z}w\bar{x} + \bar{w}\bar{x}\bar{z}$

F: $\Pi_{xyz}(1,2,6,7)$

z \ xy	00	01	11	10
0	1	0	0	1
1	0	1	0	1

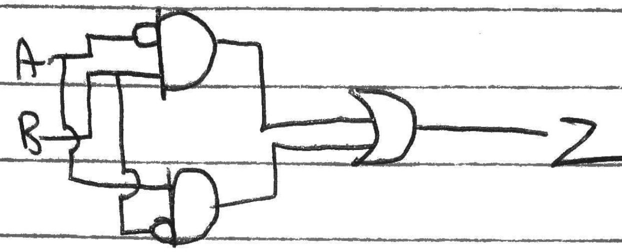
$= \bar{y}\bar{z} + x\bar{y} + \bar{x}yz$

(2) 4.35:

XOR Gate

A	B	Z
0	0	0
0	1	1
1	0	1
1	1	0

$= \boxed{\bar{A}B + A\bar{B}}$



(3) 4.39:

2 input NAND's alone do not make a complete set. This is because NAND filter out only 1. NAND cannot filter out 0. You have to at least have inverters to filter the 0. Though when you add an inverter you essentially have a NAND and NOR

(4) 4.41:

2 input XNOR does not make a complete set of logic gates. XNOR is incapable of filtering 1 or 0. Also XNOR is derived from a combination of AND, OR, and inverters. These are the complete set used to make XNOR. XNOR is not a complete set however.

HW #3 Re-Submission

1 A:

z \ xy	00	01	11	10
0	0	0	1	0
1	1	1	1	1

$\rightarrow \cancel{X}\cancel{Y}Z$

$XY\cancel{Z}$

$= \boxed{Z + XY}$

B:

yz \ wx	00	01	11	10
00	1	0	0	1
01	1	0	0	1
11	0	1	1	0
10	0	1	1	0

$\rightarrow \cancel{W}X'Y'\cancel{Z}$

$\cancel{W}XY\cancel{Z}$

$= X'Y' + XY$

$= \bar{X}\bar{Y} + XY$

E:

yz \ wx	00	01	11	10
00	1	0	0	1
01	0	0	0	0
11	0	0	1	1
10	1	0	0	1

$\rightarrow \cancel{W}X'\cancel{Y}Z'$

$\rightarrow W\cancel{X}YZ$

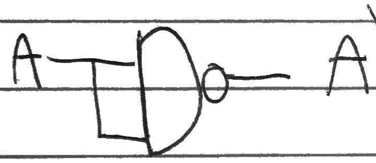
$= \boxed{\bar{X}\bar{Z} + WYZ}$

*prev. submission I forgot about the 4 corners 2x2 grouping.

③ 4.39:

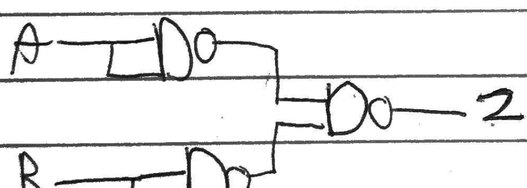
AND, OR, and NOT make a complete set because they have filtering of 1, 0, and the inversion ability. A NAND must be able to do all of these in at least 1 configuration for each.

Inversion



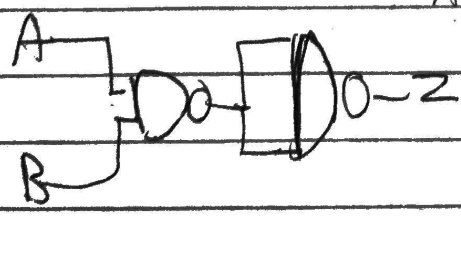
A	Z
0	1
1	0

OR



A	B	Z
0	0	0
0	1	1
1	0	1
1	1	1

AND



~~A B Z~~

A	B	Z
0	0	0
0	1	0
1	0	0
1	1	1