

Introduction to Electronics

ECSE 2050

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Summer 2020

ECSE-2050 Quiz 2

- 1) For all BJT problems, you may assume $V_{\text{thermal}} \sim 0.026V$, $V_{\text{BE}} \sim 0.7V$ when forward biased and $V_{\text{CE}} \sim 0.2V$ when in saturation.
- 2) Unless otherwise indicated, assume $r_o \rightarrow \infty$.
- 3) If you are stuck on part of a problem, use **a reasonable** value to continue to the following parts. Partial credit will depend on your choice of a reasonable value.
- 4) **For most problems, answers must have supporting work. Numbers that are provided with no supporting work will receive no credit.**

1) Short Answers (28 points)

Question 1 (7 points)

- T F An FET can act as a variable resistor.
- T F An FET can act as a voltage controlled current source (VCCS).
- T F A BJT can act as a current controlled current source (CCCS).
- T F We can approximate the base-emitter junction of a BJT as a diode.
- T F When forward biased, a Zener diode behaves like a standard diode.
- T F Transistors have internal capacitance.
- T F When in saturation, drain current can increase as VDS increases.

Question 2 (3 points)

To build an amplifier circuit that amplifies DC input signals (when v_{in} is DC), what must be true about the circuit?

there must be a large input R_{in} and small R_{out}

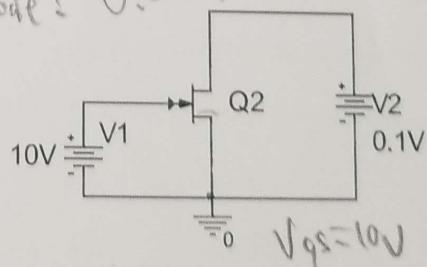
It must be in the saturation region,

small variations have to be linear

Question 3 (4 points)

$I_{DSS} = 0.01A$

The FET has characteristics, $V_{TN} = 2V$ and $K_n = 0.0125 \text{ A/V}^2$.

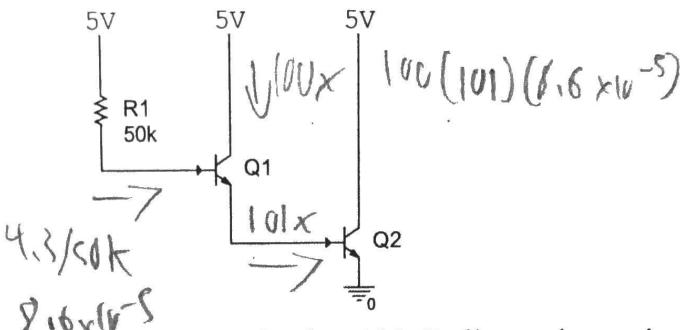


$$V_{DS} = 0.1V$$

Approximately determine the drain current, I_D .

$$I_D = k_n(V_{GS} - V_{TN})(V_D)$$

$$I_D = 0.01 A$$

Question 4 (6 points)

The above BJTs have a forward active current gain, $\beta = 100$. Indicate the region of operation for each transistor,

Q1: off saturation forward active (circle one)

Q2: off saturation forward active (circle one)

Based on your above answers, approximately determine the collector current of Q2.

$$I_C = \underline{.8686}$$

Question 5 (2 points)

When considering variations in the gate source voltage, v_{gs} , about the DC bias value, V_{GS} , which of the following conditions is necessary for a linear approximation? (Circle one)

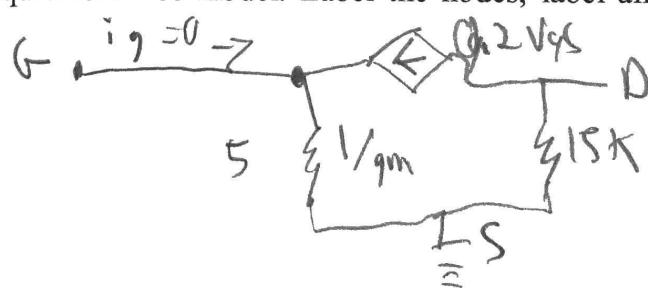
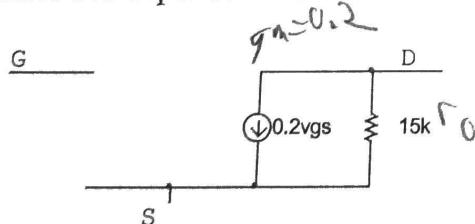
$$v_{gs} \ll V_{TN}$$

$$\underline{v_{gs} \ll V_{DS}}$$

$$v_{gs} \ll (V_{GS} - V_{TN})$$

Question 6 (4 points)

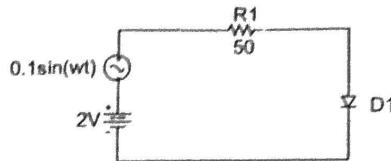
For the following Hybrid- π model, draw the equivalent Tee model. Label the nodes, label all components and dependencies.

Question 7 (2 points)

For given semiconductor materials, explain how can the FET transconductance parameter, K_n , be adjusted during fabrication.

How large the channels are depends on how much semiconductor is placed. Requiring more voltage to turn on changes conductance (K_n).

2) Diodes (18 points)



The above diode is 'real' with a reverse saturation current, $I_S = 10^{-10} \text{ A}$. The voltage across the diode in the above circuit is $V_D = 0.6 + 0.005 \sin(1000t)$

- a) Determine the equivalent circuit model for the diode. Redraw the circuit, using the equivalent circuit. (6 pts)

$$\text{Ansatz } V_D = 0.6$$

$$\frac{2 - 0.6}{50} = 0.018 = 20$$

$$V_D = 0.565$$

$$\frac{2 - 0.565}{50} = 0.018 = 20$$

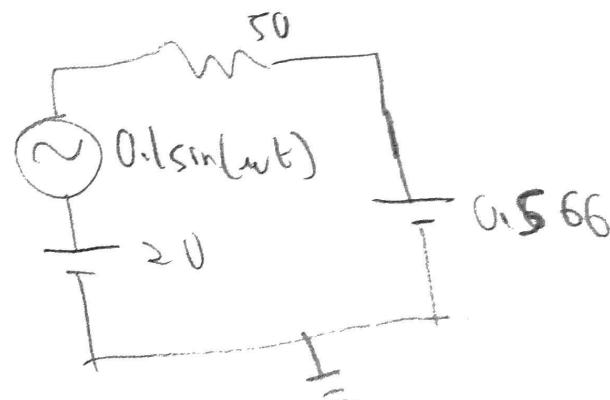
$$V_D = 0.567$$

$$\downarrow \\ V_D = 0.566$$

$$0.6 > 0.566$$

$$0.6 - 0.005 > 0.566$$

Diode always $s > 0$



- b) Using the 'real' diode model, if the DC source is decreased to 1.5V, will the AC voltage across the diode increase, decrease, or stay the same? Justify your answer. (3 pts)

The diode will be off as we calculated before.

With the diode off it is open circuit.

So there is no AC voltage drop across

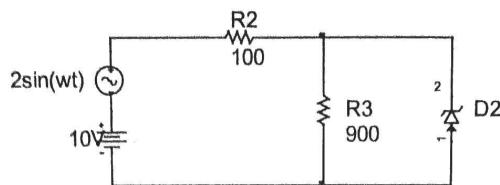
the resistor. So the AC voltage increases.

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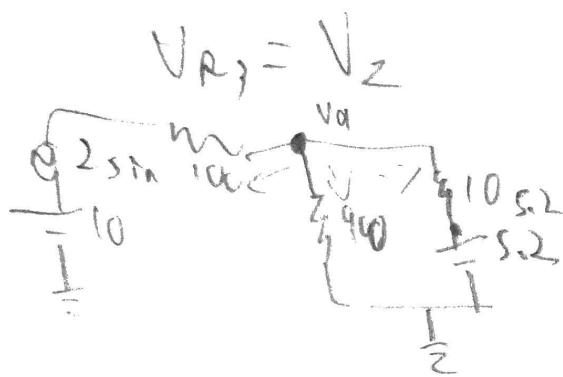
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The above Zener diode has a knee at $I_z = 0$, $V_z = 5.2V$, which is in the breakdown region for the diode. It also has a Zener resistance $r_z = 10\Omega$.

- c) Determine the voltage across R_3 . (6 pts)



$$\frac{V_{R3}}{9} = .62 + 0.02$$

$$V_{R3} = 5.58 + .18 \sin(\omega t)$$

$$5.2 + \frac{10 \cdot I_z}{10} = 5.2 + 10I_z$$

$$\frac{V_{R3} - I_z}{10} + \frac{V_{R3}}{900} + V_{R3} = 10 + 25 \sin(\omega t) = 0$$

$$\frac{V_{R3}}{10} - \frac{5.2}{10} + \frac{V_{R3}}{900} + \frac{V_{R3}}{10} - \frac{10 \cdot I_z}{10} = 0$$

$$-.52 + \frac{100}{900} V_{R3} - I_z = 0$$

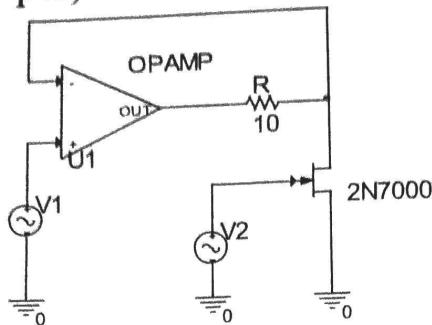
$$-.52 + .111 V_{R3} - I_z = 0$$

- d) Using the ideal breakdown model, if the DC source is decreased to 9V, will the AC voltage across the diode increase, decrease, or stay the same? Justify your answer. (3 pts)

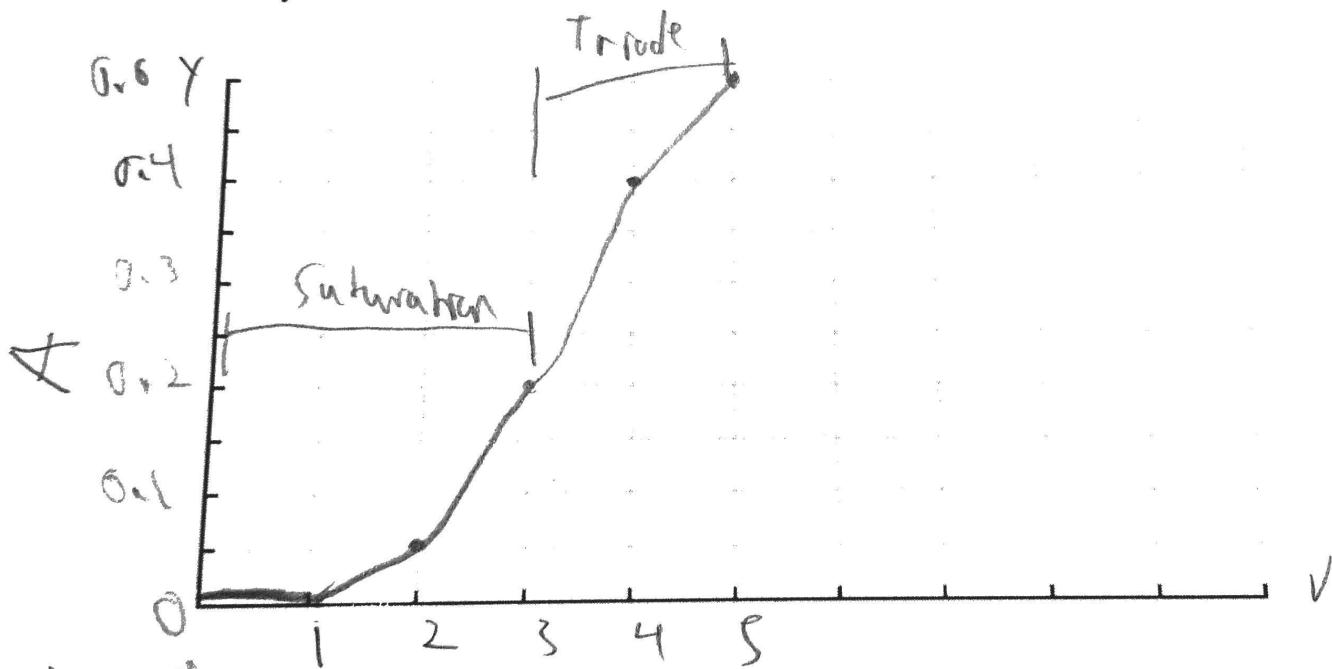
the zener diode is still in breakdown.

So the Voltage is still regulated. meaning the AC component doesn't change.

3) Curve Tracing (16 pts)



- a) In the above circuit, $V_1 = 2V$ and V_2 is a triangle wave varying from 0V to 5V. The FET has characteristics, $V_{TN} = 1V$ and $K_N = 0.1V$. Plot the drain current, ID (y-axis), against the gate source voltage, V_{GS} . On your plot, indicate the regions of operation for the FET. Label your axis such that the tick marks are consistent with the plot. (8 pts)



$$V_{GS} = V_2$$

$$V_{DS} = 2V$$

$$V_{DS} = 2$$

$$\text{triode } 3 \rightarrow 5V \Rightarrow I_D = .4$$

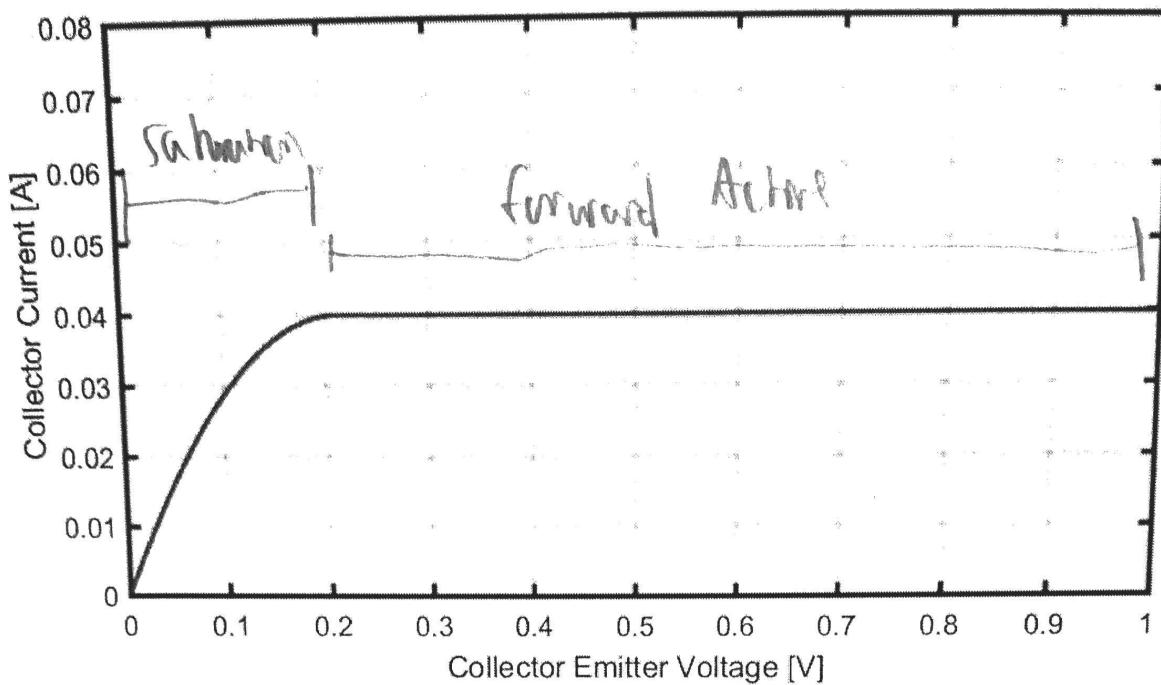
~~$$V_{GS} > V_{DS} - 1$$~~

$$3 < V_{GS} \\ \text{saturation} \Rightarrow \frac{1}{2} k(V_{GS} - V_{TN})^2 = .2 \text{ A/m}$$

$$2 < V_{GS} - 1$$

$$3 < V_{GS}$$

6



The above plot was obtained for a BJT transistor when the base current was $I_B = 0.2\text{mA}$. On the plot, identify the regions of operation. Determine the forward active current gain, β , of the transistor. Based on the curve, what approximation is being used for the output channel resistance, r_o ? (8 pts)

$$I_B \cdot \beta = I_C$$

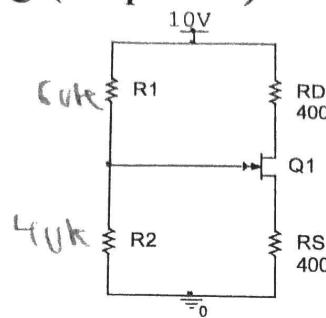
$$0.2 \times 10^{-3} \cdot \beta = 0.04$$

$$\beta = 200$$

$$r_o \rightarrow \infty$$

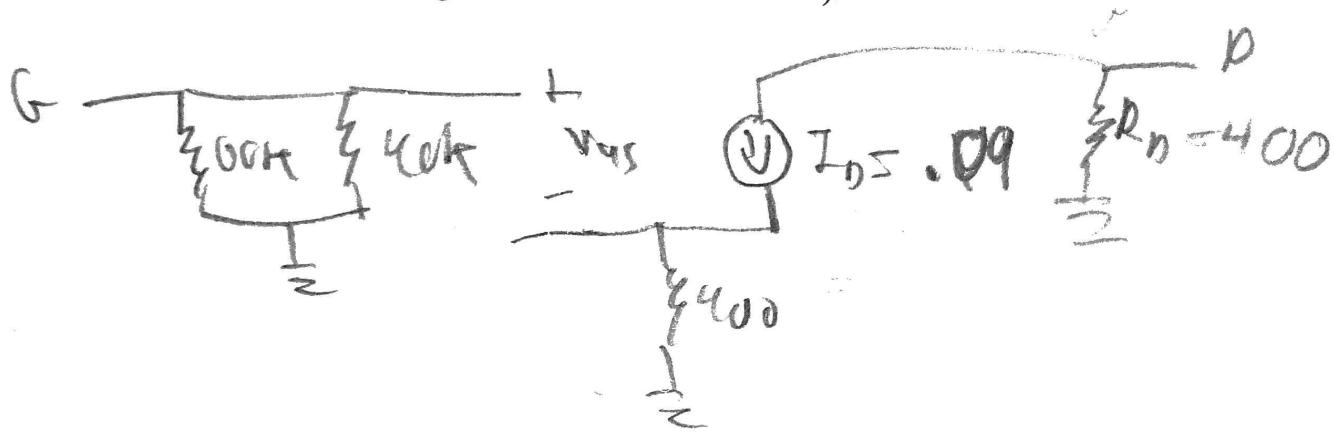
β	200
r_o	∞ [Ω]

4) Four resistor biasing (16 points)



The transistor in the above circuit has characteristics, $V_{TN} = 2V$ and $K_n = 0.05 \text{ A/V}^2$.

- a) For $R_1 = 60\text{k}$ and $R_2 = 40\text{k}$, replacing the FET with the DC equivalent circuit and sketch the full circuit (including all resistors and the source).



$$q_m = K_n(V_{GS} - V_{TN}) = 0$$

$$V_{GS} = 4$$

$$10V = I_D(400) + V_{DS}$$

guess sat

$$10 = 0.09 \cdot 400 + V_{DS}$$

$$V_{DS} = 3.9V$$

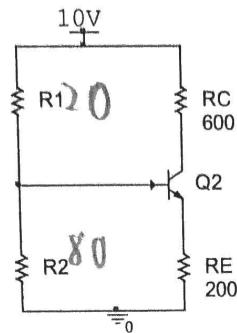
$$I_D = 0.09$$

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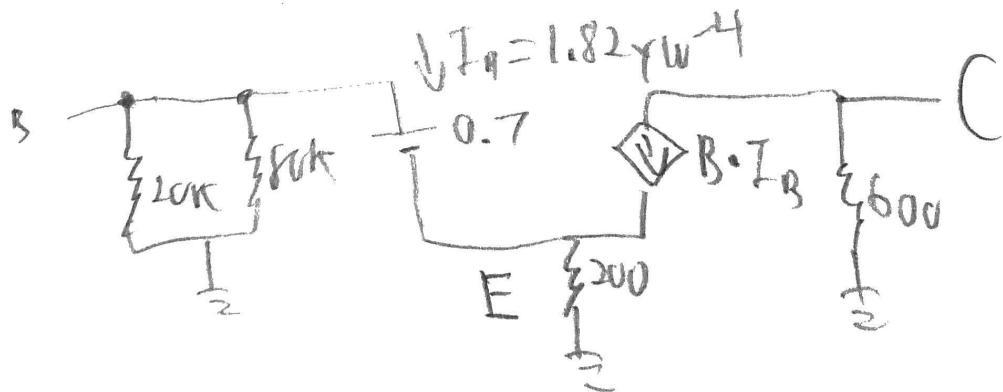
The transistor in the above circuit has a forward active current gain, $\beta = 200$;

- b) For $R_1 = 20k$ and $R_2 = 80k$, replacing the BJT with the DC equivalent circuit and sketch the full circuit (including all resistors and the source). (8 pts)

$$8 = 0.7 + (\beta + 1) I_B (R_E)$$

$$7.3 = 201 I_B (200)$$

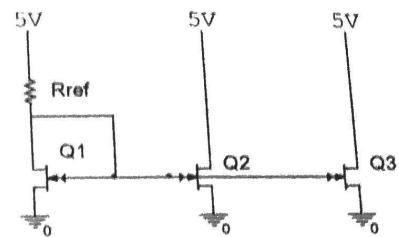
$$I_B = 1.82 \mu A$$



5) Current Mirrors (10 points)

All the transistors in the FET current mirror have characteristics, $V_{TN} = 2V$ and $K_n = 0.1 \text{ A/V}^2$.

- a) Determine the value of the reference resistor such that the drain current of Q3, I_{D3} , is 4mA. Your answer should be accurate to three significant digits. (5 pts)



same current draw
for all,

$$S_V = \frac{1}{2} k_n (V_{GS} - V_{TN})^2 \cdot R_F + V_D$$

$$\frac{1}{2} k_n (V_{GS} - V_{TN})^2 < 4 \text{ mA}$$

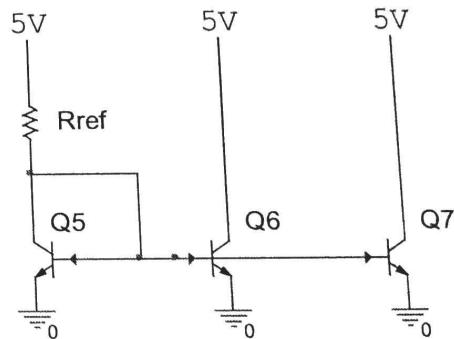
$$V_{GS} = 2.283 \rightarrow \text{verified}$$

$$R_F = 679.29$$

Rref	679.29	[Ω]
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All the transistors in the BJT current mirror have characteristics, $\beta = 100$.

- a) Determine the value of the reference resistor such that the collector current of Q7, I_{C7} , is 4mA. Your answer should be accurate to three significant digits. (5 pts)



$$I_Q = 4 \text{ mA} / 100 \\ = 4 \times 10^{-5} \text{ A}$$

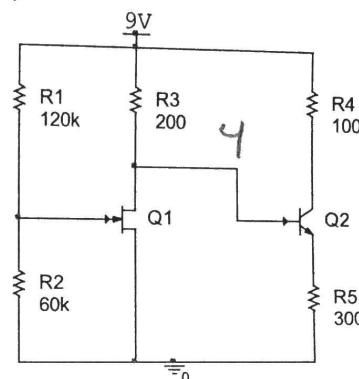
Rref		[Ω]
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6) Biasing and small signal models (16 points)

The FET transistor in the circuit has characteristics, $V_{TN} = 2.5V$ and $K_n = 0.2 \text{ A/V}^2$.

The BJT transistor in the circuit has a forward active current gain, $\beta = 200$

- a) Determine the drain current of the FET and the collector current of the BJT. (8 pts)



$$V_{DS} = 3V$$

$$qV = V_{R3} + V_{DS}$$

$$qV = \frac{1}{2} k_n (V_D - V_{TN})^2 \cdot 200 + V_{DS}$$

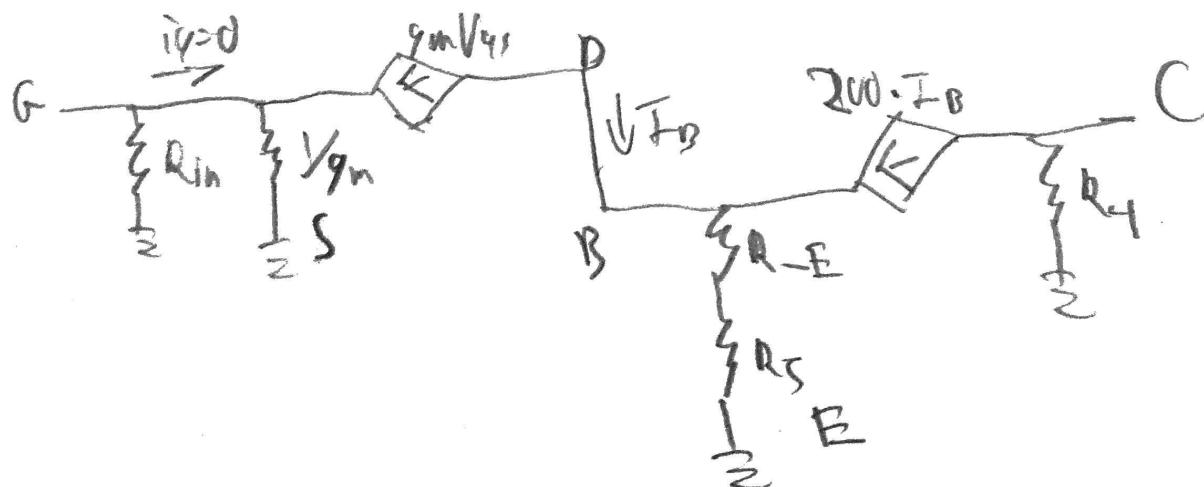
Saturation verified

$$V_{DS} = 4$$

$$\begin{aligned} I_{D1} + I_{B1} &= I_{R3} \\ &= \frac{9V - 4}{200} \end{aligned}$$

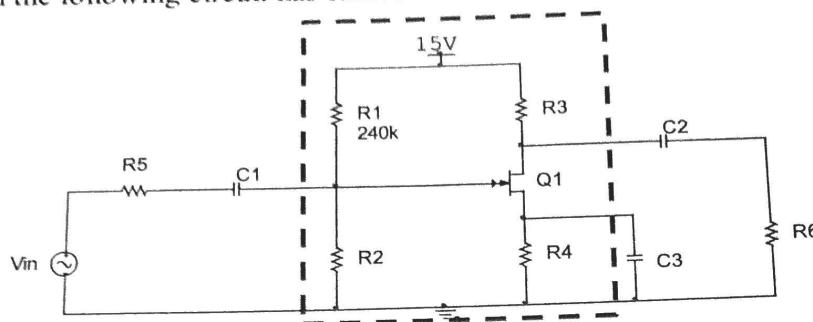
I_D	0.025	[mA]
I_C		[mA]

- b) Using the Tee model for each transistor, sketch the small signal model, labelling all component values symbolically. (8 pts)

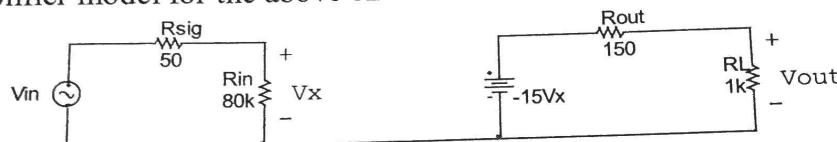


7) Common Source (15 points)

The transistor in the following circuit has characteristics, $V_{TN} = 2V$ and $K_n = 0.1 \text{ A/V}^2$.



The general amplifier model for the above circuit is shown below.



Determine the values of the unknown resistors in the circuit.

$$R_m = \left(\frac{1}{240} + \frac{1}{R_4} \right)^{-1}$$

$$R_o = R_L$$

$$R_S = R_{in}$$

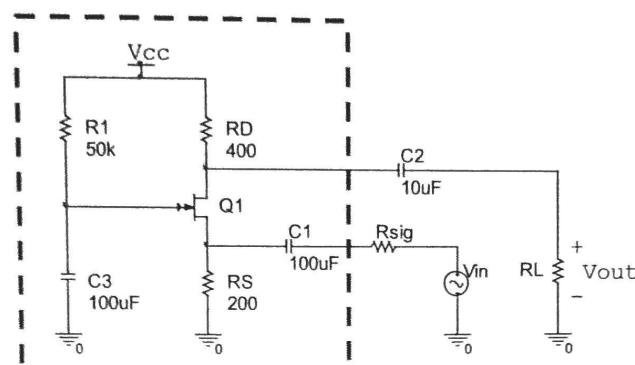
$$R_L = 120000$$

$$R_g = R_o$$

$$R_g$$

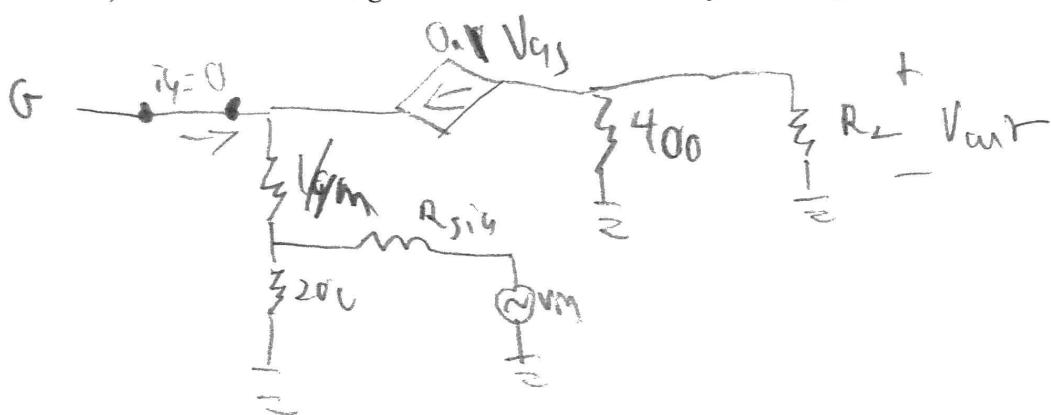
R2	120000	[Ω]
R3	150	[Ω]
R4		[Ω]
R5	50	[Ω]
R6	1K	[Ω]

8) Amplifier Circuits I (26 points)



The small signal transconductance for the above FET is $g_m = 0.1 \text{ A/V}$.

- a) Sketch the small signal model for the circuit. Symbolically label all components. (4 pts)



- b) For the indicated 'dashed box', determine the input resistance of the circuit, R_{in} . (3 pts)

$$R_s \parallel \frac{1}{g_m} = 9.52$$

- c) For the indicated 'dashed box', determine the output resistance of the circuit, R_{out} . (3 pts)

$$R_{out} = R_D = 400$$

- d) For the indicated 'dashed box', open circuit gain, A_{vo} ($R_{sig} \rightarrow 0$, $R_L \rightarrow \infty$). (3 pts)

- e) If $R_{sig} = 25\Omega$ and $R_L = 800\Omega$, determine the overall gain, $A_v = V_{out}/V_{in}$. (3 pts)

- f) Approximately, determine the low frequency 3dB cutoff. For each capacitor, indicate the associated equivalent resistance. (10 pts)

C1: $R_s \parallel V_{gm} = 9.52 \rightarrow 1050 \text{ pot}$

C2: $R_o = 400 \rightarrow 256 \text{ pot}$

C3: $R_1 = 50K \rightarrow \frac{1}{5} \text{ me}$

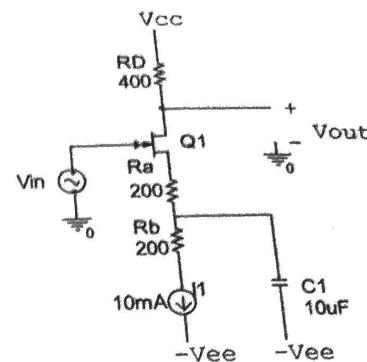
3dB low frequency cutoff:

1050 is 3dB cutoff

9) Amplifier Circuits II (27 points)

The FET has a transconductance of $K_n = 0.08 \text{ A/V}^2$.

- a) Determine the small signal transconductance. (3 pts)



- b) Sketch the small signal model for the circuit. Label all components symbolically. (4 pts)

- c) Determine the input impedance, R_{in} , 'seen by' v_{in} . (3 pts)

$$R_{in} = 0 \quad R_A = 200$$

- d) Determine the output impedance, R_{out} , 'seen by' v_{out} . (3 pts)

$$R_P = 400$$

e) Determine the gain, $A_v = v_{out}/v_{in}$. (4 pts)

f) Approximately, determine the low frequency 3dB cutoff. (4 pts)

$$\frac{1}{C_1 \cdot A_A} = \underline{500 \text{ rad/s}}$$

g) For $CGD \approx 50\text{pF}$, apply the Miller Theorem to the feedback impedance and redraw the circuit with an input side and output side impedance. (6 pts).