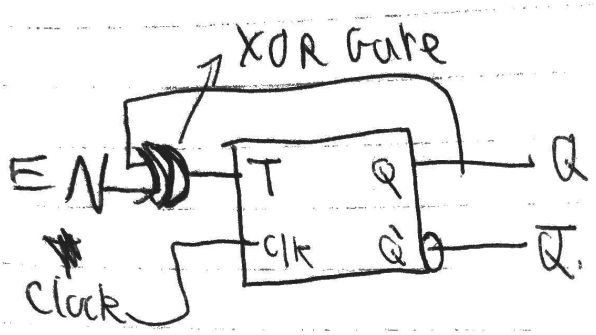
Saait Ahmed
Section 3

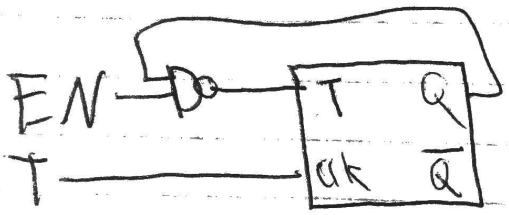
10/28/19
ahmeds7

Cdo HW 8

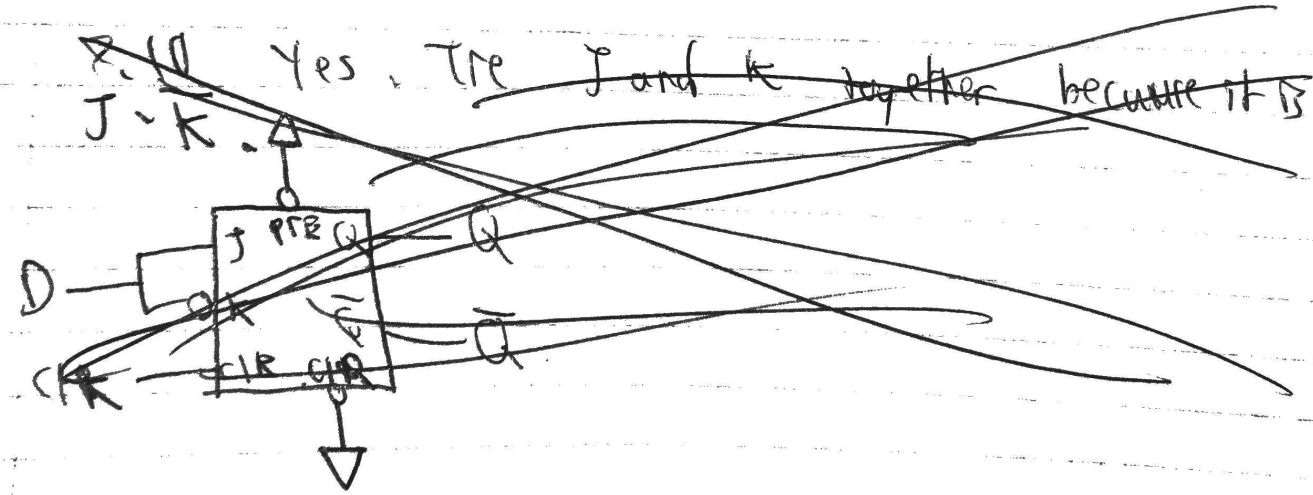
7.6:



7.7.

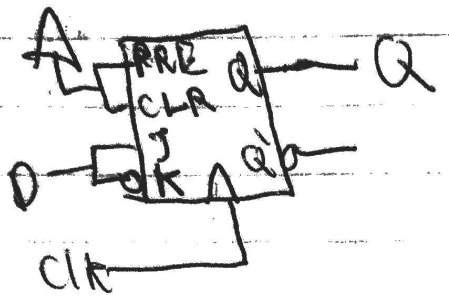


7.11 Yes. The J and K together because it is J-K.



7.10: I don't think it is possible. You'd have to alter the metastability states with logic gates external to the device. Logic gates tend to fail in that regard.

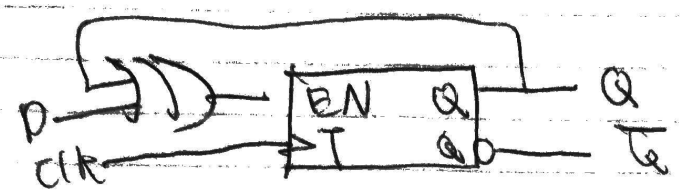
7.11: Tie J and K together



8.13: It counts multiples of 2 up to the given maximum value.

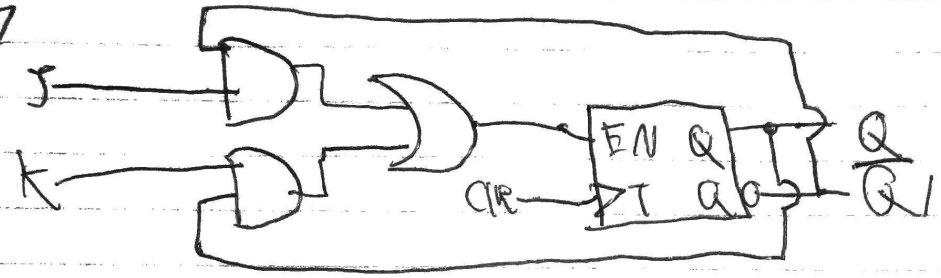
HW #8 resub

7.6.



* I had the correct idea I just messed up the pin labelings.

7.7



* I should have realized that the ~~pins~~ inputs should have matched as J-K flip flop.
I see now that Q relates with J and Q relates to K in order to create the desired flip flop.

7.10: In addition to what I said already I forgot to mention that the flip flop triggers on an edge which a logic gate cannot perform combinationally.

8.13: UP states the up or down counting. Loads occur ~~at~~ at the 0000/1111 case. Analyze from 1000~1111: 8, 9, 10, 11, 12, 13, 14, 15, 7, 6, 5, 4, 3, 2, 1, 0. So it starts from 8 counts up to 1111 then loads in 7 and counts down, then it cycles. Which means if we observe three bits it goes 0, 1, 2, 3, 4, 5, 6, 7, 7, 6, 5, 4, 3, 2, 1, 0.
It counts up to 7 then counts down from 7.