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Laboratory 3: MOSFET characteristics, Current Mirrors, Small Signal Amplifiers

Introduction:

Mosfets and their characteristics are the main topic of this lab. We analyze the DC bias component to these devices and find their use cases. These include current mirrors and amplifiers. We also analyze their real characteristics with small signal models, and find what operating conditions and frequencies they work best in. We perform this analysis with simulation and by building the circuits, with the addition of using Hybrid Pi /T models for fets.

Exercise 3.1 IV Curves

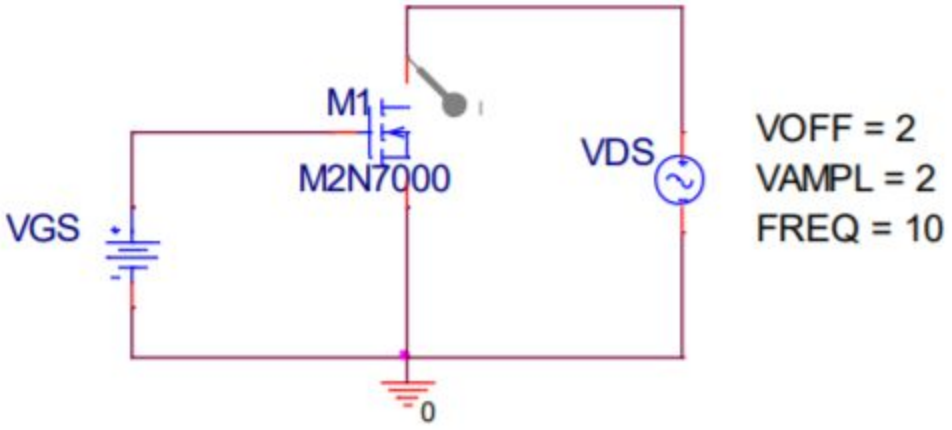


Figure 3.1.1 LTSpice Schematic

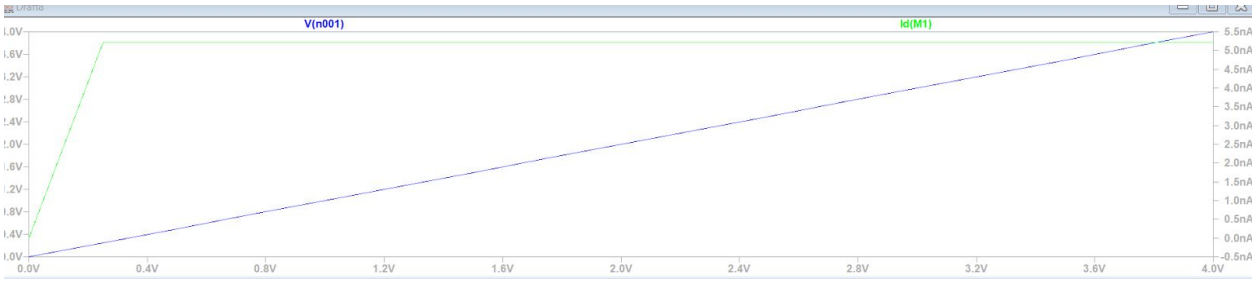


Figure 3.1.2 IV curve from Part 1 VGS = 1V

For VGS = 1V, the fet is off.

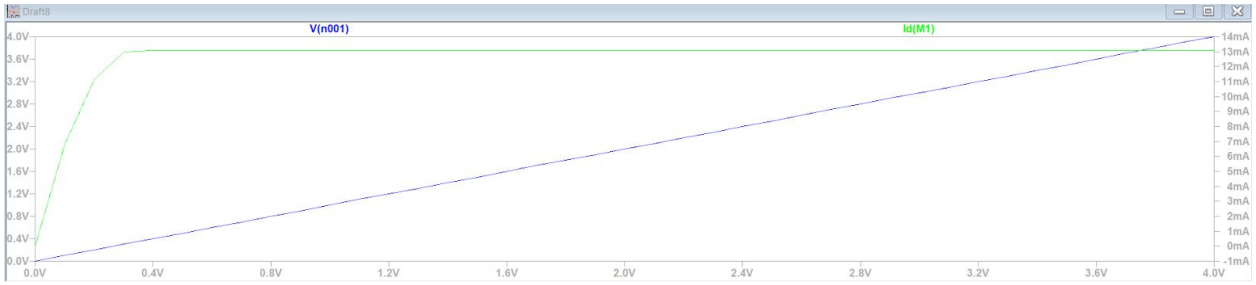


Figure 3.1.3 IV curve VGS = 2V

The saturation current is about 13mA.

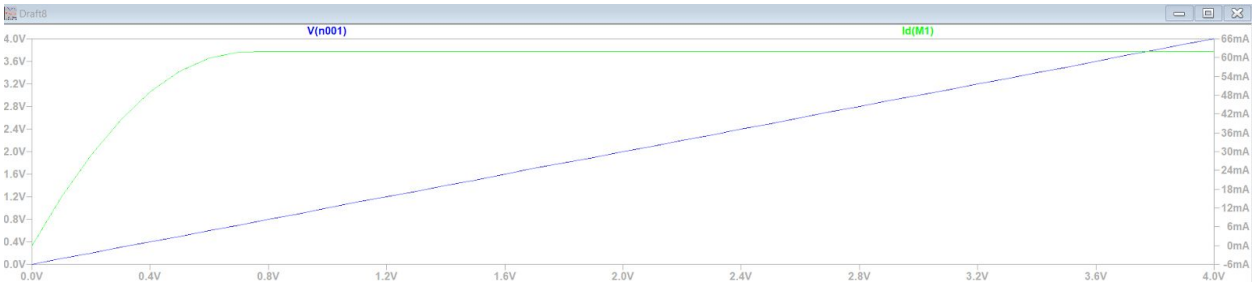


Figure 3.1.4 IV Curve VGS = 2.5V

The saturation current is about 60mA.

Figure 3.1.5 IV Curve VGS = 3V

The saturation current is about 140mA.

As VGS increases, the saturation current also increases.

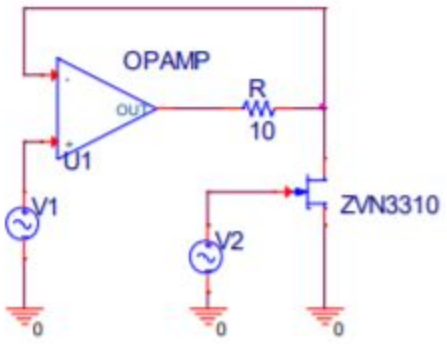


Figure 3.1.6 Circuit Schematic for discovery board

The positive amplifier input, V1 (VDS), was set to a 0.1V DC using one of the Discovery Board channels and the gate input, V2 (VGS), was set to the MOSFET to a 1kHz, 3Vpp triangle wave with a 1.5 V DC offset using the other channel.

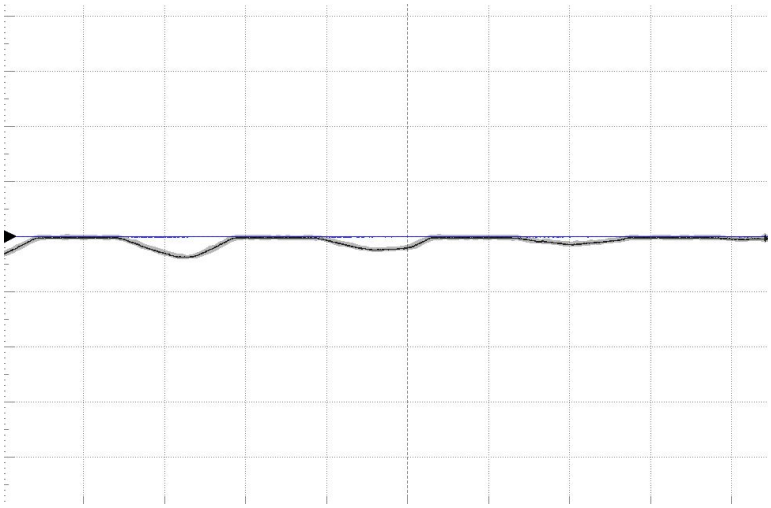


Figure 3.1.7 Current through resistor, IR

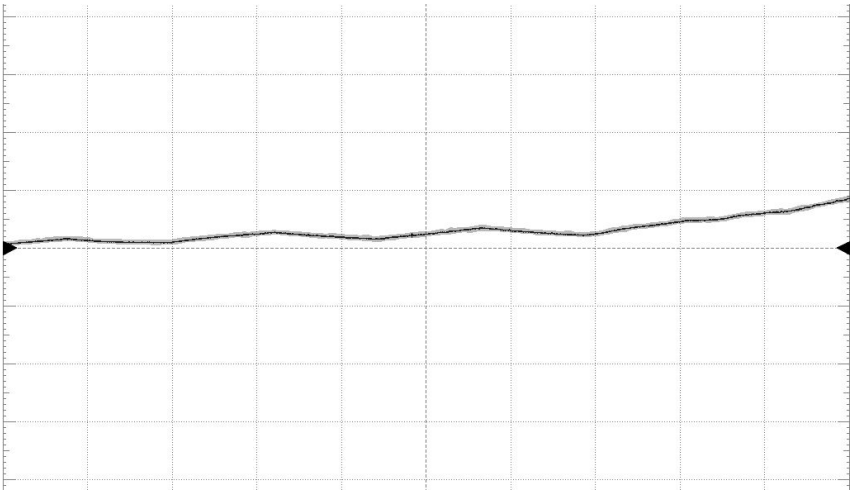


Figure 3.1.8 VGS vs ID triode

VDS,or V1 was set to a 1kHz, 5Vpp triangle wave with a 2.5V DC offset using the other channel. V2 (VGS) was set to DC and the gate input was adjusted such that you could start to see current flowing through the resistor. This threshold was compared to earlier estimations. The gate voltage was increased by 0.04V (DC) such that a larger current through the resistor was visible.

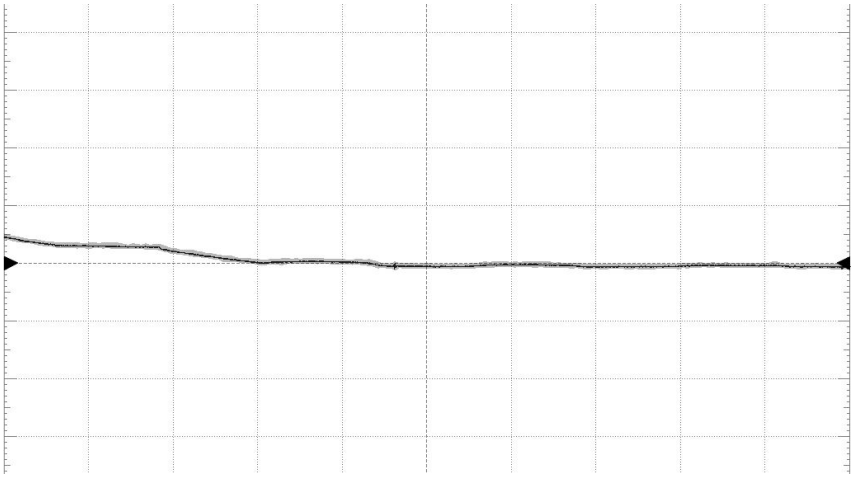


Figure 3.1.9 ID vs VGS with added .04 v

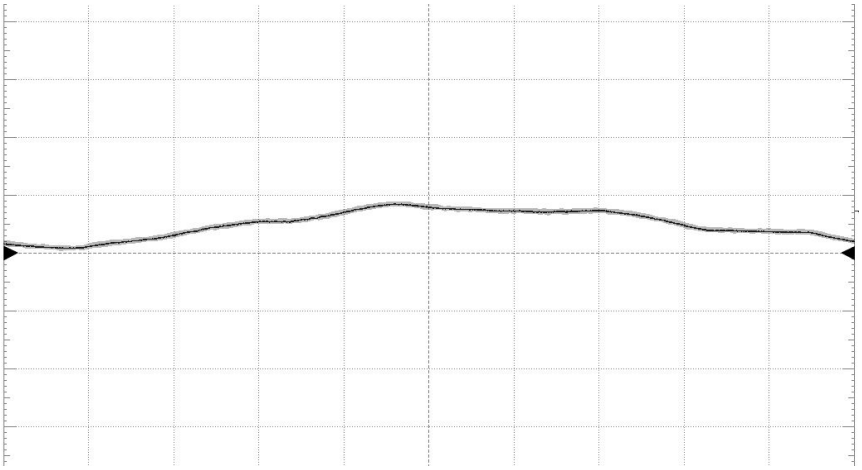


Figure 3.1.10 ID vs VGS with another added .04 v(.08V total added)

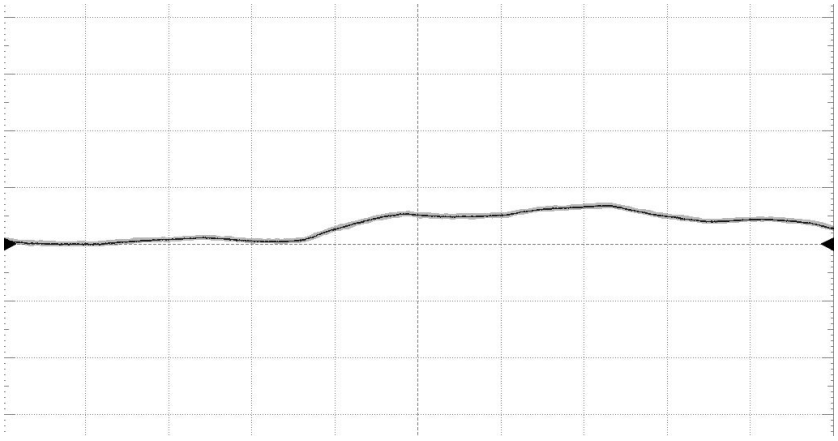


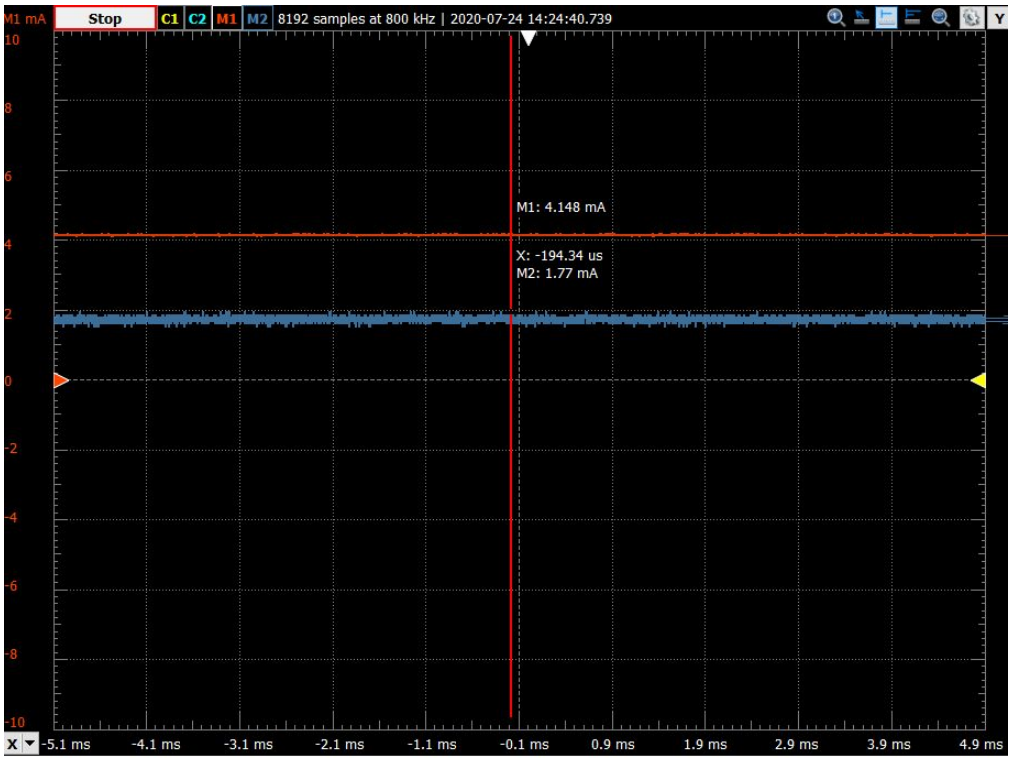
Figure 3.1.10 ID vs VGS with another added .04 v(.12 V total added)

The Kn value was found to be about .035 A/V^2 and the VTN was about ~2.1V.

Exercise 3.2: Current Mirror

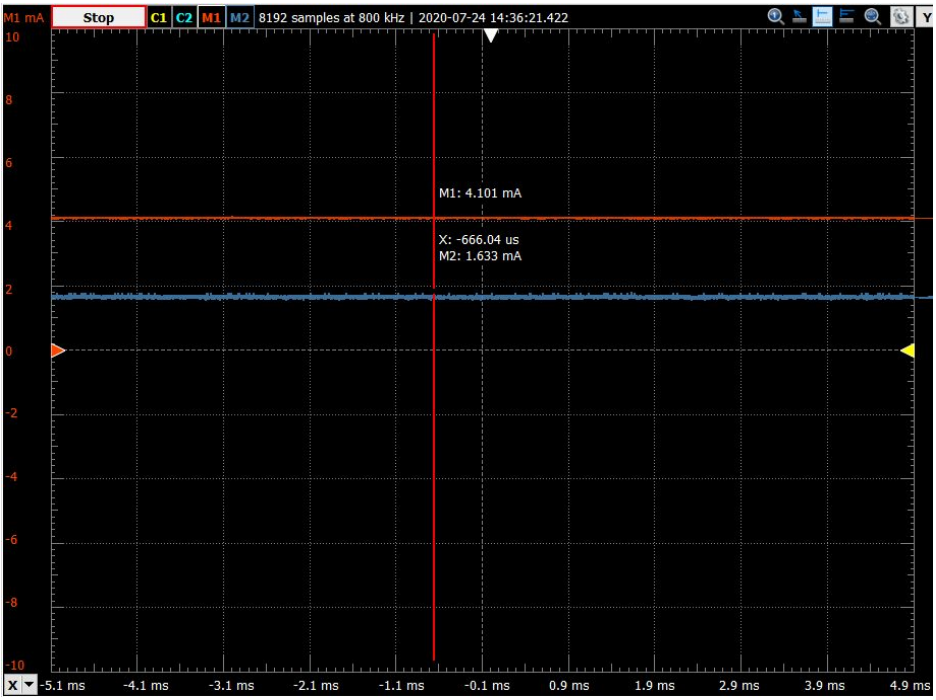
We have a current limitation so we start with 47 ohms.
Red is Fet 1 with a constant 470 resistor and Blue is Fet 2 with variable resistors

Current Mirror with R2 = 47 ohms

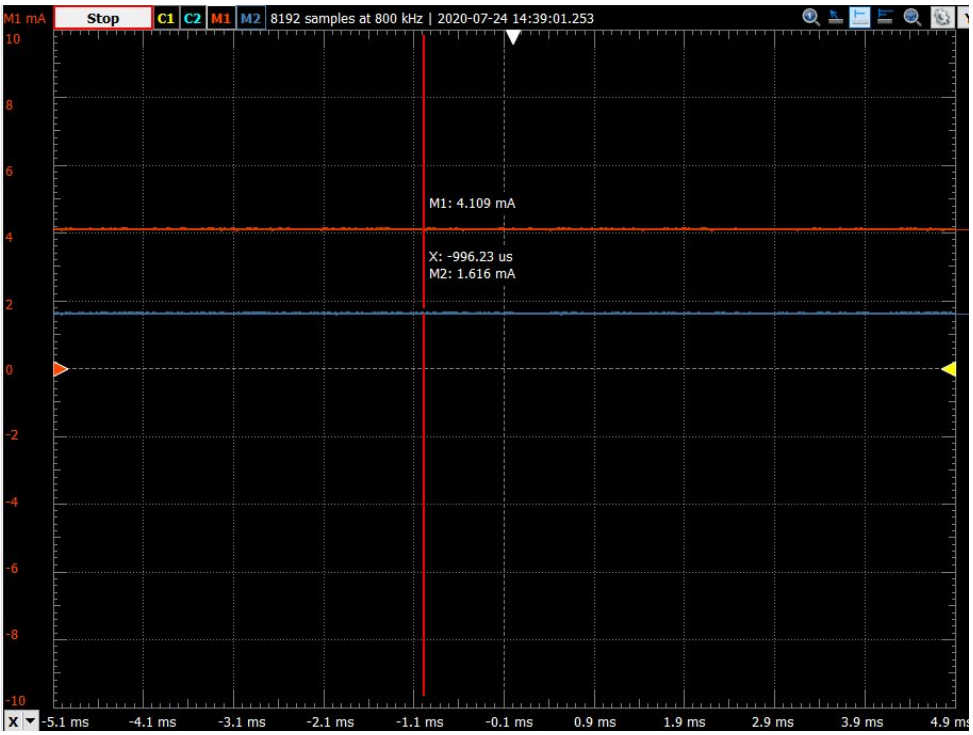


Based on the part 1 results, the current mirror is not exactly working as expected. However there are reasons for this. The math channels that measure the current divide by a constant that may not be the exact value of the resistor. Furthermore the scopes themselves act as some noise for voltage calculation.

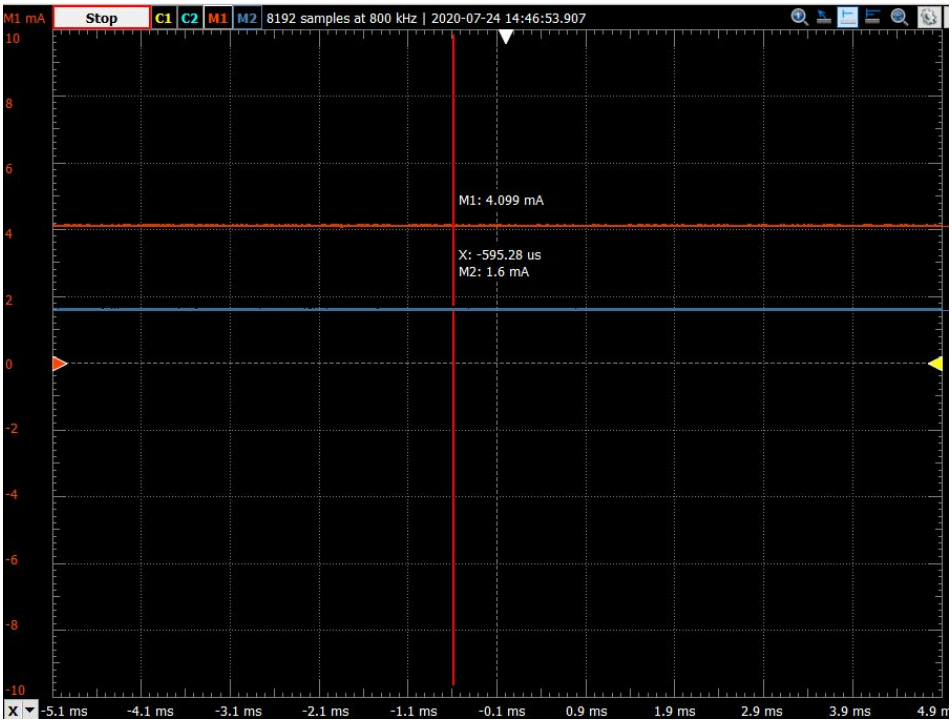
Current Mirror with R2 = 100 ohms



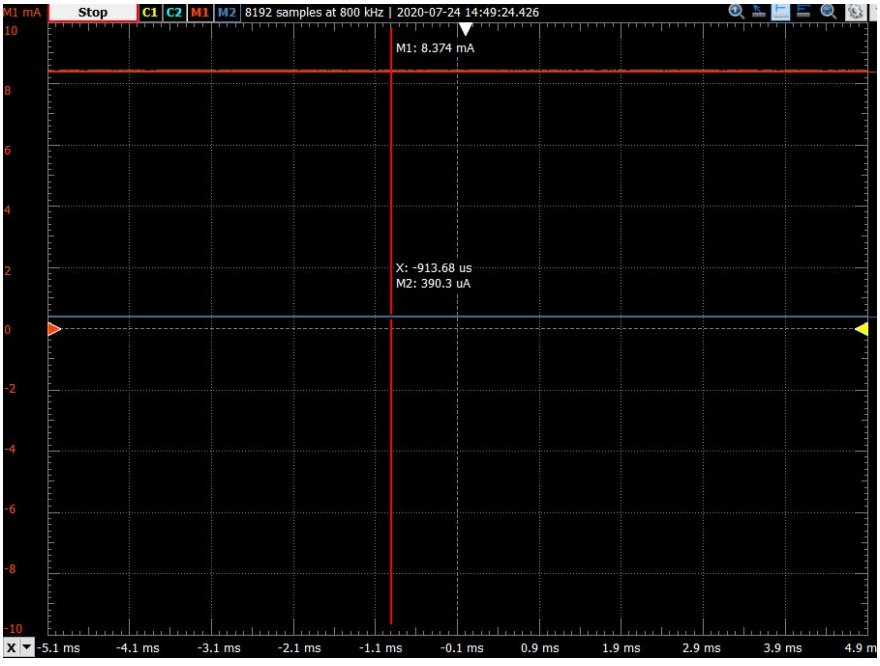
Current Mirror with R2 = 470 ohms



Current Mirror with R2 = 1k ohms



Current Mirror with R2 = 10k ohms

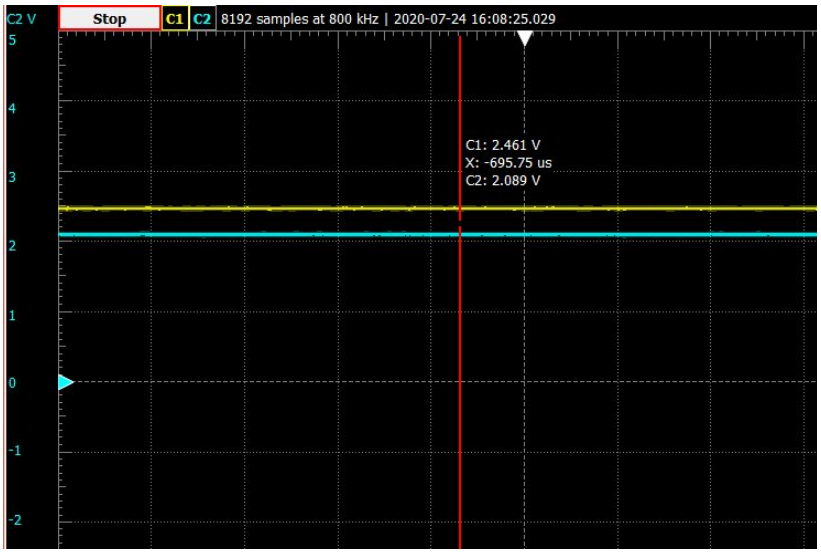


While the current mirror did not show the same current, as measured by the scope, it did manage to keep the distance between the two measurements consistent. From 47 ohms to 1k ohms, the current measured by the scope for both fets were the same. This means that while the components, and our instruments are not exactly identical, they principle of the current mirror is held.

The current mirror fails working over the 1k ohms as we measured. This result is somewhat consistent as the fet is now in deep triode.

Exercise 3.3: DC Biasing

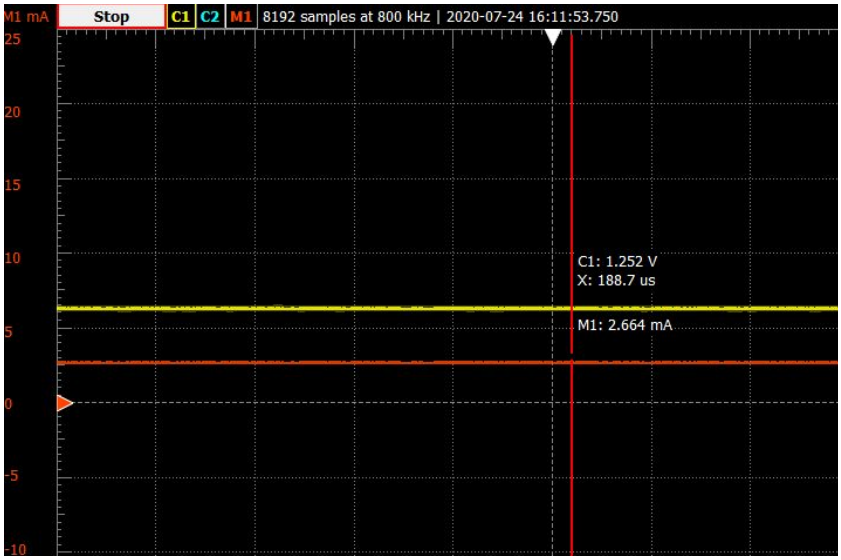
Measurement of VDS and VGS



Yellow = VDS, Blue = VGS

VDS = 2.46V

VGS = 2.09V



Yellow = VRS, Red = I_rs = ID = 2.67mA

The fet is verified to be in saturation. The measured values match roughly to the calculated values.

Exercise 3.4 Common source amplifiers – Amplifier characteristics

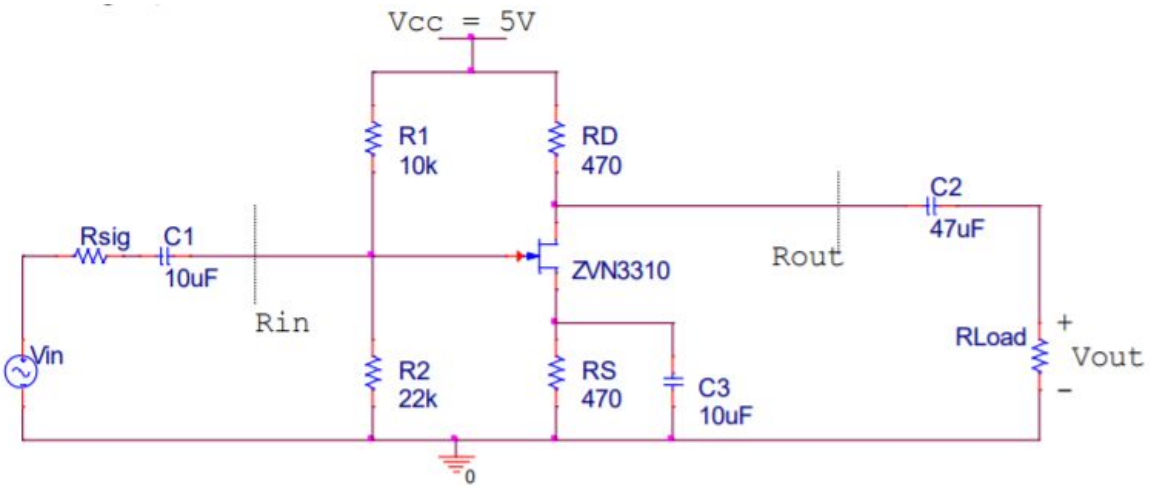
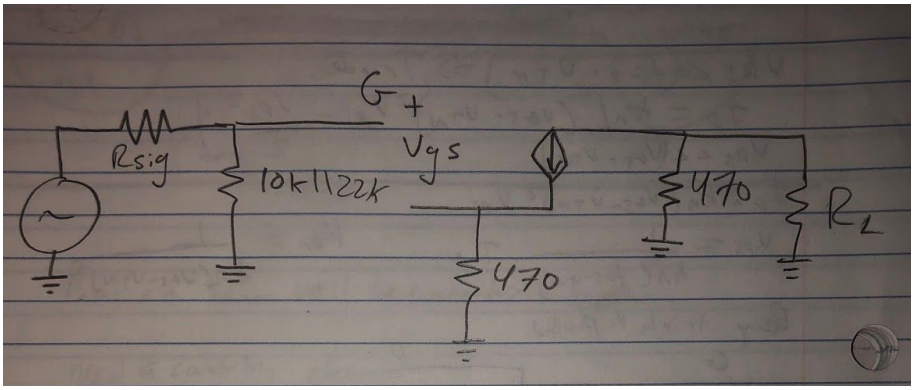


Figure 3.4.1 Circuit to be implemented in part 3.4



Avo was calculated to be 1.35 using Rsig = 0 and RL = infinity, this is acceptable because in the setup we are using 100 and 100k, which have high enough and low enough magnitudes.
My estimated values for Avo was 1.3

Figure 3.4.2 Small signal Model

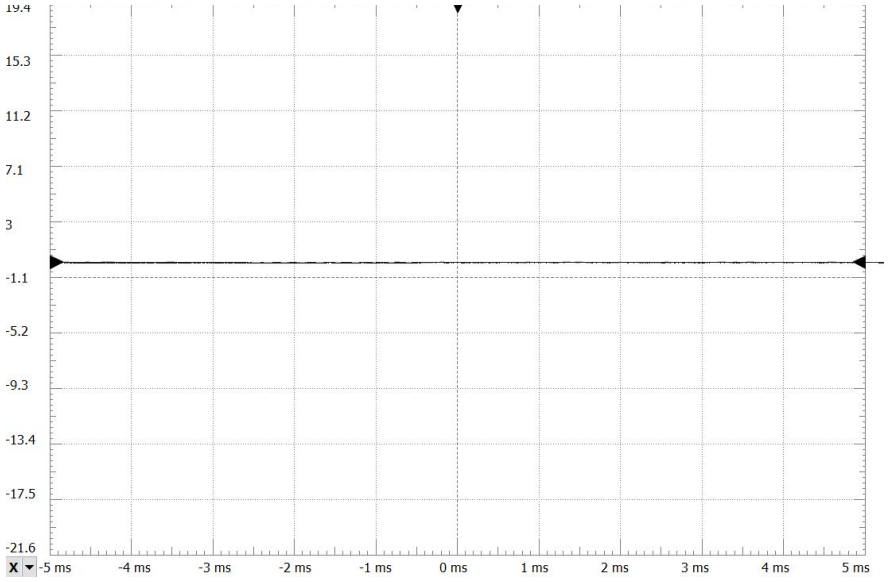


Figure 3.4.3 Output Voltage

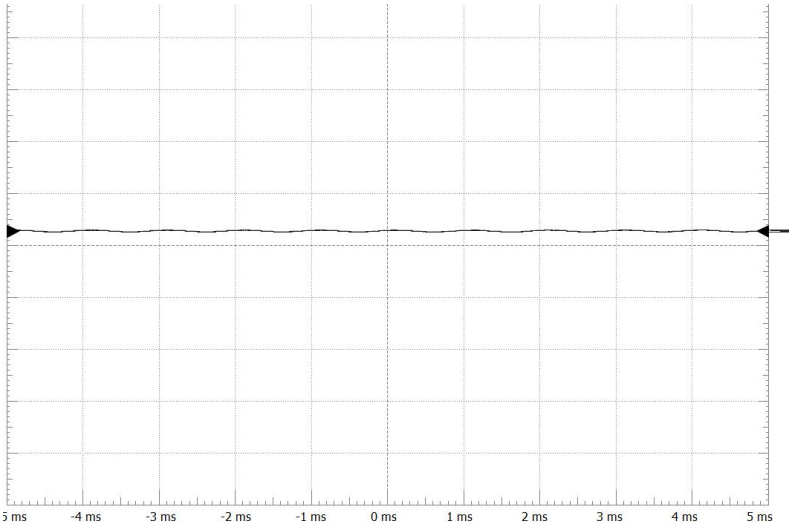


Figure 3.4.4 Current through Rsig

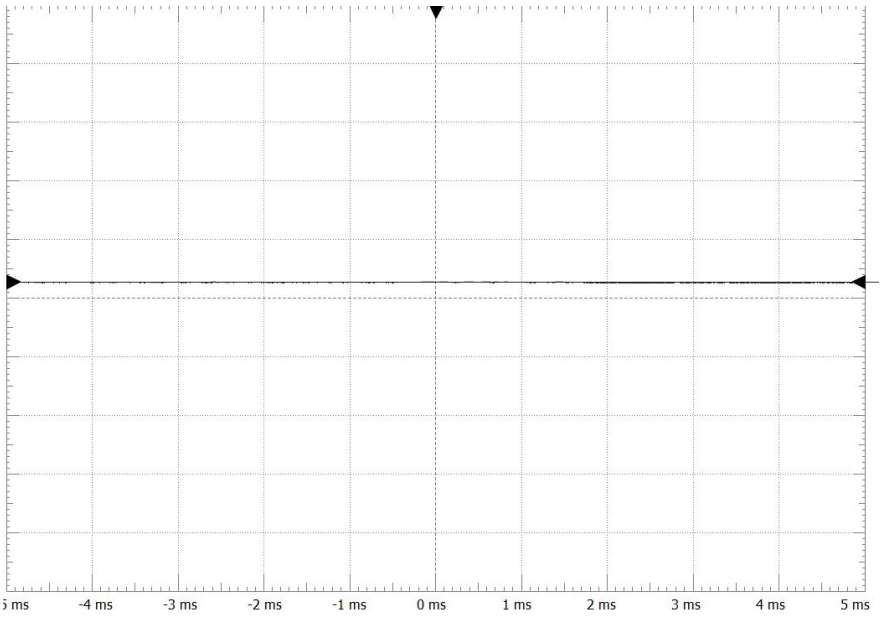


Figure 3.4.5 Current through Rsig = 4.7k Rload =470

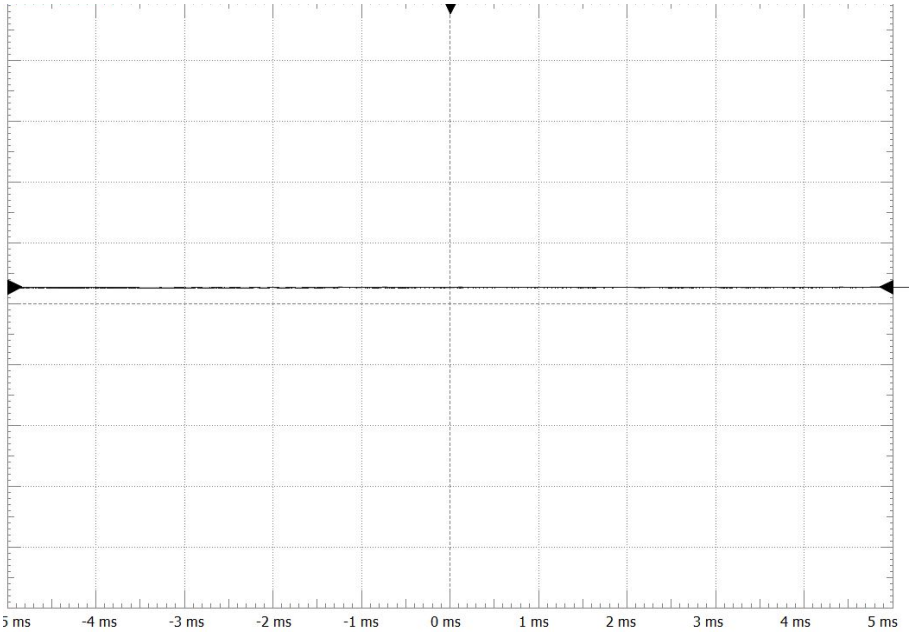


Figure 3.4.6 Current through Rsig without capacitor

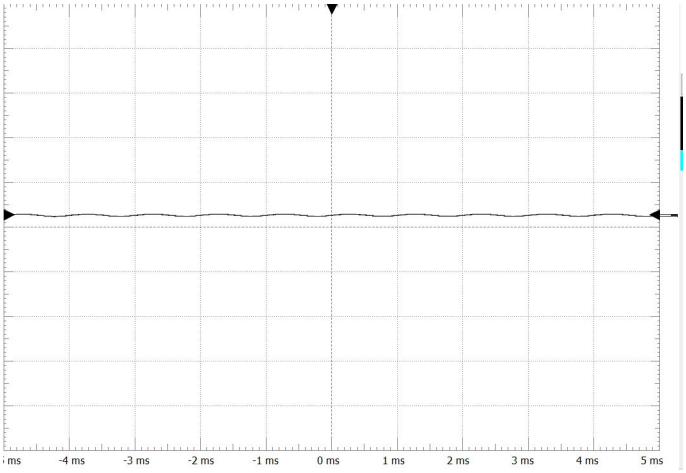


Figure 3.4.7 Current through Rsig without capacitor, with Rsig = 4.7k Rload =470

Without the capacitor, the values increase as the capacitor dampens the output.

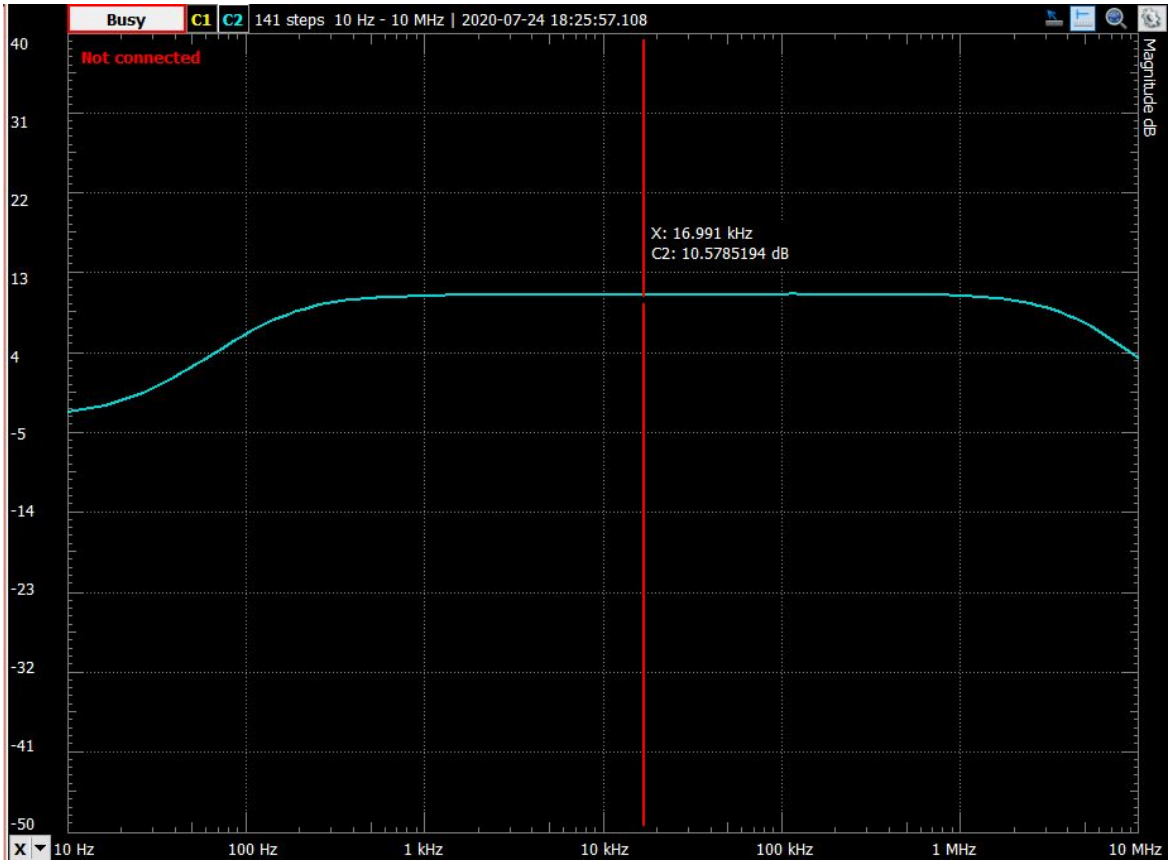
Exercise 3.5: Common Source Amplifier - Bandwidth

$$C_{iss} = C_{gd} + C_{gs}$$
$$C_{oss} = C_{ds} + C_{gd}$$
$$C_{rss} = C_{gd}$$

Thus:

$$C_{GD} = 5\,pF\ ;\ C_{GS} = 35\,pF\ ;\ C_{DS} = 10\,pF$$

Frequency Sweep



We have a pass band from 200Hz to 1 MHz

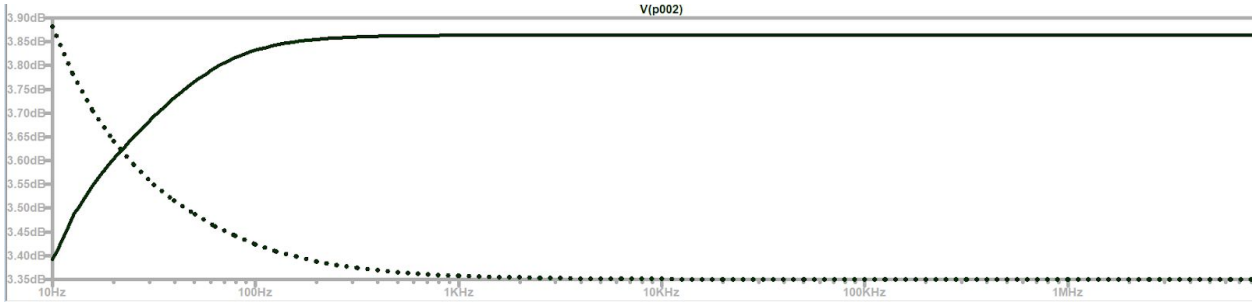
The circuit results match what we have in part 4.

We can see this in Figure 3.4.1 with the capacitors included. The cap responsible for the low band is C1 and the high band cap is CDS.

Rsig is part of the input resistance seen by the cap which means it is directly affected by the RC circuit and it's rolloff frequency. The same reason as to why changing RLoad affects the results. Rload is a resistor seen by the output cap changing the RC circuit.

The 10kHz was a good choice because it operates well within the pass band of the common source amplifier. At this frequency the caps are not affecting the circuit output.

LTSpice of Common Source Amplifier



We can see that the simulated results match decently well with the experimental results. The experimental problem we see is the rolloff at 1 MHz. This is due to internal capacitance that is parasitic. This means that we have a band of frequencies that we have to operate within. What can be done is increasing the band on the low cut off side, but pushing it back. You can choose different resistors and caps to keep the fet in saturation but also decrease the low - high frequency part of the band.

Conclusion:

Fets draw the same interest as diodes, and in a way they are the step up from diodes. They serve as another method for signal control and current flow. Fets are very interesting as we want them to be in saturation for quite a bit of operation. This is because their output is predictable at this point. If it's in deep triode or triode we aren't likely to get the output we want. This is shown with the current mirror exercise. Fets also have the ability to act as amplifiers. Even though you can hook them up differently to get the amplifier you want, nothing will change the parasitic capacitance of a real fet. This causes the fet to act like a bandpass filter. When using fets to design you have to be cognisant of these traits.