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1 A: lw, sw, slt, beq: I type
add, sub, and, or : R type

B: shifting to a new word is easier than shifting to a new byte. It increases the range of jumps.

C: RegWrite enables the ALU output to write (output) back into same register.

D: lw, sw, and other I types needs to SignExtender because they have an immediate 16 bit offset.

E: 32 lines, 1 for each bit

F: if(R[rs]==R[rt])
PC=PC+4+BranchAddr

2 A: It makes the data at the address the new read data

B: It determines where the Mux reads the data from. At 1 it reads from Read Data

C: It determines if the mux reads 20-16 or 15-11 and inputs it to Write Reg. At 0 is reads 20:16

D: Reads 15:11 of the instruction

E: It adds 4 to the PC counter

F: It inputs the sign extended instruction to the ALU

G: Does not allow a register to be written to

H: Allows a register to be written to.