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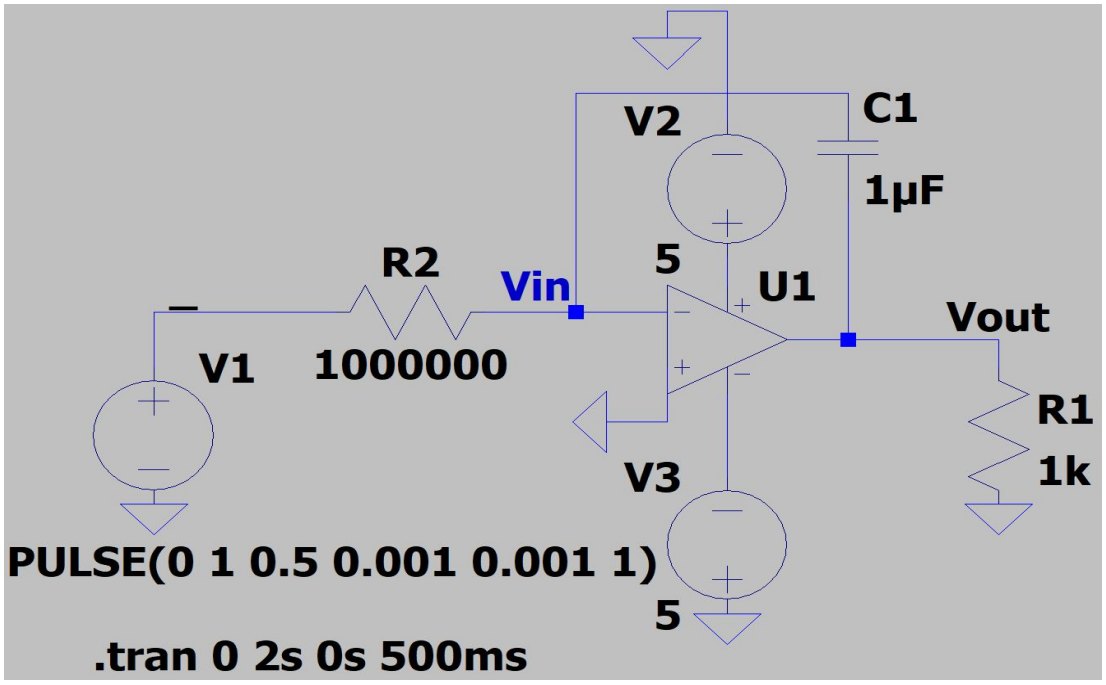
1: Prove Op Amp with Capacitive/Inductive Feedback Network

Building Block:

Description: An Integrator Circuit (first order). The positive op amp input is tied to ground and the input voltage to the negative input terminal is a square wave, where the amplitude is 1 volt. The resistor on the negative input is 1Meg ohm, The capacitor on the negative feedback loop is 1uf, and the resistor on the output terminal is 1k ohm. The power supply to the op amp is 5 volt.



Nodes to be analyzed: Vout, Vin

Analysis:

Doing KCL at node Vin:

Since the positive input terminal of the op amp is tied to ground and using the fact that voltage at positive terminal equals the voltage at the negative terminal when there is a feedback loop in the op amp, we know at node Vin at the negative input of the op amp is 0V. Doing KCL at that point, we get:

$\frac{0-Vin}{R_2} + c\frac{dv}{dt} + 0 = 0$

$c\frac{dv}{dt} = \frac{Vin}{R_2}$

$c\int \frac{dv}{dt} = \int \frac{Vin}{R_2}$ integrate both side

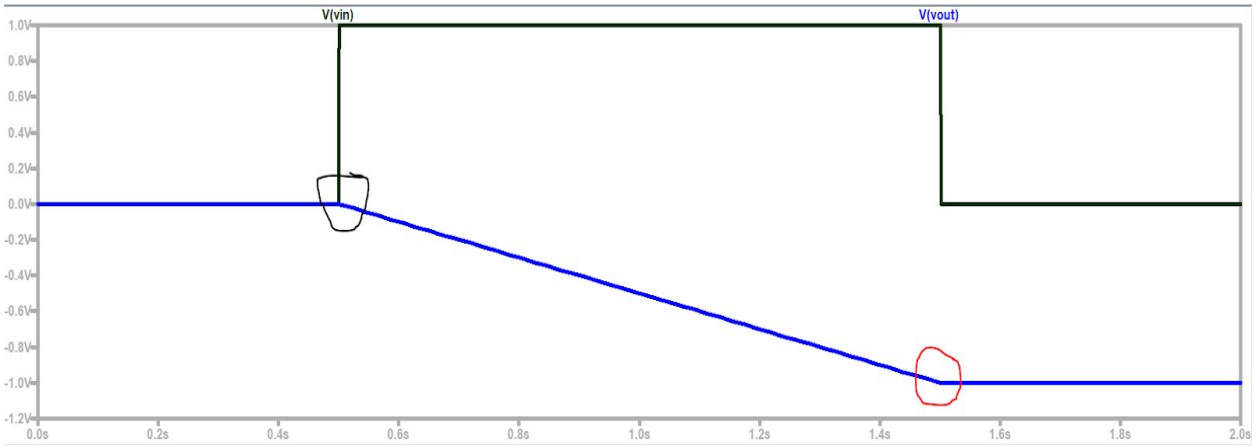
We know the change of voltage over the capacitor at node Vin is $\triangle V$ which is 0-vout

C (-vout)= $\frac{1}{R_2}\int$ Vin dt

vout=- $\frac{1}{CR_2}\int Vin\, dt$

Result from analysis is that vout is integral of the Vin signal over a specified time period divided by the product of the capacitance value on the feedback loop and the resistor value on the negative input of the op amp.

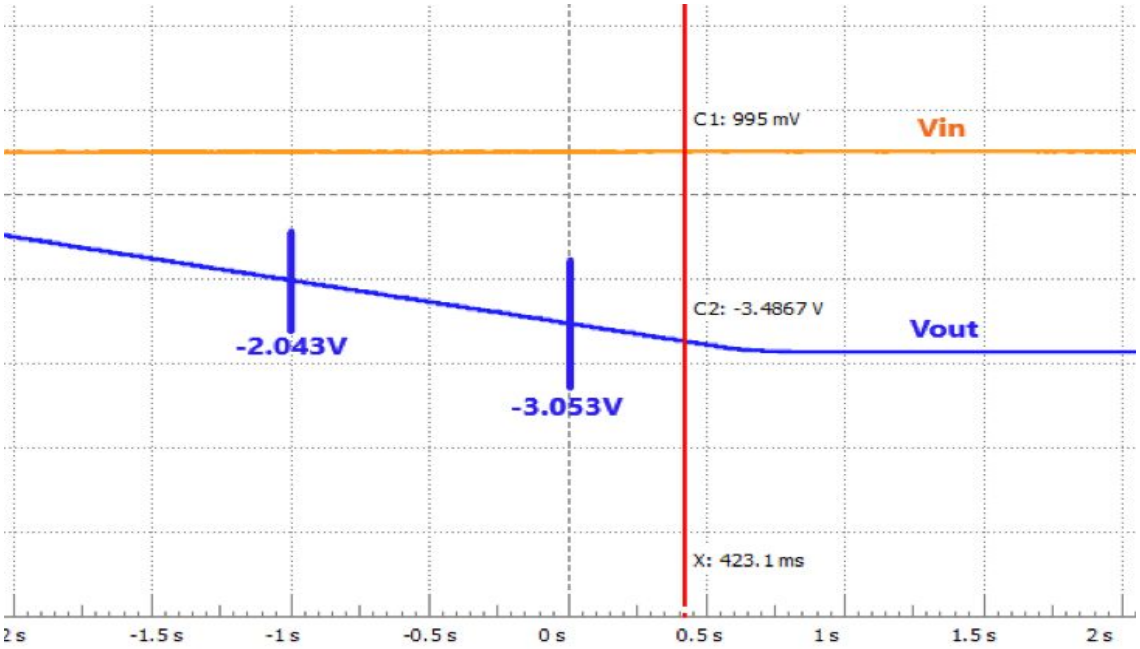
Simulation:



The black curve is the input signal. The integral or area under the curve is $1V * 1s = 1t$. The blue line is the output of the integrator op-amp. Because we chose $R * C = 1$, the output should be $-\int V_{in}$. We know that the integral is $1t$ so the output is $= -1t$. We can verify this be calculating the slope of the blue line which is -1. Thus our simulation matches our analysis.

Measurement:

Build the circuit with the resistance of 10^6 ohm and capacitor of $1\mu C$



Just like in Simulation we verify by finding the slope. $\frac{-3.053+2.043}{0+1} \approx -1$. There is some difference due to non-ideal components

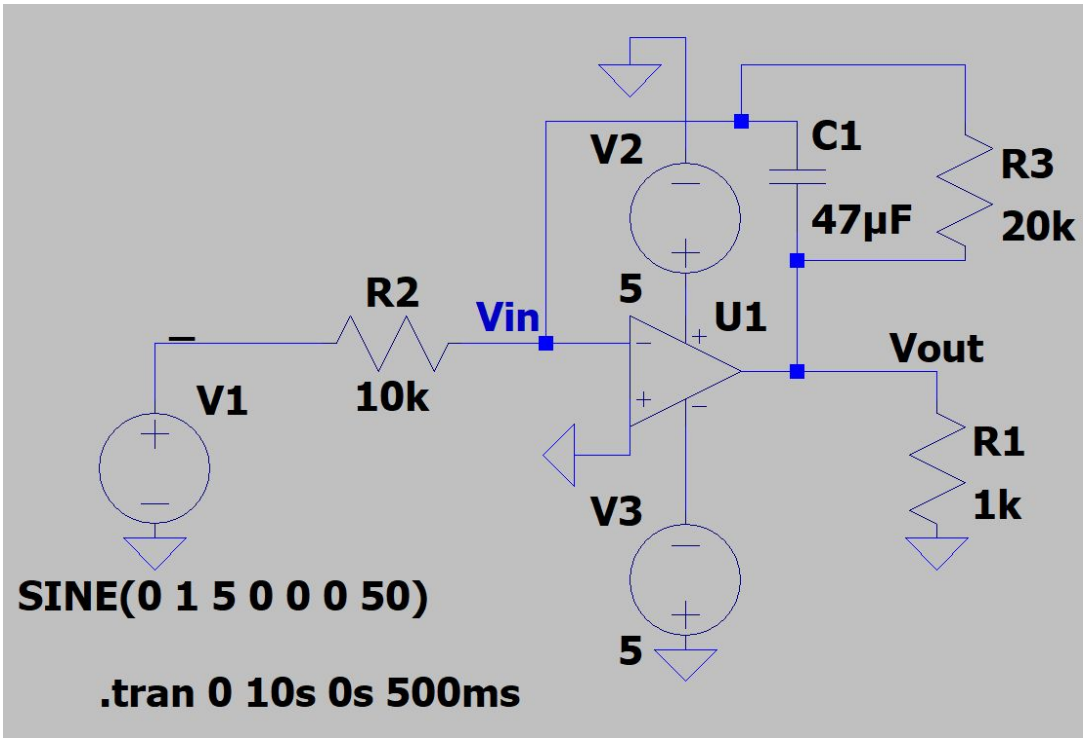
Discussion:

From the result from the analysis portion, an integrator op amp integrates the given Vin voltage signal over a given time divided by the product of the capacitance value on the feedback loop and the resistor value on the negative input of the op amp. The simulation from LTSPICE and the measurement from analog discovery backs up the analysis. We selected resistor value and capacitance that yield a value of 1 and an input is a square wave on the LTSPICE simulation and a constant voltage signal for analog discovery. It can be seen that in both scenarios the result is a negative, linear voltage signal that saturates to the power supply of the op amp. From basic calculus, the integral of a constance V is V(t) which is a linear function which matches the output of the simulation and measurement. In both simulation and measurement since $\frac{1}{RC}$ is 1 and Vin is 1V. Our integration yields a slope of 1V. From analog discovery measurement the slope calculation is $\frac{-3.053--2.043}{-1}$ = $\frac{-1}{-1}$ = 1V and from the LT splice simulation graph, the
slope calculation is $\frac{1-0}{1.5-0.5}$ = $\frac{-1}{-1}$ = 1V. The slope from measurement and simulation matches the math from the analysis.

2: Proving Equivalent Impedance

Building Block:

Description: The circuit is an op-amp with a feedback loop of a capacitor and resistor in parallel. We use this to analyze the AC steady state equivalent impedance. We input a sine wave with 1V amplitude with frequency of 5 hertz. The resistor to the negative input of the op amp is 10k, the capacitor (47uf) on the feedback is parallel to a resistor (20k). The op amp is powered by 5V.



Nodes to Be Analyzed: Vin, Vout, C1, R3, R2

Analysis:

In AC steady state the impedance of a capacitor is equal to $1/j\omega C$. Thus in our circuit, we can analyze the AC steady state impedance of the resistor in parallel with the capacitor to generate an inverting amplifier circuit.

The inverting amplifier formula is: $V_{out} = V_{in} - Z_f/Z_1$. We define our impedance values:

$$Z_f = (\frac{1}{Z_c} + \frac{1}{Z_R})^{-1} = (j\omega C + \frac{1}{20*10^3})$$

$$Z_1 = R_2 = 10k\ \Omega$$

Other values we will use: $\omega = 10\pi$; $C = 47 * 10^{-6} F$

Because this is in AC steady state we are only interested in the gain this equivalent impedance provides us. Our sin wave amplitude = 1. Plugging in our values to the equation for V_{out}

$$V_{out} = -(j(10\pi * 47 * 10^{-6}) + \frac{1}{20*10^3}) * \frac{1}{10^4}$$

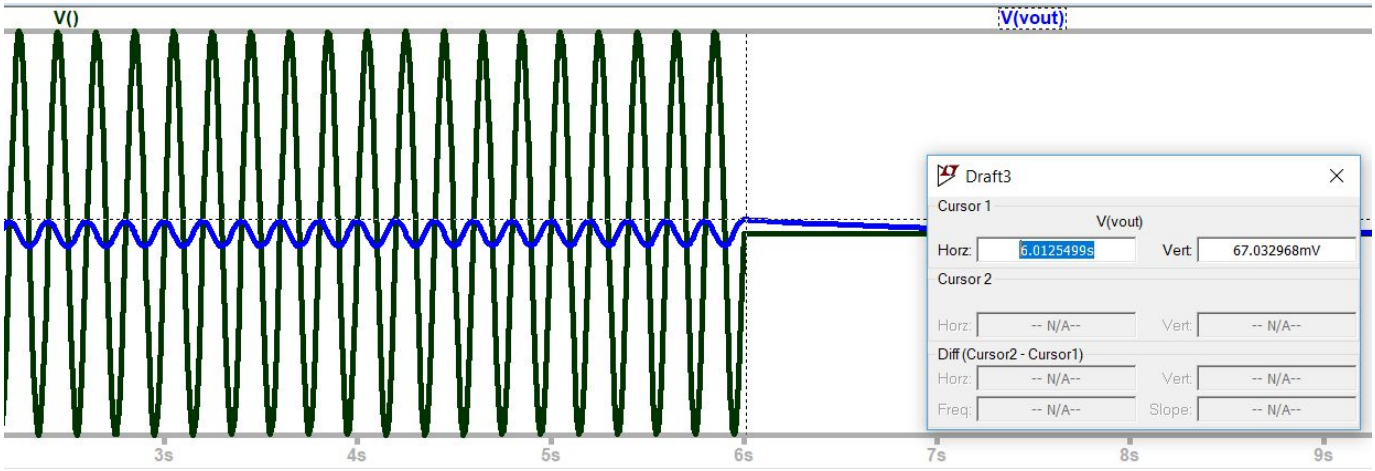
$$V_{out} = \frac{-50}{25+2209\pi^2} + j\frac{470\pi}{25+2209\pi^2}$$

While in the form $V_{out} = aj + b$, the gain will be equal to $\sqrt{a^2 + b^2}$. We calculate this.

$$\sqrt{\left(\frac{-50}{25+2209\pi^2}\right)^2 + \left(\frac{470\pi}{25+2209\pi^2}\right)} = 0.067$$

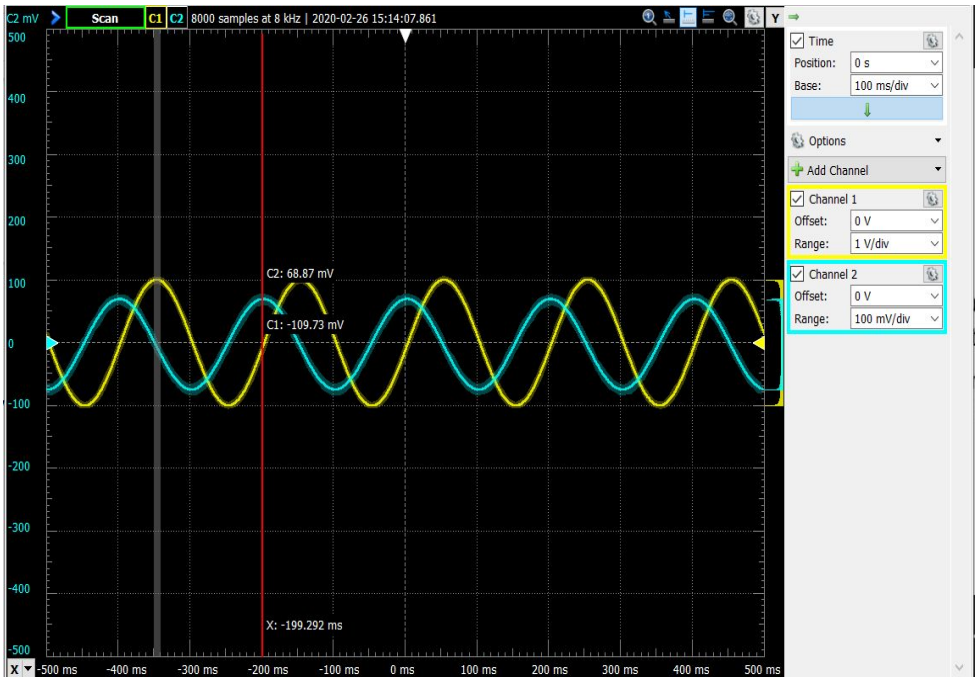
Thus with an input amplitude of 1V we expect the output to be $1V * 0.067 = 67mV$

Simulation:



Based on our predefined definition of AC steady state ($5 * \tau$), from our circuit, after roughly 5 seconds it reached AC steady state. We measure the vertical height of Vout at the cursor location and find that it is roughly 67mV. This matches our predictions from analysis

Measurement:



Blue is the output and yellow is the input.
We input 1V sine wave with a frequency of 5 hertz.

The peak on the yellow since wave is 1V and the peak on the yellow is ~68.87mV
The measurement gain is:
input*gain=output
1*gain_measurement=0.06887
gain_measurement= $\frac{0.06887}{1}$
gain_measurement=0.06887

Discussion:

With a resistor in parallel with the capacitor in the feedback loop, we get an amplifier integrator when we input a sine wave. From the analysis, we $V_{out} = \sqrt{a^2 + b^2} \angle$ tan(b/a) where **b** is the real part and **a** is the imaginary part. In our measurement, we got a gain of 0.06887 and in our simulation, the gain is 0.067 and our analysis, the gain is 0.067. The simulation and analysis match while the gain from analog discovery differs by 0.00187 due to resistor tolerance. Applying 5% tolerance, 0.06887+0.05(0.06887) and 0.06887-0.05(0.06887). The bound is [0.0654265,0.0723135], the expected result is within the 5% tolerance.This shows that with a resistor in parallel with the capacitor, we can use impedance to analyze the output voltage.