Introduction to Electronics

Summer 2020 Saaif Ahmed

Quiz 3

Administrative Notes:

1) There are 9 problems.

2) Each problem must be on a separate piece of paper(s). You can put the sub-parts on the same paper (ie. parts a,b,c,d can be on one paper if they cover multiple pages on the exam)

3) Write neatly. We do not want to learn hieroglyphics to grade your exam. If possible, I would prefer that you print out the exam and write on it.

4) There will be two submission options on Gradescope.
    1. The full document uploaded to the 'Full Exam' option
    2. Three separate uploads, Part 1 (p1-4), Part 2 (p5-7), Part 3 (p8-10) with appropriate names.

   The different options are available for those who have problems with uploading bigger files.

5) If you are having trouble uploading, you must contact me immediately. As a backup, you may want to upload to Box and share with me.

6) The exam is likely long. Do not spend excessive time on a problem. Move on to problems you can solve quickly.

7) Yes, there will be a curve.

Test Notes:

1) For all BJT problems, you may assume Vthermal ~ 0.026V, V_{BE} ~ 0.7V and when forward biased and V_{CE} ~0.2V when in saturation.

2) Unless otherwise indicated, assume $r_o \rightarrow \infty$.

3) If you are stuck on part of a problem, use **a reasonable** value to continue to the following parts. Partial credit will depend on your choice of a reasonable value.

4) **Calculation answers without supporting work will receive no credit.**

5) Incorrect answers may earn partial credit by including schematics when they are not specifically requested as part of the problem.

Problem 1) Short Answers (21 pts)

Question 1 (6 points)

For an ideal, symmetric differential amplifier (circle one answer for each question)

The differential output, $Vout_2 - Vout_1$, for a common mode input is

Zero Infinity Circuit dependent

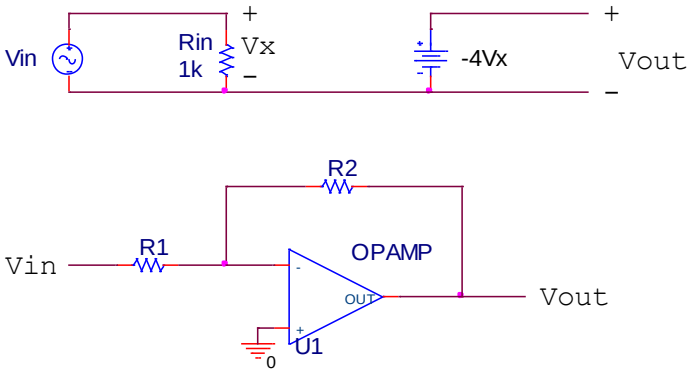
The differential output, $Vout_2 - Vout_1$, for a differential input is

Zero Infinity Circuit dependent

The common mode rejection ratio (CMRR) is

Zero Infinity Circuit dependent

Question 2 (6 points)



The top circuit represents the general amplifier model for the inverting amplifier shown in the bottom circuit. Determine values for R1 and R2

R1 = _____

R2 = _____

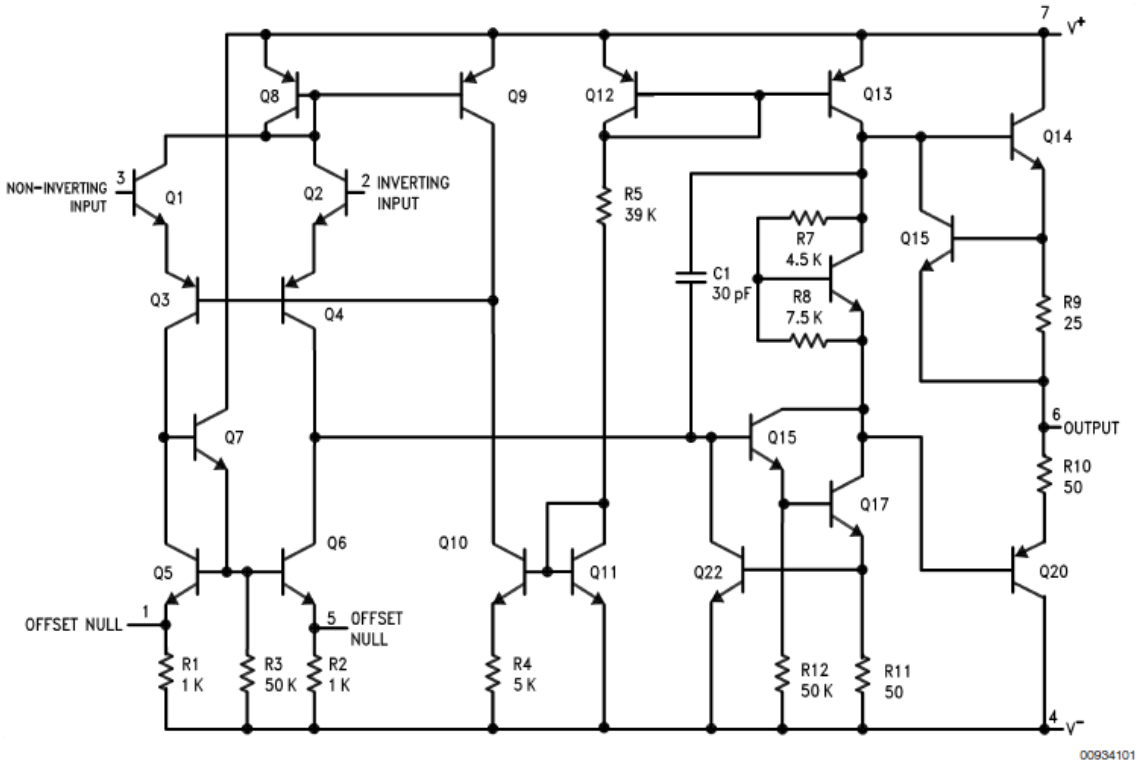
Question 3 (5 points)

General True/False questions

T / F a) Increasing the bias voltage of a diode increases the diode resistance, r_D.
T / F b) When designing a FET transistor, it is possible to change the transconductance property, K_N, by changing the transistor dimensions.
T / F c) Typically, a BJT amplifier circuit with no external capacitors can amplify small signal DC inputs.
T / F d) It is possible for a BJT transistor to be on, yet have zero collector current.
T / F e) Zener diodes can be used as standard diodes.

Question 4 (10 points)

Two transistors should be indicated in each underlined space, ie. QA and QB.



a) Using the above 741 op-amp schematic, identify two (different) transistor pairs that form a **current mirror**.

_____ _____

b) Using the above 741 op-amp schematic, identify a transistor pair that forms a **common collector** differential pair.

_____

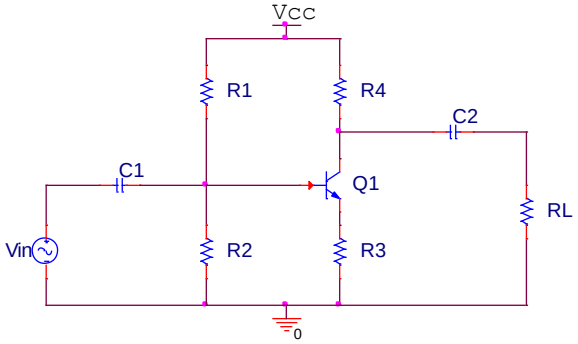
c) Using the above 741 op-amp schematic, identify a transistor pair that forms a **common base** differential pair.

_____

d) Using the above 741 op-amp schematic, identify a transistor pair that is an **current mirror load** for a differential amplifier.

_____

2) Bandwidth characteristics (12 pts)

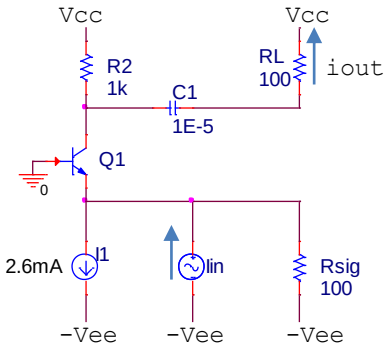


a) Based on circuit components we have used in class, which capacitor (C1 or C2) is most likely to be associated with the low frequency pole. Justify your answer. (6 pts)

b) Based on circuit components we have used in class, when applying the Miller Theorem to C_{BE}, which equivalent capacitor (C_{BEin} or C_{BEout}) is most likely to be associated with the high frequency pole. Justify your answer. (This question is a bit tricky.)(6 pts)

3) BJT Amplifiers (21 pts)

All answers should be accurate to three significant digits.



The above transistor has forward active current gain $\beta = 50$.

a) Draw the small signal model. For all components, provide numerical values. (5 pts)

b) In context of the labelled RL and Rsig (the dashed box excludes these resistors), determine the input resistance, Rin. (3 pts)

c) In context of the labelled RL and Rsig (the dashed box excludes these resistors), determine the output resistance, Rout. (3 pts)

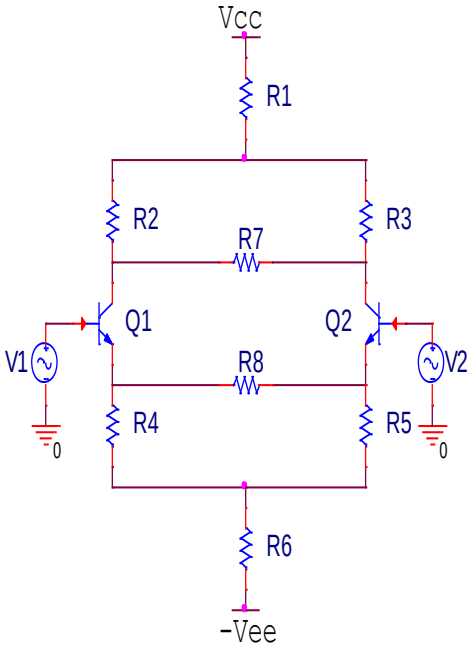
d) In context of the labelled RL and Rsig (the dashed box excludes these resistors), determine the short circuit current gain, A_{Io} (RL → 0, Rsig → ∞). (4 pts)

e) Determine the overall current gain, A_I = Iout/Iin. (3 pts)

f) Estimate the low frequency 3dB cutoff for the circuit. (3 pts)

4) Differential Amplifier Characteristics (20 pts)

a) For the differential amplifier to the right indicate any resistors that have zero **DC bias current** (when V1 = V2 = 0V). (4 pts)



_____

b) For the differential amplifier to the right, indicate any resistors that have zero **common mode small signal currents** (when V1 = V2 = VCM).. (4 pts)

_____

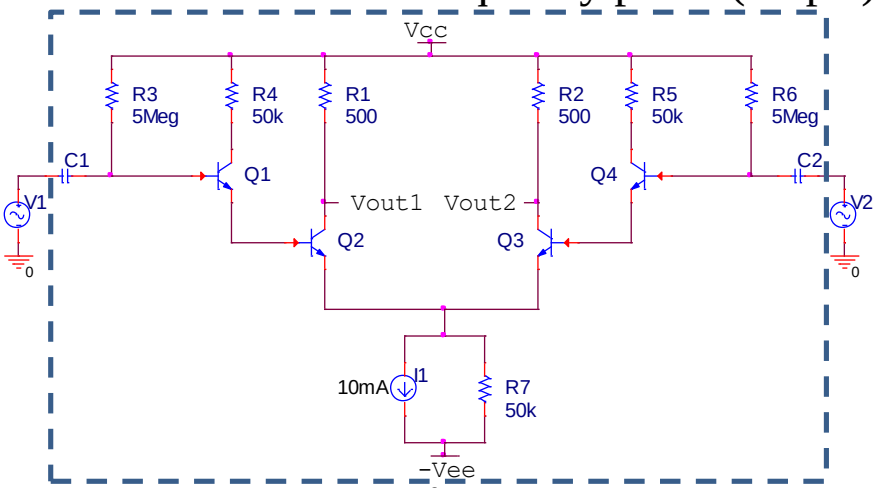
c) For the differential amplifier to the right, indicate any resistors that have zero **differential small signal currents** (when –V1 = V2 = V_{DM}/2) (4 pts)

_____

d) Sketch the common mode small signal half-circuit model, labelling all components symbolically. Use the Hybrid-π model for the transistor. (4 pts)

e) Sketch the differential mode small signal half-circuit model, labelling all components symbolically. Use the Tee model for the transistor. (4 pts)

5) Half circuit models and low frequency poles (38 pts)



a) Determine the small signal parameter r_π for Q1 and Q2.. (4 pts)

Parts b, c, and d have common mode inputs, V1 = V2 = V_{CM}.

b) Sketch the half-circuit model, labelling all components with numerical values. (6 pts)

c) Determine the full circuit common mode input resistance, R_{inCM}. Show your work including, if necessary, schematics to support your analysis. (4 pts)

d) Determine the half circuit common mode voltage gain, A_{VCM} = Vout1/V1. Show your work including, if necessary, schematics to support your analysis. (4 pts)

Parts e, f, and g have differential inputs, –V1 = V2 = V_{DM}/2.

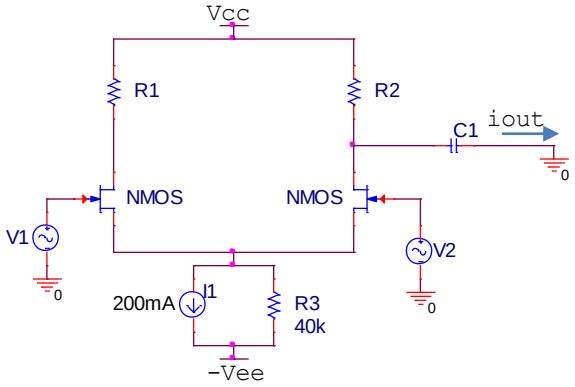
e) Sketch the half-circuit model, labelling all components with numerical values. (6 pts)

f) Determine the full circuit differential mode input resistance, R_{inDM}. Show your work including, if necessary, schematics to support your analysis. (4 pts)

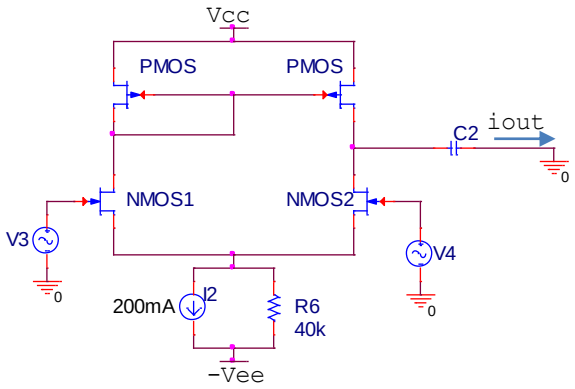
g) Determine the half circuit differential mode voltage gain, A_{VDM} = Vout1/V1. Show your work including, if necessary, schematics to support your analysis. (4 pts)

h) Based on your part d and g answers, when R1 and R2 have 5% tolerance, determine the worst case CMRR for the full circuit gain, CMRR = $20\log|A_{DM}/A_{CM}|$. Recall, for the full circuit the differential output is Vout = Vout2 – Vout1. (6 pts)

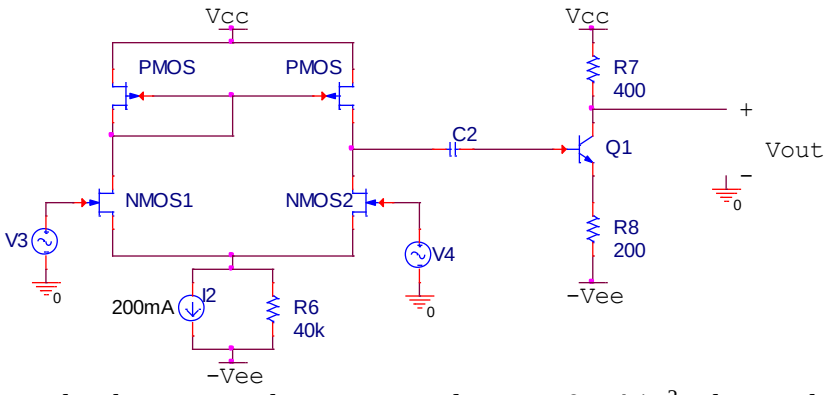
6) Small signals in differential amplifiers (18 pts)



a) The NMOS transistors in the above circuit have transconductance 0.4 A/V^2. For a differential voltage, VDM = 0.01sin(ωt), determine the small signal output current iout. You can assume the common mode contribution is zero (not very realistic). (6 pts)



b) The FETs in the above circuit have transconductance 0.4 A/V^2. For a differential voltage, VDM = 0.01sin(ωt), determine the small signal output current iout. You can assume the common mode contribution is zero (not very realistic). (4 pts)



c) The FETs in the above circuit have transconductance 0.4 A/V^2. The BJT has forward active current gain, $\beta = 100$. For a differential input voltage, VDM = 0.01sin(ωt), determine the small signal output voltage, vout. You can assume the common mode contribution is zero (not very realistic). (8 pts)

7) Resistor=Transistor Logic (12 pts)

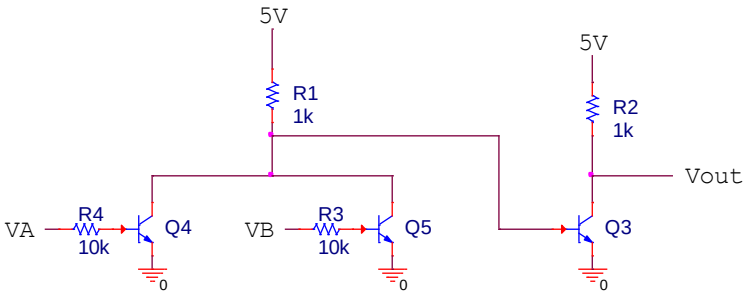
a) Design an RTL digital inverter with the following specifications.
   1) $NM_L = 0.5V$
   2) $NM_H = 2.0V$
   3) $V_{OL} = 0.2V$
   4) $V_{OH} = 3.3V$
   5) The input voltage range is 0V to Vcc.

   Include a sketch of the circuit, labelling all component values, power supply values and indicate the transistor characteristics (numerical values all of these properties). (12 pts)

8) Digital Circuits and Static Power (22 pts)

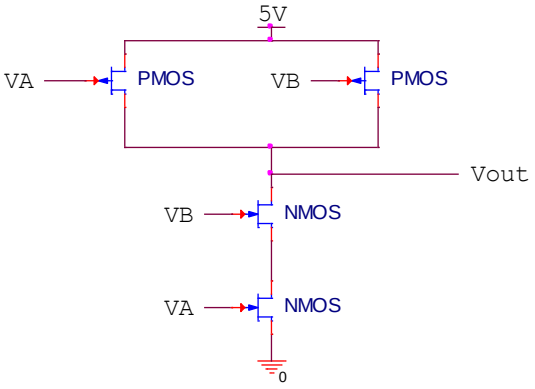
The transistors have forward active current gain, $\beta = 100$.

a) For the digital circuit, determine the output voltage for the various combinations of input voltages. For each row of the truth table, indicate which tranistros are on and which are off and indicate the static power consumed by the circuit. (12 pts)



VA	VB	On	Off	Vout	Pstatic
0V	0V				
0V	5V				
5V	0V				
5V	5V				

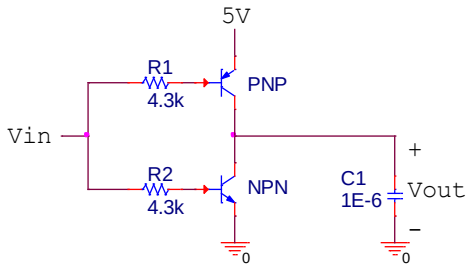
b) For the CMOS circuit, determine the output voltage for the various combinations of input voltages. For each row of the truth table, indicate the static power consumed by the circuit. If a load resistor is added between Vout and ground, indicate whether the static power in each row of the truth table increases, decreases or stays the same. You might want to include an equivalent circuits when determining your answers. (10 pts)



VA	VB	Vout	Pstatic	Power change with RL
0V	0V			
0V	5V			
5V	0V			
5V	5V			

9) Propagation delay (14 pts)

Both the NPN and PNP BJTS have a forward active current gain of $\beta = 100$.



a) Identify V_{OH} and V_{OL} for the complimentary BJT circuit circuit. (2 pts)

b) Assuming the input voltage and transistors switch instantaneously, estimate the propagation delays, t_{PHL} and t_{PLH}, for the circuit. Include the equivalent circuit schematic(s) used when analyzing the transient behavior of the circuit. (12 pts)