MIDTERM EXAM - 2021

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Subject - VLSI
Date - 04/10/21
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Q1 Given $V_{T0} = 0.6V$
$\gamma = 0.2V^{1/2}$
$K' = 20\mu A/V^2$
$\lambda = 0.04\ V^{-1}$
$2\phi_f = 0.6$

(1) aspect ratio = ?
$\because V_g = 2.7 \quad V_{gs} = 1.8V$
$V_d = 5V \quad V_{ds} = 4.1V$
$V_s = 0.9$
$I_D = 0.22mA$

$\therefore$ aspect ratio $= \frac{W}{L}$

$\because V_{gs} - V_t = 1.80 - 0.69$

$\because V_T = V_{T0} + \gamma\left(\sqrt{|2\phi_f| + V_{SB}} - \sqrt{|2\phi_f|}\right)$
$= 0.6 + 0.2\left(\sqrt{0.6 + 0.9} - \sqrt{0.6}\right)$
$V_T = 0.6 + 0.2(\sqrt{1.5} - \sqrt{0.6})$
$0.6 + 0.2(1.22 - 0.77)$
$= 0.69 = 0.69$

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$V_T = 0.63V$

$V_{ds} : 4.1 \; ? \; 1.2$

So I_d is in saturation mode

$$I_D = \frac{K'}{2} \frac{W}{L} (V_{gs} - V_T)^2 (1 + \lambda V_{ds})$$

$$\frac{W}{L} = \frac{2 . I_D}{K' (V_{gs} - V_T)^2 (1 + \lambda V_{ds})}$$

$$= \frac{2 \times 0.22 \times 10^{-3}}{20 \times 10^{-6} (1.2)^2 (1 + 0.04 \times 4.1)}$$

$$= \frac{0.44 \times 10^{-3}}{33.5 \times 10^{-6}}$$

$$= 0.0131 \times 10^{3}$$

~~13.13~~ 17.46

(b) $\because \; V_g = 5V \quad V_d = 3.0 \quad V_S = 1.0$

$V_B = 0$

$I_d = ?$

$$V_T = 0.6 + 0.2 \sqrt{0.6 + 1.0} - \sqrt{0.6}$$

$$= 0.6 + 0.2 (1.5 - 0.5)$$

(1)

$$= 0.8$$

$V_T = 0.8$

$V_{ds} = 1.2 \; ? \; (3.2 - 0.8)$

$= 1.2 < 2.4$

this is linear region

$$I_d = \frac{K'}{2} \frac{W}{L} [2 (V_{gs} - V_T) V_{ds} - V_{ds}^2] [1 + \lambda V_{ds}]$$

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$= \frac{20 \times 10^{-4}}{2} \times 13.13 \left[7 \times (2.4 \times 2 - 4) \right] \left[1 + 0.04 \times 8 \right]$

$= 10 \times 10^{-4} \times 13.13 \left(9.6 - 4 \right) \left[1.08 \right]$

17.46

$13.3 \times 5.4 \times 1.08$

$= 765.74 \times 10^{-6}$

~~$= 765 \text{ m}(\Omega)$~~

$= 0.101 \text{ m}(\Omega)$

(c) $N_n = 450 \text{ cm}^2/\text{V.S}$ $r_j = 10^{-15} \text{ F}$

W and L = ?

$r_{ox} = \frac{K'}{N_n} = \frac{26 \times 10^{-6}}{450}$

$= 0.04 \times 10^{-6}$

$= 4 \times 10^{-8}$

$W.L = \frac{r_j}{r_{ox}} = \frac{10^{-15}}{4 \times 10^{-8}} = 2.5 \times 10^{-8} \text{ F/cm}^2$

$= 2.43$

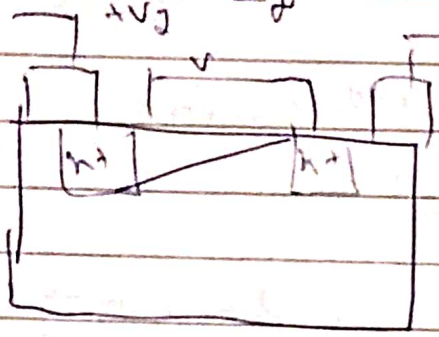
$\frac{W}{L} = 17.4$

$W.L = 2.5 \times 10^{-8} \text{ F/cm}^2$

$W = 4.5 \mu m$

$L = 0.32 \mu m$

(iv) The resistance of the channel is inversly proportional to its length ratio reducing the length to diverse resistance and hence higher current than thus than channel length modulation the Saturation region drain current



$$I_D = \frac{1}{2} \mu_n C_{ox} \left[\frac{W}{L}\right] [V_{GS} - V_T]^2$$

Q.2 If channel length is doubled the drain current half of the original drain current

Q.3 In Saturation region drain current

$$I_d = \frac{B(V_{GS} - V_t)^2}{2}$$

where $B = \frac{\mu_n}{t_{ox}} \left(\frac{W}{L}\right)$

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(a) If channel 'w' doubled the drain is half of the given drain current

(b) If channel width is doubled the drain current will also be doubled

(c) If overdrive voltage is doubled the drain becames 2 times of drain current

(d) if drain to source voltage is increased the drain current became 2 times $V_{ds} = V_{gs} - V_t$

(e) if a, b, c, d are applied simultaneously the drain current became 4 times.

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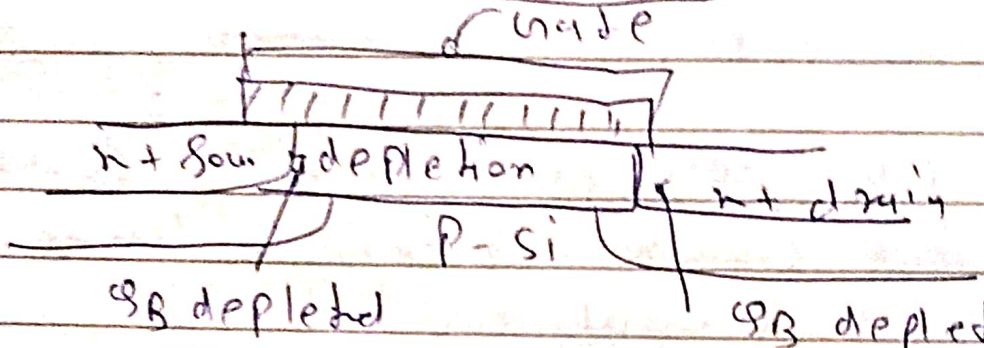
Q.4 (i) DIBL: Drain induced Barrier lowering (DIBL) is a short channel effect in mosfet prominent in ultra scaled mosfet having channel length less than 100 nm ~~to understand the~~



(ii) Hot carrier effect- is a reliability problem which occurs when hot carriers carry $Si-SiO_2$ interface damage and/or oxide trapping. this leads to the degradation of the current drive capability of the transistor, thus eventually causing circuit failure.

(iii) Velocity Saturation: Saturation velocity is the maximum velocity a charge carrier in a semiconductor generally electron attains in the presence

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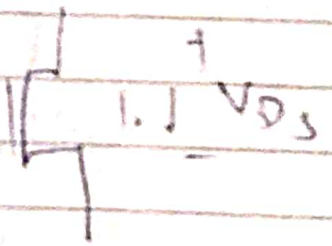
very high electric fields. When this happen, the semiconductor is said to be in a state of velocity saturation

(d) Full Scaling on power

Static power in mosfet can be described as sub drain current flows between source and drain terminal

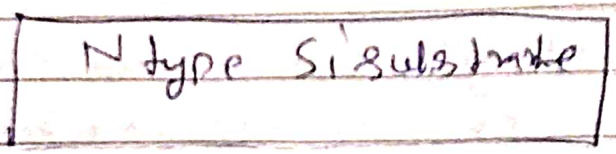
$$P = I_{DS} V_{DS}$$

$$P' = \frac{I_{DS}}{S} \cdot \frac{V_{DS}}{S} = \frac{P}{S^2}$$



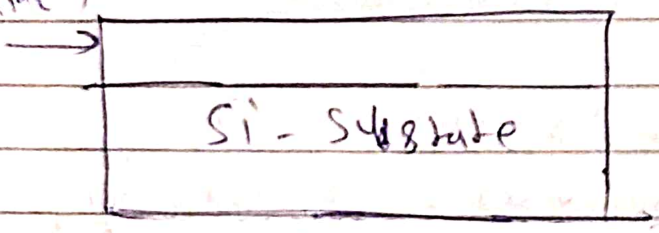
Q.3 : PMOS Consist N-Type Substrate and P type of Source and Drain.

Step① Wafer of Si

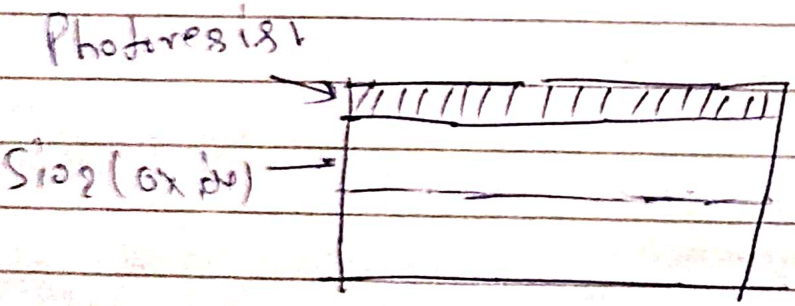


Step② thermal oxidation of Si Surface

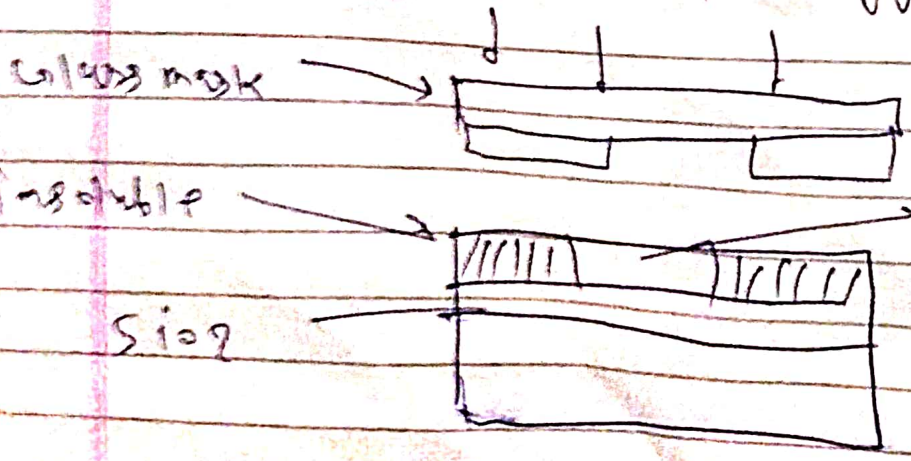
SiO_2 (oxide)



Step3 Photo resist

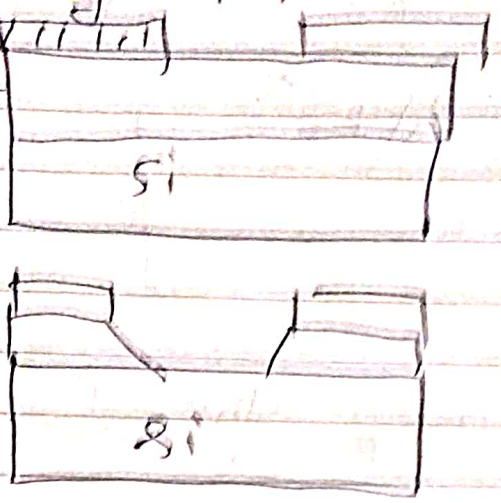


Step 4- glass mask UV light



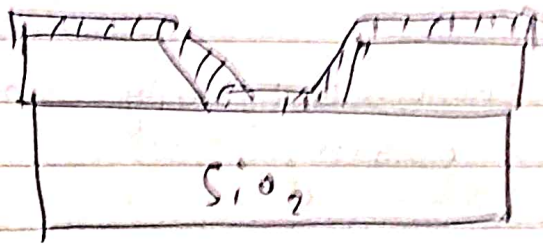
Step 5 - etching (Chemical etch)

Hardened SiO_2

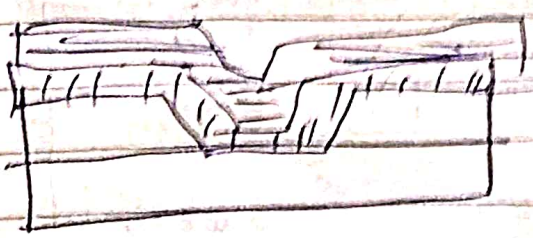


Step 6 - Stripped from the gate surface and Solvent.

now layer covered by thin layer



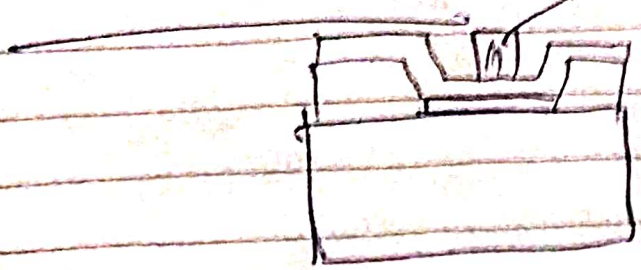
Step 7 Now Polysilicon layer



Polysilicon
Thin oxide

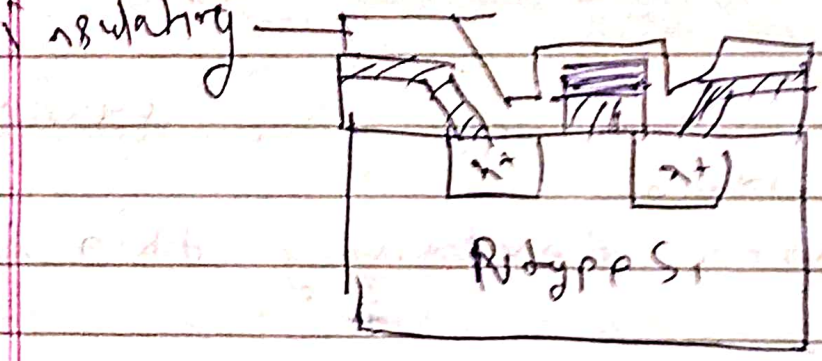
8 Photography

Polysilicon (metal gate)

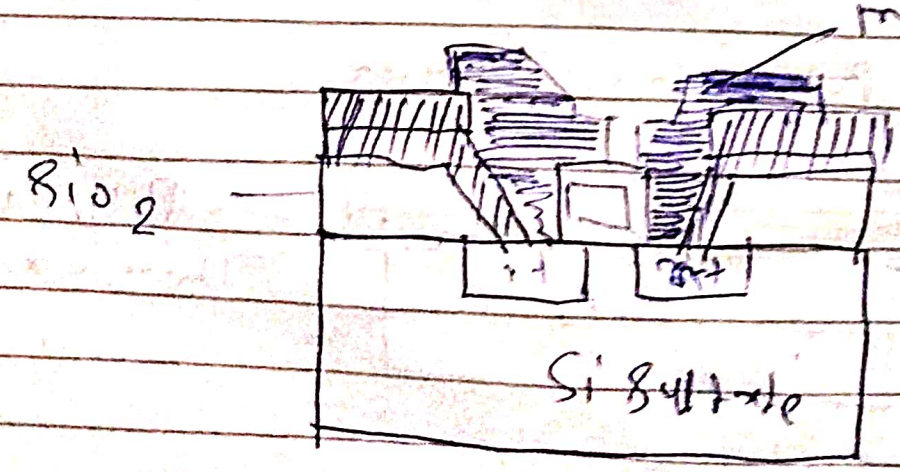


Step X etching Polysilicon

Step XI dopping and insulating



Step XII Photolithography and evaporated and etching



PMOS

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Q-3 $V_{DD} = 5V$.

$V_{tn}, V_T = -1V - 7V$.

$\mu_n C_{ox} = 60\mu A/V^2$

$\frac{W}{L} = C_o$

(i) For Pmos to Conduct

$V_{SG} > |V_{TP}|$

$V_S - V_G > 1$

$V_S - 1 > V_G$

$V_G < 5 - 1$

$\boxed{V_G < 4}$

(ii) For triode region

$V_{SD} \leq V_{SG} - |V_{TP}|$

$V_D \geq V_G + |V_{TP}|$

$\boxed{V_D \geq V_{G+1}}$

$\boxed{V_D > V_{G+1}}$

(iii) $V_{SD} \geq V_{SG} - (V_{TP})$

$5 - V_D \geq 5 - V_{or} - |V_{TP}|$

$\boxed{V_D \leq V_{G+1}}$

(iv) $d = 0$, $V_{SG} = ?$, $I_d = 75\mu A$

$I_D = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} (V_{SG} - |V_{TP}|)^2$

$75 = \frac{60}{2} (4 - V_G)^2$

$V_G = 3.5$ $V_C = 4.5$

$V_A = 3.5 < 4 = D$

$V_{GD} = V_{SD}$

We know that

$V_D \leq 4.5$ For P mos to be saturation

$V_D = 4.5$

$V_D = 4.5$

$V_{SD} = 5 - 4.5$

$V_{SD} = 0.5$

(V) $R_0 = \frac{V_D + V_{SD}}{I_{SD}}$

$R_0 = \frac{\left|\frac{1}{d}\right| + V_{SD}}{I_{SD}} = \frac{50.5}{75}$

$R_0 = 673.3 k\Omega$