090505201172

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Activity 8-3

COA

· Case Sterdy en working of DMA
Controller

AMA Controller 8- The ferm DMA Stands
for direct Memory access. The
hardware denice used for direct Memory
access is Called the DMA Controller
DMA Controller is a Control unit, part
of I/o denice's interface Circuit, which
Can transfer blocks of data between
I/o denices and main remory with
minimal interface intervention from the
processor

Herking of DMA Controller 8-

AMA Centreller has to share the bus
with the processer to Make the data
transfer. The device that holds the bus
at a given time is Called bus
Master. When a transfer from To

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denice to the runery or Vice-Verse has to be made, the processor stops the execution of the current program, increm-- ente the program Counter, nouses data Uner Stack then Sends a RMA Select Signal to DNA Centraller Our the address ben.

If the DMA Controller is free, it requisite the Control of bus from the processes by having the bus request signal Processor grants the Bus to the Controller by hairing the bus grant signal, now DNA Centroller is the bus Martin The processor initiates the DMA Controller of blocks of data to be transferred and direction of data transfer. After d Drie Controller, instead of maiting ideally till Completion of data transfer, the processor herence the execution of the program after retrieung instructions from the Stack

Page No. 3 Date: / / Interrupt BLY BR RAM CPU RD WR Address State Read Control RO WR Address Data white Central Address bus Address Select Data bus De RD WR Address Llater BR LOMA I/o Denle AMA request Intercupt DMA Controller now has the full Control of busis and Can interact directly with Menery and I/o dewices independent of CPV. It Mosses the data transfer according to the Control instructions hereined by the processor After Competicer of data transfer, it disables the bus request signal and CPV disables the ben grant signal thereby moving Control of buses to the cpu

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When an I/o device wants to untrate the transfer their "it bends a DMA refust signal to the DNA Controller, for nehåde the Controller ocknowledges if it is fice the the Centreller requite the processor for the bus, having the bus request signal After receiving the best quant signal it trousfer the data from the device for n chameled DNA Centraller a number of External devices Can be Comented.

- The DMA transfer the data in three Heder Which include the following.

ay Breut Hode &- In this Made DMA handown

the burn to CPV Only after Completion

ef nehole data transfor.

gives Control of buses to CPV after transfer of tevery byte

y transparent Mode :- Hur, DMA transfer data Only when CPV is Executing the instructions which deer not require the Use of busic.