Sai Kaushik S

Hardware Enthusiast

I am pursuing Dual Degree (B. Tech + M. Tech) in Computer Science and Engineering at IIITD&M Kancheepuram, Chennai.

Passionate about VLSI Design, Computer Architecture and Reconfigurable Computation.

Want to utilize my skills to achieve real world targets, pipelined with increasing my knowledge in the topics.

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Address

101, 2nd Main,
Subbanna Garden Vijayanagar,
Bangalore, KA – 560 040

Skills

C, C++, Python, Verilog, ARM

Education

July 2018 - Present

Dual Degree (B. Tech + M. Tech) Computer Science and Engineering
Indian Institute of Information Technology, Design and Manufacturing, Kancheepuram, Chennai
CGPA: 8.67 / 10

July 2016 – April 2018

Class 12 (Karnataka State Board) PCME
VVS Sardar Patel PU College, Bangalore
Percentage: 93.33%

May 2015 – April 2016

Class 10 (CBSE Board)
Narayana e-Techno School Ramamurthy Nagar, Bangalore
CGPA: 10 / 10

Projects

Sim File Generator Build Passing Language Python

A python program that generates a .sim file from an input Boolean expression.

Dadda Multiplier Build Passing Language Verilog

Applications that implement the fast Dadda multiplier with different compression ratios

5:2 15:4 4:2

Graph Generator Build Ongoing Language Python

A python program that generates a graph from a input Verilog .v file, (structural modelled) or Verilog netlist .vm file.

VLIW Architecture Simulator Build Ongoing Language Verilog

A program that simulates the working of the VLIW Architecture.