

# Sai Kaushik

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Hardware Enthusiast

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### Sai Kaushik S

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[LinkedIn Profile](#) | [Github Profile](#) | [Personal Website](#)

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### Skills

C, C++, Python, Verilog, Bluespec SystemVerilog  
Problem Solving, Leadership skills

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### Education

**Indian Institute of Information Technology, Design & Manufacturing, Kancheepuram, Chennai, Dual Degree (B. Tech + M. Tech) Computer Science and Engineering**

JULY 2018 - PRESENT, CHENNAI

CGPA: 8.79/10

**VVS Sardar Patel PU College, Class 12 (Karnataka State Board)**

PCME

JULY 2016 - APRIL 2018, BANGALORE

Percentage: 93.33%

**Narayana e-Techno School, Class 10 (CBSE Board)**

JULY 2015 - APRIL 2016, BANGALORE

CGPA: 10/10

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### Projects

#### Lorenz Attractor Parallelization Algorithm

C program for visualization of Lorenz Attractor using OpenMP, MPI, CUDA C/C++ and OpenGL.

#### VLIW Architecture Simulation

A python-verilog program that simulates the working of VLIW architecture.

#### Key Distribution Center (Kerberos)

A multi-threaded GUI application for a secure client-server communication using sockets and PyQt5.

### Awards

Participated in Swadeshi Microprocessor Challenge 2020.

Secured 93.5 percentile in GATE CS 2021