Sai Kaushik S

3rd Year CSE Student,
Hardware Enthusiast

Passionate about VLSI Design, Computer Architecture and Reconfigurable Computation.

Actively looking for challenging problems to solve.

Available for long-term internships.

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Sai Kaushik S

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101, Sri Venugopala Nilaya,
2nd Main, Subbanna Garden,
Vijayanagar,
Bangalore, KA – 560 040

Skills

C, C++, Python, Verilog, Arm

Education

July 2018 - Present

Dual Degree (B. Tech + M. Tech)
Computer Science and Engineering
Indian Institute of Information Technology, Design & Manufacturing, Kancheepuram, Chennai
CGPA: 8.76 / 10

July 2016 – April 2018

Class 12 (Karnataka State Board) PCME
VVS Sardar Patel PU College, Bangalore
Percentage: 93.33%

May 2015 – April 2016

Class 10 (CBSE Board)
Narayana e-Techno School, Bangalore
CGPA: 10 / 10

Projects

VLIW Simulator Build Passing Language Verilog

A program that simulates the VLIW Architecture.

Netlist Viewer Build Passing Language Python

A python program that generates a graph from an input Verilog .v file or Verilog netlist .vm file. .v .vm

Sim File Generator Build Passing Language Python

A python program that generates a .sim file from an input Boolean expression.

Dadda Multiplier Build Passing Language Verilog

Applications that implement the fast Dadda multiplier with different compression ratios 5:2 15:4 4:2

Extra-curricular

- Participated in Swadeshi Microprocessor Challenge 2020.
- Secured 93.5 percentile in GATE CS 2021.