



## 1. Description

### 1.1. Project

Project Name	demorun
Board Name	custom
Generated with:	STM32CubeMX 6.15.0
Date	10/26/2025

### 1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F446
MCU name	STM32F446RETx
MCU Package	LQFP64
MCU Pin number	64

### 1.3. Core(s) information

Core(s)	Arm Cortex-M4
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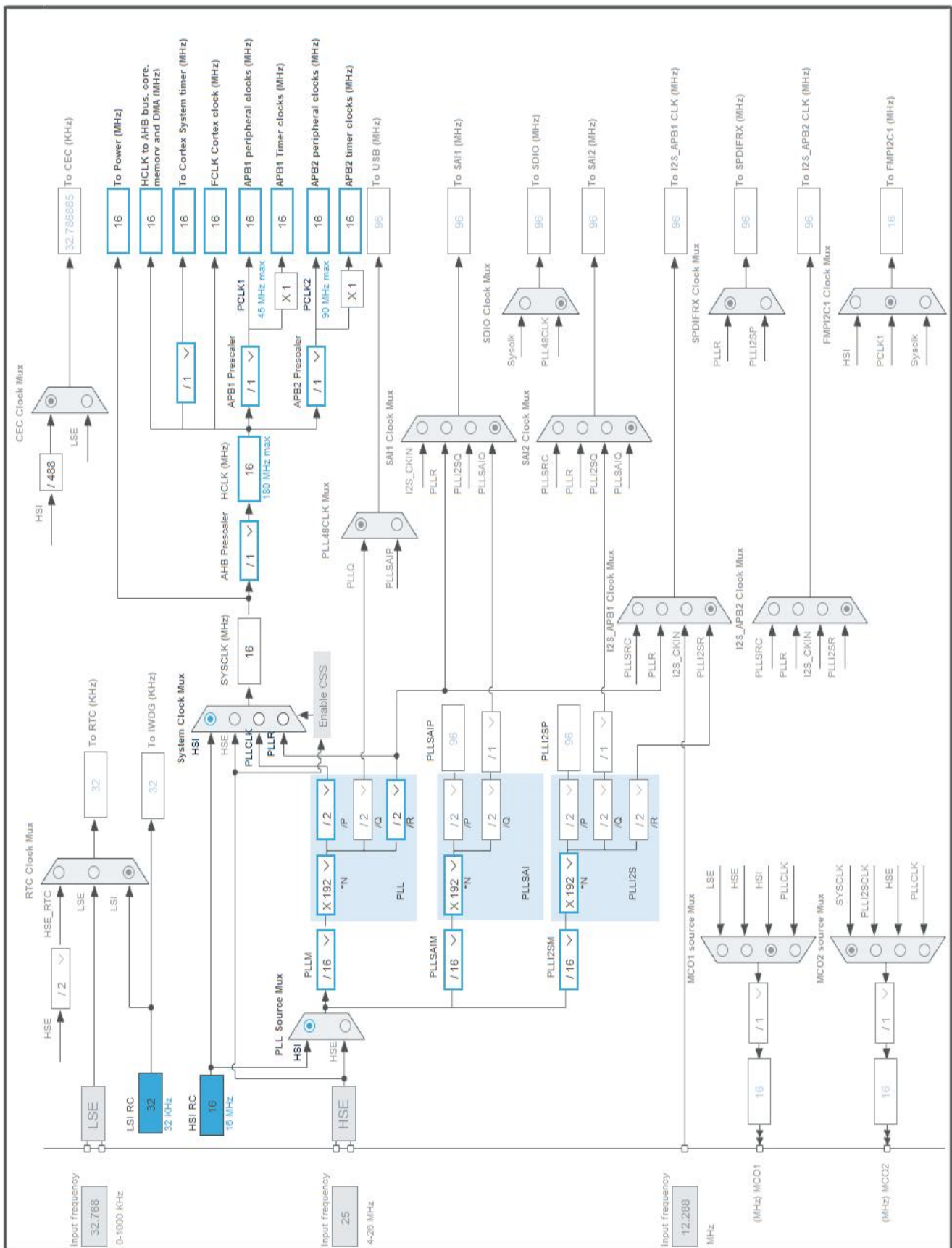


### 3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13	I/O	GPIO_EXTI13	
7	NRST	Reset		
12	VSSA	Power		
13	VDDA	Power		
16	PA2	I/O	USART2_TX	
17	PA3	I/O	USART2_RX	
18	VSS	Power		
19	VDD	Power		
21	PA5 *	I/O	GPIO_Output	
22	PA6	I/O	ADC1_IN6	
26	PB0	I/O	ADC1_IN8	
30	VCAP_1	Power		
31	VSS	Power		
32	VDD	Power		
42	PA9	I/O	USART1_TX	
46	PA13	I/O	SYS_JTMS-SWDIO	
47	VSS	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	
60	BOOT0	Boot		
63	VSS	Power		
64	VDD	Power		

\* The pin is affected with an I/O function

## 4. Clock Tree Configuration



## 1. Power Consumption Calculator report

### 1.1. Microcontroller Selection

Series	STM32F4
Line	STM32F446
MCU	STM32F446RETx
Datasheet	DS10693_Rev6

### 1.2. Parameter Selection

Temperature	25
Vdd	3.3

### 1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

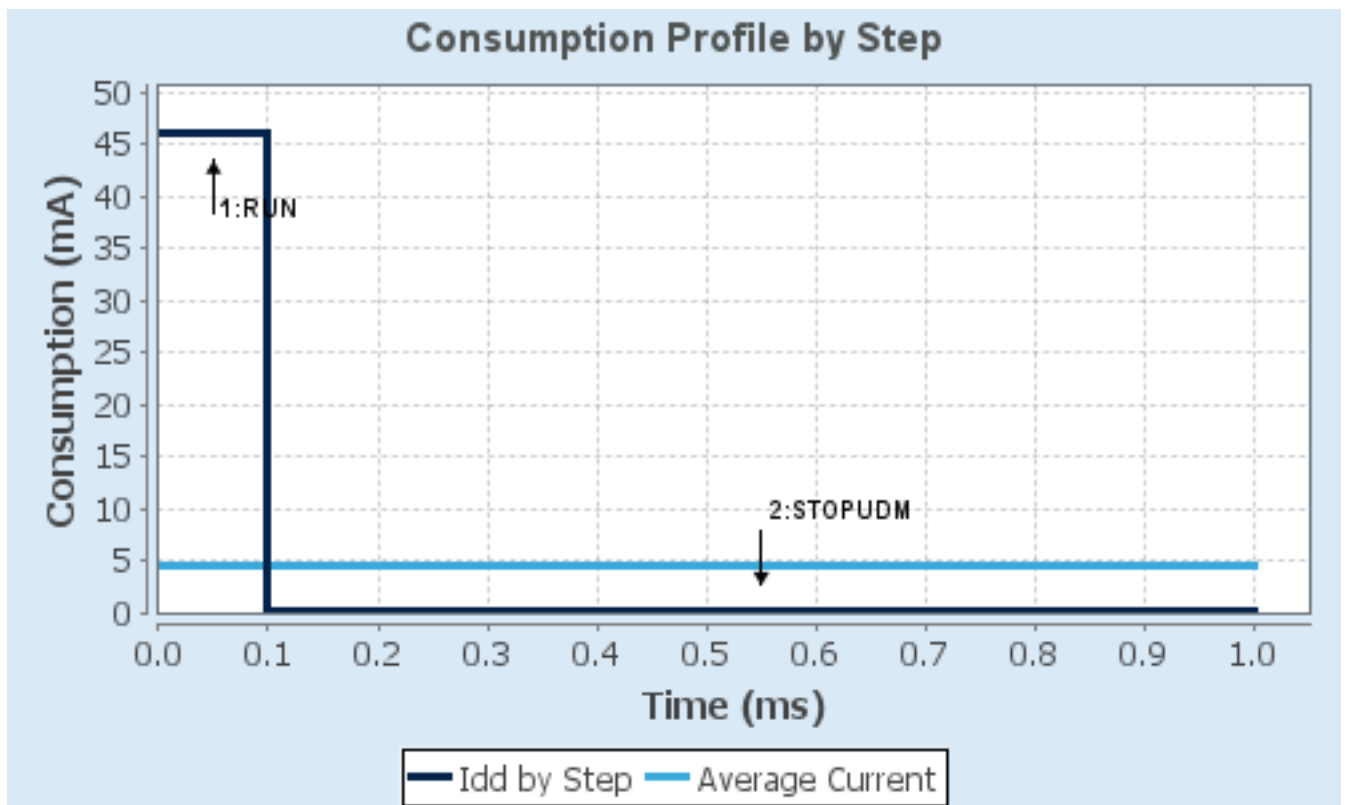
#### 1.4. Sequence

<b>Step</b>	Step1	Step2
<b>Mode</b>	RUN	STOP UDM (Under Drive)
<b>Vdd</b>	3.3	3.3
<b>Voltage Source</b>	Battery	Battery
<b>Range</b>	Scale1-High	No Scale
<b>Fetch Type</b>	RAM/FLASH/REGON/ART/P REFETCH	n/a
<b>CPU Frequency</b>	180 MHz	0 Hz
<b>Clock Configuration</b>	HSE PLL	Regulator LP Flash-PwrDwn
<b>Clock Source Frequency</b>	4 MHz	0 Hz
<b>Peripherals</b>		
<b>Additional Cons.</b>	0 mA	0 mA
<b>Average Current</b>	46 mA	55 $\mu$ A
<b>Duration</b>	0.1 ms	0.9 ms
<b>DMIPS</b>	225.0	0.0
<b>Ta Max</b>	98.02	104.99
<b>Category</b>	In DS Table	In DS Table

#### 1.5. Results

Sequence Time	1 ms	Average Current	4.65 mA
Battery Life	1 month	Average DMIPS	225.0 DMIPS

#### 1.6. Chart





## 2. Software Project

### 2.1. Project Settings

Name	Value
Project Name	demorun
Project Folder	C:\Users\sakku\STM32CubeIDE\workspace_1.14.1\demorun
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.28.3
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

### 2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

### 2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_USART2_UART_Init	USART2
5	MX_ADC1_Init	ADC1
6	MX_USART1_UART_Init	USART1

## 3. Peripherals and Middlewares Configuration

### 3.1. ADC1

mode: IN6

mode: IN8

#### 3.1.1. Parameter Settings:

##### ADCs\_Common\_Settings:

Mode Independent mode

##### ADC\_Settings:

Clock Prescaler

**PCLK2 divided by 8 \***

Resolution

12 bits (15 ADC Clock cycles)

Data Alignment

Right alignment

Scan Conversion Mode

Enabled

Continuous Conversion Mode

**Enabled \***

Discontinuous Conversion Mode

Disabled

DMA Continuous Requests

**Enabled \***

End Of Conversion Selection

EOC flag at the end of single channel conversion

##### ADC\_Regular\_ConversionMode:

Number Of Conversion

**2 \***

External Trigger Conversion Source

Regular Conversion launched by software

External Trigger Conversion Edge

None

Rank

1

Channel

Channel 6

Sampling Time

**84 Cycles \***

Rank

**2 \***

Channel

**Channel 8 \***

Sampling Time

**84 Cycles \***

##### ADC\_Injected\_ConversionMode:

Number Of Conversions

0

##### WatchDog:

Enable Analog WatchDog Mode

false

### 3.2. RCC

#### 3.2.1. Parameter Settings:

##### System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	0 WS (1 CPU cycle)

**RCC Parameters:**

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

**Power Parameters:**

Power Regulator Voltage Scale	Power Regulator Voltage Scale 3
Power Over Drive	Disabled

### 3.3. SYS

**Debug: Serial Wire**

**Timebase Source: SysTick**

### 3.4. USART1

**Mode: Single Wire (Half-Duplex)**

#### 3.4.1. Parameter Settings:

**Basic Parameters:**

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

**Advanced Parameters:**

Data Direction	Receive and Transmit
Over Sampling	16 Samples

### 3.5. USART2

**Mode: Asynchronous**

#### 3.5.1. Parameter Settings:

**Basic Parameters:**

Baud Rate	115200
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Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

**Advanced Parameters:**

Data Direction	Receive and Transmit
Over Sampling	16 Samples

\* User modified value

## 4. System Configuration

### 4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA6	ADC1_IN6	Analog mode	No pull-up and no pull-down	n/a	
	PB0	ADC1_IN8	Analog mode	No pull-up and no pull-down	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
USART1	PA9	USART1_TX	Alternate Function Open Drain	No pull-up and no pull-down	<b>Very High</b> *	
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	
GPIO	PC13	GPIO_EXTI13	<b>External Interrupt Mode with Falling edge trigger detection</b>	No pull-up and no pull-down	n/a	
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

## 4.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA2_Stream0	Peripheral To Memory	Low
USART1_RX	DMA2_Stream2	Peripheral To Memory	Low
USART1_TX	DMA2_Stream7	Memory To Peripheral	Low

### ADC1: DMA2\_Stream0 DMA request Settings:

Mode: **Circular \***  
 Use fifo: Disable  
 Peripheral Increment: Disable  
 Memory Increment: **Enable \***  
 Peripheral Data Width: Half Word  
 Memory Data Width: Half Word

### USART1\_RX: DMA2\_Stream2 DMA request Settings:

Mode: Normal  
 Use fifo: Disable  
 Peripheral Increment: Disable  
 Memory Increment: **Enable \***  
 Peripheral Data Width: Byte  
 Memory Data Width: Byte

### USART1\_TX: DMA2\_Stream7 DMA request Settings:

Mode: Normal  
 Use fifo: Disable  
 Peripheral Increment: Disable  
 Memory Increment: **Enable \***  
 Peripheral Data Width: Byte  
 Memory Data Width: Byte

### 4.3. NVIC configuration

#### 4.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
ADC1, ADC2 and ADC3 interrupts	true	0	0
USART1 global interrupt	true	0	0
EXTI line[15:10] interrupts	true	0	0
DMA2 stream0 global interrupt	true	0	0
DMA2 stream2 global interrupt	true	0	0
DMA2 stream7 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
USART2 global interrupt	unused		
FPU global interrupt	unused		

#### 4.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
ADC1, ADC2 and ADC3 interrupts	false	true	true
USART1 global interrupt	false	true	true
EXTI line[15:10] interrupts	false	true	true
DMA2 stream0 global interrupt	false	true	true

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
DMA2 stream2 global interrupt	false	true	true
DMA2 stream7 global interrupt	false	true	true

\* User modified value



## 5. System Views

### 5.1. Category view

#### 5.1.1. Current

Middleware					
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System Core	Analog	Timers	Connectivity	Multimedia	Computing
DMA ✓	ADC1 ✓		USART1 ✓		
GPIO ✓			USART2 ✓		
IVVIC ✓					
RCC ✓					
SYS ✓					

## 6. Docs & Resources

Type	Link
BSDL files	<a href="https://www.st.com/resource/en/bsdl_model/stm32f446_bsdl.zip">https://www.st.com/resource/en/bsdl_model/stm32f446_bsdl.zip</a>
IBIS models	<a href="https://www.st.com/resource/en/ibis_model/stm32f446_ibis.zip">https://www.st.com/resource/en/ibis_model/stm32f446_ibis.zip</a>
System View Description	<a href="https://www.st.com/resource/en/svd/stm32f4-svd.zip">https://www.st.com/resource/en/svd/stm32f4-svd.zip</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf">https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32_eval_tools_portfolio.pdf">https://www.st.com/resource/en/product_presentation/stm32_eval_tools_portfolio.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf">https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf</a>
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Brochures	<a href="https://www.st.com/resource/en/brochure/products-and-solutions-for-plcs-and-smart-i-os.pdf">https://www.st.com/resource/en/brochure/products-and-solutions-for-plcs-and-smart-i-os.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstm32nucleo.pdf">https://www.st.com/resource/en/flyer/flstm32nucleo.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstm32trust.pdf">https://www.st.com/resource/en/flyer/flstm32trust.pdf</a>
Product Certifications	<a href="https://www.st.com/resource/en/certification_document/stm32_authentication_can.pdf">https://www.st.com/resource/en/certification_document/stm32_authentication_can.pdf</a>
Security Bulletin	<a href="https://www.st.com/resource/en/technical_note/tn1489-security-bulletin-tn1489stpsirt-physical-attacks-on-stm32-and-stm32cube-firmware-stmicroelectronics.pdf">https://www.st.com/resource/en/technical_note/tn1489-security-bulletin-tn1489stpsirt-physical-attacks-on-stm32-and-stm32cube-firmware-stmicroelectronics.pdf</a>
Application Notes	<a href="https://www.st.com/resource/en/application_note/an1709-emc-design-guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf">https://www.st.com/resource/en/application_note/an1709-emc-design-guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf</a>
Application Notes	<a href="https://www.st.com/resource/en/application_note/an2606-stm32-microcontroller-system-memory-boot-mode-stmicroelectronics.pdf">https://www.st.com/resource/en/application_note/an2606-stm32-microcontroller-system-memory-boot-mode-stmicroelectronics.pdf</a>
Application Notes	<a href="https://www.st.com/resource/en/application_note/an2945-stm8s-and-stm32-mcus-a-consistent-832bit-product-line-for-painless-migration-">https://www.st.com/resource/en/application_note/an2945-stm8s-and-stm32-mcus-a-consistent-832bit-product-line-for-painless-migration-</a>

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- Application Notes [https://www.st.com/resource/en/application\\_note/an3070-managing-the-driver-enable-signal-for-rs485-and-iolink-communications-with-the-stm32s-usart-stmicroelectronics.pdf](https://www.st.com/resource/en/application_note/an3070-managing-the-driver-enable-signal-for-rs485-and-iolink-communications-with-the-stm32s-usart-stmicroelectronics.pdf)
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Technical Notes & Articles	<a href="https://www.st.com/resource/en/technical_note/tn1433-reference-device-marking-schematics-for-stm32-microcontrollers-and-microprocessors-stmicroelectronics.pdf">https://www.st.com/resource/en/technical_note/tn1433-reference-device-marking-schematics-for-stm32-microcontrollers-and-microprocessors-stmicroelectronics.pdf</a>
User Manuals	<a href="https://www.st.com/resource/en/user_manual/um3461-stm32f4-series-ulcsaiec-607301603351-selftest-library-user-guide-stmicroelectronics.pdf">https://www.st.com/resource/en/user_manual/um3461-stm32f4-series-ulcsaiec-607301603351-selftest-library-user-guide-stmicroelectronics.pdf</a>