

# The ADC-DAC board

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The purpose of this document is to introduce an add-on card (ADC-DAC board) to be plugged into the Krypton board for capturing analog signals and converting them back to analog form.

## 1 The ADC-DAC board

The ADC-DAC board is used to accept analog signals, convert it to 8-bit digital values (using an ADC) and feed it into the Krypton CPLD board. The processed digital values can be fed back to the board, which will be converted to analog signals using a DAC.

This board contains ADC0804, DAC0808 and an I-to-V converter using LF351. The board has to be inserted into the *HEADER 1* of the Krypton board as shown in Fig. 1. For external connections refer Fig.2. Simplified schematic diagram of ADC-DAC board is shown in Fig.3

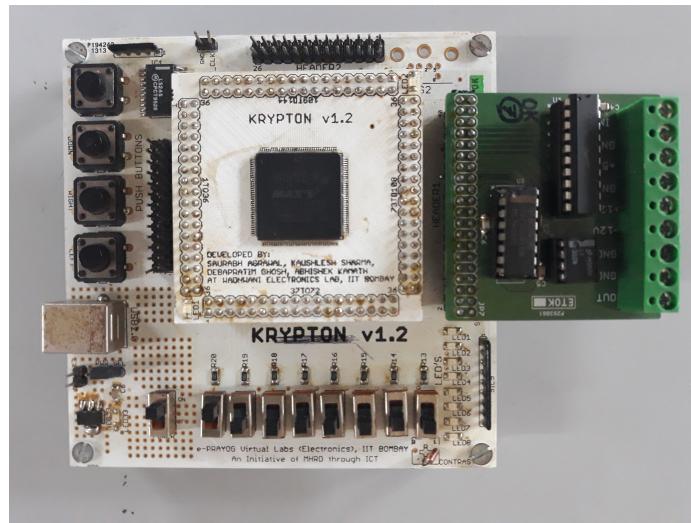


Figure 1: The ADC-DAC board inserted into the HEADER 1 of Krypton board

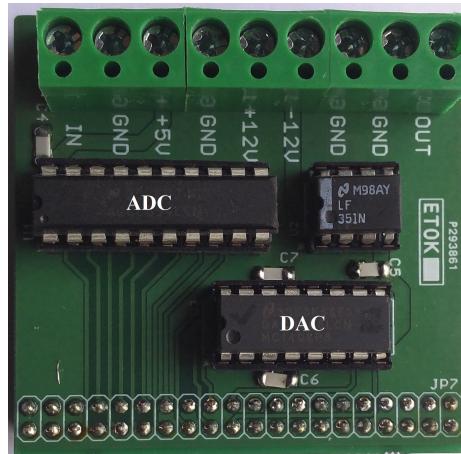


Figure 2: Use screw terminals(top row) for the external connections

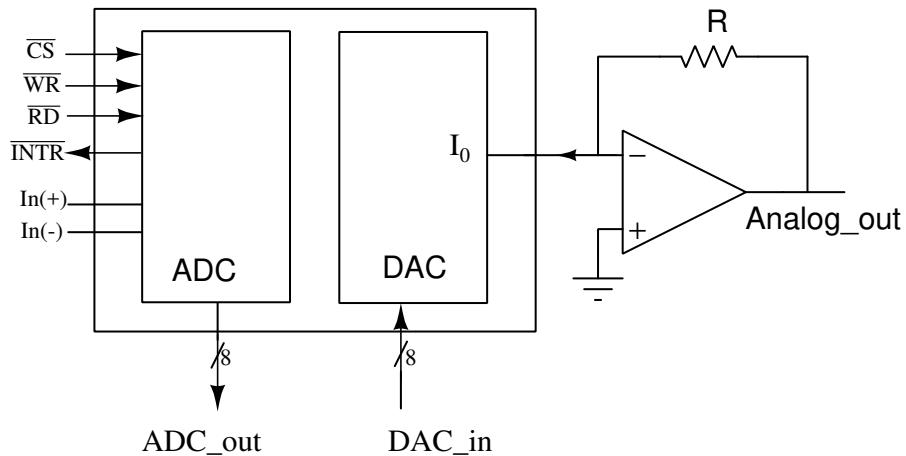


Figure 3: Simplified block diagram of ADC-DAC board

## 2 Interfacing of ADC

ADC interface consists of three incoming control signals to ADC viz.  $\overline{CS}$ ,  $\overline{WR}$ ,  $\overline{RD}$ , and  $\overline{INTR}$  as an outgoing signal. These signals are required to be read or asserted appropriately at appropriate instants by Krypton. Also a clock is required for operation of ADC.

- $\overline{CS}$ (Chip Select): The  $\overline{CS}$  should be low for any of the operations, i.e. to start the conversion or to read the converted data output.
- $\overline{WR}$ (Write): After falling edge on  $\overline{WR}$ , the conversion starts.
- $\overline{RD}$ (Read): After falling edge on  $\overline{RD}$ , we can read the converted data after some delay. Refer Fig.4.

- $\overline{INTR}$ (Interrupt): Falling edge of this signal indicates that the conversion is completed. Refer Fig.4.
- Clock: Clock of 640kHz (generated on this board using RC components)is used.

### 3 Timing diagram of the ADC

The timing diagram for the interfacing of the ADC is shown in Fig.4. In the diagram four timing constraints are shown.

- $\overline{WR}$  should be made low and it should remain low for at least 100ns and thereafter should be made high.
- Delay from falling edge of  $\overline{WR}$  or  $\overline{RD}$  to reset  $\overline{INTR}$  is typically 300 ns.  $\overline{INTR}$  is the control signal from the ADC chip, which indicates end of conversion by sending a signal high to low.
- When  $\overline{RD}$  is made low, the data will be available on the bus after 135 ns. Also when  $\overline{RD}$  is made high, the data will remain on the bus for 125 ns.

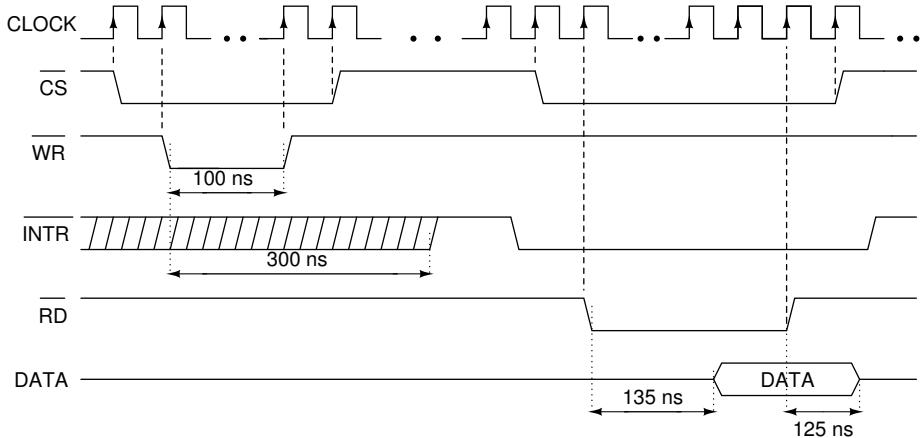


Figure 4: ADC timing diagram

## 4 DAC section

DAC 0808 is an 8 bit parallel DAC that generates current output proportional to the digital input. This current output is converted to voltage using I-V converter using LF351 as shown in Fig.3. The interfacing of DAC does not involve any timing constraints and hence it can directly be connected for digital to analog conversion. The -3dB frequency for DAC (without LF351) is around 800kHz.

## 5 Pin planning for interfacing ADC-DAC card

In Table 1 we show all the interfacing signals and their pin planning required for this board.

ADC Input/Output	Pin no. on the Krypton	DAC Input/Output	Pin no. on the Krypton
$CS$	108		
$RD$	105		
$INTR$	103		
$WR$	107		
ADC_out(0)	106	DAC_in(0)	96
ADC_out(1)	101	DAC_in(1)	79
ADC_out(2)	104	DAC_in(2)	94
ADC_out(3)	97	DAC_in(3)	87
ADC_out(4)	102	DAC_in(4)	88
ADC_out(5)	95	DAC_in(5)	85
ADC_out(6)	98	DAC_in(6)	86
ADC_out(7)	93	DAC_in(7)	81

Table 1: Connections required in the ADC-DAC board(pin planning)

## 6 References

- ADC0804 datasheet
- DAC0808 datasheet
- LF351 datasheet

## 7 Acknowledgement

We thank Prof. M. P. Desai, Madhumita Date and Vineesh V S for their help in writing this document.

## 8 Appendix

