EE 204 : Analog Circuits, Assignment Report

Design of Amplifier and its applications

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Contents

1 Differential Amplifier

1.1 Design methodology

The fundamental circuit for a differential amplifier is as shown below:

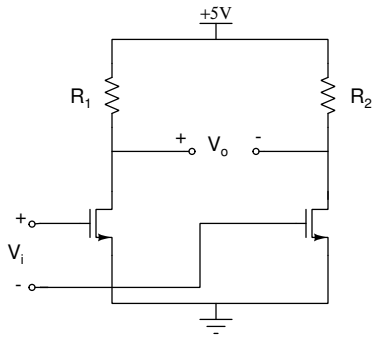


Figure 1: Basic Differential Amplifier

However, with given constraints that no passive loads being used for the design of the amplifier, the resistive loads are then replaced with active loads using PMOS. The equivalent small signal model is as shown:

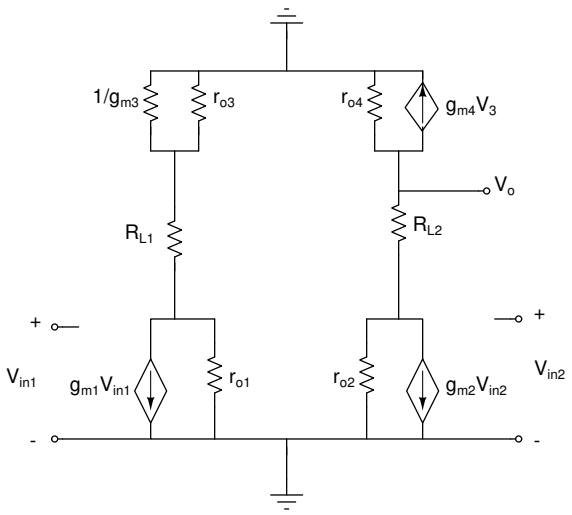


Figure 2: Small signal model of differential Amplifier

Since, the required gain of the amplifier required was about 1000, NMOS are added in the place of load resistors as shown above to increase the gain with appropriate gate bias. A current source needs to be added at the sink of the differential amplifier to bias the circuit and impacts the gain also. Thus, a current mirror circuit (voltage controlled) is implemented as shown below:

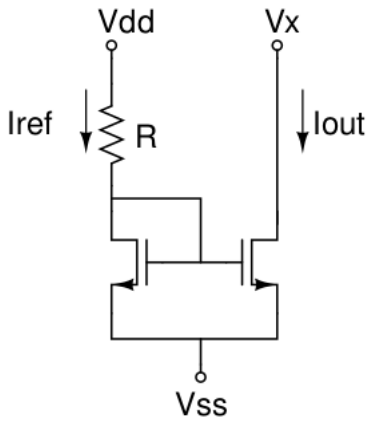


Figure 3: Current mirror

Thus, same current as I_{ref} would flow in other branch which can be easily voltage modulated. The resistor in the mirror circuit is of course replaced by another NMOS with appropriate bias condition.

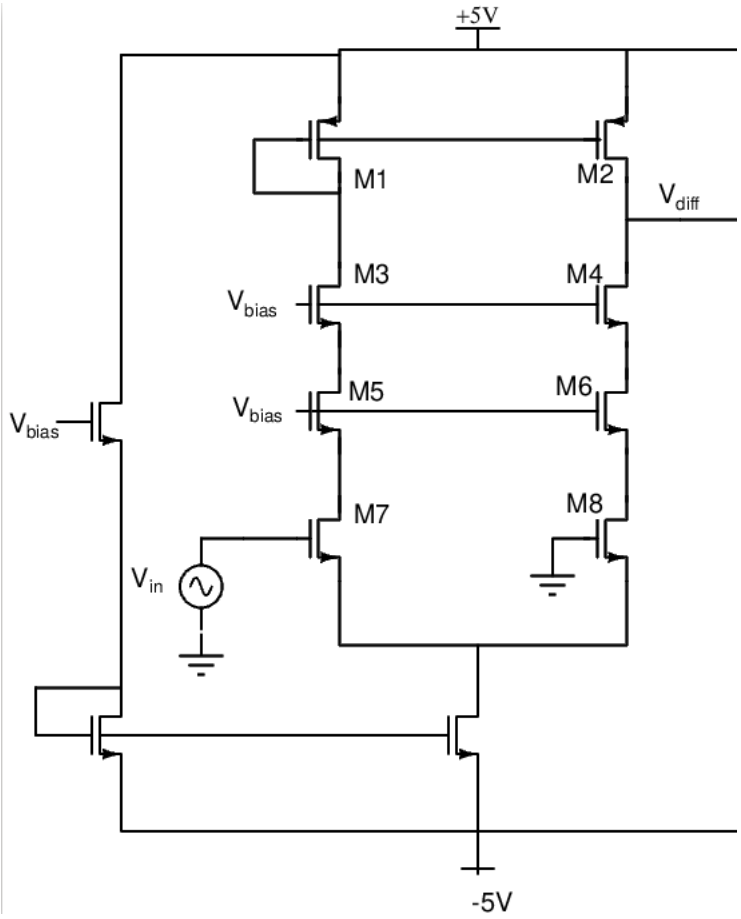


Figure 4: Differential Amplifier circuit

Since too much load was added for the sole reason to increase the gain, the output resistance of this circuit would be very large. Hence, to limit it, this is cascaded with a

source follower.

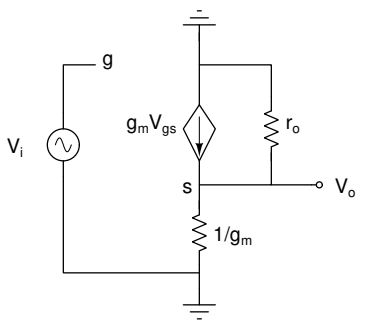


Figure 5: Small signal model of source follower

The load at source is replaced by NMOS as shown below. The gain is given by $\frac{g_m r_o}{1+(g_m+g_{m1})r_o}$, which is almost unity and the output impedance is small ($\frac{1}{g_m}$). The overall circuit is:

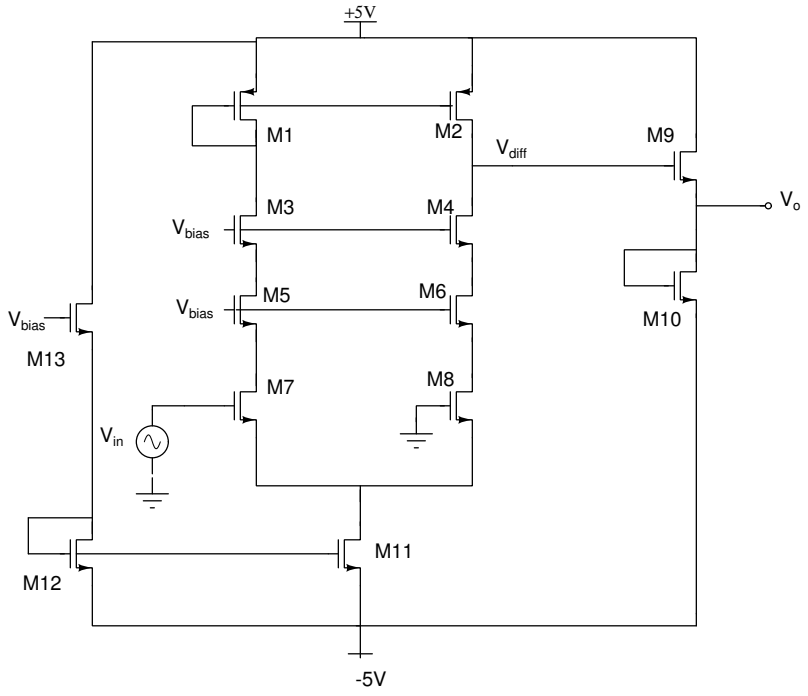


Figure 6: Amplifier circuit

1.2 Simulation

1.2.1 Gain of differential amplifier

The required gain of the amplifier alone in open loop condition should be at least 1000.
Source code to measure gain:

```
*q1_amp
.include tsmc.txt
vdd 1 0 5v
vss 9 0 -5v
```

```
vin1 5 0 ac sin(0 1u 1k 0 0)
vin2 4 0 dc 0V
msf 1 3 15 9 CMOSN W=1m *M9
ms 15 15 9 9 CMOSN W=10u *M10
mr 7 7 1 1 CMOSP W=100u *M13
Vm56 8 0 DC 5V
Vm78 11 0 DC 5V
mt1 2 2 1 1 CMOSP W=50u *M1
mt2 3 2 1 1 CMOSP W=50u *M2
m5 2 8 10 9 CMOSN W=30u *M3
m6 3 8 12 9 CMOSN W=30u *M4
m7 10 11 13 9 CMOSN W=1m *M5
m8 12 11 14 9 CMOSN W=1m *M6
m1 13 4 6 9 CMOSN W=1m *M7
m2 14 5 6 9 CMOSN W=1m *M8
m3 6 7 9 9 CMOSN W=1u *M11
m4 7 7 9 9 CMOSN W=1u *M12
.tran 0.01ms 20ms
.control
run
plot  v(15)- 2.18309 *to display only AC component
hardcopy q1_ampgain v(15)- 2.18309
.endc
.end
```

NOTE: External biases if used are only of 5V..could have been extracted from Vdd directly. Bipolar power supply also used.
When input of $1\mu V$ amplitude sin wave with frequency of 1kHz is applied, the corresponding output observed is as shown below:

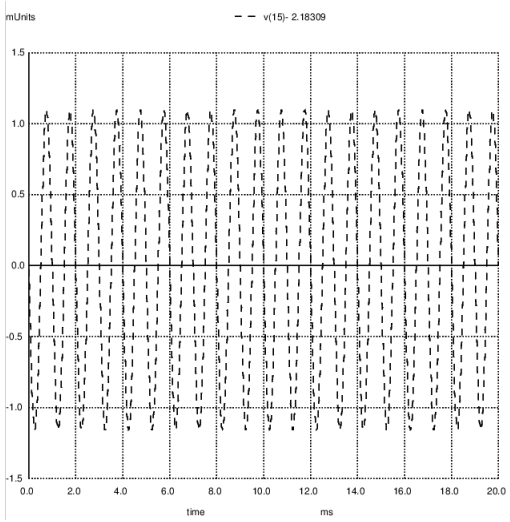


Figure 7: Output of amplifier

The amplitude of output voltage is 1mV and hence gain observed is greater than 1000!!

The corresponding MOS labelled in circuit is also specified in the source code.

1.2.2 Output impedance of amplifier

The input is grounded and a voltage source is connected at the output and current through it was measured to calculate the output impedance of the amplifier.
Source code to measure output impedance:

```
*q1_rout
.include tsmc.txt
vdd 1 0 5v
vss 9 0 -5v
vin1 5 0 dc 0V
vin2 4 0 dc 0V
msf 1 3 15 9 CMOSN W=1m
ms 15 15 9 9 CMOSN W=10u
mr 7 7 1 1 CMOSP W=100u
Vm56 8 0 DC 5V
Vm78 11 0 DC 5V
Vin 15 16 ac sin(0 10u 1k)
Vdummy 16 0 dc 0V
mt1 2 2 1 1 CMOSP W=50u
mt2 3 2 1 1 CMOSP W=50u
m5 2 8 10 9 CMOSN W=30u
m6 3 8 12 9 CMOSN W=30u
m7 10 11 13 9 CMOSN W=1m
m8 12 11 14 9 CMOSN W=1m
m1 13 4 6 9 CMOSN W=1m
m2 14 5 6 9 CMOSN W=1m
m3 6 7 9 9 CMOSN W=1u
m4 7 7 9 9 CMOSN W=1u
.tran 0.01ms 20ms
.control
run
plot I(Vdummy)-0.0581449+2.07317e-08
hardcopy q_imp I(Vdummy)-0.0581449+2.07317e-08
.endc
.end
```

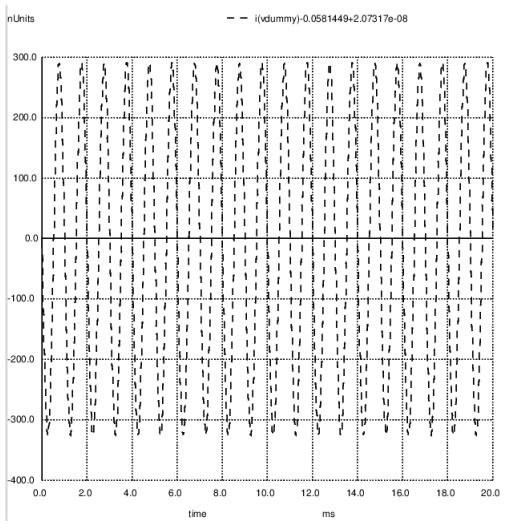


Figure 8: Current through external source connected at output

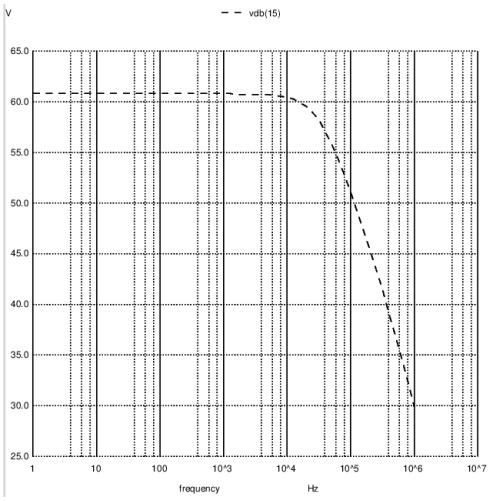
For the maximum current amplitude to be taken as about 300nA, the impedance calculated is 33.33Ω which is less than required value (100Ω).

1.2.3 Bode plot of gain and phase

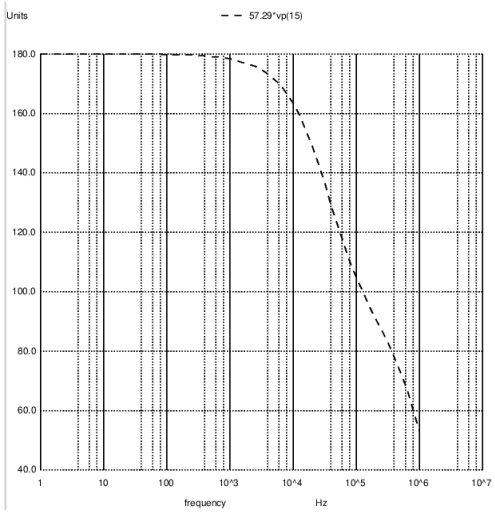
Source code for Bode plot:

```
*q1_bode
.include tsmc.txt
vdd 1 0 5v
vss 9 0 -5v
vin1 5 0 dc 0 ac 1
vin2 4 0 dc 0V
msf 1 3 15 9 CMOSN W=1m
ms 15 15 9 9 CMOSN W=10u
mr 7 7 1 1 CMOSP W=100u
Vm56 8 0 DC 5V
Vm78 11 0 DC 5V
mt1 2 2 1 1 CMOSP W=50u
mt2 3 2 1 1 CMOSP W=50u
m5 2 8 10 9 CMOSN W=30u
m6 3 8 12 9 CMOSN W=30u
m7 10 11 13 9 CMOSN W=1m
m8 12 11 14 9 CMOSN W=1m
m1 13 4 6 9 CMOSN W=1m
m2 14 5 6 9 CMOSN W=1m
m3 6 7 9 9 CMOSN W=1u
m4 7 7 9 9 CMOSN W=1u
.ac dec 10 1 1Meg
.control
run
```

```
plot vdb(15) xlog
plot {57.29*vp(15)} xlog
hardcopy gain vdb(15) xlog
hardcopy phase {57.29*vp(15)} xlog
.endc
.end
```



(a) Gain in (dB) vs frequency in log scale



(b) Phase in degrees vs frequency in log scale

The pass band gain is 60.76dB and the cut-off frequency measured 3dB below from pass-band is 349.74kHz. The gain-bandwidth product is 2.12×10^7.

1.2.4 Inverting Amplifier

The following circuit is implemented using the amplifier designed above:

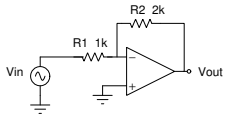


Figure 10: Inverting Amplifier

Source code for Inverting Amplifier:

```
*q1_opamp
*.subckt 4 5 15 opamp
.include tsmc.txt
vdd 1 0 5v
vss 9 0 -5v
*vin1 5 0 ac sin(0 10u 1k 0 0)
vin2 4 0 dc 0V
```

```
*4: non inv inp
*5: inv inp
*15: output
r1 5 16 1k
r2 5 15 2k
Vin 16 0 ac sin(0 10u 1k)
msf 1 3 15 9 CMOSN W=1m
ms 15 15 9 9 CMOSN W=10u
mr 7 7 1 1 CMOSP W=100u
Vm56 8 0 DC 5V
Vm78 11 0 DC 5V
mt1 2 2 1 1 CMOSP W=50u
mt2 3 2 1 1 CMOSP W=50u
m5 2 8 10 9 CMOSN W=30u
m6 3 8 12 9 CMOSN W=30u
m7 10 11 13 9 CMOSN W=1m
m8 12 11 14 9 CMOSN W=1m
m1 13 4 6 9 CMOSN W=1m
m2 14 5 6 9 CMOSN W=1m
m3 6 7 9 9 CMOSN W=1u
m4 7 7 9 9 CMOSN W=1u
.tran 0.01ms 5ms
.control
run
plot  v(15)-0.0141059 V(16)
hardcopy invamp v(15)-0.0141059 V(16)
.endc
.end
```

The output plot obtained is as shown below:

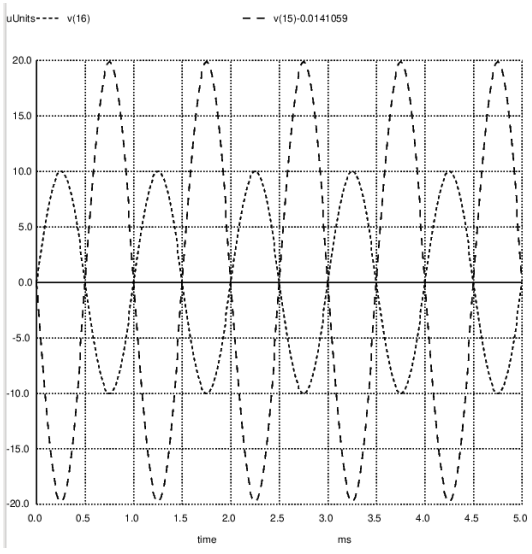


Figure 11: Inverting Amplifier Input and Output voltage waveforms

It is clearly seen that the gain very close to -2.

1.2.5 Bode plot of gain and frequency of Inverting Amplifier

Source code for Inverting Amplifier Bode plot:

```
*q1_opamp
.include tsmc.txt
vdd 1 0 5v
vss 9 0 -5v
*vin1 5 0 dc 0 ac 1
vin2 4 0 dc 0V
*4: non inv inp
*5: inv inp
*15: output
r1 5 16 1k
r2 5 15 2k
Vin 16 0 dc 0 ac 1
msf 1 3 15 9 CMOSN W=1m
ms 15 15 9 9 CMOSN W=10u
mr 7 7 1 1 CMOSP W=100u
Vm56 8 0 DC 5V
Vm78 11 0 DC 5V
mt1 2 2 1 1 CMOSP W=50u
mt2 3 2 1 1 CMOSP W=50u
m5 2 8 10 9 CMOSN W=30u
m6 3 8 12 9 CMOSN W=30u
m7 10 11 13 9 CMOSN W=1m
m8 12 11 14 9 CMOSN W=1m
m1 13 4 6 9 CMOSN W=1m
m2 14 5 6 9 CMOSN W=1m
m3 6 7 9 9 CMOSN W=1u
m4 7 7 9 9 CMOSN W=1u
.ac dec 10 1 1Meg
.control
run
plot vdb(15) xlog
hardcopy opgain vdb(15) xlog
.endc
.end
```

The obtained bode plot is as shown below:

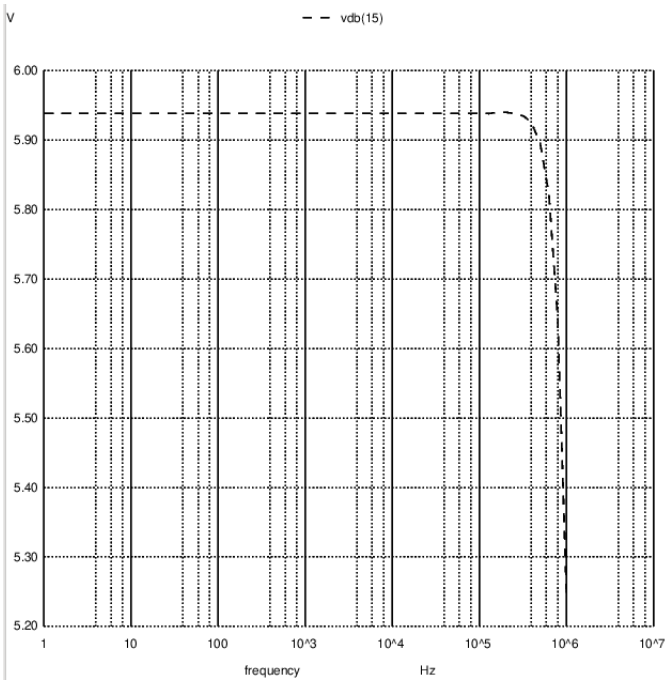


Figure 12: Gain in (dB) vs frequency in log scale

The pass band gain is 5.94dB and the cut-off frequency measured 3dB below from pass-band is 3.7MHz. The gain-bandwidth product is 2.19×10^7 (close to the previously calculated product)

2 Design of Filters

2.1 Low Pass Filter

2.1.1 Design

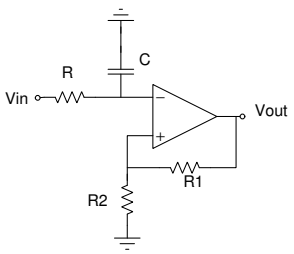


Figure 13: Low pass filter circuit

The transfer function of this filter is $\frac{1}{RCs+1}(1+\frac{R_2}{R_1})$. For a cut-off frequency of 1kHz = $\frac{1}{2\pi RC}$, R=10kΩ and C=16nF were selected. Using $R_1 = 1k\Omega$ and $R_2 = 2.163k\Omega$, the pass-band gain was set to 10dB.

2.1.2 Simulation

Source code for Low Pass filter:

```
*q2_lpf
.include tsmc.txt
vdd 1 0 5v
vss 9 0 -5v
*vin1 5 0 ac sin(0 10u 1k 0 0)
*vin2 4 0 dc 0V
*4: non inv inp
*5: inv inp
*15: output
r 4 16 10k
C 4 0 16n
Vin 16 0 dc 0 ac 1
r1 5 0 1k
r2 5 15 2.163k
msf 1 3 15 9 CMOSN W=1m
ms 15 15 9 9 CMOSN W=10u
mr 7 7 1 1 CMOSP W=100u
Vm56 8 0 DC 5V
Vm78 11 0 DC 5V
mt1 2 2 1 1 CMOSP W=50u
mt2 3 2 1 1 CMOSP W=50u
m5 2 8 10 9 CMOSN W=30u
m6 3 8 12 9 CMOSN W=30u
m7 10 11 13 9 CMOSN W=1m
```

```
m8 12 11 14 9 CMOSN W=1m
m1 13 4 6 9 CMOSN W=1m
m2 14 5 6 9 CMOSN W=1m
m3 6 7 9 9 CMOSN W=1u
m4 7 7 9 9 CMOSN W=1u
.ac dec 10 1 1Meg
.control
run
plot vdb(15) xlog
hardcopy lpf vdb(15) xlog
.endc
.end
```

The obtained bode plot is as shown below:

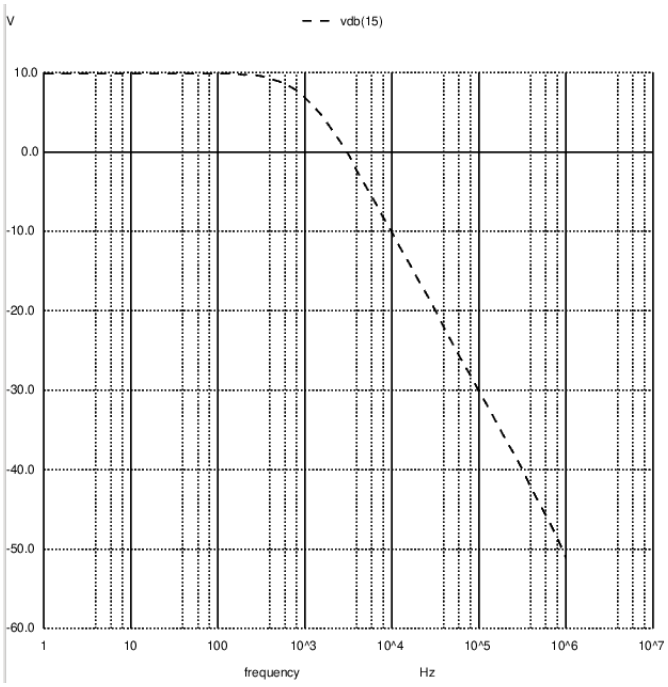


Figure 14: Gain in (dB) vs frequency in log scale

The pass-band gain is 10dB and the cut-off frequency (3dB below passband) is 1kHz.

2.2 High Pass Filter

2.2.1 Design

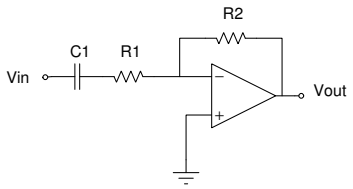


Figure 15: High pass filter circuit

The transfer function of this filter is $\frac{1}{R_2C_1s+1}(R_1C_1s+1)$. For a cut-off frequency of 10kHz $= \frac{1}{2\pi R_1 C}$, C=1.6nF was selected. Using $R_1 = 10k\Omega$ and $R_2 = 30k\Omega$, the pass-band gain was set to 10dB.

2.2.2 Simulation

Source code for High Pass filter:

```
*q2_hpf
.include tsmc.txt
vdd 1 0 5v
vss 9 0 -5v
*vin1 5 0 ac sin(0 10u 1k 0 0)
vin2 4 0 dc 0V
*4: non inv inp
*5: inv inp
*15: output
C 16 17 1.6nF
Vin 17 0 dc 0 ac 1
r1 5 16 10k
r2 5 15 30k
msf 1 3 15 9 CMOSN W=1m
ms 15 15 9 9 CMOSN W=10u
mr 7 7 1 1 CMOSP W=100u
Vm56 8 0 DC 5V
Vm78 11 0 DC 5V
mt1 2 2 1 1 CMOSP W=50u
mt2 3 2 1 1 CMOSP W=50u
m5 2 8 10 9 CMOSN W=30u
m6 3 8 12 9 CMOSN W=30u
m7 10 11 13 9 CMOSN W=1m
m8 12 11 14 9 CMOSN W=1m
m1 13 4 6 9 CMOSN W=1m
m2 14 5 6 9 CMOSN W=1m
m3 6 7 9 9 CMOSN W=1u
```

```
m4 7 7 9 9 CMOSN W=1u
.ac dec 10 1 1Meg
.control
run
plot vdb(15) xlog
hardcopy hpf vdb(15) xlog
.endc
.end
```

The obtained bode plot is as shown below:

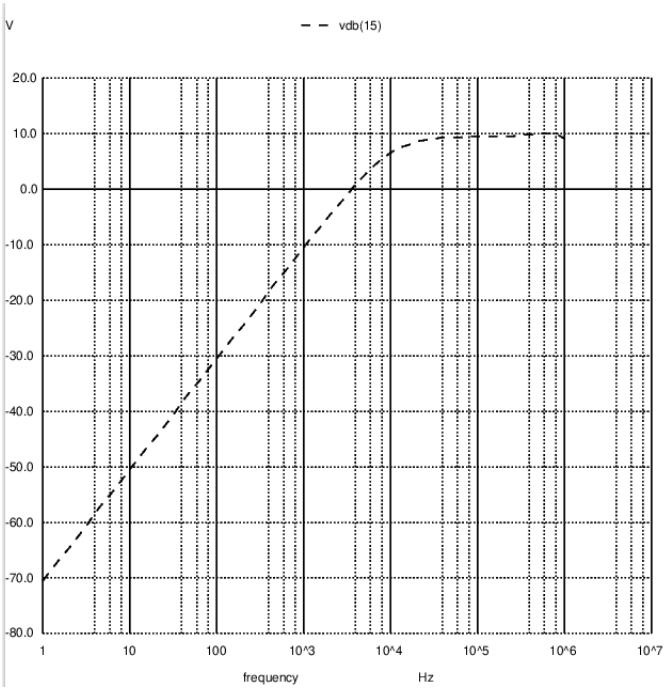


Figure 16: Gain in (dB) vs frequency in log scale

The pass-band gain is 10dB and the cut-off frequency (3dB below passband) is 10kHz.

2.3 Band Pass Filter

2.3.1 Design

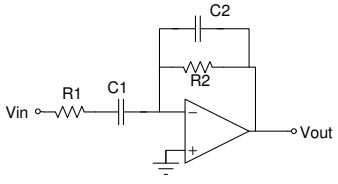


Figure 17: Band pass filter circuit

The transfer function of this filter is $\frac{-sC_1R_2}{(1+sC_1R_1).(1+sC_2R_2)}$. For a cut-off frequency of 1kHz = $\frac{1}{2\pi R_1C_1}$, $R_1 = 6.4k\Omega$ and C=25nF and for 10kHz = = $\frac{1}{2\pi R_2C_2}$, $R_1 = 16k\Omega$ and C=1nF were selected.

2.3.2 Simulation

Source code for Band Pass filter:

```
*q2_bpf
.include tsmc.txt
vdd 1 0 5v
vss 9 0 -5v
*vin1 5 0 ac sin(0 10u 1k 0 0)
*vin2 4 0 dc 0V
*4: non inv inp
*5: inv inp
*15: output
C1 5 16 25n
Vin 4 0 dc 0 ac 1
r1 16 0 6.4k
r2 5 15 16k
c2 5 15 1n
msf 1 3 15 9 CMOSN W=1m
ms 15 15 9 9 CMOSN W=10u
mr 7 7 1 1 CMOSP W=100u
Vm56 8 0 DC 5V
Vm78 11 0 DC 5V
mt1 2 2 1 1 CMOSP W=50u
mt2 3 2 1 1 CMOSP W=50u
m5 2 8 10 9 CMOSN W=30u
m6 3 8 12 9 CMOSN W=30u
m7 10 11 13 9 CMOSN W=1m
m8 12 11 14 9 CMOSN W=1m
m1 13 4 6 9 CMOSN W=1m
m2 14 5 6 9 CMOSN W=1m
m3 6 7 9 9 CMOSN W=1u
m4 7 7 9 9 CMOSN W=1u
.ac dec 10 1 1Meg
.control
run
plot vdb(15) xlog
hardcopy bpf vdb(15) xlog
.endc
.end
```

The obtained bode plot is as shown below:

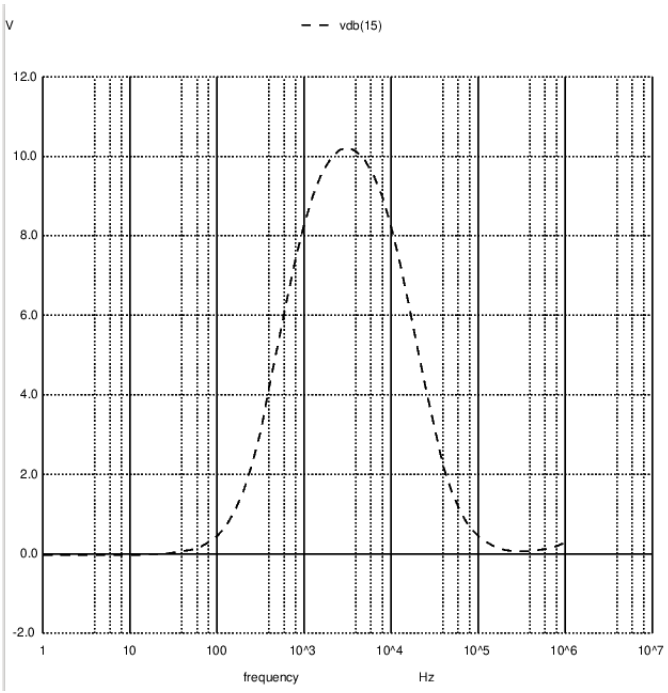


Figure 18: Gain in (dB) vs frequency in log scale

The pass-band gain is almost 10dB and the cut-off frequencies (3dB below passband) are close to 1kHz and 10kHz. Bandwidth observed is slightly higher than that expected.

3 Wein-Bridge Oscillator

3.1 Design

The previously designed amplifier is used to design the oscillator, the circuit for which is shown below:

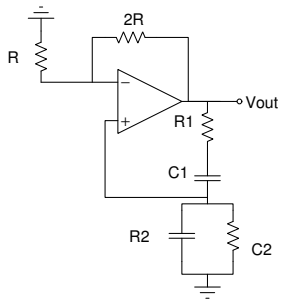


Figure 19: circuit for wein-bridge oscillator

The feedback gain for this circuit is given by $\beta = \frac{R_2C_1s}{R_1R_2C_1C_2s^2+s(R_1C_1+R_2C_2+R_2C_1)+1}$. If $R_1 = R_2$ and $C_1 = C_2$, then $\beta = \frac{1}{3}$, hence A $= 3 = 1 + \frac{2R}{R}$.
The oscillatory frequency is $\frac{1}{2\pi R_1C_1}$. Hence, $R_1 = 10k\Omega$ and C_1 =16nF chosen.

3.2 Simulation

Source code for Wein-Bridge oscillator:

```
*q3_wien
.include tsmc.txt
vdd 1 0 5v
vss 9 0 -5v
vin 17 0 sin(0 10n 5000k) *Noise
r1 5 17 1k
r2 5 15 2k
rc1 15 16 10k
cr1 16 4 15.9155n
rc2 4 0 10k
cr2 4 0 15.9155n
msf 1 3 15 9 CMOSN W=1m
ms 15 15 9 9 CMOSN W=10u
mr 7 7 1 1 CMOSP W=100u
Vm56 8 0 DC 5V
Vm78 11 0 DC 5V
mt1 2 2 1 1 CMOSP W=50u
mt2 3 2 1 1 CMOSP W=50u
m5 2 8 10 9 CMOSN W=30u
m6 3 8 12 9 CMOSN W=30u
m7 10 11 13 9 CMOSN W=1m
```

```
m8 12 11 14 9 CMOSN W=1m
m1 13 4 6 9 CMOSN W=1m
m2 14 5 6 9 CMOSN W=1m
m3 6 7 9 9 CMOSN W=1u
m4 7 7 9 9 CMOSN W=1u
.tran 0.01ms 5ms
.control
run
plot  v(15)
hardcopy wein v(15)
.endc
.end
```

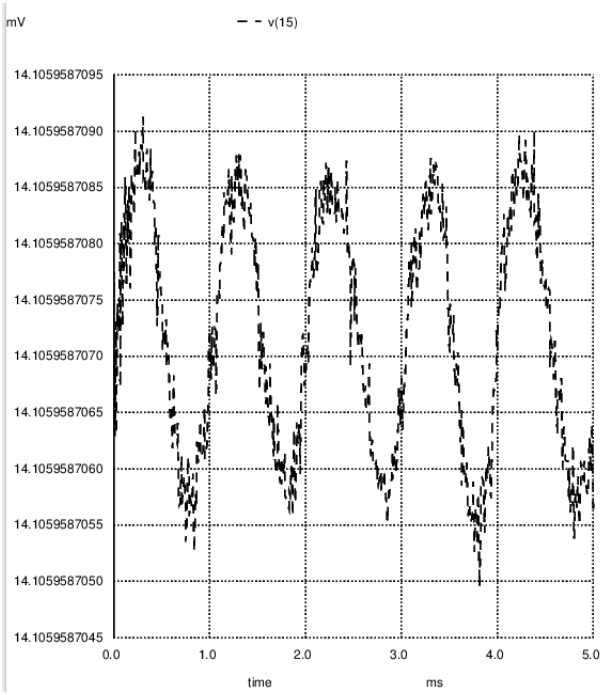


Figure 20: Output waveform

The Oscillatory time period is observed to be almost 1ms or frequency = 1kHz. Since high frequency noise was deliberately added without which oscillations weren't observed and hence, such distortions were expected to be observed.

4 Cross-coupled Oscillator

4.1 Design

The previously designed amplifier is modified and L-C filters are added to obtain the given circuit:

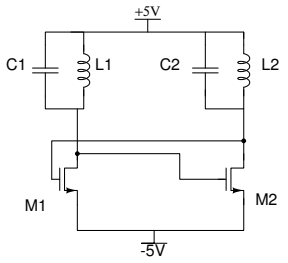


Figure 21: Cross-coupled oscillator circuit

The circuit oscillates at resonant frequency $= \frac{1}{2\pi\sqrt{LC}}$. Since, the circuit desgined should oscillate at 1kHz, L=2.533mH and C=10μF are chosen.

4.2 Simulation

Source code for cross-coupled oscillator:

```
*q4
.include tsmc.txt
vdd 1 0 5v
vss 9 0 -5v
mr 7 7 1 1 CMOSP W=100u
l1 1 13 2.533m
c1 1 13 10u
l2 1 14 2.533m
c2 1 14 10u
m1 13 14 6 9 CMOSN W=1m
m2 14 13 6 9 CMOSN W=1m
m3 6 7 9 9 CMOSN W=1u
m4 7 7 9 9 CMOSN W=1u
.tran 0.01ms 5ms
.control
run
plot  v(14)
hardcopy q4 v(14)
.endc
.end
```

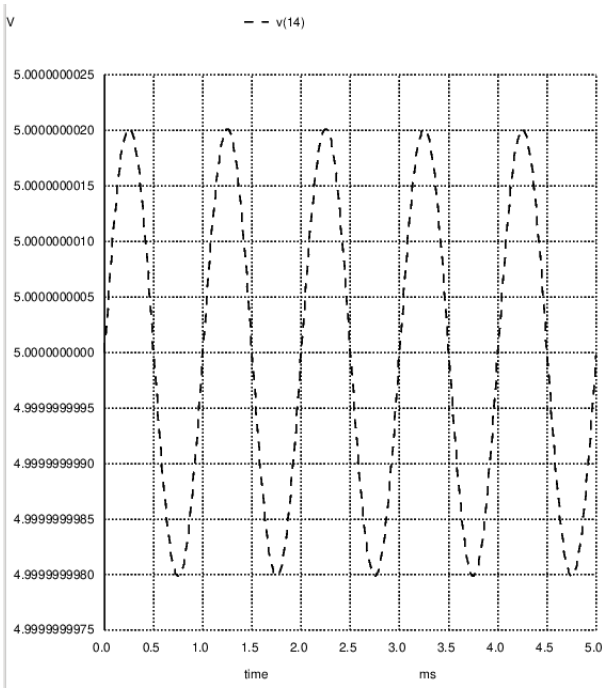


Figure 22: Output waveform

The Oscillatory time period is observed to be almost 1ms or frequency = 1kHz.

5 Negative differential Resistor

5.1 Design

Using the amplifier designed before, the below feedback connection is made to obtain negative differential resistance:

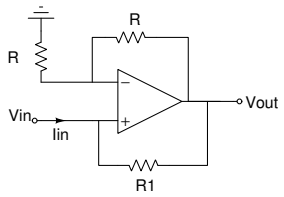


Figure 23: Negative Differential resistance circuit

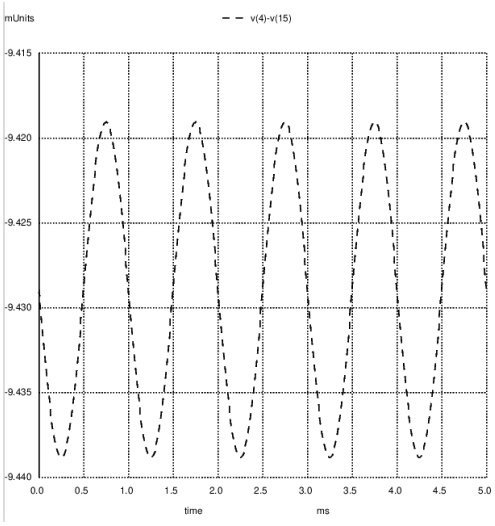
Thus, in this case, $V_{out} = V_{in}.(1 + \frac{R}{R})$. $I_{in} = \frac{V_{in} - Vout}{R_1}$.
Hence, $\frac{V_{in}}{I_{in}} = -2R_1 = R_{in}$. Here, for simulation R = $R_1 = 1k\Omega$ are used.

5.2 Simulation

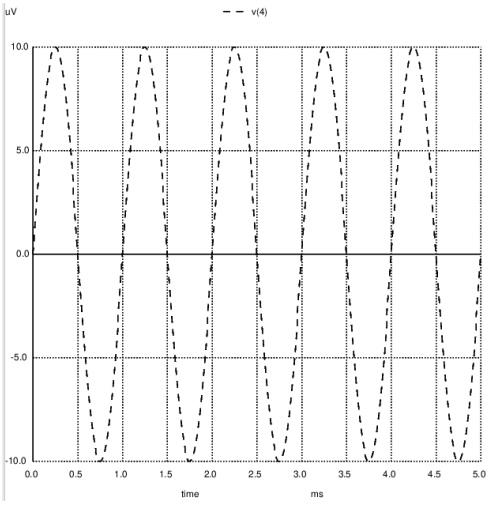
Source code for Negative differential Resistor:

```
*q5
.include tsmc.txt
vdd 1 0 5v
vss 9 0 -5v
*vin1 5 0 ac sin(0 10u 1k 0 0)
*vin2 4 0 dc 0V
*4: non inv inp
*5: inv inp
*15: output
r1 5 15 1k
r2 5 0 1k
r3 4 15 1k
Vin 4 0 ac sin(0 10u 1k)
msf 1 3 15 9 CMOSN W=1m
ms 15 15 9 9 CMOSN W=10u
mr 7 7 1 1 CMOSP W=100u
Vm56 8 0 DC 5V
Vm78 11 0 DC 5V
mt1 2 2 1 1 CMOSP W=50u
mt2 3 2 1 1 CMOSP W=50u
m5 2 8 10 9 CMOSN W=30u
m6 3 8 12 9 CMOSN W=30u
m7 10 11 13 9 CMOSN W=1m
m8 12 11 14 9 CMOSN W=1m
```

```
m1 13 4 6 9 CMOSN W=1m
m2 14 5 6 9 CMOSN W=1m
m3 6 7 9 9 CMOSN W=1u
m4 7 7 9 9 CMOSN W=1u
.tran 0.01ms 5ms
.control
run
plot V(4)-V(15)
plot V(4)
hardcopy current V(4)-V(15)
hardcopy voltage V(4)
.endc
.end
```



(a) Voltage across resistor R_1 which is directly proportional to current



(b) Input voltage

It is clearly seen that the input current and voltage are out of phase as though the circuit block is behaving as a negative resistance. The ac current amplitude passing through R is 9.8nA and hence equivalent resistance of the entire block is -2.04kΩ which is almost twice that of R_1 as expected.