

EE224 Course Project

Design of a multi cycle processor, IITBProc

This is the complete design document containing the state diagrams for all the instructions and the complete entity.

-Submitted by

Anugole Sai Gaurav(170070008)

Jayesh Choudhary(170070038)

Vishesh Verma(170070039)

Saksham Khandelwal(170070024)

ADD

Date:

youvλ

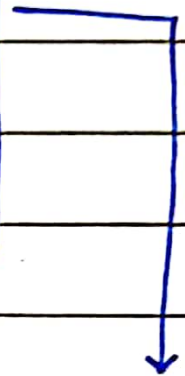
IP \rightarrow MEM_A
MEM_D \rightarrow IR

S₀



IR₁₁₋₉ \rightarrow RF_A1
RF_D1 \rightarrow T1
IR₈₋₆ \rightarrow RF_A2
RF_D2 \rightarrow T2

S₁



if C=1 T_c=1
if T₃=0 T₂=1

S₃



T1 \rightarrow ALU_A
T2 \rightarrow ALU_B
ALU_C \rightarrow T3

S₂

add



IR₅₋₃ \rightarrow RF_A3
T3 \rightarrow RF_D3

S₄



IP \rightarrow ALU_A
+1 \rightarrow ALU_B
ALU_C \rightarrow IP

S₅

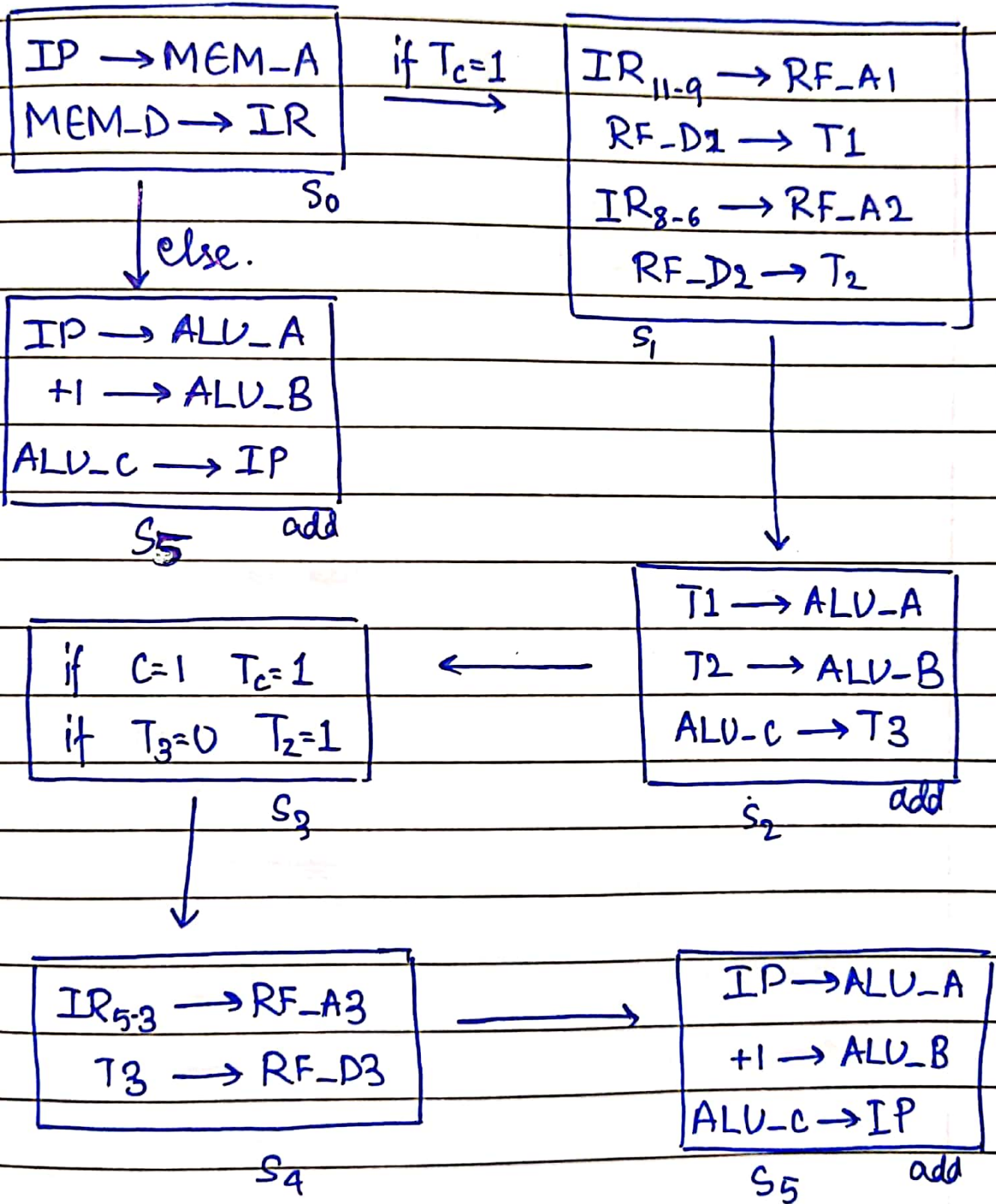
add

ADC

Page No.:

Date:

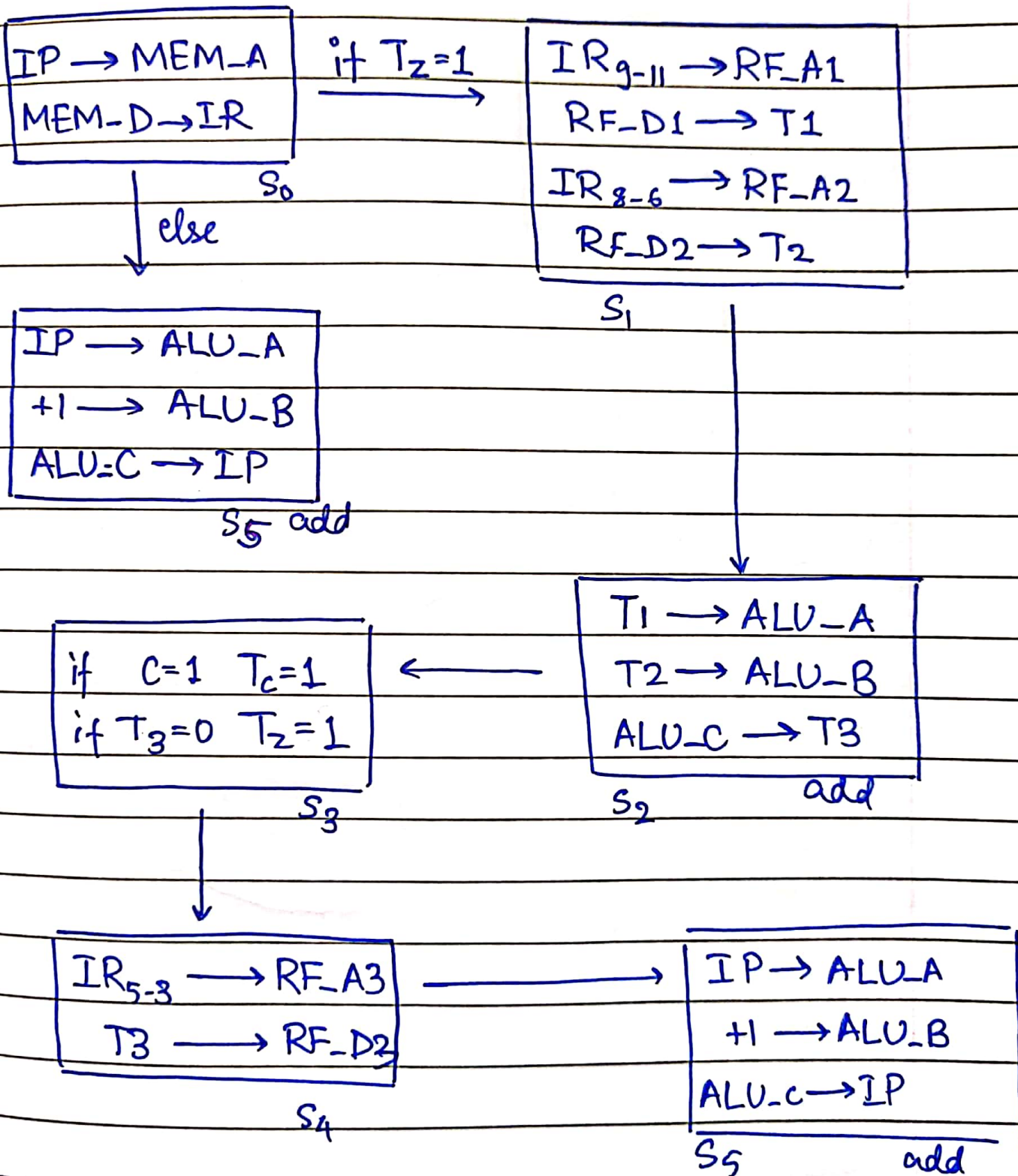
youva



ADZ

Date:

YOUVA



ADI

IP → MEM_A
MEM_D → IR

S₀



IR₁₁₋₉ → RF_A1
RF_D1 → T1
IR₅₋₀ → SEID → T2

S₁



T1 → ALU_A
T2 → ALU_B
ALU_C → T3

S₂

add



if C=1 T_c=1
if T3=0 T_z=1

S₃



IR₈₋₆ → RF_A3
T3 → RF_D3

S₄



IP → ALU_A
+1 → ALU_B
ALU_C → IP

S₅

add

NDU

Page No.:

YOUVA

Date:

IP \rightarrow MEM_A
MEM_D \rightarrow IR

S₀



IR₁₁₋₉ \rightarrow RF_A1
RF_D1 \rightarrow T1
IR₈₋₆ \rightarrow RF_A2
RF_D2 \rightarrow T2

S₁



if T₃ = 0
T₂ = 1

S₀



T1 \rightarrow ALU_A
T2 \rightarrow ALU_B
ALU_C \rightarrow T3

S₉

nand

IR₅₋₃ \rightarrow RF_A3
T3 \rightarrow RF_D3

S₄



IP \rightarrow ALU_A
+1 \rightarrow ALU_B
ALU_C \rightarrow IP

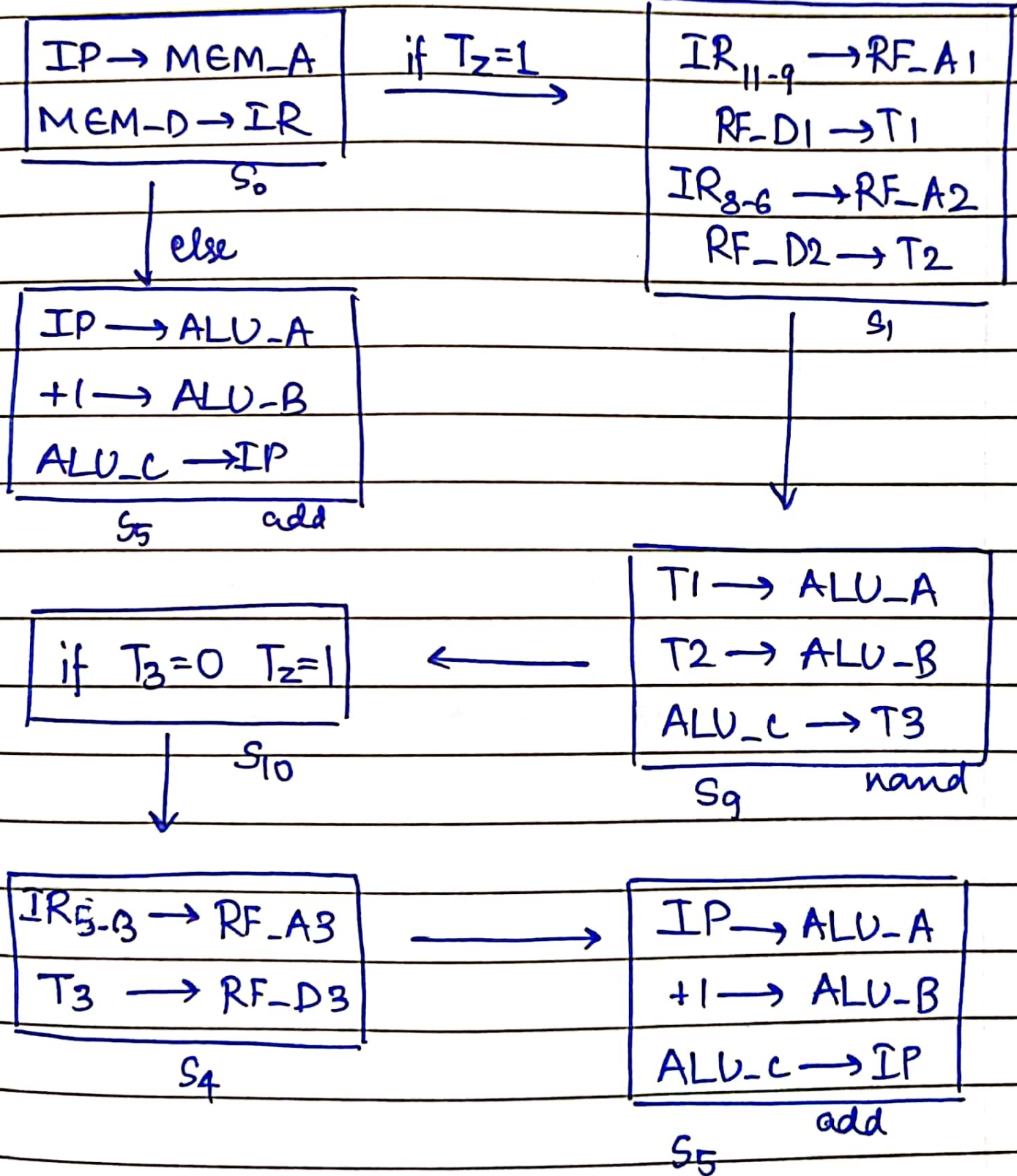
S₅

add

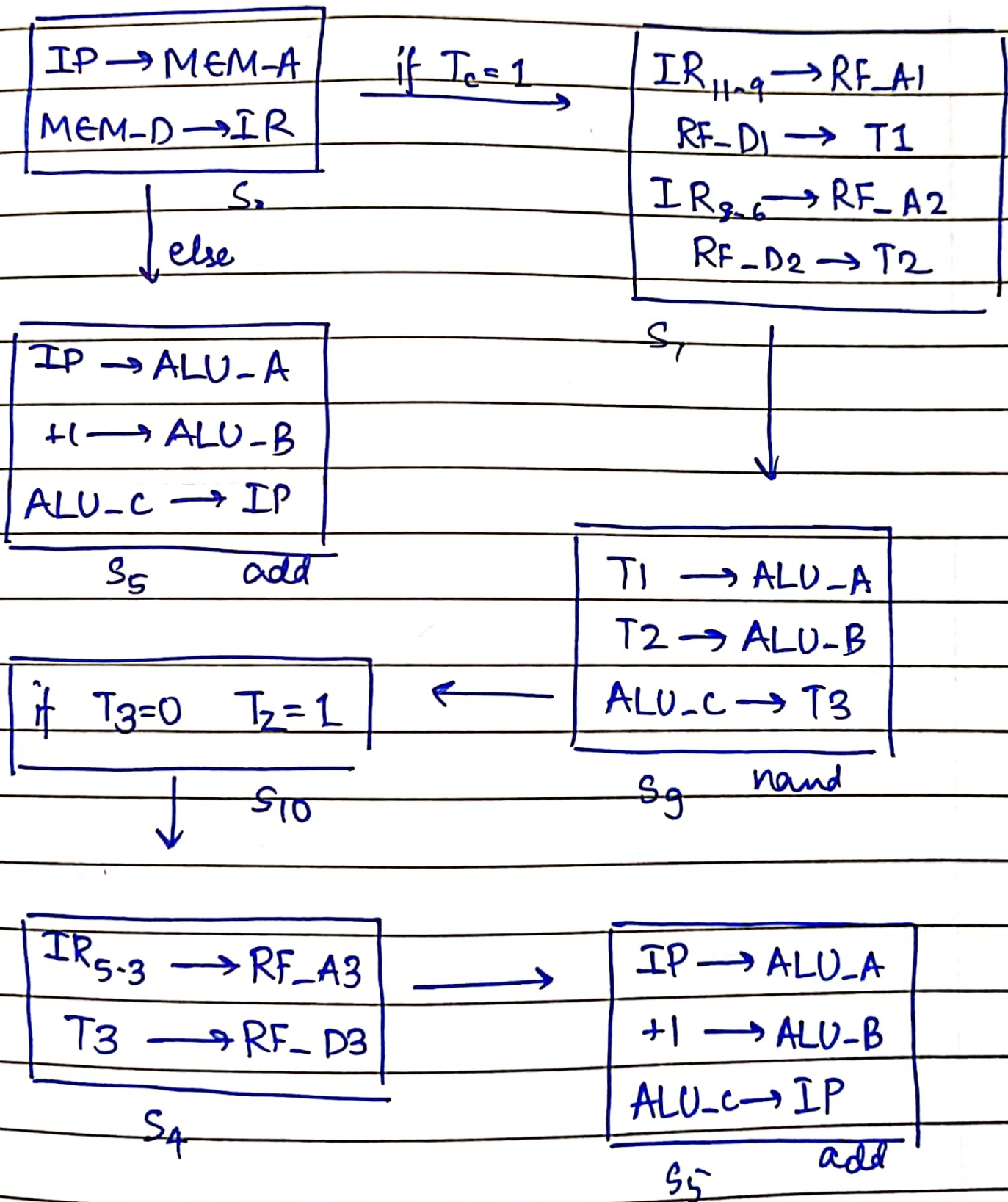
NDZ

Date:

youva

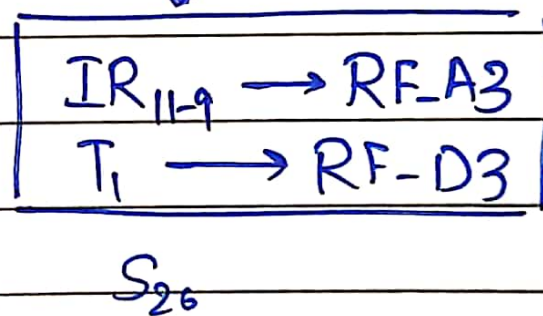
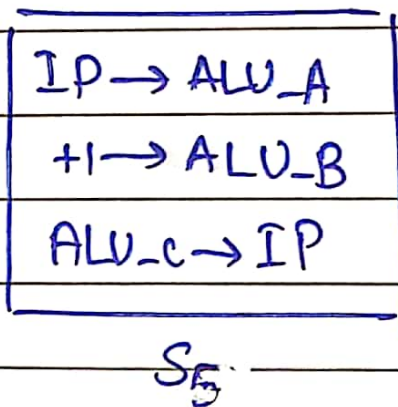
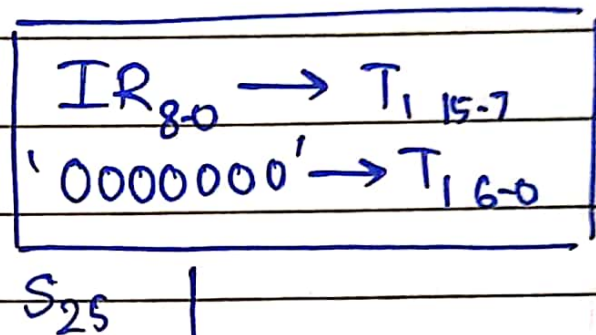
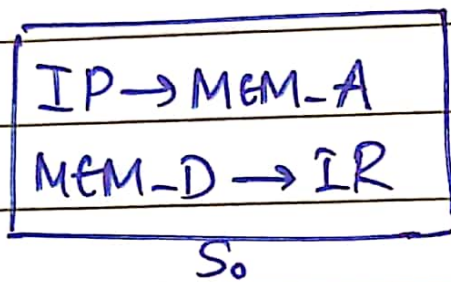


NDC

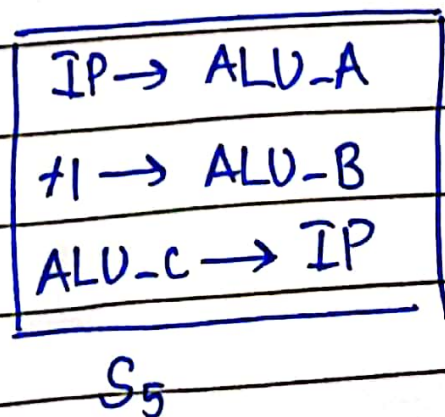
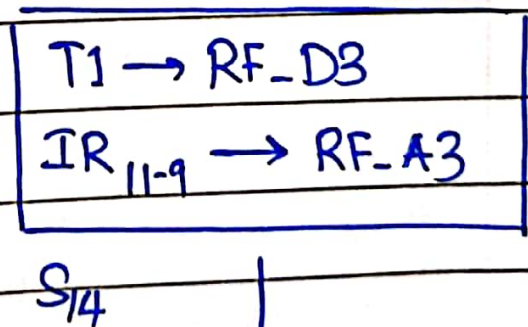
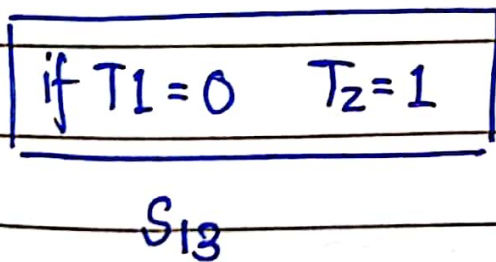
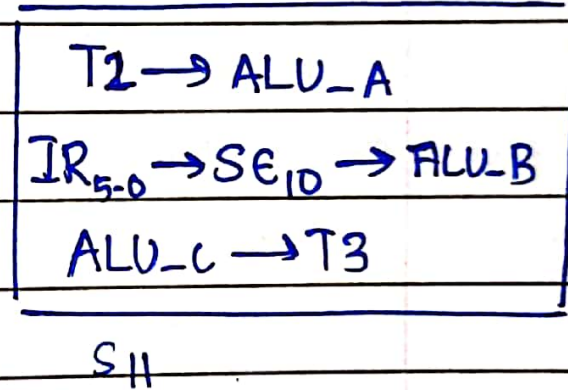
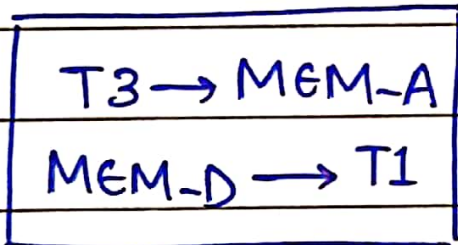
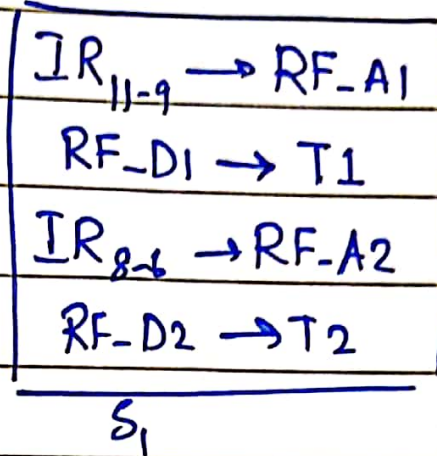
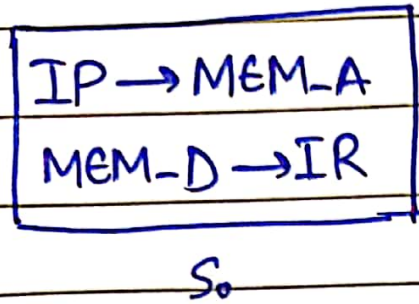


Date: / /

LHI



LW

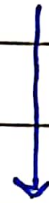


SW

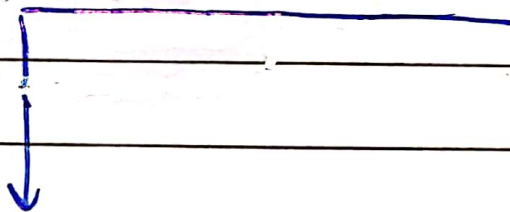
$IP \rightarrow MEM-A$
 $MEM-D \rightarrow IR$

 S_0 

$IR_{11-9} \rightarrow RF-A1$
 $RF-D1 \rightarrow T1$
 $IR_{8-6} \rightarrow RF-A2$
 $RF-D2 \rightarrow T2$

 S_1 

$T2 \rightarrow ALU-A$
 $IR_{5-0} \rightarrow SE-ID \rightarrow ALU-B$
 $ALU-C \rightarrow T3$

 S_{11} 

$T3 \rightarrow MEM-A$
 $T1 \rightarrow MEM-D$

 S_{15} 

$IP \rightarrow ALU-A$
 $+1 \rightarrow ALU-B$
 $ALU-C \rightarrow IP$

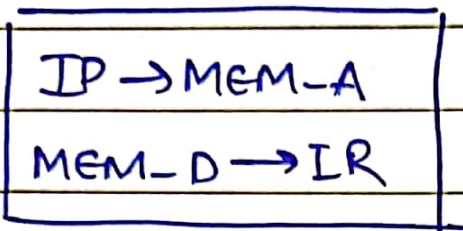
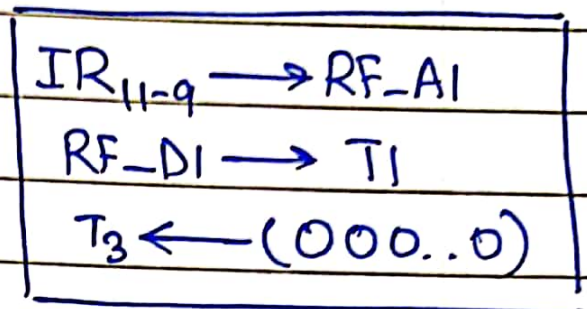
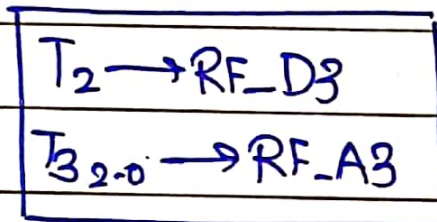
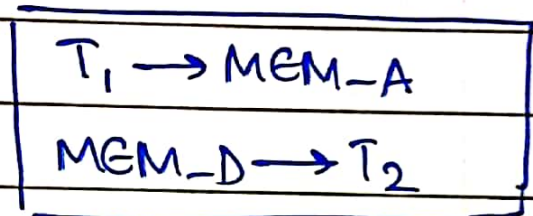
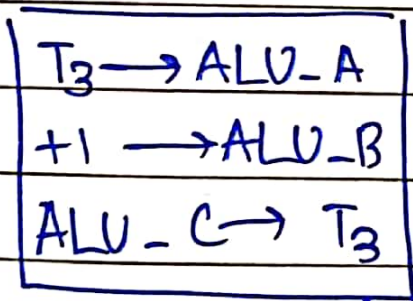
 S_5

LA

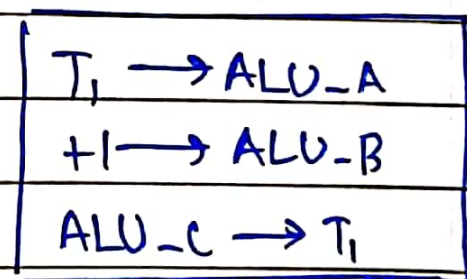
Page No.:

Date:

youvΛ

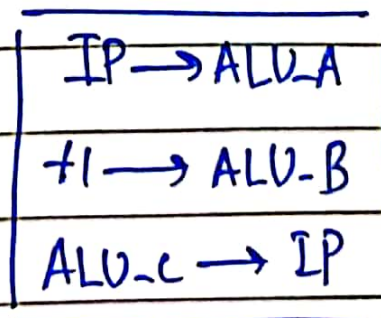
 S_0  S_{16}  S_{18}  S_{17}  S_{19}

add

 S_{20}

add

else

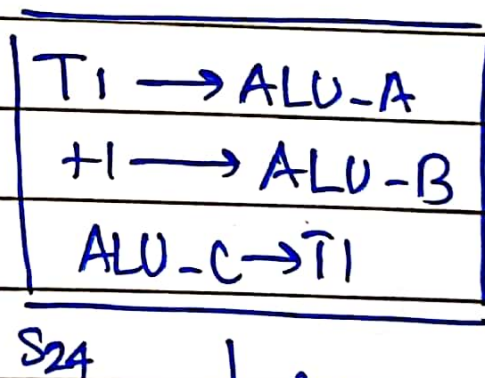
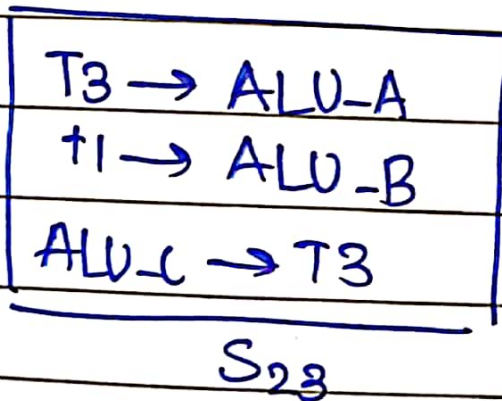
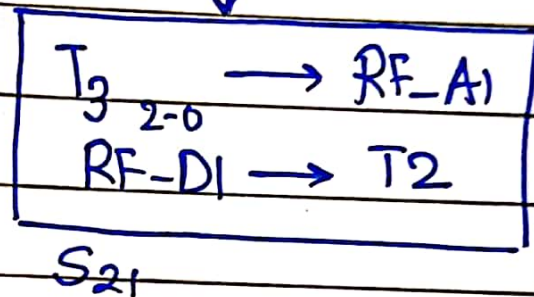
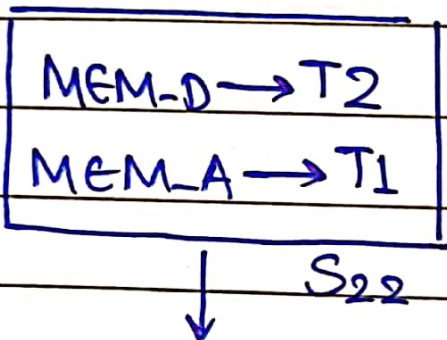
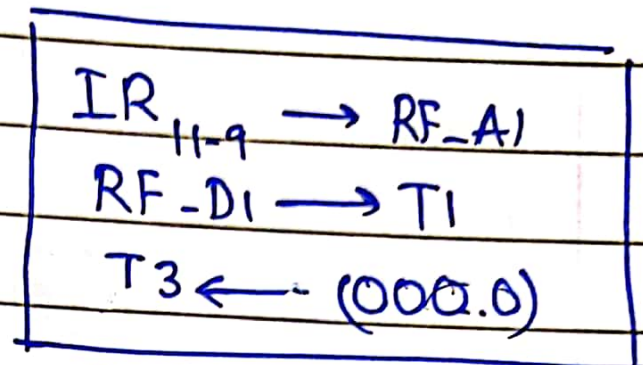
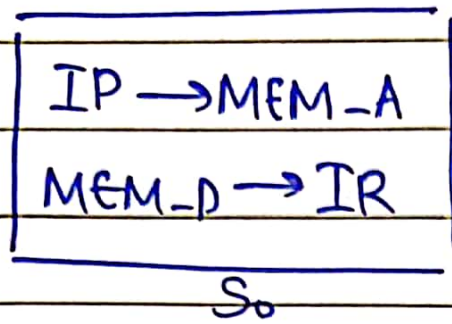
 S_5 if
 $T_3 < 8$

SA

Page No.:

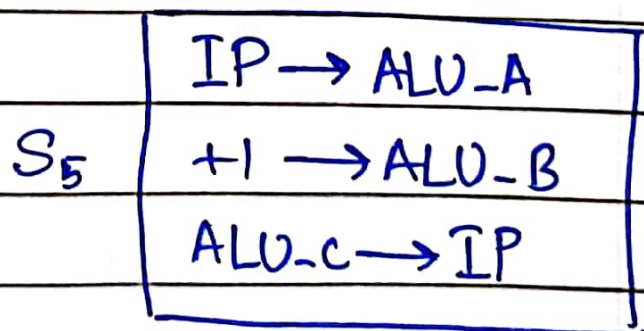
Date:

youva



if
T₃ < 8

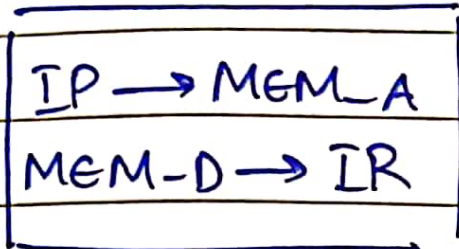
else



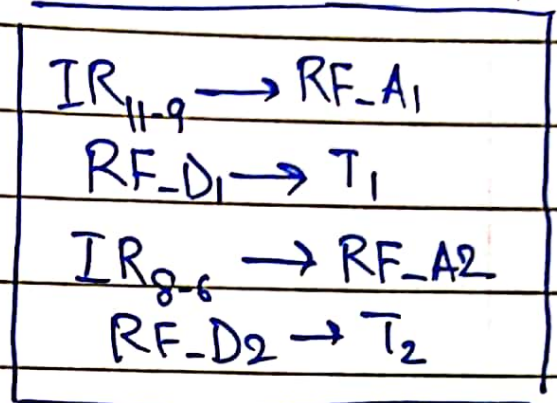
BEQ

Date:

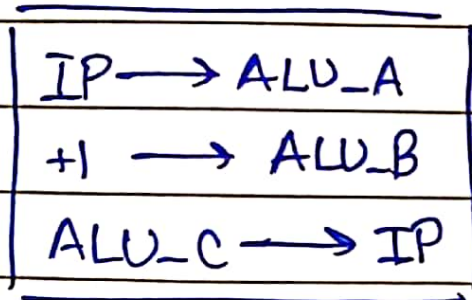
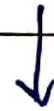
youvΛ



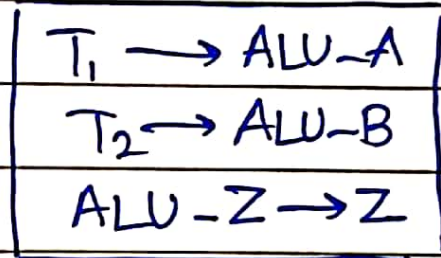
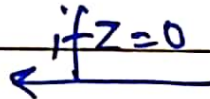
S₀



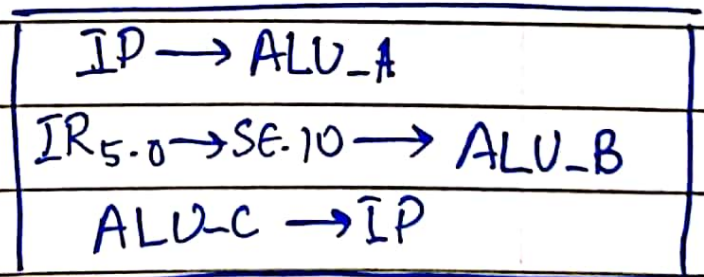
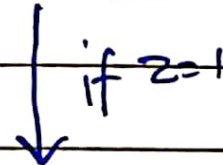
S₁



S₅

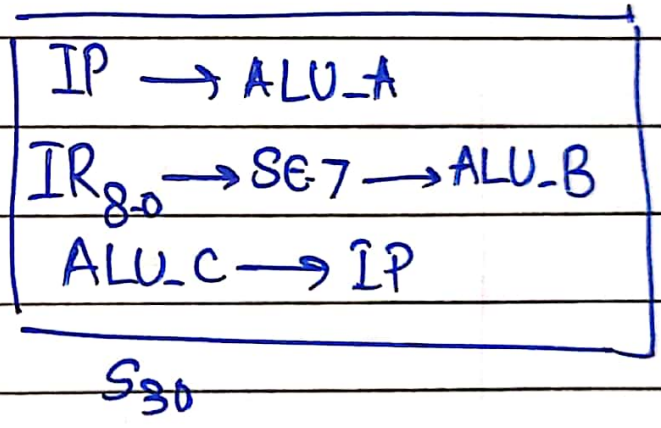
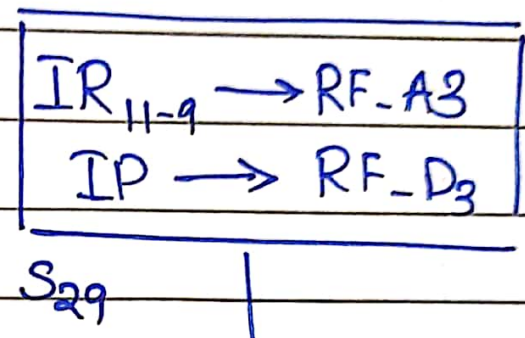
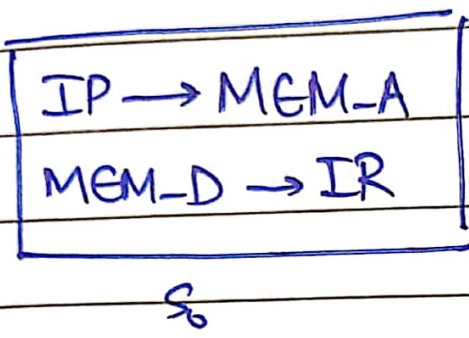


S₂₇



S₂₈

JAL



JLR

Date:

YOUVA

IP \rightarrow MEM-A
MEM-D \rightarrow IR

S₀



IR₁₁₋₉ \rightarrow RF-A1
RF-D1 \rightarrow T₁
IR₈₋₆ \rightarrow RF-A2
RF-D2 \rightarrow T₂

S₁



IP \leftarrow T₂

S₃₂



RF-A3 \leftarrow IR₁₁₋₉
RF-D3 \leftarrow IP

S₃₁

