Design a cache simulator using the Pin tool.
The simulator should read in a configuration file which would specify all the parameters of the cache.

Example configuration file

[Level 1]
Size = 32KB
Associativity = 4
Block size = 32bytes
Hit Latency = 4
Replacement Policy = LRU

[Level 2]
Size = 64KB
Associativity = 8
Block size = 32bytes
Hit Latency = 16
Replacement Policy = LRU

[Main Memory]
Hit Latency = 200

The above configuration file specifies a 2 level cache. The accesses that miss at level 2 cache hit at the main memory. Latencies are specified in cycles.
Main memory should always be the last level with a hit ratio of 1.
All caches are inclusive.
As of now you need to implement only LRU replacement policy in your simulator.

The simulator needs to print these statistics at the end of the simulation : Miss ratio, total number of cache hits and accesses for each level.

A matrix multiplication program with varying matrix sizes will be run on the simulator and cache statistics for the same should be collected. A separate mail regarding the input size and the program will be sent soon.

PS: Your program should not collect memory traces using pin, dump it into a file and then simulate the cache. As and when memory accesses are collected using pin the cache should be simulated. No intermediate file to hold the dump of accesses should be used.

Pin tool : http://software.intel.com/en-us/articles/pin-a-dynamic-binary-instrumentation-tool