GS QuickSilicon   **Hands-on RTL Design**   Buy

1   Cross Correlation

| **Question** | Solution | Video | Discussion |

Alice wants to design a circuit which takes two serial inputs `sig_x_i` and `sig_y_i` such that the input s
circuit produces an output z_o which is asserted whenever there is an expectation of seeing a 1 on the s

All the flops should be positive edge triggered with asynchronous reset (if any).

Interface Specifications

- The interface guarantees that a 1 on `sig_x_i` will be seen on input `sig_y_i` within 32-clock cycle
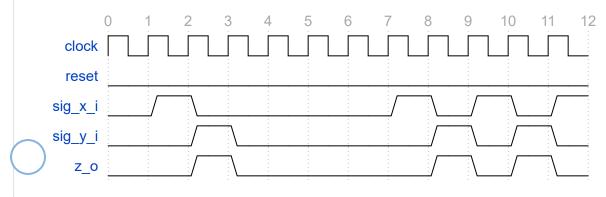
Interface Definition

```
sig_x_i: Serial input to the module
sig_y_i: Serial input to the module
z_o    : Single bit output which is `1` whenever there is an expectation of seei
         a `1` on the input sig_y_i
```

Sample Waveform

| Bug | Next Module   >_ Console   **Run Testcases**   **Submit**