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Async Resets

Question | Solution | Video | Discussion

You are asked to design a circuit which would avoid boot-up issues in silicon during asynchronous reset d
domain. The circuit is responsible for driving two signals:

- `release_reset_o`: This signal should be asserted when it is safe to deassert the reset to the rest
- `gate_clk_o`: This circuit would gate the clock to the rest of the circuit

The specifications mention that reset should only be released to the rest of the circuit if the asynchrono
that the clock tree time takes 7 cycles while the reset tree time takes 8 cycles to be distributed to all the

All the flops (if any) should be positive edge triggered with asynchronous resets.

Design the module which would drive the two outputs and thus allow the circuit to come out of reset cle