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Perf Counters

Question | Solution | Video | Discussion

You are working on the next generation Processor unit and are responsible for designing the CPU perfo number of counters which can be programmed to be triggered on an event from different CPU units.

Design the base counter module which can be instantiated depending on the implemented number of su received from the CPU pipeline. The counter output should only be accessible to software reads and thu mandate that after the read is complete the counter should reset the value to 0. Both software read and have any protocol requirements.

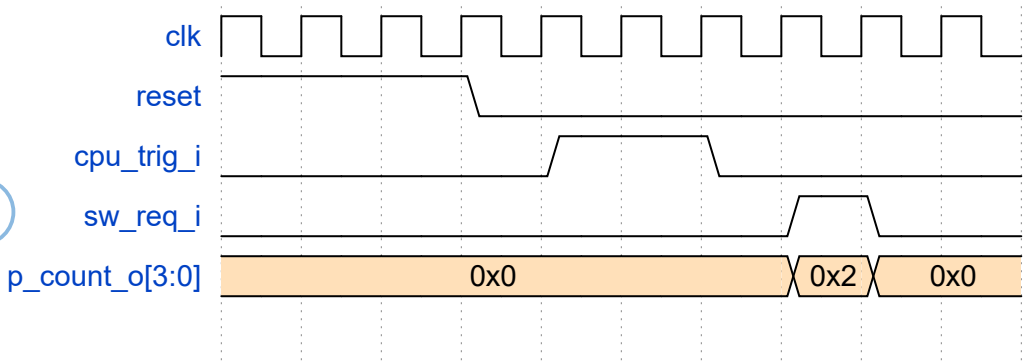
The width of the counter is parameterizable.

All the flops should be positive edge triggered with asynchronous resets (if any).

Interface Definition

```
sw_req_i    : Software read request to the counter. Will read the `p_count_o` va
cpu_trig_i  : CPU trigger event to the counter
p_count     : Performance counter read value to software. Should be zero when th
              request in progress
```

Sample Simulation



Explanation

On reset the counter value should be zero which is what is reflected in the p_count_o signal. The count on p_count_o interface once the software read request is seen. The counter resets to zero one cycle aft protocol requirement.

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