

Hands-on RTL Design

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1 Compression Engine

Question

Solution

Video

Discussion

Breaking a large vector into a combination of mantissa and exponent is a frequently used technique to combination of the vector with some impact on the accuracy.

Rohan wants to deploy a similar scheme where he wants a 24-bit vector to be compressed into a 12-bit I mantissa and exponent in the following manner:

```
if (exponent == 0) then
  vector = mantissa
else
  vector = {1'b1, mantissa, {exponent-1{0}}}
end
```

The above compression scheme shows how the resultant vector can be obtained using mantissa and expconcatenating 1'b1 on the MSB side of mantissa and adding exponent - 1 zeros to the vector. Consic mantissa and exponent:

```
Example 1:
Vector[23:0] = 0xFC
```

Since the entire information can be given in the mantissa alone, exponent will be 0 and mantissa would be equal to the vector:

```
Mantissa[11:0] = 0xFC
Exponent[3:0] = 0x0
```

```
Example 2:
```

```
Vector[23:0] = 0xFFC01D
```

The mantissa can alone not contain the entire vector hence the exponent will be non-zero in this case. Given the resultant vector is formed as: `{1'b1, mantissa, {exponent-1{0}}}` this implies that mantissa should take the upper most 12-bits after the fist set bit from MSB as that is already included in the resultant vector. Using this information Mantissa would be:

```
Mantissa[11:0] = 0xFF8
```

Bug

Next Module

>_ Console

Run Testcases

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