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Edge Capture

Question | Solution | Video | Discussion

Quite often your logic needs to react to a change on some control signal. That can be an external input, s done it's job and that it is safe to continue. All sorts of scenarios exist that call for a signal generated by c different system.

Implement a sticky edge detector (or a edge capture) circuit which captures any neg-edge (from 1-0) tra capture must be performed on per bit basis for all the 32-bits of the input. All the flops should be positiv

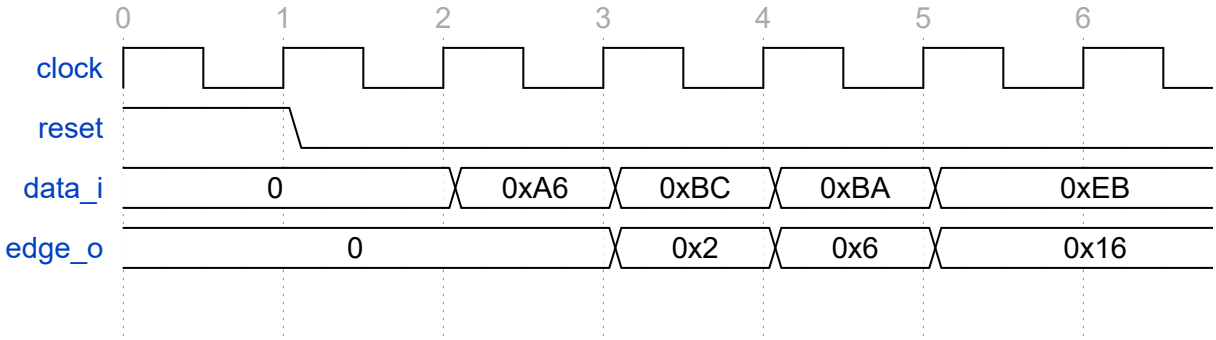
Interface Definition

```
data_i[31:0] : Input bits to the module
edge_o[31:0] : Output which says a neg-edge was detected
```

Interface Requirements

- The detection should be sticky - once neg-edge is detected on any bit of the input, the particular b seen
- The module should produce the output on every cycle

Sample Simulation



Explanation

- **Cycle T1** : Reset is asserted
- **Cycle T2** : Reset is de-asserted. `data_i` is 0x0
- **Cycle T3** : `data_i` is 0xA6
- **Cycle T4** : `data_i` is 0xBC. `edge_o` is 0x2 (since data changed from 0xA6 to 0xBC where the bit p
- **Cycle T5** : `data_i` is 0xBA. `edge_o` is 0x6 (honouring the sticky property)

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