ECE1388 VLSI Design Methodology
Project-2 Report

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Q. 1.1 Solution Calculation of propagation delay

The method of Logical Effort [Sutherland99] provides a simple method "on the back of an envelope" to choose the best topology and number of stages of logic for a function. Based on the linear delay model, it allows the designer to quickly estimate the best number of stages for a path, the minimum possible delay for the given topology, and the gate sizes that achieve this delay.

The minimum possible delay of an N stage path with path effort F and path parasitic delay(P) is

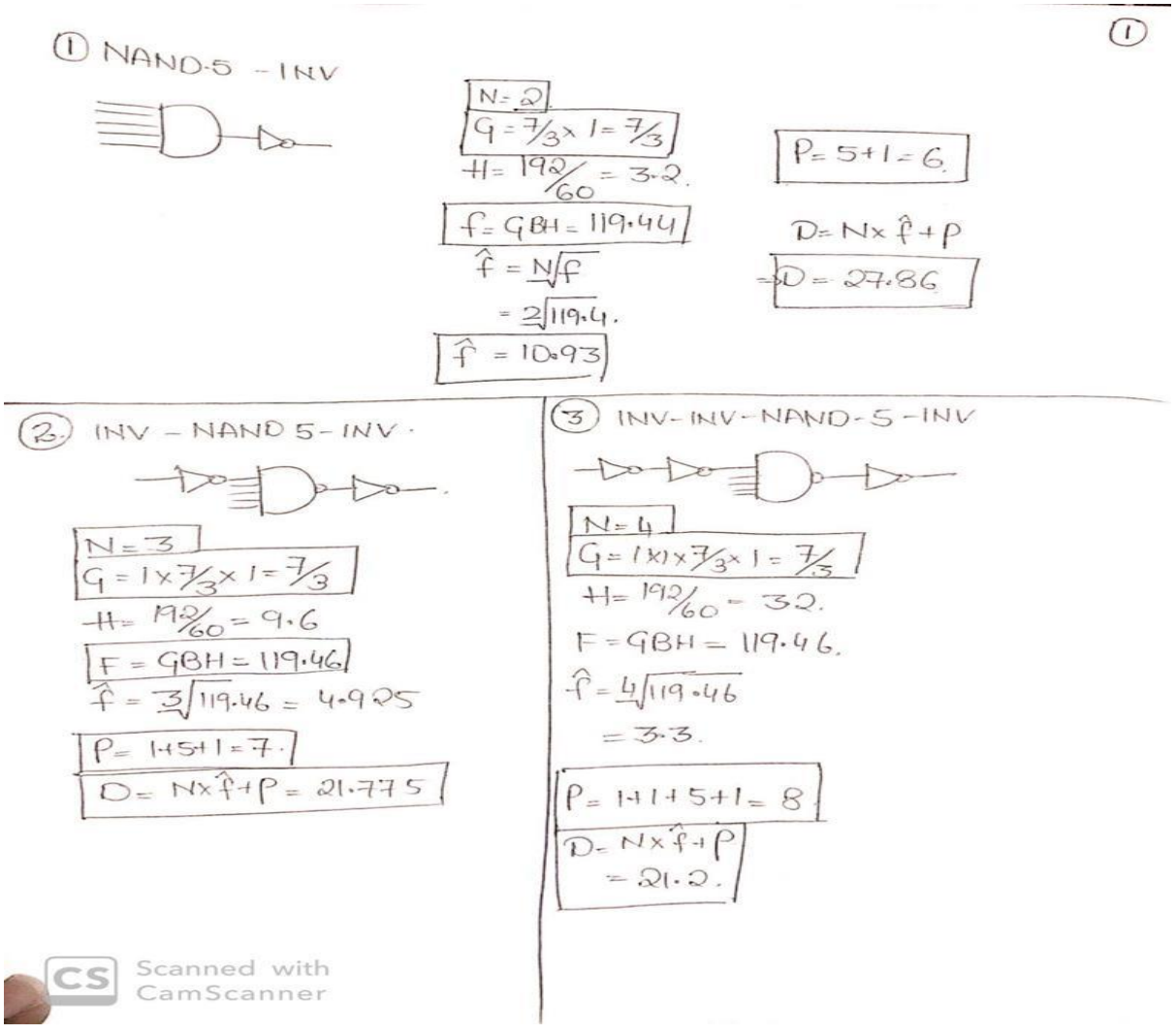
$$D = N(F)^{\wedge}(1/N) + P$$

In general, the normalized delay of a gate can be expressed in units of **τ**as

$$d = f + p$$

p is the parasitic delay inherent to the gate when no load is attached. f is the effort delay or stage effort that depends on the complexity and fanout of the gate:

$$f = gh$$



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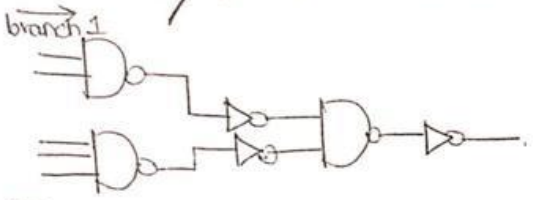
④ NAND-2 / 3-INV - NAND2 - INV.



The branch with NAND-3 has highest delay.

for branch-1

$N = 4$.

$G = 16/9$

$H = 3.2$.

$f = 91.022$.

$\hat{f} = 3.088$

$P = 6$

$D = 18.352$.

branch-2.

$N = 4$

$G = 20/9$.

$H = 3.2$

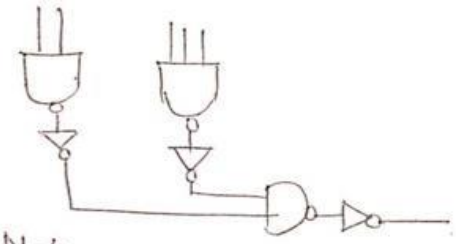
$F = 113.77$.

$\hat{f} = 3.26$

$P = 3+1+2+1 = 7$.

$D = 20.04$

⑤ NAND2 / 3-inv - NANN2 - INV (with predecoder)



$N = 4$.

$G = 20/9$.

$H = 3.2$.

B value varies due to branching difference.

But rest all values tend to ~~bar~~ be same as ④

$N = 4$.

$G = 20/9$.

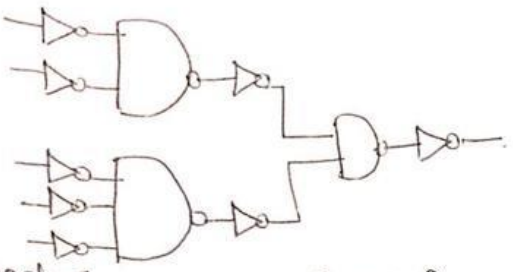
$H = 3.2$.

$F = 113.77$

$P = 7$

$D = 20.04$

(6) INV-NAND2/NAND3 - INV - NAND2 - INV. (2)



Branch-1

N=5.

G=16/9.

H=3.2.

B=16

F=91.022

$\hat{f} = \sqrt[5]{91.022} = 2.46$

P=7.

D=19.3

Branch-2.

N=5.

G=20/9.

B=16.

H=16/9

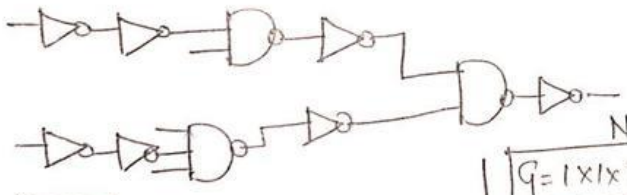
F=113.77

$\hat{f} = 2.57$.

P=8. ✓

D=20.85 ✓

(7)



N=6

G=1x1x5/3x1x4/3x1 = 20/9.

H=3.2 B=16 F=113.77

$\hat{f} = \sqrt[6]{213.33} = 2.201$

P=9.

D=23.64.

N=6

H=3.2.

B=16

F=16.96x16/9=91.022.

$\hat{f} = \sqrt[6]{91.022} = 2.12$.

P=8

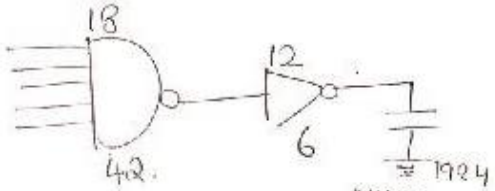
D=6.2.12/3.55+8=20.72.

The transistor sizings can be obtained by working backward based on input capacitances of each gate.

$Cin = Cout_i * g_i / f_{cap}$

GATE SIZING.

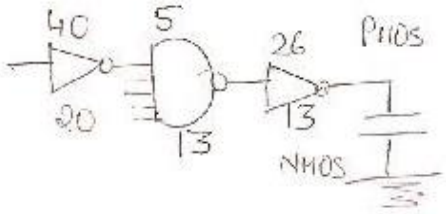
(1)



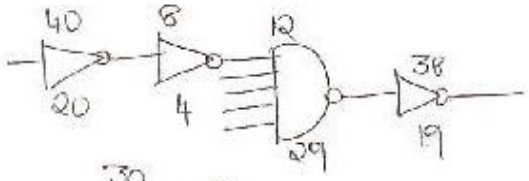
PMOS=

$$C_{in} = \frac{C_{out} \times g}{f}$$

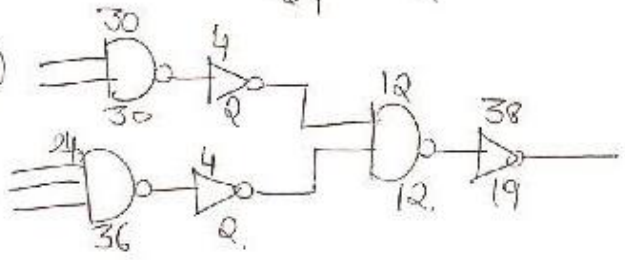
(2)



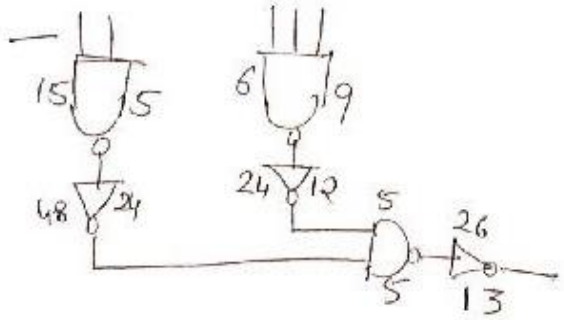
(3)

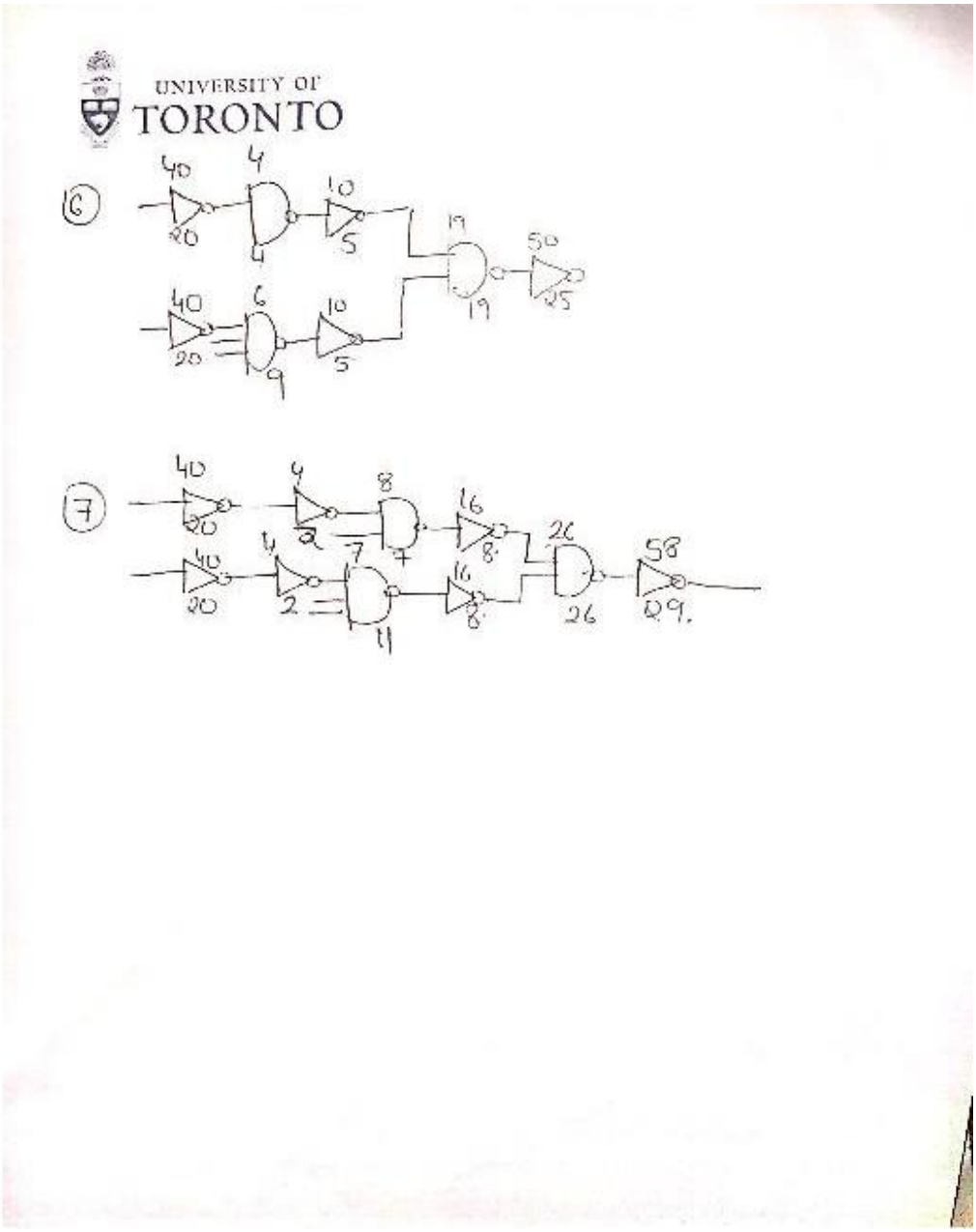


(4)



(5)





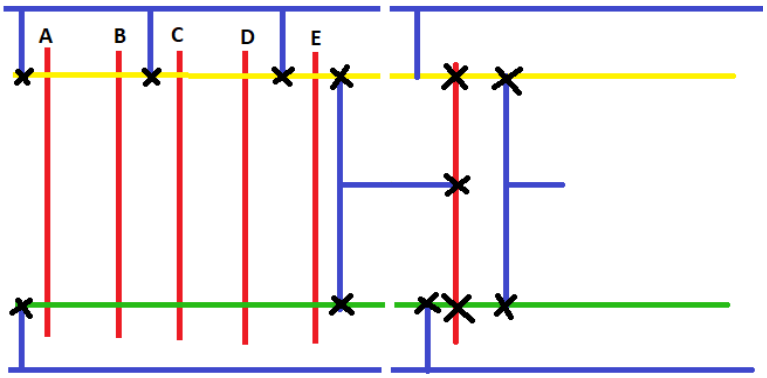
Q 1.2 Area Estimation using Stick Diagrams

Equations to calculate the stick diagrams are given by:

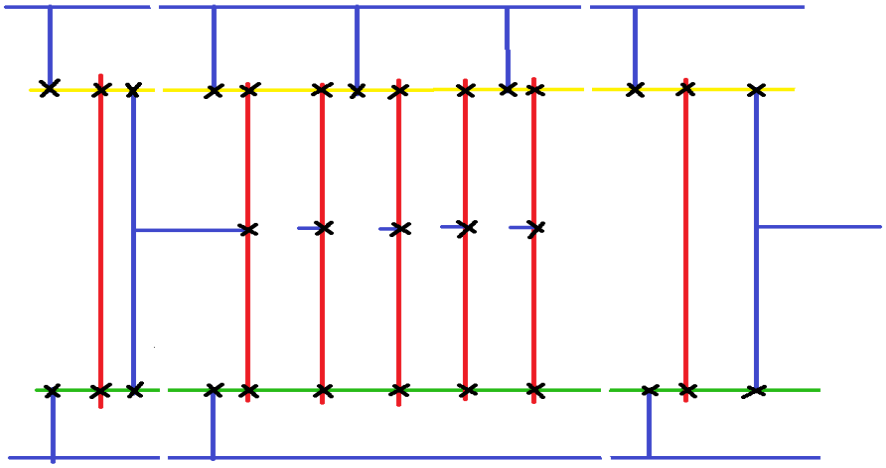
$$\text{Area} = \text{Width} * \text{Length}$$

$$\text{Width} = \text{Horizontal Wires}* 8\lambda + (\text{Largest Gate Sizing}) + 4\lambda$$

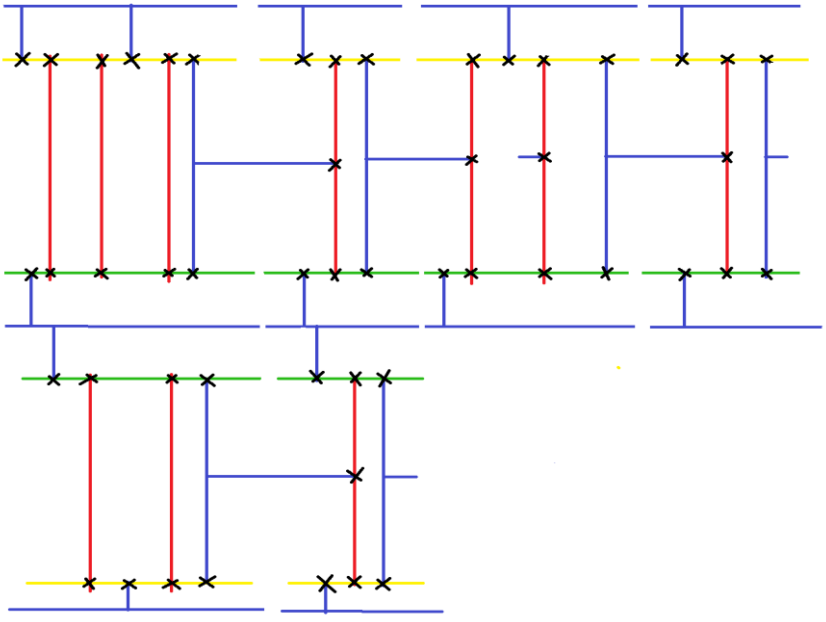
$$\text{Length} = \text{No of Vertical lines} * 8\lambda$$



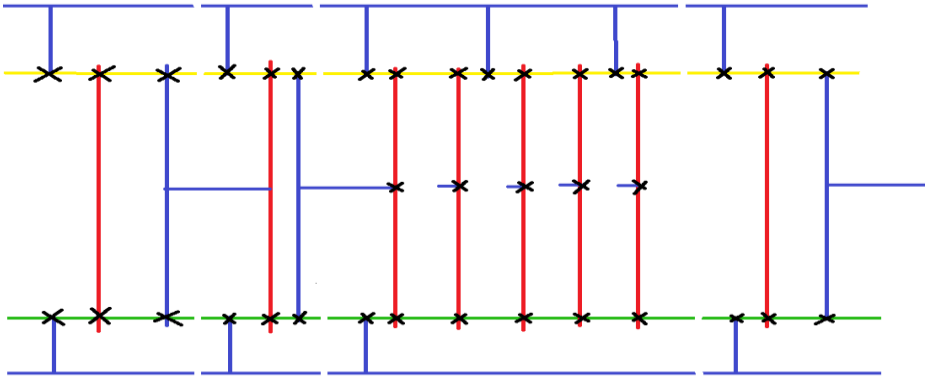
Stick Diagram of NAND5-INV



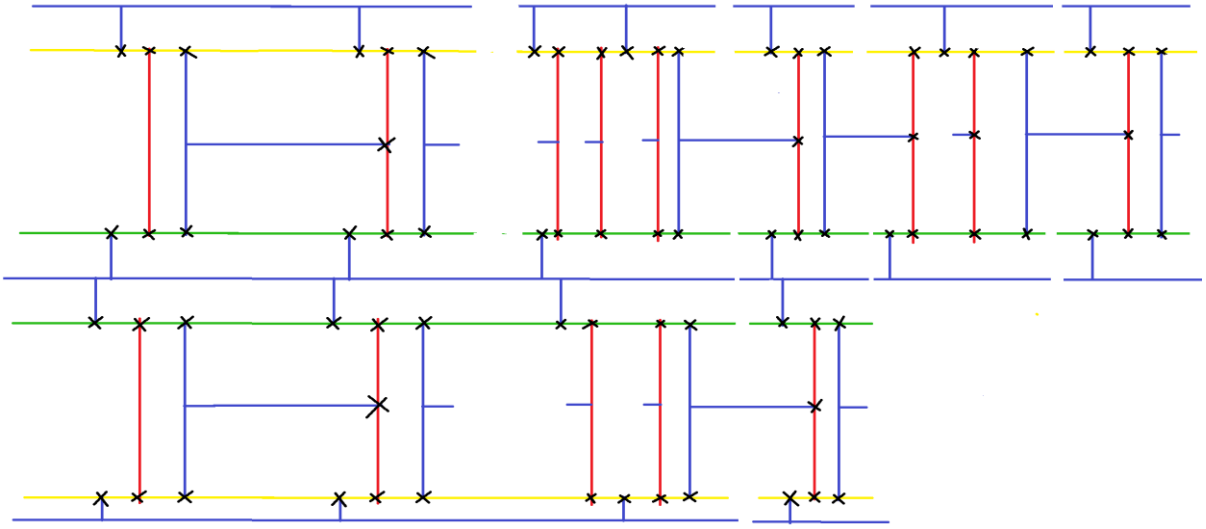
Stick Diagram of INV-NAND5-INV



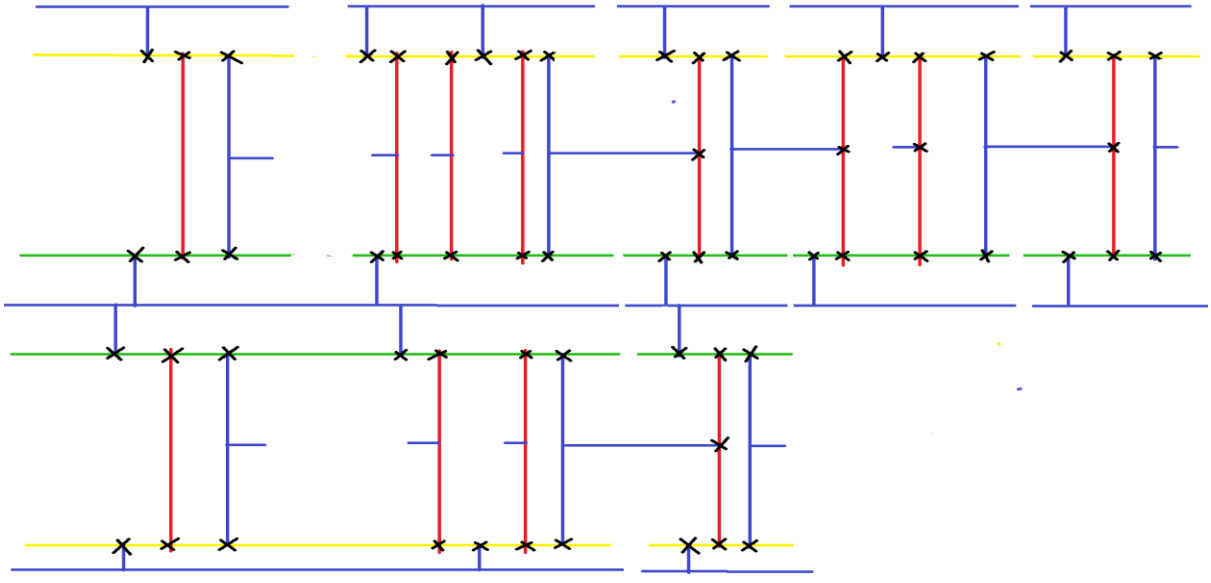
Stick diagram of NAND2/3-INV-NAND2-INV



Stick Diagram of INV-INV-NAND5-INV



Stick Diagram of INV-INV-NAND2/3-INV-NAND2-INV



Stick Diagram of INV-NAND2/3-INVNAND2-INV

Area	
λ2	µm2
123904	111.51
376012.8	338.411
770048	693.04
383918	345.52
312576	281.31
638064.64	574.258
890081	801.07

Q 1.3 Average Dynamic Power Dissipation

$$P_{switching} = \alpha C V_{DD}^2 f$$

From the question

f= 1 Mhz

VDD=1 V

α_i = Pi*Pi`(Switching Factor)

Gate	P_Y
AND2	$P_A P_B$
AND3	$P_A P_B P_C$
OR2	$1 - \overline{P}_A \overline{P}_B$
NAND2	$1 - P_A P_B$
NOR2	$\overline{P}_A \overline{P}_B$
XOR2	$P_A \overline{P}_B + \overline{P}_A P_B$

The above table shows the different values of α for different gates

The output capacitance of unit size inverter is

$$C_{out}(NMOS) = \frac{C_{d(Shared)} + C_{d(Diff)} \times 120 \times 10^{-9}}{10^6}$$

$$= (0.76 + 1.28) \times 120 \times 10^{-3}$$

$$= \boxed{0.244\,fF}$$

$$C_{out}(PMOS) = \frac{C_{d(Shared)} + C_{d(Cd)} \times 240 \times 10^{-9}}{10^6}$$

$$= \frac{0.73 + 1.253 \times 240 \times 10^{-9}}{10^6}$$

$$= 0.4752$$

C_{out} of unit sized inverter $= 0.244 + 0.4752\,ff.$

$$= \boxed{0.719\,fF}$$

The capacitance of unit sized inverter =

$C_{in} = C_g$ (Pmos width + NMOS width)

$\boxed{C_{in} = 0.385\,fF}$

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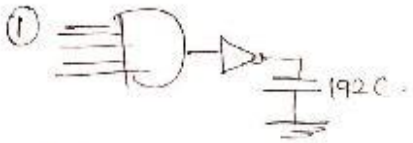

At $n_1 = 17.56 \times 0.38fF$

$= 6.68fF.$

$T_A = \frac{31}{32}.$

$\alpha = \frac{31}{1024}.$

Power at $n_1 = \alpha C V_{dd}^2 \times f$

$= \frac{31}{1024} \times 6.67 \times 10^{-15} \times \frac{1}{32} \times 10^6$

$= 0.201nW$

Power of inv

$C = 192 \times 0.38$

$P_{inv} = \alpha C V_{dd}^2 f$

$= \frac{31}{1024} \times 72.96 \times 10^{-15} \times 10^6$

$= 2.208.$

Total power = 2.409 nW

for 32 = 77.028nW

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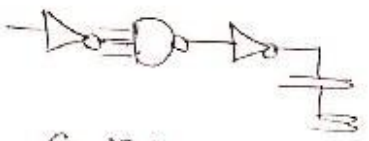
INV – NAND-5 – INV



$C = 18.469 \times 0.39 = 7.018\,fF$

$\alpha = 1/2$

$P_{n_1} = \alpha C V_{dd}^2 f$

$= \frac{1}{2} \times 7.018 \times 10^{-15} \times 10^6$

$= 3.505\,nF$

At n_2

$C = 38.98 \times 0.38 \times 10^{-15}\,F$

$C = 14.812\,fF$

$\alpha = \frac{31}{1024}$ $\quad P_A \cdot P_B = \frac{1}{32} \times \frac{31}{32}$

$P_{n_2} = \alpha C V_{dd}^2 f$

$= 0.448\,nF$

At n_3

$C = 192 \times 0.38$

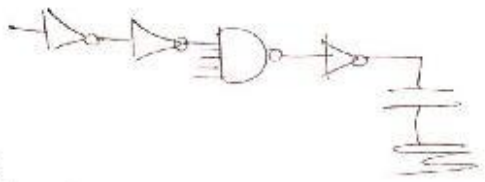
$\alpha = \frac{31}{1024}$

$P_{n3} = 2.20nW$

Total Power = 6.185nW

For 32 = 197.92nW

(3) INV - INV - N-S - INV



n_1 $C = 12.36 \times 0.38 \times 1^2 \times 1 \times 10^{-6}$

$= 4.699$

$X = 1/2$ $P_{n_1} = 0.5 \times 4.699 \times 10^{-15} \times 10^6$

$= \boxed{2.3495\,nW}$

n_2

$C = 40.93 \times 0.38 = 15.55\,fF$

$X = 0.5$

$P_{n_2} = X V_{dd}^2 C f$

$= 7.775\,nW$

n_3 $C = 58 \times 0.38\,fF$

$= 22.04\,fF$

$X = \frac{31}{1024}$

$P_{n_3} = \frac{31}{1024} \times 22.04 \times 10^{-9}$

$= \boxed{0.667\,nW}$

$n_4 = C = 19 \times 0.38\,fF$

$= 7.296\,fF$

$X = \frac{31}{1294}$

$P_{n_4} = 2.208\,nW$

Total power = 13.05 nW

For Decoder 13.05nW x 32

$\boxed{416.96\,nW}$

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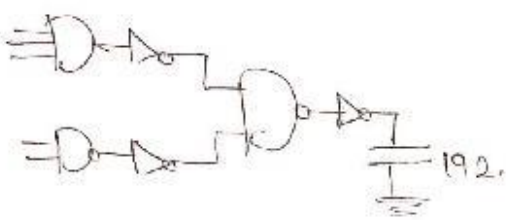
(4)



$C = 2.905$

$\alpha = 7/64$

$P_{n_1} = 0.317\,nW$

$n_2 = C = 24.46.$

$P = 1.01\,nW$

n_3 $C = 58.805 \times 0.38\,ff$

$= 223\,ff$

$\alpha = \frac{31}{1024}$

$n_4 = 192 \times 0.38\,ff$

$= 72.96$

$P = 2.208\,nW$

$n_3 = 24.46 \times 0.38\,ff$

$\alpha = \frac{31}{1024}$

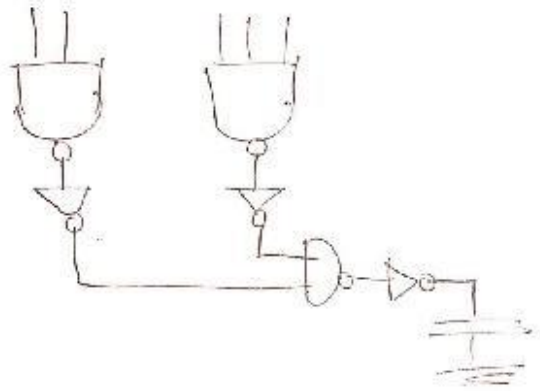
$P_{n_3} = 0.038\,nW$

$P_{n_4} = 0.56$

Total power = 6.06 nW

Total power = 20.7 nW

(5)



n_1:

$C_1 = 30 \times 0.38$

$= 11.4\,fF$

$P = 2.138\,nW$

n_2: $C = 59 \times 0.38$

$\alpha = 3/16$

$P = 4.203\,nW$

n_3:

$C = 24 \times 0.38$

$= 0.27\,nW$

$n_4 = 29.95 \times 0.38$

$= 11.22\,fF$

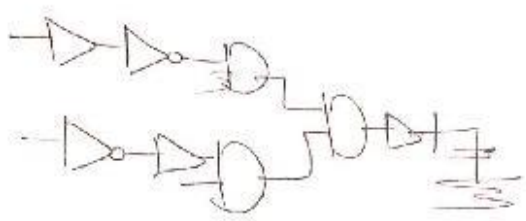
$\alpha = 7/64$

$P = 1.228\,nW$

Total power $= 25.32 + 4.54 + 80$

$= \boxed{148.72}$

(7)



$n_1 = C = 8.259 \times 0.38$

$X = 0.5$

$P = 1.56$

$n_2 : C = 18.179 \times 0.38$

$= 6.9nF$

$X = 0.5$

$P = 3.45nW$

$n_3 : C = 24.008 \times 0.38$

$= 9.12$

$P = 0.997nW$

$n_4 = 52.89 \times 0.38$

$= 20.07nF$

$X = 7/64.$

For 32 . 642.24nW

$n_5 = 81.23 \times 0.38.$

$X = 31/1024.$

$P = 1.003nW$

n6.

P.

$C = 7.12 \times 0.38 = 2.7$

$P = 1.35nW$

$n_7 \quad C = 15.62 \times 0.38 = 5.93fF$

$X = 3/8$

$P = 2.22nW$

$n_8 : C = 9.469 fF$

$X = 3/8$

$P = 3.55nW$

Total power = 20.7 nW

The predecoder circuit has same values as 5 but due to branching effort there is difference in capacitance and the total power is 148.72nW

Q 1.4 Solution Table

Design	N	G	P	D	Area		Pd	PD
					λ2	μm2		
NAND5-INV	2	2.33	6	27.86	103322	90.29	*77.024nW*	2145.8nWsec
INV-NAND5-INV	3	2.33	7	27.76	323394	291.05	197.92nW	5494.25 nWsec
INV-INV-NAND5-INV	4	2.33	8	21.2	667648	600	416.96nW	8838.5 nWsec
NAND2/3-INV-NAND2-INV	4	2.22	7	20.04	372224	335	193.92nW	3886.1568 nWsec
NAND2/3-INV-NAND2-INV (with predecoder)	4	2.22	7	**20.04**	306688	276	148.72nW	2980.34 nWsec
INV-NAND2/3-INV-NAND2-INV	5	2.22	8	20.85	620661	558.59	93.92nW	1958.232 nWsec
INV-INV-NAND2/3-INV-NAND2-INV	6	2.22	9	22.19	901795	811.6	95.616nW	2121.71 nWsec

The smallest area was for NAND5-INV : (90.29um^2)

The smallest delay was for NAND2/3-INV-NAND2-INV (with predecoder) : 20.04uS

The smallest power was for NAND5-INV: 77.024 uW

Number of Stages(N):

The number of stages can be defined as the number of gates that are connected in series.

Path Logical Effort(G):

The logical effort of a gate is defined as the ratio of the input capacitance of the gate to the input the capacitance of an inverter that can deliver the same output current.

Gate type	Number of inputs				
	1	2	3	4	n
Inverter	1				
NAND		**4/3**	5/3	6/3	(n+2)/3
NOR		**5/3**	7/3	9/3	(2n+1)/3
Tristate / mux	2	2	2	2	2
XOR, XNOR		4, 4	6, 12, 6	8, 16, 16, 8	

Table showing Logical effort values for different gates

Path parasitic delay:

It is an intrinsic delay of the gate and can be found by considering the gate driving no load.

Path delay:

Path delay is the sum of the path effort delay (D) and path parasitic delay(P).

Dynamic power:

Dynamic power arises from the switching of the load.

$\mathbf{P_{switching} = \alpha C V_{DD}^2 f}$

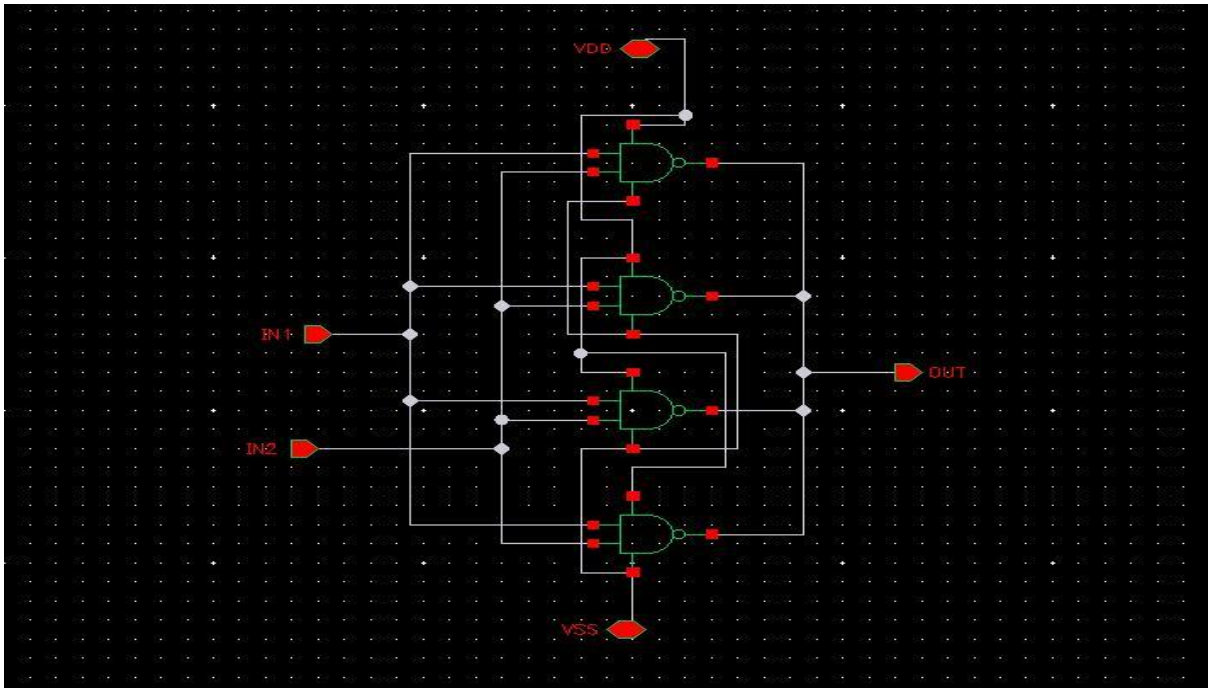
Q 2.1 Schematic and Simulations

From question 1 the drive strengths for each logic gate in the decoder design with predecoder circuit were found using the following formula

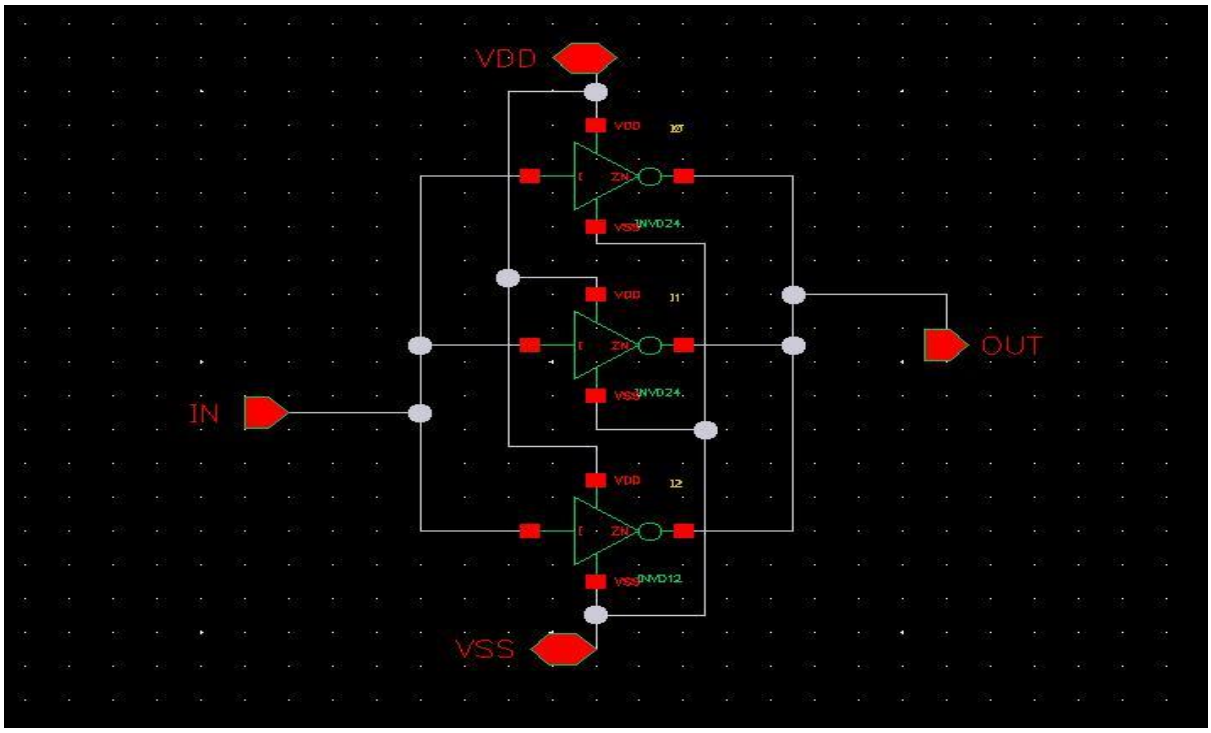
$$Drive\ Strength(x) = cin/g$$

Logical Gate	Drive Strength
NAND-2	22
INVERTER	60
NAND-3	9
INVERTER	28
NAND-2	18
INVERTER	58

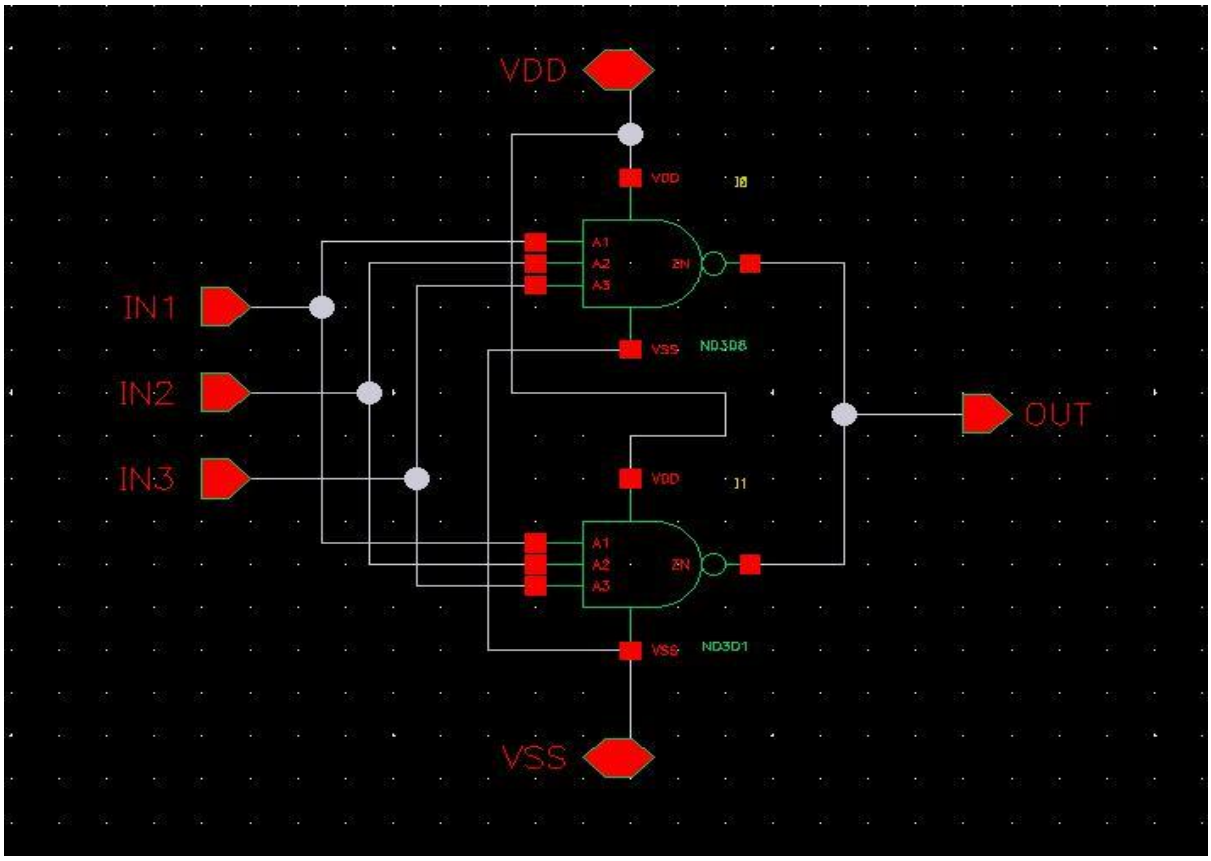
Schematics of Individual logic gates based on drive strengths



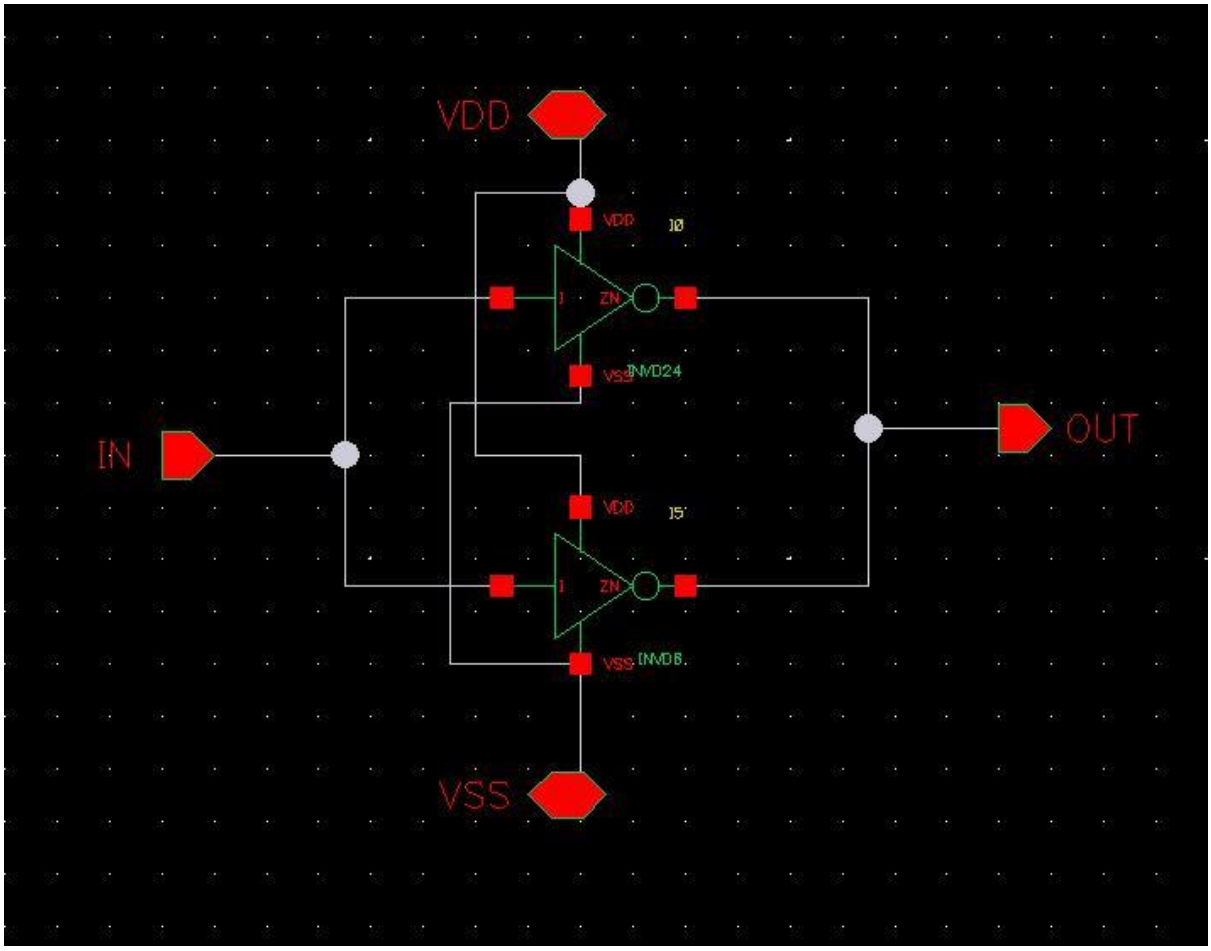
Schematic of 2 input NAND of drive strength 22



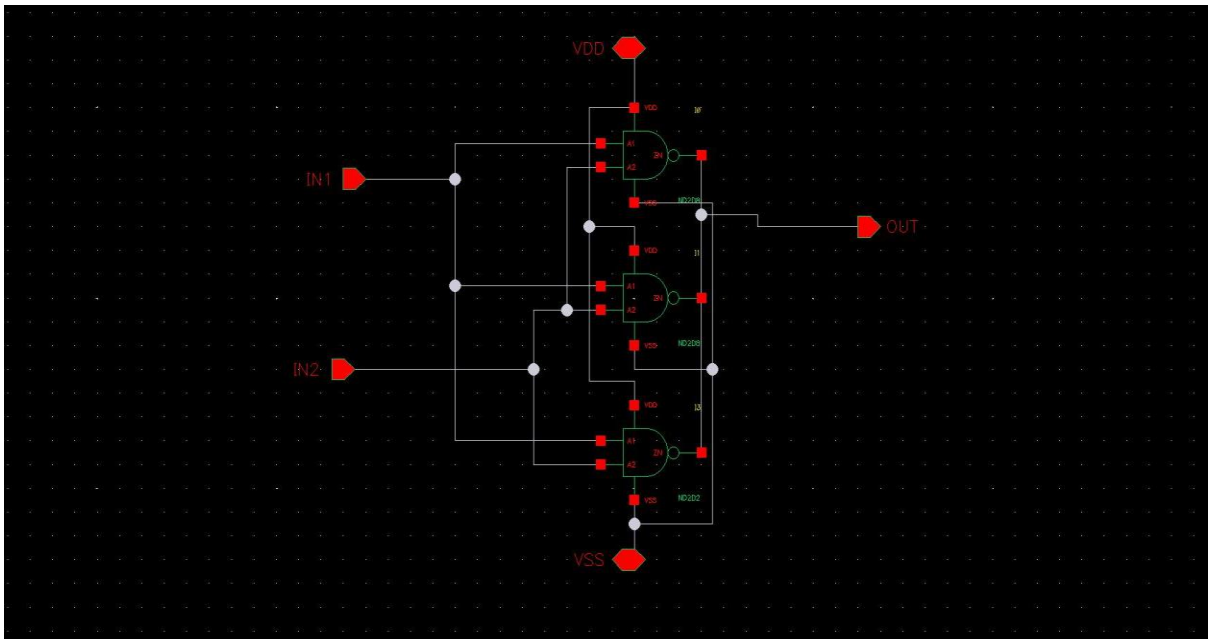
Schematic of Inverter of drive strength 60



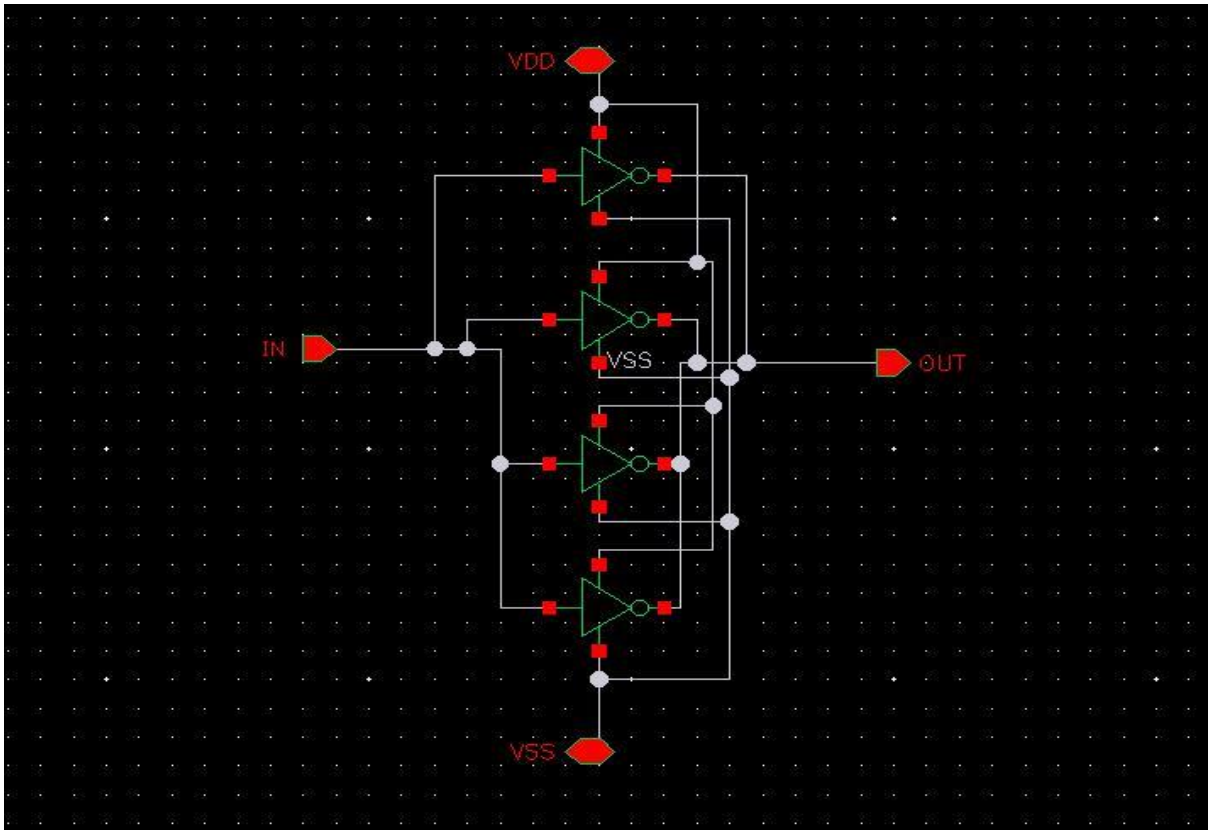
Schematic of 3 input NAND of drive strength 9



Schematic of Inverter of drive strength 30

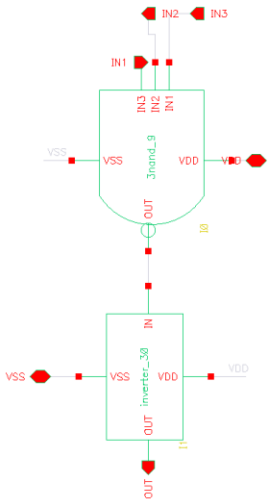


Schematic of 2-input NAND of drive strength 18

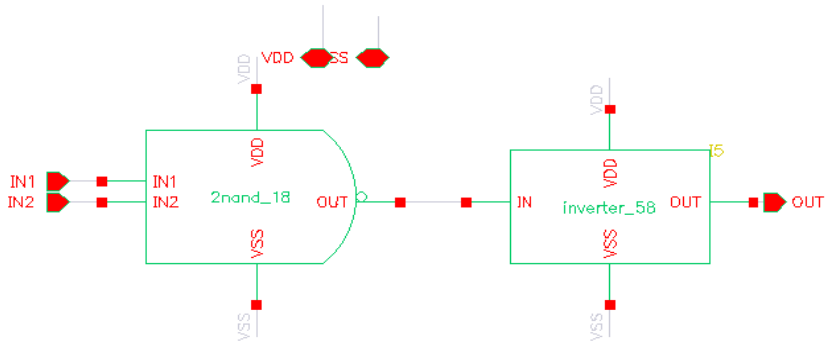


Schematic of Inverter of drive strength 58

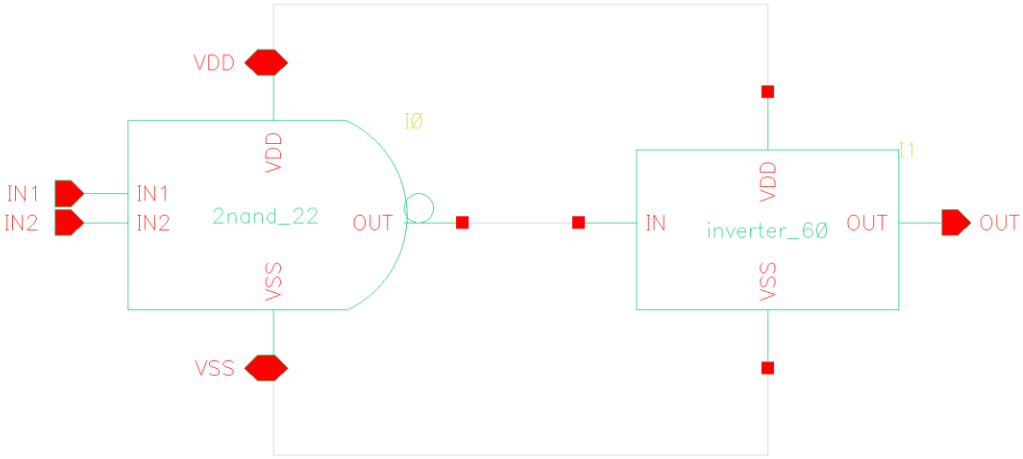
Stage-2 of hierarchy



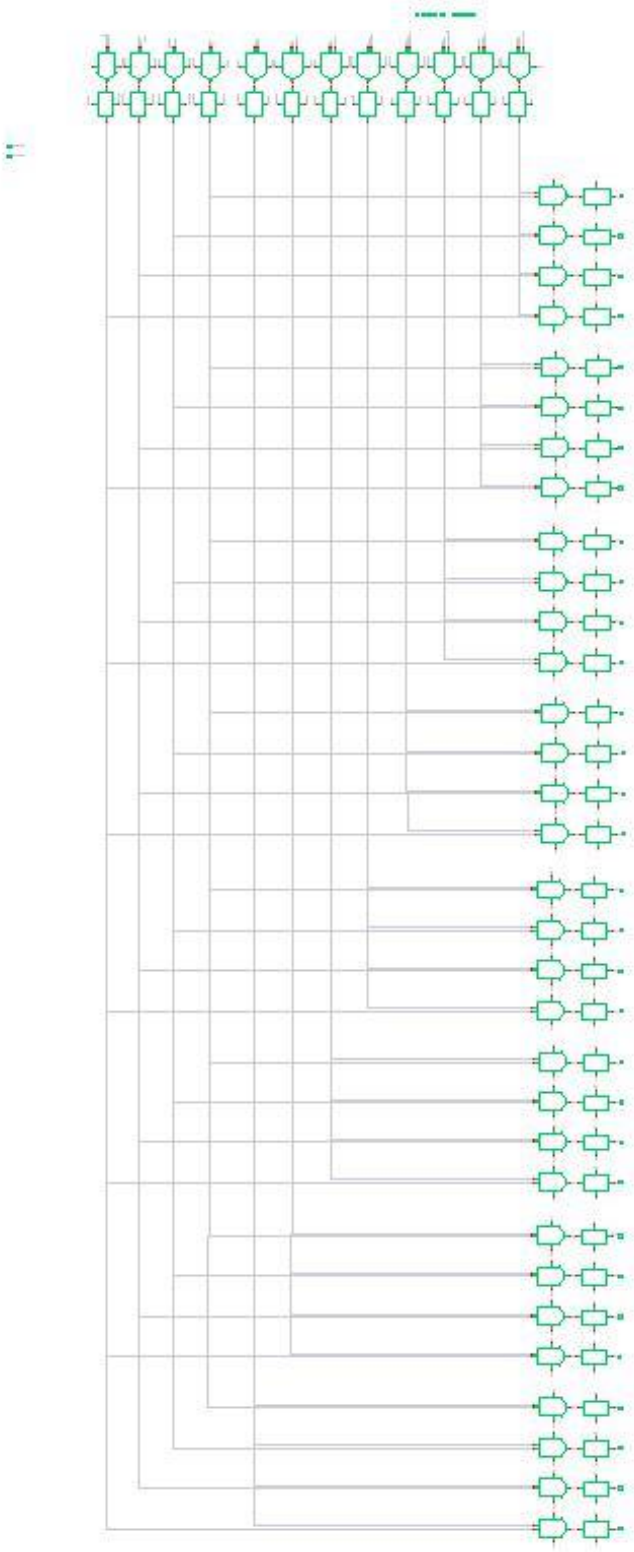
Schematic of 3-NAND and Inverter



Schematic of 2-NAND and inverter

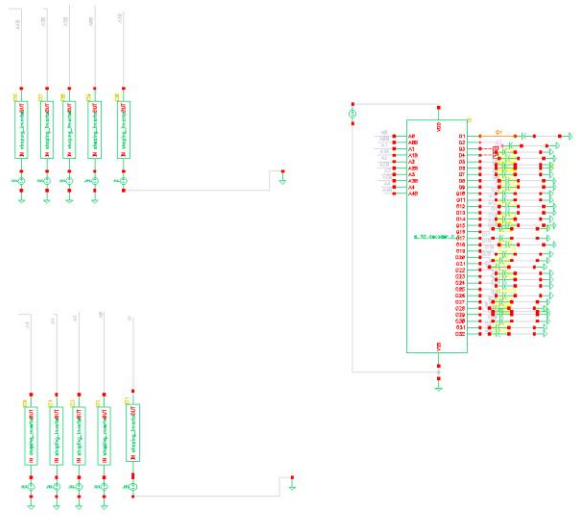


Schematic of 2 NAND and inverter 60



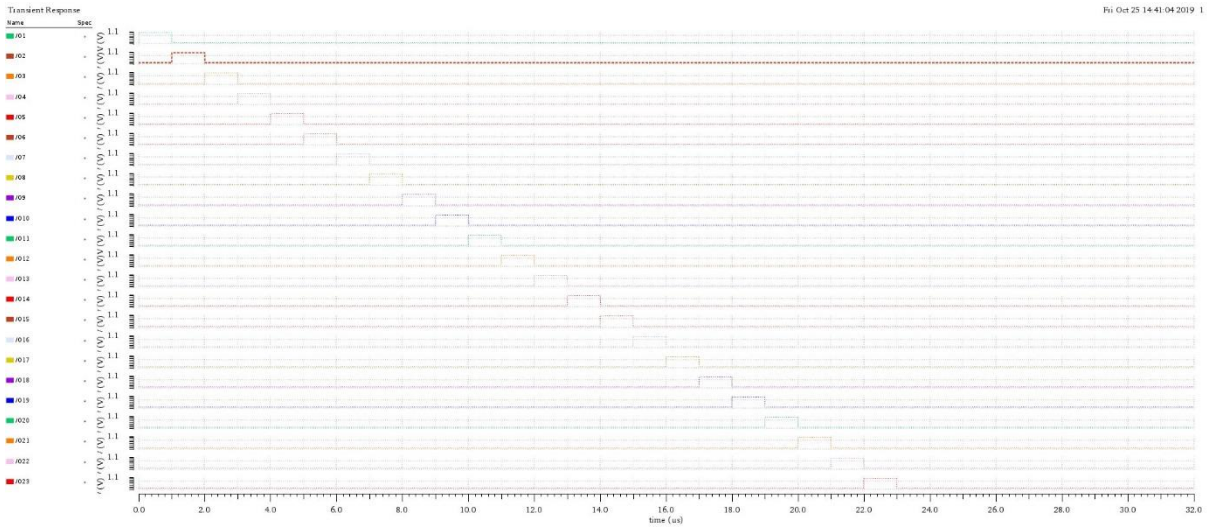
Schematic of 32 bit decoder design with a predecoder circuit.

Testbench



Schematic of 32 bit decoder test bench

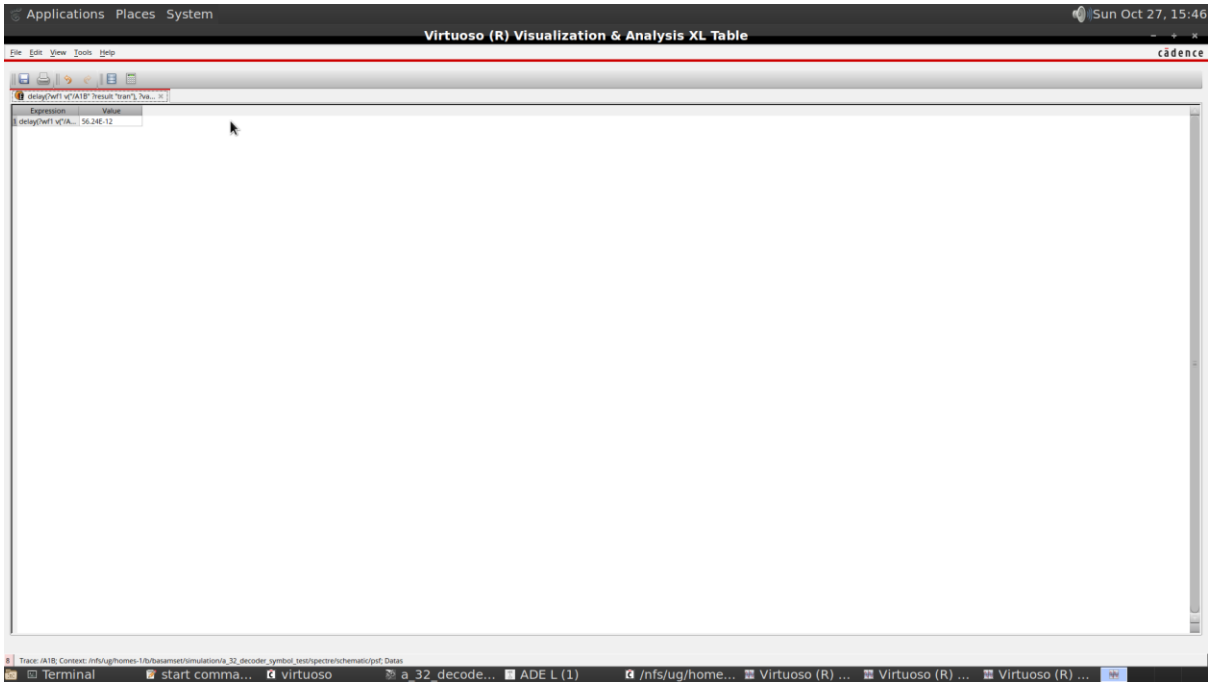
For the test bench an output load capacitor of 138f F was used and shaping inverters were used at input stage.



The figure shows the output of the 32-bit Decoder

Q 2.2 Delay measurement

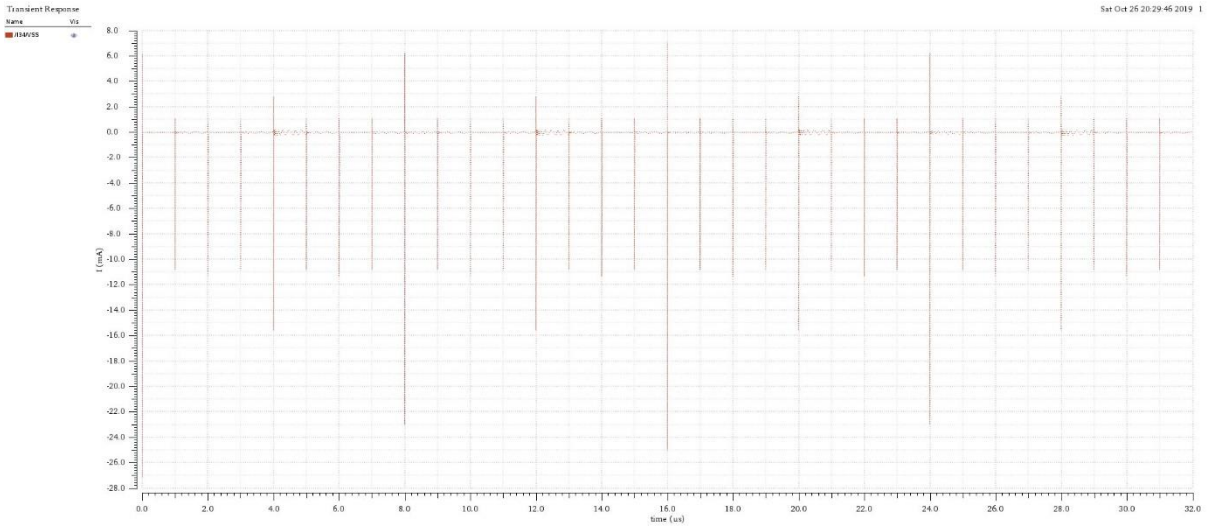
The propagation delay can be calculated by calculating the difference between input and output waveforms.



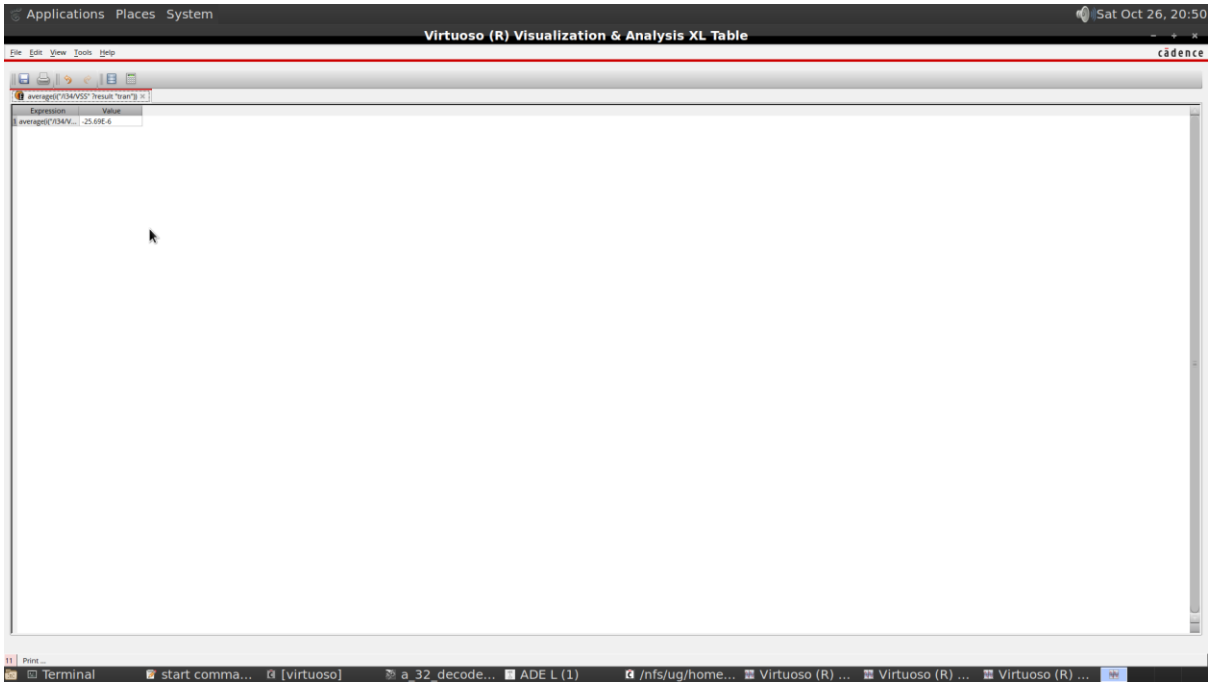
Screenshot of calculated delay

The propagation delay was found to be 56.24p sec.

Q 2.3 Simulated value for the total power dissipation



Screenshot of Average current waveform



Screenshot of Value of current

The power is given as P=V*I

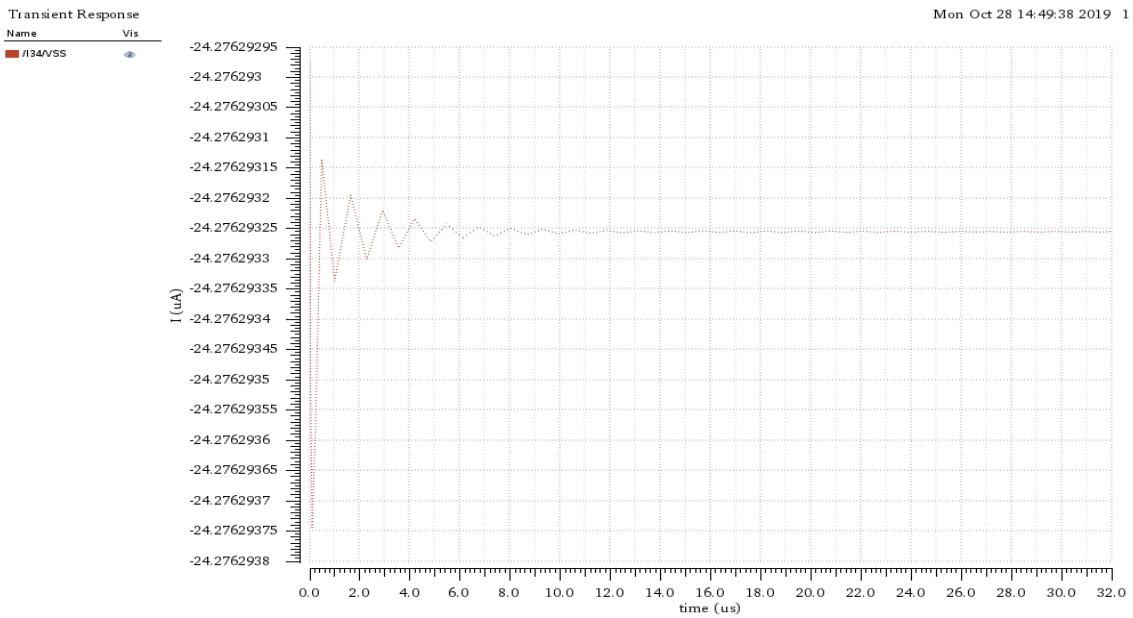
The voltage is 1v

So the total power is 25.69µW

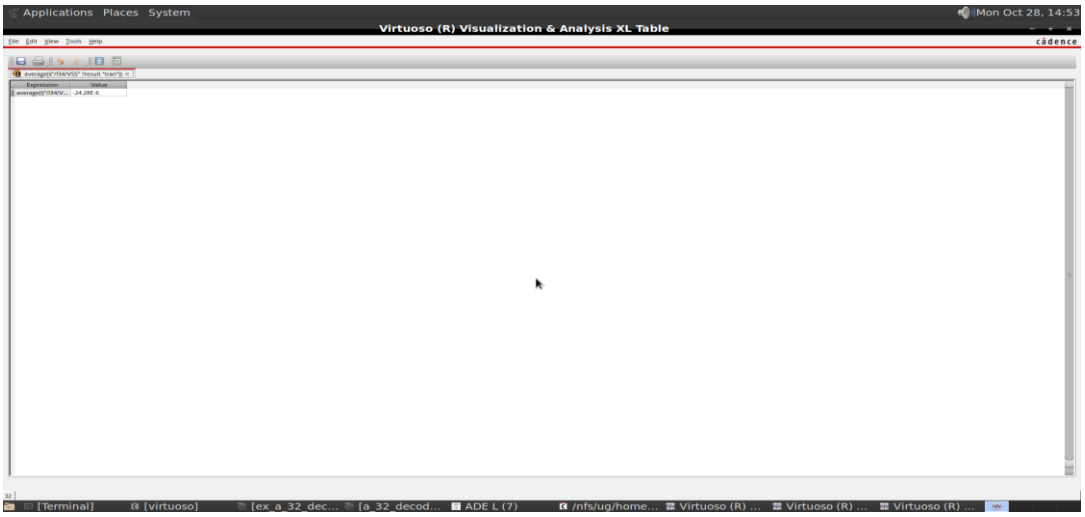
Q 2.4 Static power measurement

Static power is consumed even when a chip is not switching.

All the sources are changed to DC sources of 1V to measure the static power.



The figure shows the Static current Graph.



Screenshot of measured Static current value

Power=V*i

=1v*24.2uA

=24.28uW

Therefore the simulated static power is 24.28uW

Q 2.5 Dynamic power calculation

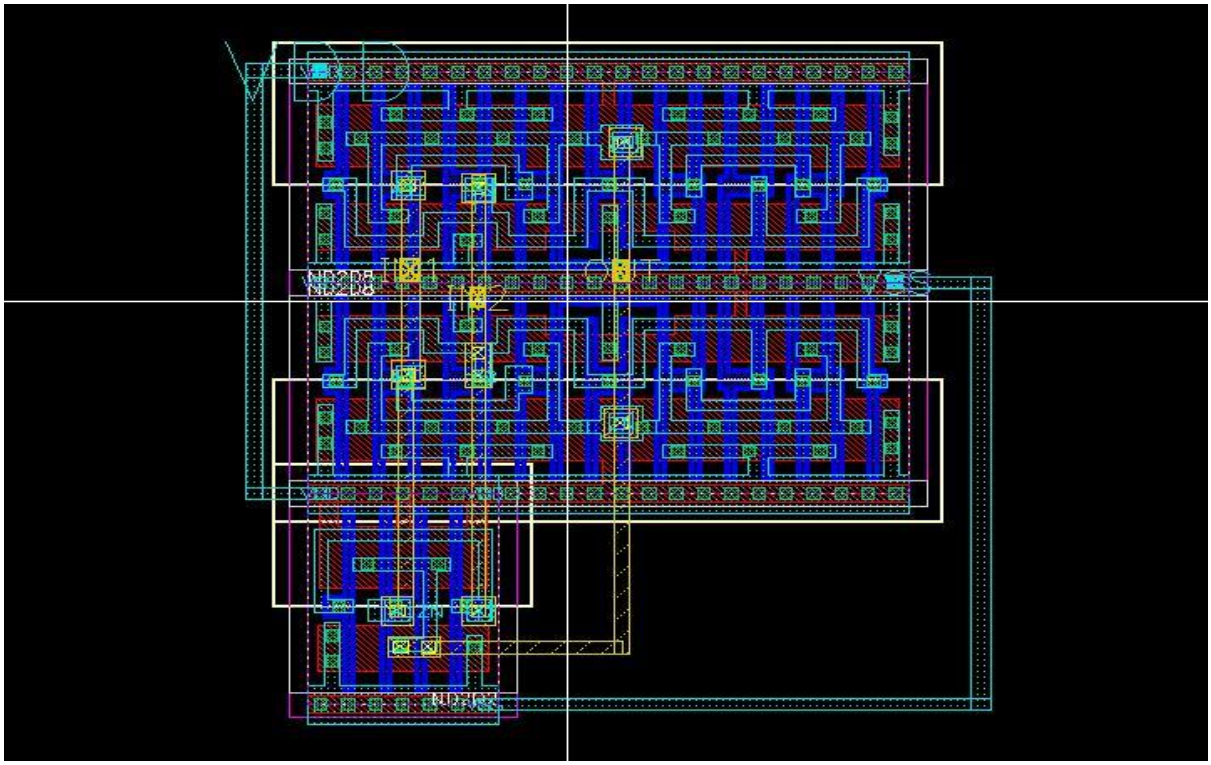
Total power= Static Power + Dynamic Power

Dynamic power = Total power- Static power

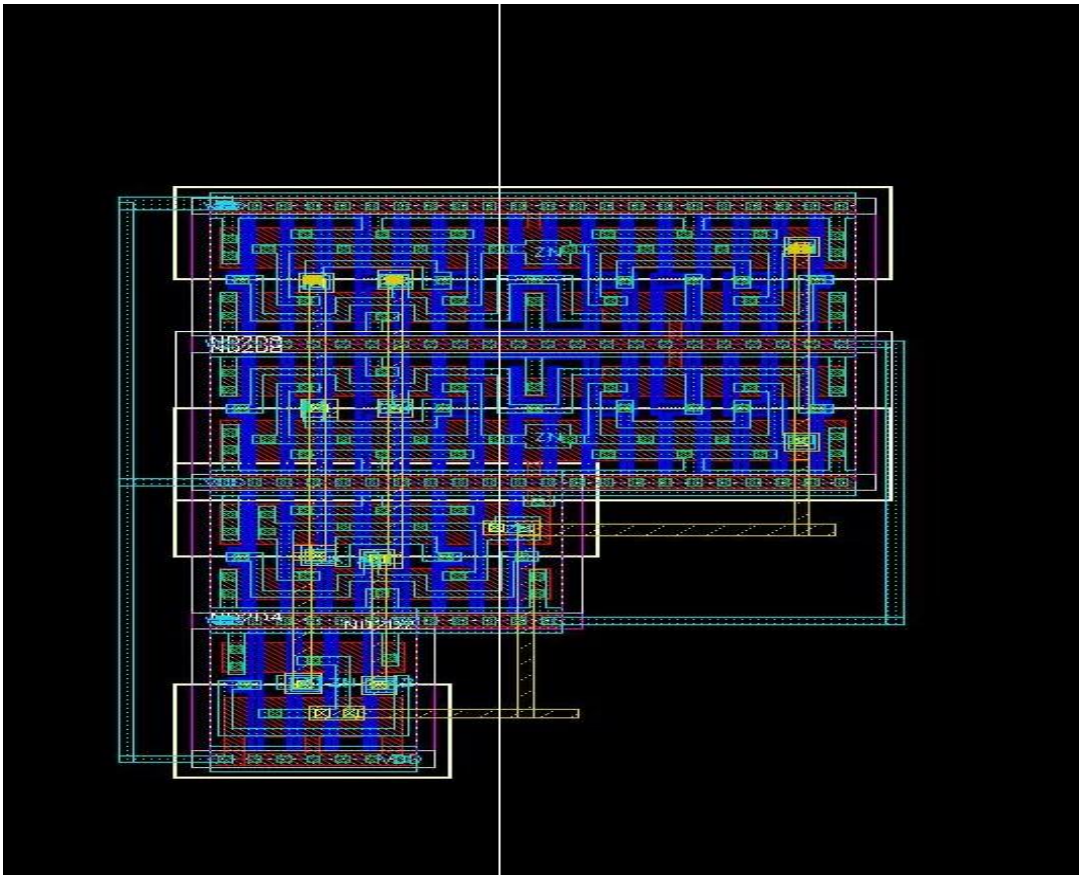
25.69-24.28= 1.39uW

Therefore the calculated dynamic power is 1.01uW

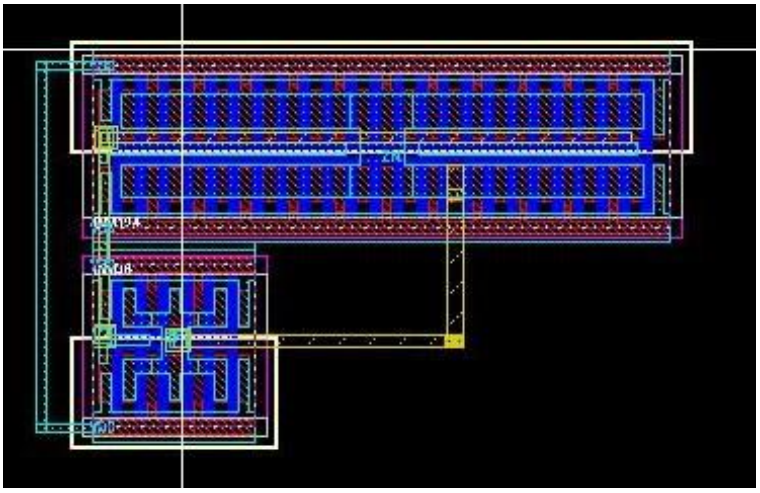
Q 3.1 Layout



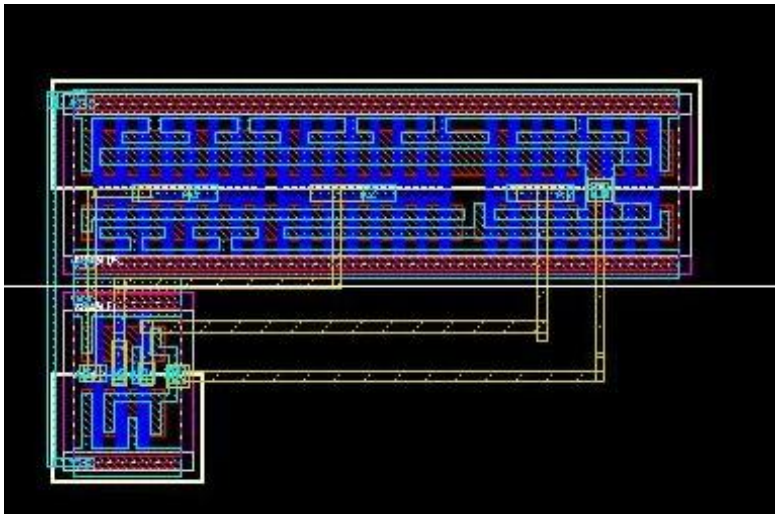
The layout of NAND2 of drive strength 18



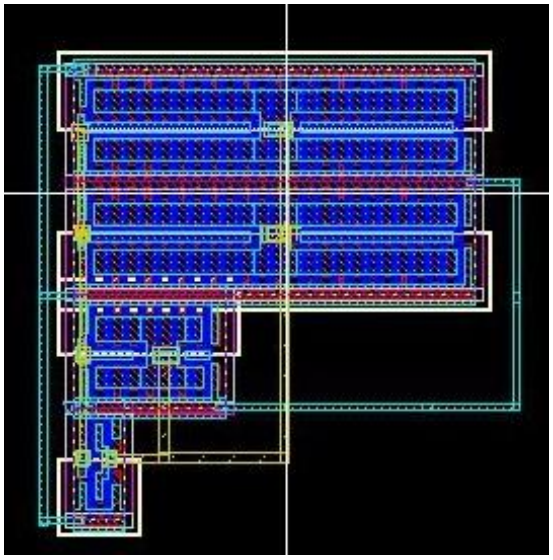
The layout of NAND2 of drive strength 22



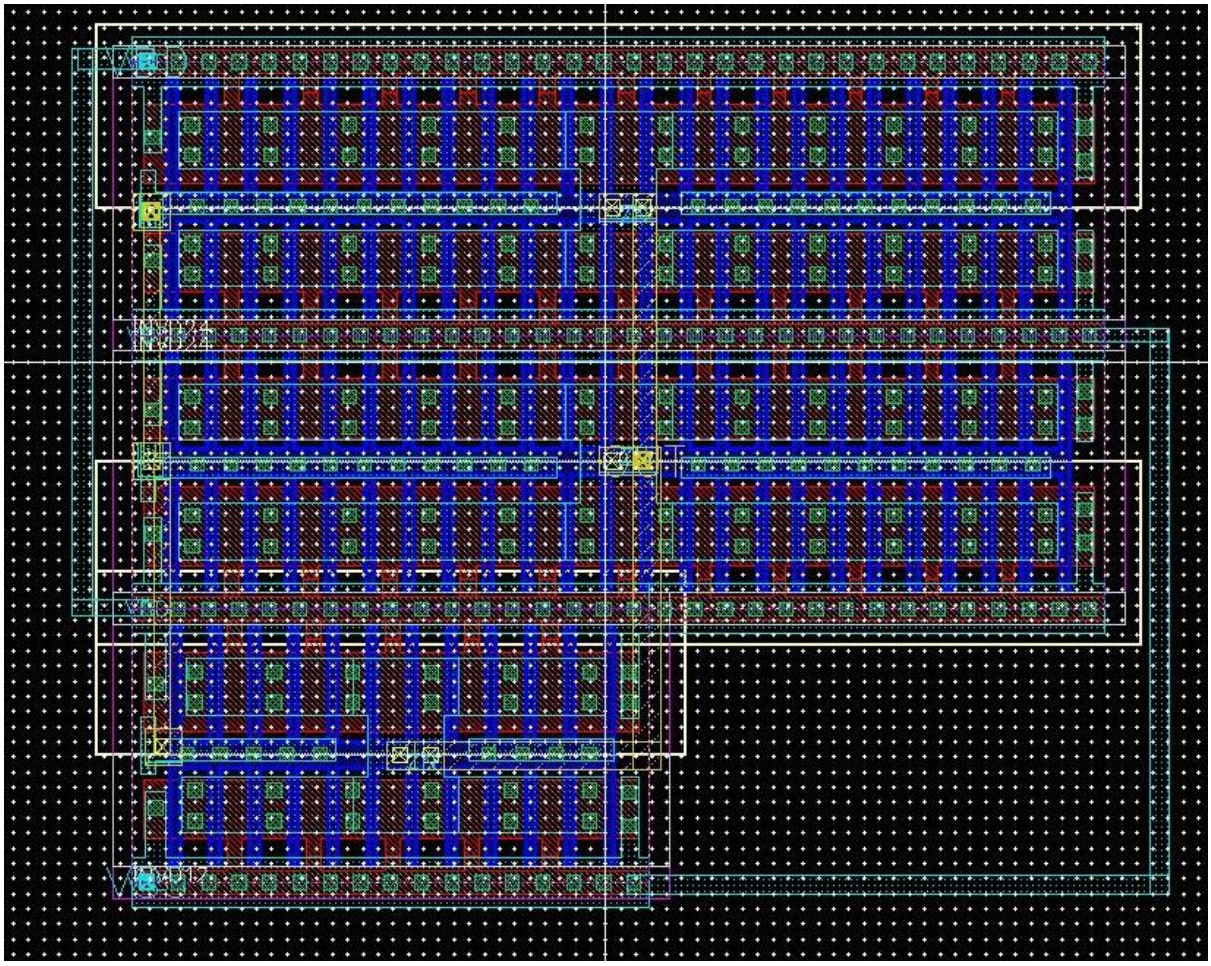
The layout of Inverter of drive strength 28



Layout of NAND 3 of drive strength 9

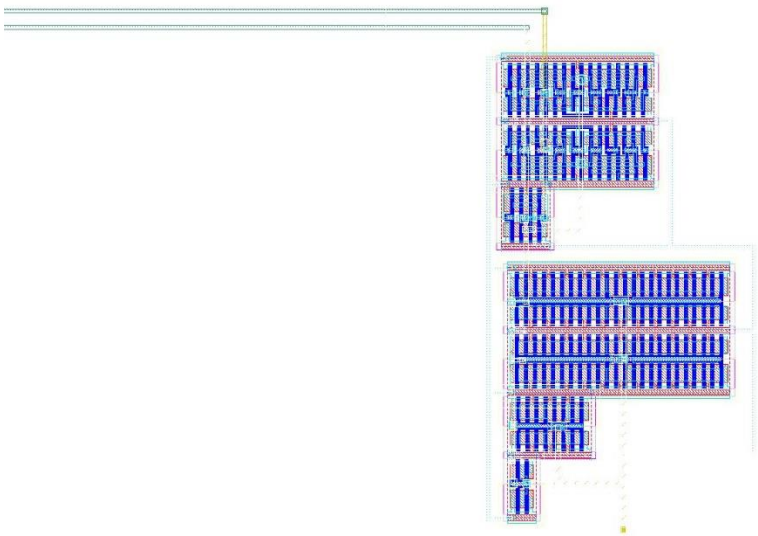


The layout of the inverter of drive strength 58

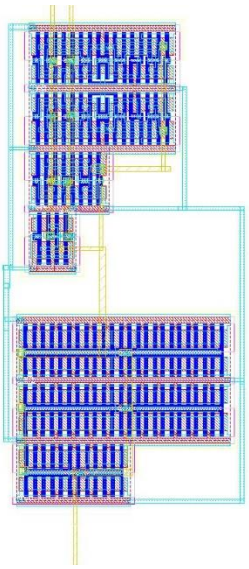


Layout of an inverter of drive strength 60

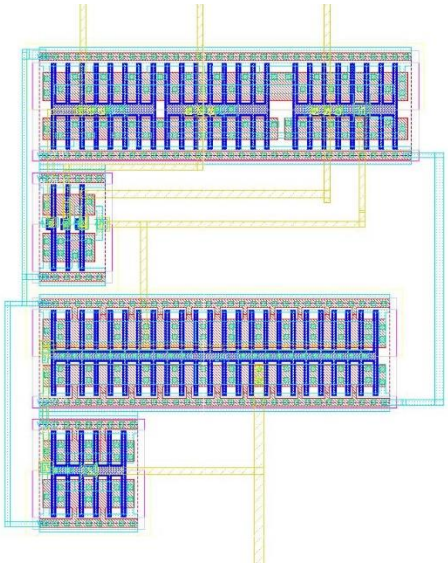
Stage-2



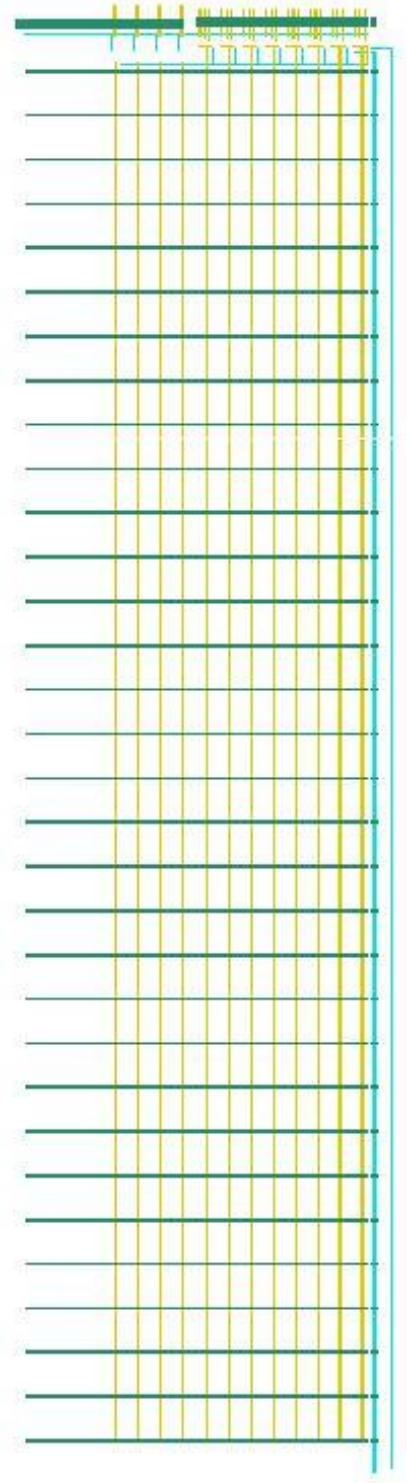
Layout of nand2-inverter



Layout of Nand2-Inverter

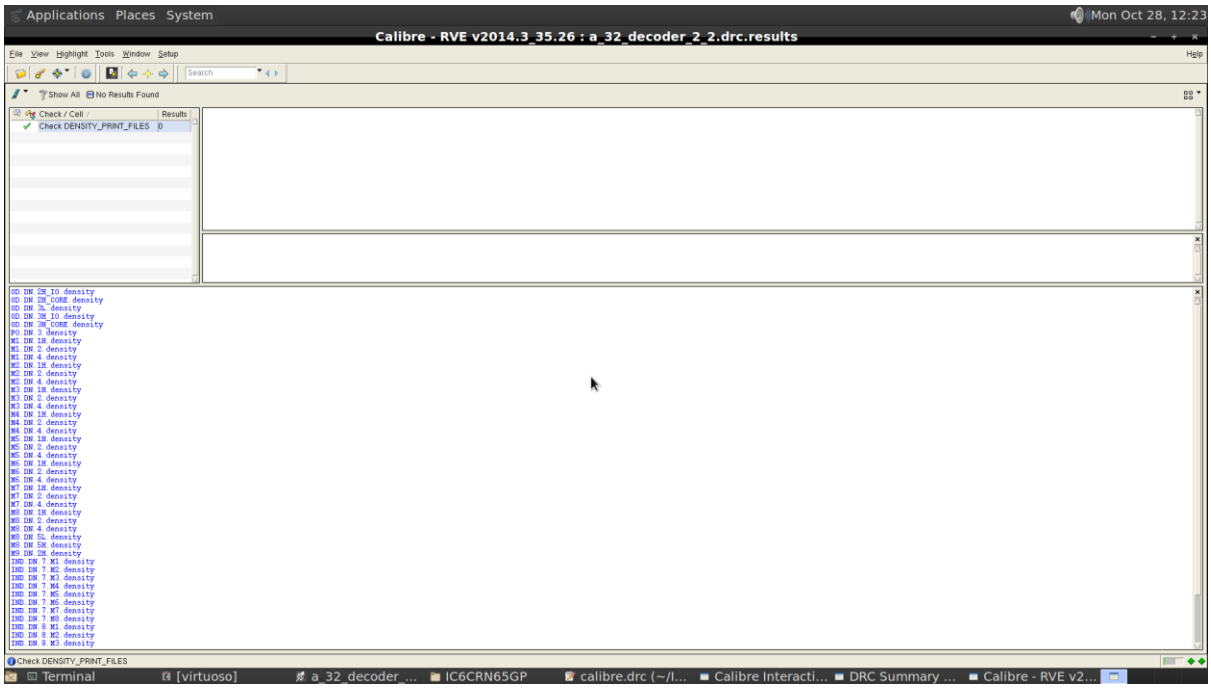


The layout of Nand2- inverter

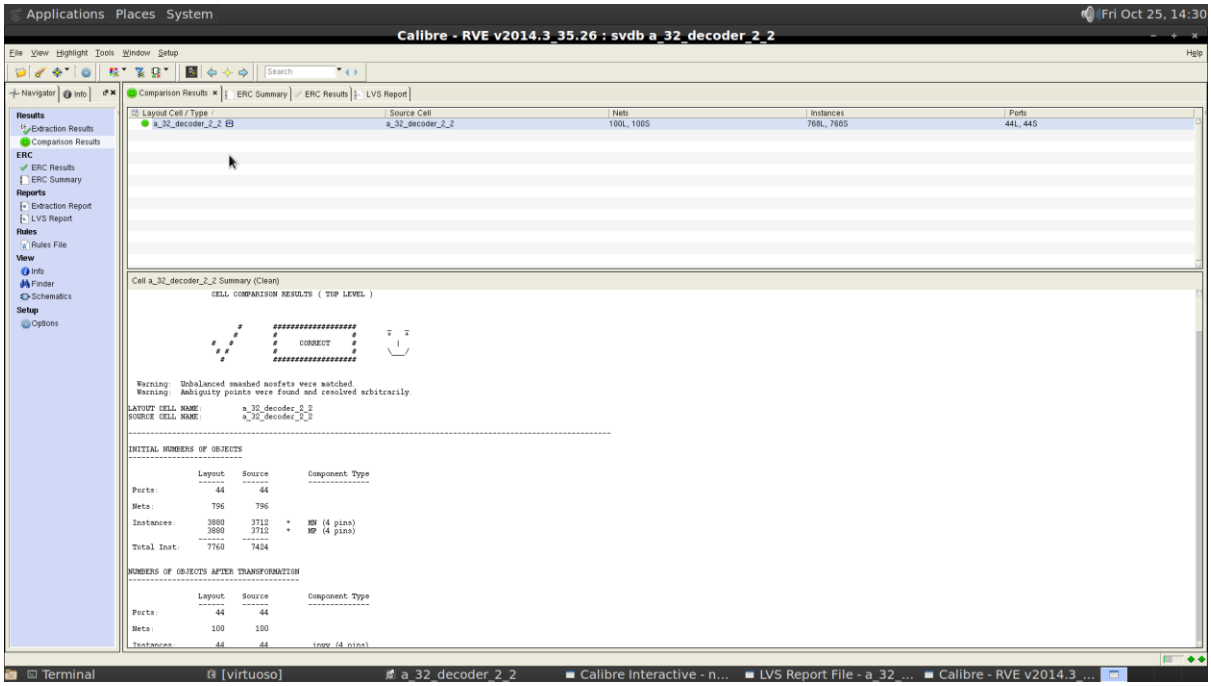


The layout of the 32-bit Decoder

DRC check



LVS report(Complete LVS report has been enclosed under appendix at the end)



##

##

C A L I B R E S Y S T E M

##

L V S R E P O R T

##

##

REPORT FILE NAME: a_32_decoder_2_2.lvs.report

LAYOUT NAME: /nfs/ug/homes-1/b/basamset/IC6CRN65GP/./CalibreLVS/a_32_decoder_2_2.sp ('a_32_decoder_2_2')

SOURCE NAME: /nfs/ug/homes-1/b/basamset/IC6CRN65GP/./CalibreLVS/a_32_decoder_2_2.src.net ('a_32_decoder_2_2')

RULE FILE: /nfs/ug/homes-1/b/basamset/IC6CRN65GP/./CalibreLVS/_calibre.lvs_

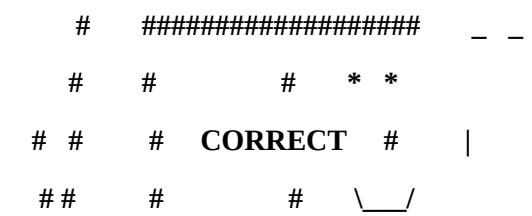
CREATION TIME: Fri Oct 25 13:48:10 2019

CURRENT DIRECTORY: /nfs/ug/homes-1/b/basamset/IC6CRN65GP/CalibreLVS

USER NAME: basamset

CALIBRE VERSION: v2014.3_35.26 Wed Oct 1 13:01:36 PDT 2014

OVERALL COMPARISON RESULTS



```
#        ###################
```

Warning: Unbalanced smashed mosfets were matched.

Warning: Ambiguity points were found and resolved arbitrarily.

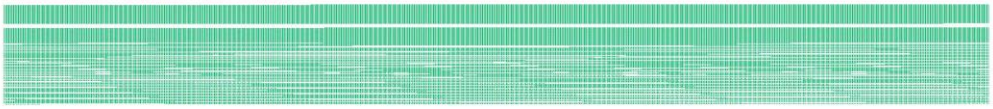
****
****

CELL SUMMARY

****
****

Result	Layout	Source
CORRECT	a_32_decoder_2_2	a_32_decoder_2_2

Q 3.2 Extracted view



Screenshot of Extracted View

Test bench for extracted view

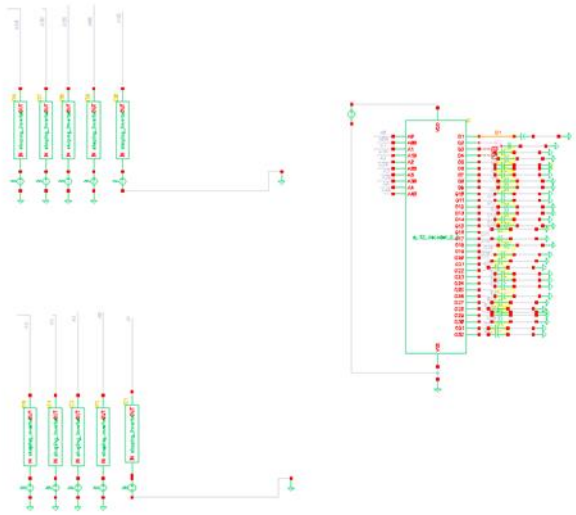
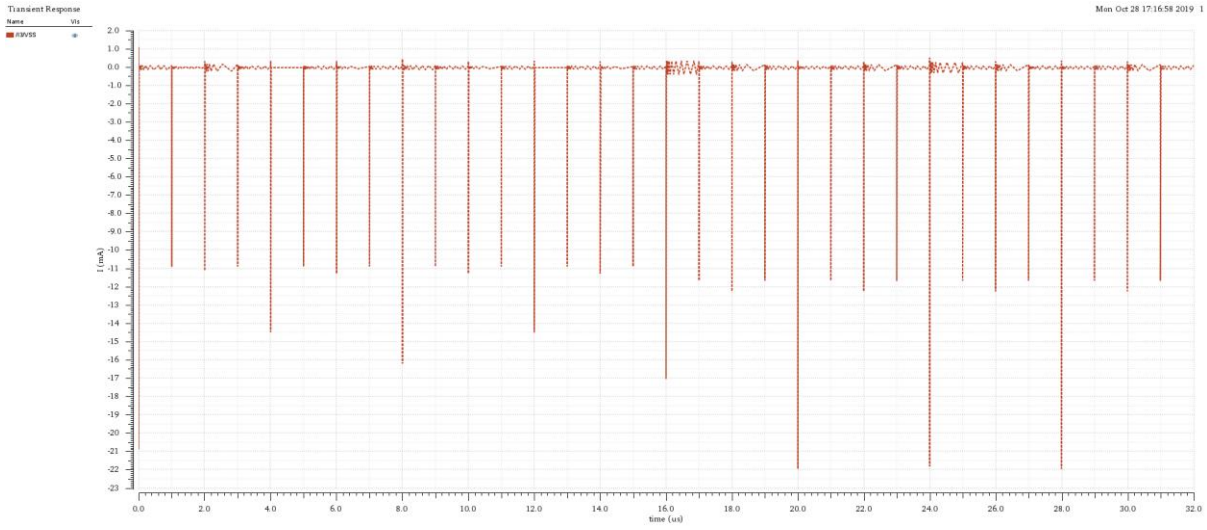
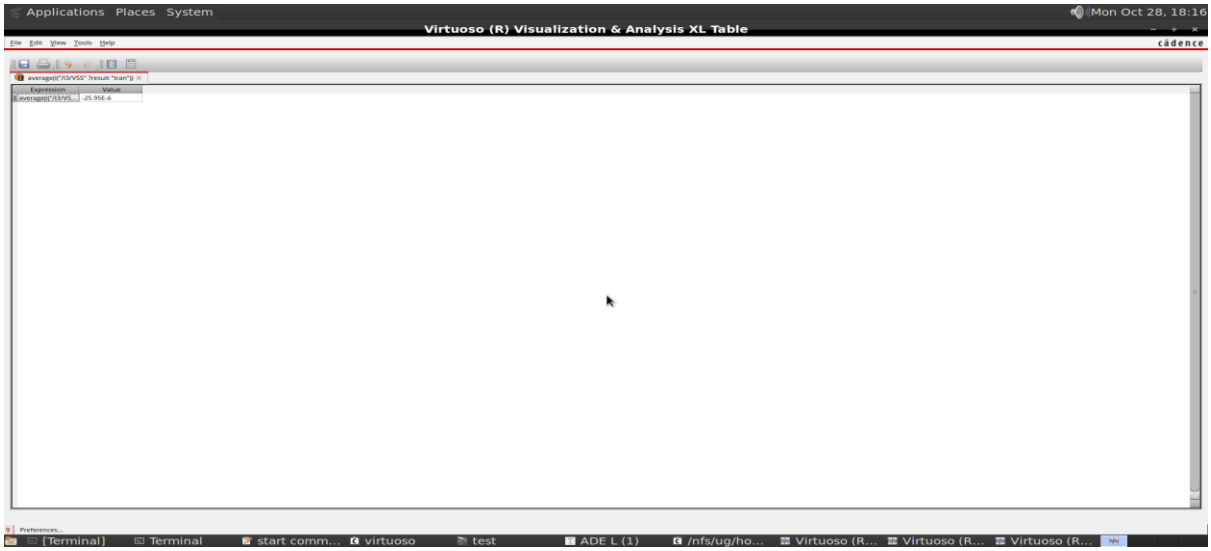


Figure shows schematic of extracted view symbol and testbench

Total power measurement

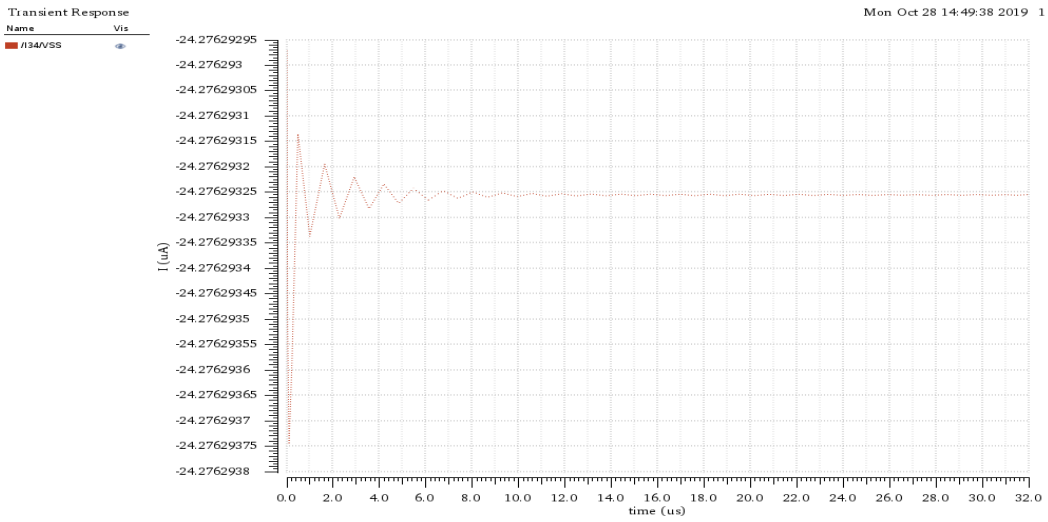


Screenshot of Total current graph



Screenshot of average total current value

Static power measurement



Screenshot of the static current graph

Screenshot of the average value of static current value

Delay= 65.55ps

Static power dissipation=24.28uW

Dynamic power dissipation=1.67uW

Total power= 25.95uW

Q 3.3 Comparision of values

Design Type	Delay	Static power dissipation	Dynamic Power Dissipation	Total Power
Calculated		-	0.14872uW	-
Schematic	56.24ps	24.38uW	1.01uW	25.69uW
Extracted	65.55ps	23.28uW	1.67uW	25.95uW

The observed differences in delays and powers are due to additional resistances and capacitances of wires in the circuit.

Appendix

```
##################################################
##                                              ##
##      C A L I B R E   S Y S T E M      ##
##                                              ##
##         L V S   R E P O R T          ##
##                                              ##
##################################################
```

REPORT FILE NAME: a_32_decoder_2_2.lvs.report

LAYOUT NAME: /nfs/ug/homes-1/b/basamset/IC6CRN65GP/./CalibreLVS/a_32_decoder_2_2.sp ('a_32_decoder_2_2')

SOURCE NAME: /nfs/ug/homes-1/b/basamset/IC6CRN65GP/./CalibreLVS/a_32_decoder_2_2.src.net ('a_32_decoder_2_2')

RULE FILE: /nfs/ug/homes-1/b/basamset/IC6CRN65GP/./CalibreLVS/_calibre.lvs_

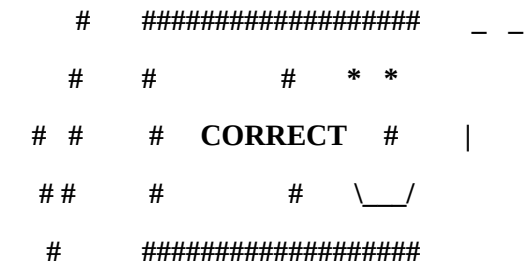
CREATION TIME: Fri Oct 25 13:48:10 2019

CURRENT DIRECTORY: /nfs/ug/homes-1/b/basamset/IC6CRN65GP/CalibreLVS

USER NAME: basamset

CALIBRE VERSION: v2014.3_35.26 Wed Oct 1 13:01:36 PDT 2014

OVERALL COMPARISON RESULTS



Warning: Unbalanced smashed mosfets were matched.

Warning: Ambiguity points were found and resolved arbitrarily.

****

CELL SUMMARY

****

Result	Layout	Source
---	---	---

CORRECT a_32_decoder_2_2 a_32_decoder_2_2

****

LVS PARAMETERS

****

o LVS Setup:

// LVS COMPONENT TYPE PROPERTY

// LVS COMPONENT SUBTYPE PROPERTY

// LVS PIN NAME PROPERTY

LVS POWER NAME "AHVDD" "AHVDDB" "AHVDDG" "AHVDDR" "AHVDDWELL" "AVDD" "AVDDB" "AVDDBG" "AVDDG" "AVDDR"

"AVDWELL" "DHVDD" "DVDD" "HVDDWELL" "TACVDD" "TAVD33" "TAVD33PST" "TAVDD" "TAVDDPST"

"VD33" "VDD" "VDD5V" "VDDG" "VDDM" "VDDPST" "VDDSA" "VDWELL"

LVS GROUND NAME "AGND" "AHVSS" "AHVSSB" "AHVSSG" "AHVSSR" "AHVSSUB" "AVSS" "AVSSB" "AVSSBG" "AVSSG"

"AVSSR" "AVSSUB" "DHVSS" "DVSS" "GND" "HVSSUB" "TAVSS" "TAVSSPST" "VS33" "VSS" "VSSG"

"VSSM" "VSSPST" "VSSUB"

LVS CELL SUPPLY NO

LVS RECOGNIZE GATES ALL

LVS IGNORE PORTS NO

LVS CHECK PORT NAMES YES

LVS IGNORE TRIVIAL NAMED PORTS NO

LVS BUILTIN DEVICE PIN SWAP YES

LVS ALL CAPACITOR PINS SWAPPABLE YES

LVS DISCARD PINS BY DEVICE NO

LVS SOFT SUBSTRATE PINS NO

LVS INJECT LOGIC YES

LVS EXPAND UNBALANCED CELLS YES

LVS FLATTEN INSIDE CELL NO

LVS EXPAND SEED PROMOTIONS NO

LVS PRESERVE PARAMETERIZED CELLS NO

LVS GLOBALS ARE PORTS YES

LVS REVERSE WL NO

LVS SPICE PREFER PINS YES

LVS SPICE SLASH IS SPACE YES

LVS SPICE ALLOW FLOATING PINS YES

// LVS SPICE ALLOW INLINE PARAMETERS

LVS SPICE ALLOW UNQUOTED STRINGS NO

LVS SPICE CONDITIONAL LDD NO

LVS SPICE CULL PRIMITIVE SUBCIRCUITS NO

LVS SPICE IMPLIED MOS AREA NO

// LVS SPICE MULTIPLIER NAME

LVS SPICE OVERRIDE GLOBALS NO

LVS SPICE REDEFINE PARAM NO

LVS SPICE REPLICATE DEVICES NO

LVS SPICE SCALE X PARAMETERS NO

LVS SPICE STRICT WL NO

// LVS SPICE OPTION

LVS STRICT SUBTYPES NO

LVS EXACT SUBTYPES NO

LAYOUT CASE YES

SOURCE CASE YES

LVS COMPARE CASE NAMES TYPES

LVS DOWNCASE DEVICE NO

LVS REPORT MAXIMUM 50

LVS PROPERTY RESOLUTION MAXIMUM 65536

// LVS SIGNATURE MAXIMUM

```
// LVS FILTER UNUSED OPTION
// LVS REPORT OPTION
LVS REPORT UNITS                YES
// LVS NON USER NAME PORT
// LVS NON USER NAME NET
// LVS NON USER NAME INSTANCE
// LVS IGNORE DEVICE PIN

// Device Type Map

LVS DEVICE TYPE                 RESISTOR "rm1" "rm10" "rm2" "rm3" "rm4" "rm5"
"rm6" "rm7" "rm8" "rm9" "rnodl" "rnodl_m"
                                "rnods" "rnods_m" "rnodwo" "rnodwo_m" "rnpolyl"
"rnpolyl_m" "rnpolys"
                                "rnpolys_m" "rnpolywo" "rnpolywo_m" "rnwod" "rnwod_m"
"rnwsti" "rnwsti_m"
                                "rpodl" "rpodl_m" "rpods" "rpods_m" "rpodwo" "rpodwo_m"
"rppolyl" "rppolyl_m"
                                "rppolyl_rf" "rppolys" "rppolys_m" "rppolys_rf" "rppolywo"
"rppolywo_m"
                                "rppolywo_rf" [ POS=PLUS NEG=MINUS ]  SOURCE
LAYOUT

// Reduction

LVS REDUCE SERIES MOS           NO
LVS REDUCE PARALLEL MOS         YES
LVS REDUCE SEMI SERIES MOS      NO
LVS REDUCE SPLIT GATES          NO
LVS REDUCE PARALLEL BIPOLAR     YES
LVS REDUCE SERIES CAPACITORS    YES
LVS REDUCE PARALLEL CAPACITORS  YES
LVS REDUCE SERIES RESISTORS     YES
LVS REDUCE PARALLEL RESISTORS   YES
```

LVS REDUCE PARALLEL DIODES YES

LVS REDUCE rnwsti_m PARALLEL [TOLERANCE lr 0]

LVS REDUCE rnwsti_m SERIES PLUS MINUS [TOLERANCE wr 0]

LVS REDUCE rnwod_m PARALLEL [TOLERANCE lr 0]

LVS REDUCE rnwod_m SERIES PLUS MINUS [TOLERANCE wr 0]

LVS REDUCE rpodwo_m PARALLEL [TOLERANCE lr 0]

LVS REDUCE rpodwo_m SERIES PLUS MINUS [TOLERANCE wr 0]

LVS REDUCE rnodwo_m PARALLEL [TOLERANCE lr 0]

LVS REDUCE rnodwo_m SERIES PLUS MINUS [TOLERANCE wr 0]

LVS REDUCE rpodl_m PARALLEL [TOLERANCE lr 0]

LVS REDUCE rpodl_m SERIES PLUS MINUS [TOLERANCE wr 0]

LVS REDUCE rnodl_m PARALLEL [TOLERANCE lr 0]

LVS REDUCE rnodl_m SERIES PLUS MINUS [TOLERANCE wr 0]

LVS REDUCE rpods_m PARALLEL [TOLERANCE lr 0]

LVS REDUCE rpods_m SERIES PLUS MINUS [TOLERANCE wr 0]

LVS REDUCE rnods_m PARALLEL [TOLERANCE lr 0]

LVS REDUCE rnods_m SERIES PLUS MINUS [TOLERANCE wr 0]

LVS REDUCE rppolys_m PARALLEL [TOLERANCE lr 0]

LVS REDUCE rppolys_m SERIES PLUS MINUS [TOLERANCE wr 0]

LVS REDUCE rnpolys_m PARALLEL [TOLERANCE lr 0]

LVS REDUCE rnpolys_m SERIES PLUS MINUS [TOLERANCE wr 0]

LVS REDUCE rppolyl_m PARALLEL [TOLERANCE lr 0]

LVS REDUCE rppolyl_m SERIES PLUS MINUS [TOLERANCE wr 0]

LVS REDUCE rnpolyl_m PARALLEL [TOLERANCE lr 0]

LVS REDUCE rnpolyl_m SERIES PLUS MINUS [TOLERANCE wr 0]

LVS REDUCE rppolywo_m PARALLEL [TOLERANCE lr 0]

LVS REDUCE rppolywo_m SERIES PLUS MINUS [TOLERANCE wr 0]

LVS REDUCE rnpolywo_m PARALLEL [TOLERANCE lr 0]

LVS REDUCE rnpolywo_m SERIES PLUS MINUS [TOLERANCE wr 0]

LVS REDUCE rppolyl_rf PARALLEL NO

LVS REDUCE rppolyl_rf SERIES PLUS MINUS NO

LVS REDUCE rppolys_rf PARALLEL NO

LVS REDUCE rppolys_rf SERIES PLUS MINUS NO

LVS REDUCE rppolywo_rf PARALLEL NO

LVS REDUCE rppolywo_rf SERIES PLUS MINUS NO

LVS REDUCTION PRIORITY PARALLEL

LVS SHORT EQUIVALENT NODES NO

// Trace Property

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TRACE PROPERTY crtmom_mx mf mf 0

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TRACE PROPERTY moscap_rf33_nw gr gr 0

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TRACE PROPERTY pmos_rf_25_nwod lr lr 0

TRACE PROPERTY pmos_rf_25_nwod nr nr 0

TRACE PROPERTY pmos_rf_25_nwud wr wr 0

TRACE PROPERTY pmos_rf_25_nwud lr lr 0

TRACE PROPERTY pmos_rf_25_nwud nr nr 0

TRACE PROPERTY pmos_rf_25od wr wr 0

TRACE PROPERTY pmos_rf_25od lr lr 0

TRACE PROPERTY pmos_rf_25od nr nr 0

TRACE PROPERTY pmos_rf_25od33_5t wr wr 0

TRACE PROPERTY pmos_rf_25od33_5t lr lr 0

TRACE PROPERTY pmos_rf_25od33_5t nr nr 0

TRACE PROPERTY pmos_rf_25od33_nw_5t wr wr 0

TRACE PROPERTY pmos_rf_25od33_nw_5t lr lr 0

TRACE PROPERTY pmos_rf_25od33_nw_5t nr nr 0

TRACE PROPERTY pmos_rf_25ud wr wr 0

TRACE PROPERTY pmos_rf_25ud lr lr 0

TRACE PROPERTY pmos_rf_25ud nr nr 0

TRACE PROPERTY pmos_rf_25ud18_5t wr wr 0

TRACE PROPERTY pmos_rf_25ud18_5t lr lr 0

TRACE PROPERTY pmos_rf_25ud18_5t nr nr 0

TRACE PROPERTY pmos_rf_25ud18_nw_5t wr wr 0

TRACE PROPERTY pmos_rf_25ud18_nw_5t lr lr 0

TRACE PROPERTY pmos_rf_25ud18_nw_5t nr nr 0

TRACE PROPERTY pmos_rf_33 wr wr 0

TRACE PROPERTY pmos_rf_33 lr lr 0

TRACE PROPERTY pmos_rf_33 nr nr 0

TRACE PROPERTY pmos_rf_33_5t wr wr 0

TRACE PROPERTY pmos_rf_33_5t lr lr 0

TRACE PROPERTY pmos_rf_33_5t nr nr 0

TRACE PROPERTY pmos_rf_33_nw wr wr 0

TRACE PROPERTY pmos_rf_33_nw lr lr 0

TRACE PROPERTY pmos_rf_33_nw nr nr 0

TRACE PROPERTY pmos_rf_33_nw_5t wr wr 0

TRACE PROPERTY pmos_rf_33_nw_5t lr lr 0

TRACE PROPERTY pmos_rf_33_nw_5t nr nr 0

TRACE PROPERTY pmos_rf_5t wr wr 0

TRACE PROPERTY pmos_rf_5t lr lr 0

TRACE PROPERTY pmos_rf_5t nr nr 0

TRACE PROPERTY pmos_rf_hvt wr wr 0

TRACE PROPERTY pmos_rf_hvt lr lr 0

TRACE PROPERTY pmos_rf_hvt nr nr 0

TRACE PROPERTY pmos_rf_hvt_5t wr wr 0

TRACE PROPERTY pmos_rf_hvt_5t lr lr 0

TRACE PROPERTY pmos_rf_hvt_5t nr nr 0

TRACE PROPERTY pmos_rf_hvt_nw wr wr 0

TRACE PROPERTY pmos_rf_hvt_nw lr lr 0

TRACE PROPERTY pmos_rf_hvt_nw nr nr 0

TRACE PROPERTY pmos_rf_hvt_nw_5t wr wr 0

TRACE PROPERTY pmos_rf_hvt_nw_5t lr lr 0

TRACE PROPERTY pmos_rf_hvt_nw_5t nr nr 0

TRACE PROPERTY pmos_rf_lvt wr wr 0

TRACE PROPERTY pmos_rf_lvt lr lr 0

TRACE PROPERTY pmos_rf_lvt nr nr 0

TRACE PROPERTY pmos_rf_lvt_5t wr wr 0

TRACE PROPERTY pmos_rf_lvt_5t lr lr 0

TRACE PROPERTY pmos_rf_lvt_5t nr nr 0

TRACE PROPERTY pmos_rf_lvt_nw wr wr 0

TRACE PROPERTY pmos_rf_lvt_nw lr lr 0

TRACE PROPERTY pmos_rf_lvt_nw nr nr 0

TRACE PROPERTY pmos_rf_lvt_nw_5t wr wr 0

TRACE PROPERTY pmos_rf_lvt_nw_5t lr lr 0

TRACE PROPERTY pmos_rf_lvt_nw_5t nr nr 0

TRACE PROPERTY pmos_rf_mlvt wr wr 0

TRACE PROPERTY pmos_rf_mlvt lr lr 0

TRACE PROPERTY pmos_rf_mlvt nr nr 0

TRACE PROPERTY pmos_rf_mlvt_5t wr wr 0

TRACE PROPERTY pmos_rf_mlvt_5t lr lr 0

TRACE PROPERTY pmos_rf_mlvt_5t nr nr 0

TRACE PROPERTY pmos_rf_mlvt_nw wr wr 0

TRACE PROPERTY pmos_rf_mlvt_nw lr lr 0

TRACE PROPERTY pmos_rf_mlvt_nw nr nr 0

TRACE PROPERTY pmos_rf_mlvt_nw_5t wr wr 0

TRACE PROPERTY pmos_rf_mlvt_nw_5t lr lr 0

TRACE PROPERTY pmos_rf_mlvt_nw_5t nr nr 0

TRACE PROPERTY pmos_rf_nw wr wr 0

TRACE PROPERTY pmos_rf_nw lr lr 0

TRACE PROPERTY pmos_rf_nw nr nr 0

TRACE PROPERTY pmos_rf_nw_5t wr wr 0

TRACE PROPERTY pmos_rf_nw_5t lr lr 0

TRACE PROPERTY pmos_rf_nw_5t nr nr 0

TRACE PROPERTY pmoscap_rf lr lr 0

TRACE PROPERTY pmoscap_rf wr wr 0

TRACE PROPERTY pmoscap_rf br br 0

TRACE PROPERTY pmoscap_rf gr gr 0

TRACE PROPERTY pmoscap_rf18 lr lr 0

TRACE PROPERTY pmoscap_rf18 wr wr 0

TRACE PROPERTY pmoscap_rf18 br br 0

TRACE PROPERTY pmoscap_rf18 gr gr 0

TRACE PROPERTY pmoscap_rf25 lr lr 0

TRACE PROPERTY pmoscap_rf25 wr wr 0

TRACE PROPERTY pmoscap_rf25 br br 0

TRACE PROPERTY pmoscap_rf25 gr gr 0

TRACE PROPERTY probe1 a a 0

TRACE PROPERTY probe1 pj pj 0

TRACE PROPERTY probe2 a a 0

TRACE PROPERTY probe2 pj pj 0

TRACE PROPERTY probe3 a a 0

TRACE PROPERTY probe3 pj pj 0

TRACE PROPERTY probe4 a a 0

TRACE PROPERTY probe4 pj pj 0

TRACE PROPERTY probe5 a a 0

TRACE PROPERTY probe5 pj pj 0

TRACE PROPERTY probe6 a a 0

TRACE PROPERTY probe6 pj pj 0

TRACE PROPERTY probe7 a a 0

TRACE PROPERTY probe7 pj pj 0

TRACE PROPERTY rm1 w w 0

TRACE PROPERTY rm1 l l 0

TRACE PROPERTY rm10 w w 0

TRACE PROPERTY rm10 l l 0

TRACE PROPERTY rm2 w w 0

TRACE PROPERTY rm2 l l 0

TRACE PROPERTY rm3 w w 0

TRACE PROPERTY rm3 l l 0

TRACE PROPERTY rm4 w w 0

TRACE PROPERTY rm4 l l 0

TRACE PROPERTY rm5 w w 0

TRACE PROPERTY rm5 l l 0

TRACE PROPERTY rm6 w w 0

TRACE PROPERTY rm6 l l 0

TRACE PROPERTY rm7 w w 0

TRACE PROPERTY rm7 l l 0

TRACE PROPERTY rm8 w w 0

TRACE PROPERTY rm8 l l 0

TRACE PROPERTY rm9 w w 0

TRACE PROPERTY rm9 l l 0

TRACE PROPERTY rnodl l l 0

TRACE PROPERTY rnodl w w 0

TRACE PROPERTY rnodl_m lr lr 0

TRACE PROPERTY rnodl_m wr wr 0

TRACE PROPERTY rnods l l 0

TRACE PROPERTY rnods w w 0

TRACE PROPERTY rnods_m lr lr 0

TRACE PROPERTY rnods_m wr wr 0

TRACE PROPERTY rnodwo l l 0

TRACE PROPERTY rnodwo w w 0

TRACE PROPERTY rnodwo_m lr lr 0

TRACE PROPERTY rnodwo_m wr wr 0

TRACE PROPERTY rnpolyl l l 0

TRACE PROPERTY rnpolyl w w 0

TRACE PROPERTY rnpolyl_m lr lr 0

TRACE PROPERTY rnpolyl_m wr wr 0

TRACE PROPERTY rnpolys l l 0

TRACE PROPERTY rnpolys w w 0

TRACE PROPERTY rnpolys_m lr lr 0

TRACE PROPERTY rnpolys_m wr wr 0

TRACE PROPERTY rnpolywo l l 0

TRACE PROPERTY rnpolywo w w 0

TRACE PROPERTY rnpolywo_m lr lr 0

TRACE PROPERTY rnpolywo_m wr wr 0

TRACE PROPERTY rnwod l l 0

TRACE PROPERTY rnwod w w 0

TRACE PROPERTY rnwod_m lr lr 0

TRACE PROPERTY rnwod_m wr wr 0

TRACE PROPERTY rnwsti l l 0

TRACE PROPERTY rnwsti w w 0

TRACE PROPERTY rnwsti_m lr lr 0

TRACE PROPERTY rnwsti_m wr wr 0

TRACE PROPERTY rpodl l l 0

TRACE PROPERTY rpodl w w 0

TRACE PROPERTY rpodl_m lr lr 0

TRACE PROPERTY rpodl_m wr wr 0

TRACE PROPERTY rpods l l 0

TRACE PROPERTY rpods w w 0

TRACE PROPERTY rpods_m lr lr 0

TRACE PROPERTY rpods_m wr wr 0

TRACE PROPERTY rpodwo l l 0

TRACE PROPERTY rpodwo w w 0

TRACE PROPERTY rpodwo_m lr lr 0

TRACE PROPERTY rpodwo_m wr wr 0

TRACE PROPERTY rppolyl l l 0

TRACE PROPERTY rppolyl w w 0

TRACE PROPERTY rppolyl_m lr lr 0

TRACE PROPERTY rppolyl_m wr wr 0

TRACE PROPERTY rppolyl_rf w w 0

TRACE PROPERTY rppolyl_rf l l 0

TRACE PROPERTY rppolys l l 0

TRACE PROPERTY rppolys w w 0

TRACE PROPERTY rppolys_m lr lr 0

TRACE PROPERTY rppolys_m wr wr 0

TRACE PROPERTY rppolys_rf w w 0

TRACE PROPERTY rppolys_rf l l 0

TRACE PROPERTY rppolywo l l 0

TRACE PROPERTY rppolywo w w 0

TRACE PROPERTY rppolywo_m lr lr 0

TRACE PROPERTY rppolywo_m wr wr 0

TRACE PROPERTY rppolywo_rf w w 0

TRACE PROPERTY rppolywo_rf l l 0

TRACE PROPERTY sbd_rf nf nf 0

TRACE PROPERTY sbd_rf w w 0

TRACE PROPERTY sbd_rf l l 0

TRACE PROPERTY sbd_rf_nw nf nf 0

TRACE PROPERTY sbd_rf_nw w w 0

TRACE PROPERTY sbd_rf_nw l l 0

TRACE PROPERTY spiral_std_mu_z lay lay 0

TRACE PROPERTY spiral_std_mu_z w w 0.05

TRACE PROPERTY spiral_std_mu_z nr nr 0

TRACE PROPERTY spiral_std_mu_z rad rad 0

TRACE PROPERTY spiral_std_mu_z gdis gdis 0

TRACE PROPERTY spiral_std_mu_z spacing spacing 0

TRACE PROPERTY spiral_sym_ct_mu_z lay lay 0

TRACE PROPERTY spiral_sym_ct_mu_z w w 0.05

TRACE PROPERTY spiral_sym_ct_mu_z nr nr 0

TRACE PROPERTY spiral_sym_ct_mu_z rad rad 0

TRACE PROPERTY spiral_sym_ct_mu_z gdis gdis 0

TRACE PROPERTY spiral_sym_ct_mu_z spacing spacing 0

TRACE PROPERTY spiral_sym_mu_z lay lay 0

TRACE PROPERTY spiral_sym_mu_z w w 0.05

TRACE PROPERTY spiral_sym_mu_z nr nr 0

TRACE PROPERTY spiral_sym_mu_z rad rad 0

TRACE PROPERTY spiral_sym_mu_z gdis gdis 0

TRACE PROPERTY spiral_sym_mu_z spacing spacing 0

TRACE PROPERTY xjvar w w 0

TRACE PROPERTY xjvar l l 0

TRACE PROPERTY xjvar nr nr 0

TRACE PROPERTY xjvar_nw w w 0

TRACE PROPERTY xjvar_nw l l 0

TRACE PROPERTY xjvar_nw nr nr 0

CELL COMPARISON RESULTS (TOP LEVEL)

 # ################## _ _

 # # # * *

 # # # CORRECT # |

Warning: Unbalanced smashed mosfets were matched.

Warning: Ambiguity points were found and resolved arbitrarily.

LAYOUT CELL NAME: a_32_decoder_2_2

SOURCE CELL NAME: a_32_decoder_2_2

INITIAL NUMBERS OF OBJECTS

	Layout	Source	Component Type
Ports:	**44**	**44**	
Nets:	**796**	**796**	
Instances:	**3880**	**3712**	* MN (4 pins)
	3880	**3712**	* MP (4 pins)
Total Inst:	**7760**	**7424**	

NUMBERS OF OBJECTS AFTER TRANSFORMATION

	Layout	Source	Component Type

Ports: 44 44

Nets: 100 100

Instances: 44 44 _invv (4 pins)
36 36 _pup2v (4 pins)
8 8 _pup3v (5 pins)
664 664 _sdw2v (4 pins)
16 16 _sdw3v (5 pins)
------ ------
Total Inst: 768 768

*** = Number of objects in layout different from number in source.**

****
****

INFORMATION AND WARNINGS

****
****

	Matched Layout	Matched Source	Unmatched Layout	Unmatched Source	Component Type
Ports:	44	44	0	0	
Nets:	100	100	0	0	
Instances:	44	44	0	0	_invv
	36	36	0	0	_pup2v

8 8 0 0 _pup3v

664 664 0 0 _sdw2v

16 16 0 0 _sdw3v

------- ------- --------- ---------

Total Inst: 768 768 0 0

o Statistics:

6408 layout mos transistors were reduced to 208.

6200 mos transistors were deleted by parallel reduction.

6048 source mos transistors were reduced to 184.

5864 mos transistors were deleted by parallel reduction.

64 instances were matched arbitrarily.

o Initial Correspondence Points:

Ports: VDD VSS A0 A1 A1B A0B A4 A3 A2 A4B A3B A2B O32 O31 O30 O29 O28 O27 O26 O25 O24

O23 O22 O21 O20 O19 O18 O17 O16 O15 O14 O13 O12 O11 O10 O9 O8 O7 O6 O5 O4 O3 O2

O1

o Ambiguity Resolution Points:

(Each one of the following objects belongs to a group of indistinguishable objects.

The listed objects were matched arbitrarily by the Ambiguity Resolution feature of LVS.

Arbitrary matching may be prevented by assigning names to these objects or to adjacent nets).

Layout **Source**

------ **------**

Instances

(_sdw2v) **(_sdw2v)**

Devices:

X19/X24/M15(6.490,-316.085) MN(nch) **XI269/XI3/MMU3_1-M_u4 MN(nch)**

X19/X24/M14(6.205,-316.085) MN(nch) **XI269/XI3/MMU3_1-M_u3 MN(nch)**

(_sdw2v) **(_sdw2v)**

Devices:

X19/X24/M13(5.945,-316.085) MN(nch) **XI269/XI3/MMU3_0-M_u3 MN(nch)**

X19/X24/M12(5.685,-316.085) MN(nch) **XI269/XI3/MMU3_0-M_u4 MN(nch)**

(_sdw2v) **(_sdw2v)**

Devices:

X19/X24/M11(5.445,-316.085) MN(nch) **XI269/XI0/MMI25 MN(nch)**

X19/X24/M10(5.255,-316.085) MN(nch) **XI269/XI0/MMI26 MN(nch)**

(_sdw2v) **(_sdw2v)**

Devices:

X19/X24/M4(3.695,-316.085) MN(nch) **XI269/XI0/MMI28 MN(nch)**

X19/X24/M5(3.955,-316.085) MN(nch) **XI269/XI0/MMI27 MN(nch)**

(_sdw2v) **(_sdw2v)**

Devices:

X19/X24/M3(3.435,-316.085) MN(nch) **XI269/XI0/MMI24 MN(nch)**

X19/X24/M2(3.175,-316.085) MN(nch) **XI269/XI0/MMI23 MN(nch)**

(_sdw2v) **(_sdw2v)**

Devices:

X19/X24/M0(2.655,-316.085) MN(nch) XI269/XI0/MMI21 MN(nch)

X19/X24/M1(2.915,-316.085) MN(nch) XI269/XI0/MMI22 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X19/X23/M14(6.205,-316.655) MN(nch) XI269/XI0/MMI17 MN(nch)

X19/X23/M15(6.490,-316.655) MN(nch) XI269/XI0/MMI20 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X19/X23/M13(5.945,-316.655) MN(nch) XI269/XI0/MMI19 MN(nch)

X19/X23/M12(5.685,-316.655) MN(nch) XI269/XI0/MMI18 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X19/X23/M11(5.445,-316.655) MN(nch) XI269/XI1/MMI25 MN(nch)

X19/X23/M10(5.255,-316.655) MN(nch) XI269/XI1/MMI26 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X19/X23/M4(3.695,-316.655) MN(nch) XI269/XI1/MMI28 MN(nch)

X19/X23/M5(3.955,-316.655) MN(nch) XI269/XI1/MMI27 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X19/X23/M3(3.435,-316.655) MN(nch) XI269/XI1/MMI24 MN(nch)

X19/X23/M2(3.175,-316.655) MN(nch) XI269/XI1/MMI23 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X19/X23/M0(2.655,-316.655) MN(nch) XI269/XI1/MMI21 MN(nch)

X19/X23/M1(2.915,-316.655) MN(nch) XI269/XI1/MMI22 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X19/X22/M2(3.025,-319.685) MN(nch) XI269/XI1/MMI17 MN(nch)

X19/X22/M3(2.765,-319.685) MN(nch) XI269/XI1/MMI20 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X19/X24/M8(4.735,-315.925) MN(nch) XI269/XI0/MMI36 MN(nch)

X19/X24/M9(4.995,-315.925) MN(nch) XI269/XI0/MMI35 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X19/X24/M6(4.215,-315.925) MN(nch) XI269/XI0/MMI30 MN(nch)

X19/X24/M7(4.475,-315.925) MN(nch) XI269/XI0/MMI29 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X19/X23/M8(4.735,-316.815) MN(nch) XI269/XI1/MMI36 MN(nch)

X19/X23/M9(4.995,-316.815) MN(nch) XI269/XI1/MMI35 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X27/X24/M15(6.490,-156.085) MN(nch) XI268/XI3/MMU3_1-M_u4 MN(nch)

X27/X24/M14(6.205,-156.085) MN(nch) XI268/XI3/MMU3_1-M_u3 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X27/X24/M13(5.945,-156.085) MN(nch) XI268/XI3/MMU3_0-M_u3 MN(nch)

X27/X24/M12(5.685,-156.085) MN(nch) XI268/XI3/MMU3_0-M_u4 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X27/X24/M11(5.445,-156.085) MN(nch) XI268/XI0/MMI25 MN(nch)

X27/X24/M10(5.255,-156.085) MN(nch) XI268/XI0/MMI26 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X27/X24/M4(3.695,-156.085) MN(nch) XI268/XI0/MMI28 MN(nch)

X27/X24/M5(3.955,-156.085) MN(nch) XI268/XI0/MMI27 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X27/X24/M3(3.435,-156.085) MN(nch) XI268/XI0/MMI24 MN(nch)

X27/X24/M2(3.175,-156.085) MN(nch) XI268/XI0/MMI23 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X27/X24/M0(2.655,-156.085) MN(nch) XI268/XI0/MMI21 MN(nch)

X27/X24/M1(2.915,-156.085) MN(nch) XI268/XI0/MMI22 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X27/X23/M14(6.205,-156.655) MN(nch) XI268/XI0/MMI17 MN(nch)

X27/X23/M15(6.490,-156.655) MN(nch) XI268/XI0/MMI20 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X27/X23/M13(5.945,-156.655) MN(nch) XI268/XI0/MMI19 MN(nch)

X27/X23/M12(5.685,-156.655) MN(nch) XI268/XI0/MMI18 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X27/X23/M11(5.445,-156.655) MN(nch) XI268/XI1/MMI25 MN(nch)

X27/X23/M10(5.255,-156.655) MN(nch) XI268/XI1/MMI26 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X27/X23/M4(3.695,-156.655) MN(nch) XI268/XI1/MMI28 MN(nch)

X27/X23/M5(3.955,-156.655) MN(nch) XI268/XI1/MMI27 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X27/X23/M3(3.435,-156.655) MN(nch) XI268/XI1/MMI24 MN(nch)

X27/X23/M2(3.175,-156.655) MN(nch) XI268/XI1/MMI23 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X27/X23/M0(2.655,-156.655) MN(nch) XI268/XI1/MMI21 MN(nch)

X27/X23/M1(2.915,-156.655) MN(nch) XI268/XI1/MMI22 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X27/X22/M2(3.025,-159.685) MN(nch) XI268/XI1/MMI17 MN(nch)

X27/X22/M3(2.765,-159.685) MN(nch) XI268/XI1/MMI20 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X27/X24/M8(4.735,-155.925) MN(nch) XI268/XI0/MMI36 MN(nch)

X27/X24/M9(4.995,-155.925) MN(nch) XI268/XI0/MMI35 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X27/X24/M6(4.215,-155.925) MN(nch) XI268/XI0/MMI30 MN(nch)

X27/X24/M7(4.475,-155.925) MN(nch) XI268/XI0/MMI29 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X27/X23/M8(4.735,-156.815) MN(nch) XI268/XI1/MMI36 MN(nch)

X27/X23/M9(4.995,-156.815) MN(nch) XI268/XI1/MMI35 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X15/X24/M15(6.490,-396.085) MN(nch) XI266/XI3/MMU3_1-M_u4 MN(nch)

X15/X24/M14(6.205,-396.085) MN(nch) XI266/XI3/MMU3_1-M_u3 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X15/X24/M13(5.945,-396.085) MN(nch) XI266/XI3/MMU3_0-M_u3 MN(nch)

X15/X24/M12(5.685,-396.085) MN(nch) XI266/XI3/MMU3_0-M_u4 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X15/X24/M11(5.445,-396.085) MN(nch) XI266/XI0/MMI25 MN(nch)

X15/X24/M10(5.255,-396.085) MN(nch) XI266/XI0/MMI26 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X15/X24/M4(3.695,-396.085) MN(nch) XI266/XI0/MMI28 MN(nch)

X15/X24/M5(3.955,-396.085) MN(nch) XI266/XI0/MMI27 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X15/X24/M3(3.435,-396.085) MN(nch) XI266/XI0/MMI24 MN(nch)

X15/X24/M2(3.175,-396.085) MN(nch) XI266/XI0/MMI23 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X15/X24/M0(2.655,-396.085) MN(nch) XI266/XI0/MMI21 MN(nch)

X15/X24/M1(2.915,-396.085) MN(nch) XI266/XI0/MMI22 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X15/X23/M14(6.205,-396.655) MN(nch) XI266/XI0/MMI17 MN(nch)

X15/X23/M15(6.490,-396.655) MN(nch) XI266/XI0/MMI20 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X15/X23/M13(5.945,-396.655) MN(nch) XI266/XI0/MMI19 MN(nch)

X15/X23/M12(5.685,-396.655) MN(nch) XI266/XI0/MMI18 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X15/X23/M11(5.445,-396.655) MN(nch) XI266/XI1/MMI25 MN(nch)

X15/X23/M10(5.255,-396.655) MN(nch) XI266/XI1/MMI26 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X15/X23/M4(3.695,-396.655) MN(nch) XI266/XI1/MMI28 MN(nch)

X15/X23/M5(3.955,-396.655) MN(nch) XI266/XI1/MMI27 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X15/X23/M3(3.435,-396.655) MN(nch) XI266/XI1/MMI24 MN(nch)

X15/X23/M2(3.175,-396.655) MN(nch) XI266/XI1/MMI23 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X15/X23/M0(2.655,-396.655) MN(nch) XI266/XI1/MMI21 MN(nch)

X15/X23/M1(2.915,-396.655) MN(nch) XI266/XI1/MMI22 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X15/X22/M2(3.025,-399.685) MN(nch) XI266/XI1/MMI17 MN(nch)

X15/X22/M3(2.765,-399.685) MN(nch) XI266/XI1/MMI20 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X15/X24/M8(4.735,-395.925) MN(nch) XI266/XI0/MMI36 MN(nch)

X15/X24/M9(4.995,-395.925) MN(nch) XI266/XI0/MMI35 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X15/X24/M6(4.215,-395.925) MN(nch) XI266/XI0/MMI30 MN(nch)

X15/X24/M7(4.475,-395.925) MN(nch) XI266/XI0/MMI29 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X15/X23/M8(4.735,-396.815) MN(nch) XI266/XI1/MMI36 MN(nch)

X15/X23/M9(4.995,-396.815) MN(nch) XI266/XI1/MMI35 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X13/X24/M15(6.490,-436.085) MN(nch) XI264/XI3/MMU3_1-M_u4 MN(nch)

X13/X24/M14(6.205,-436.085) MN(nch) XI264/XI3/MMU3_1-M_u3 MN(nch)

(_sdw2v) (_sdw2v)

Devices:

X13/X24/M13(5.945,-436.085) MN(nch) XI264/XI3/MMU3_0-M_u3 MN(nch)

X13/X24/M12(5.685,-436.085) MN(nch) XI264/XI3/MMU3_0-M_u4 MN(nch)

o Matched Mosfets Which Have Been Unequally Reduced:

X3/M40(-46.635,179.770)	**XI132/XI0/MMI0-M_u2**
X3/M65(-40.915,182.700)	**XI132/XI1/MMI1-M_u2**
X3/M64(-41.175,182.700)	**** missing smashed mosfet ****
X3/M63(-41.435,182.700)	**** missing smashed mosfet ****
X3/M62(-41.695,182.700)	**** missing smashed mosfet ****
X3/M61(-41.955,182.700)	**** missing smashed mosfet ****
X3/M60(-42.215,182.700)	**** missing smashed mosfet ****
X3/M59(-42.475,182.700)	**** missing smashed mosfet ****
X3/M58(-42.735,182.700)	**** missing smashed mosfet ****
X3/M37(-46.895,179.770)	**XI132/XI0/MMI0-M_u3**
X3/M57(-43.255,182.700)	**XI132/XI1/MMI1-M_u3**
X3/M56(-43.515,182.700)	**** missing smashed mosfet ****
X3/M55(-43.775,182.700)	**** missing smashed mosfet ****
X3/M54(-44.035,182.700)	**** missing smashed mosfet ****
X3/M53(-44.295,182.700)	**** missing smashed mosfet ****
X3/M52(-44.555,182.700)	**** missing smashed mosfet ****
X3/M51(-44.815,182.700)	**** missing smashed mosfet ****
X3/M50(-45.075,182.700)	**** missing smashed mosfet ****
X3/M34(-47.155,179.770)	**XI132/XI0/MMI0-M_u1**
X3/M49(-45.335,182.700)	**XI132/XI1/MMI1-M_u1**
X3/M48(-45.595,182.700)	**** missing smashed mosfet ****
X3/M47(-45.855,182.700)	**** missing smashed mosfet ****
X3/M45(-46.115,182.700)	**** missing smashed mosfet ****
X3/M43(-46.375,182.700)	**** missing smashed mosfet ****
X3/M41(-46.635,182.700)	**** missing smashed mosfet ****

X3/M38(-46.895,182.700)	**** missing smashed mosfet ****
X3/M35(-47.155,182.700)	**** missing smashed mosfet ****
X4/M40(-36.635,179.770)	**XI137/XI0/MMI0-M_u2**
X4/M65(-30.915,182.700)	**XI137/XI1/MMI1-M_u2**
X4/M64(-31.175,182.700)	**** missing smashed mosfet ****
X4/M63(-31.435,182.700)	**** missing smashed mosfet ****
X4/M62(-31.695,182.700)	**** missing smashed mosfet ****
X4/M61(-31.955,182.700)	**** missing smashed mosfet ****
X4/M60(-32.215,182.700)	**** missing smashed mosfet ****
X4/M59(-32.475,182.700)	**** missing smashed mosfet ****
X4/M58(-32.735,182.700)	**** missing smashed mosfet ****
X4/M37(-36.895,179.770)	**XI137/XI0/MMI0-M_u3**
X4/M57(-33.255,182.700)	**XI137/XI1/MMI1-M_u3**
X4/M56(-33.515,182.700)	**** missing smashed mosfet ****
X4/M55(-33.775,182.700)	**** missing smashed mosfet ****
X4/M54(-34.035,182.700)	**** missing smashed mosfet ****
X4/M53(-34.295,182.700)	**** missing smashed mosfet ****
X4/M52(-34.555,182.700)	**** missing smashed mosfet ****
X4/M51(-34.815,182.700)	**** missing smashed mosfet ****
X4/M50(-35.075,182.700)	**** missing smashed mosfet ****
X4/M34(-37.155,179.770)	**XI137/XI0/MMI0-M_u1**
X4/M49(-35.335,182.700)	**XI137/XI1/MMI1-M_u1**
X4/M48(-35.595,182.700)	**** missing smashed mosfet ****
X4/M47(-35.855,182.700)	**** missing smashed mosfet ****
X4/M45(-36.115,182.700)	**** missing smashed mosfet ****
X4/M43(-36.375,182.700)	**** missing smashed mosfet ****
X4/M41(-36.635,182.700)	**** missing smashed mosfet ****
X4/M38(-36.895,182.700)	**** missing smashed mosfet ****
X4/M35(-37.155,182.700)	**** missing smashed mosfet ****

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SUMMARY

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Total CPU Time: 0 sec

Total Elapsed Time: 0 sec