ECE1388 VLSI Design Methodology

Project-1 Report

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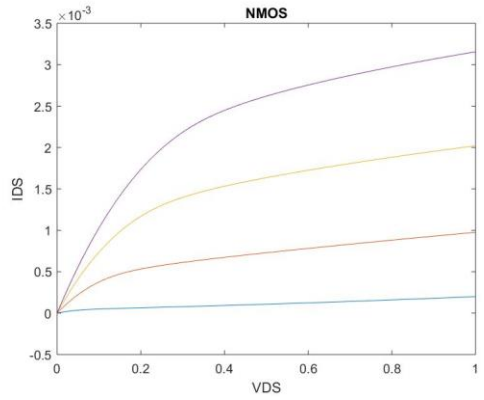
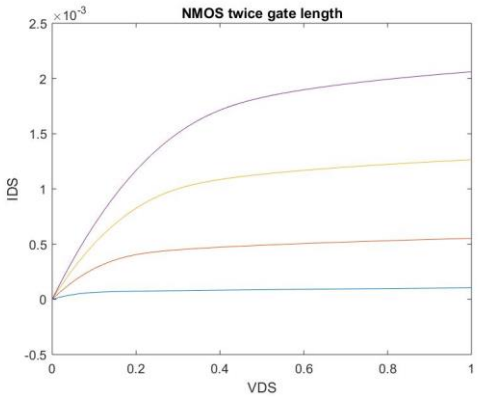
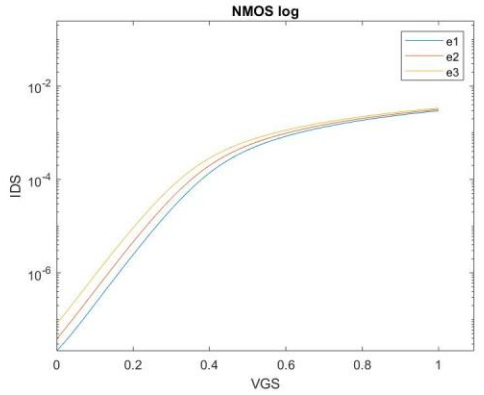
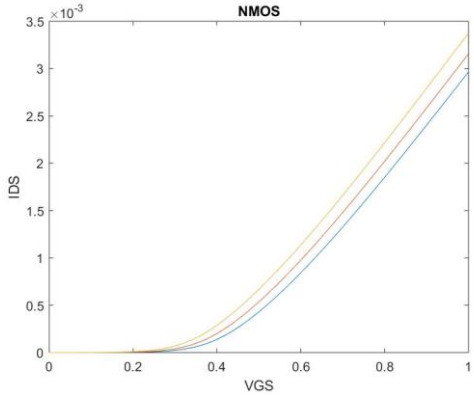
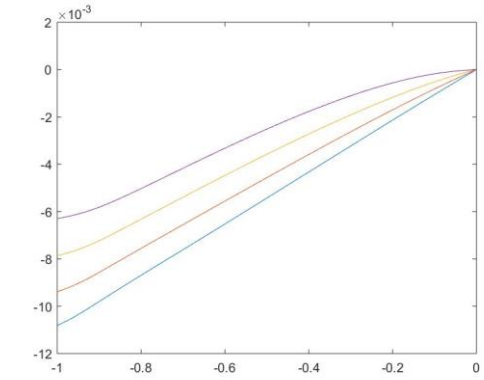
Q.1

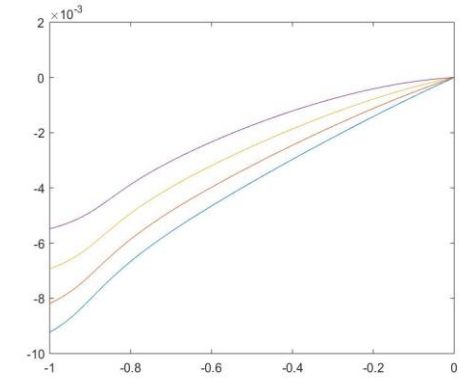

NMOS
×10^-3
IDS
VDS

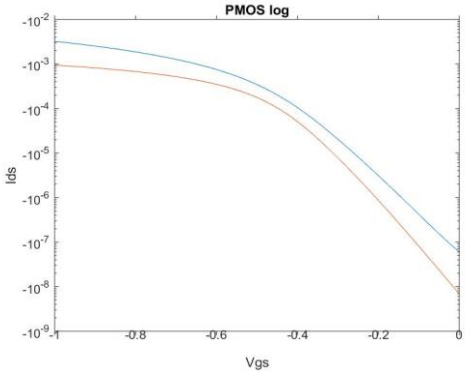

NMOS twice gate length
×10^-3
IDS
VDS

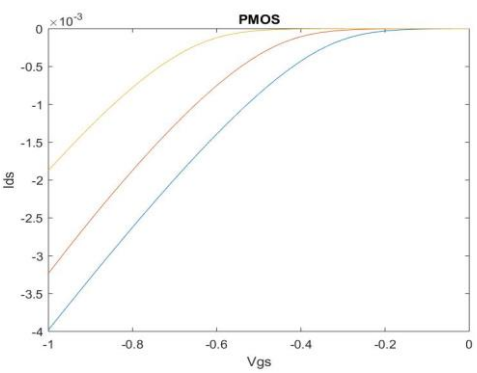

NMOS log
e1
e2
e3
IDS
VGS


NMOS
×10^-3
IDS
VGS


×10^-3


×10^-3


PMOS log
Ids
Vgs


PMOS
×10^-3
Ids
Vgs

The graphs above show the VI characteristics of PMOS and NMOS in cadence 6. The graphs for different gate and source voltages were generated using parametric analysis.

Procedure:

The following connections were made for NMOS

- Gate:1 V DC input from VDC
- Source: Grounded
- Drain: VDD of 1V dc from VDC
- Substrate: Grounded

The following connections were made for Pmos:

- Gate:-1 V DC input from VDC
- Source: VDD of -1V dc from VDC
- Drain: Grounded
- Substrate: VDD of -1V dc from VDC

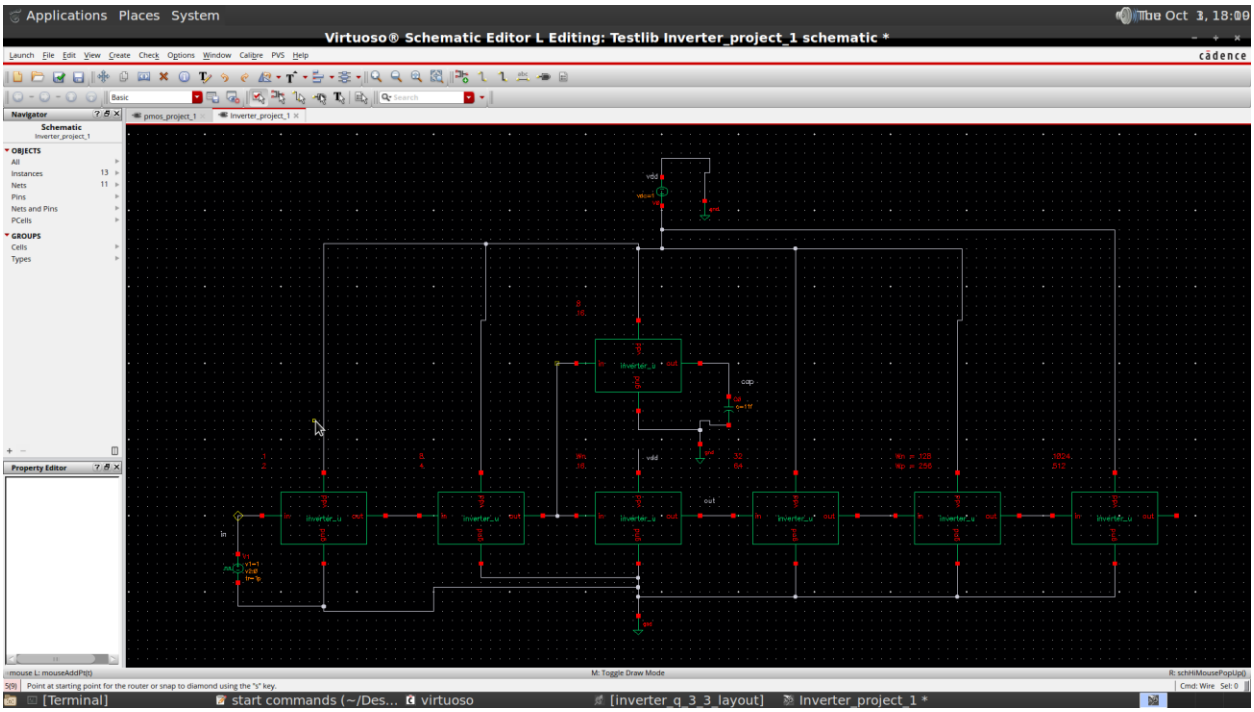
Then the graphs were plotted using DC analysis in ADE L by fixing VGS and varying VDS and vice versa.

Q 2.1

By studying the transient analysis and changing the capacitor value, the best capacitor value that reduces the values of delay from c to d and c to g is 11f F. Hence the value of gate capacitence of 64/32 is **11f F** . The delay was found to be 10.81f s

Procedure:

The following circuit was designed by using the inverter cell and the values of Wp and Wn are specified as mentioned in the question i.e(2/1,8/4,16/8,16/8,64/32,256/128,1024/512). The delay was calculated at the capacitor and at the input of the 4^{th} inverter. By changing the value of capacitor the gate capacitance was determined.



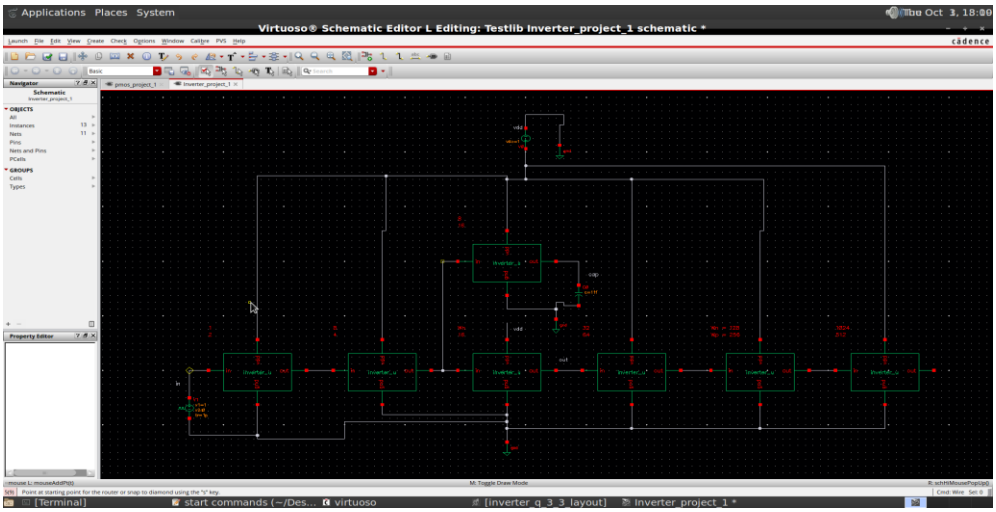
The value of gate capacitance of 64/32 is 11f F . The delay was found to be 10.81f s

Q 2.2

The value of Rp is 1.7 kΩ

The value of Rn is 3.6 kΩ

Procedure:



The following circuit was designed and the propagation delay was measured across 64/32 inverter having a fanout of 4(i.e 256/128). After the rising and falling delays were measured the circuit was modified such that 64/32 has a fanout of 5(i.e 320/160) and the delays were calculated.

To calculate the effective resistance

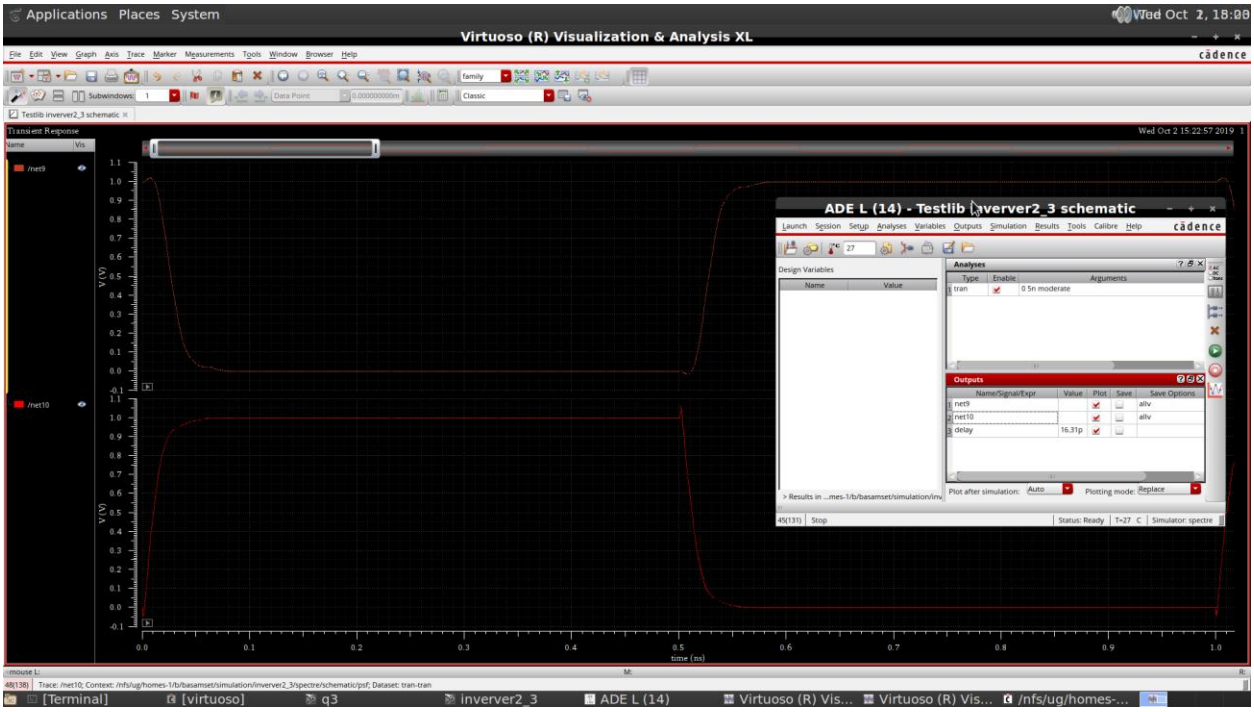
$$\Delta t_{pdr} = \frac{R_p}{2}\left(3\times 4\times C + 3C_d\right) - \frac{R_p}{2}\left(3\times 3\times C + 3C_d\right) = \frac{3}{2}R_p C$$

$$\Delta t_{pdf} = R_n\left(3\times 4\times C + 3C_d\right) - R_n\left(3\times 3\times C + 3C_d\right) = 3R_n C$$

We get Δ_{tpdr}=1.87ps, Δ_{tpdf}=1.78ps, C=11fF(from 2.1)

On substituting the values we get Rp=54Ω*32=1.7kΩ and Rn= 113Ω*32=3.6kΩ

Q 2.3



The input for the circuit is given as a step(rise time=1ps and fall time=1ps and period=1ns) and the delay was calculated as 16.31ps. The percentage difference between the delays is 1.9%

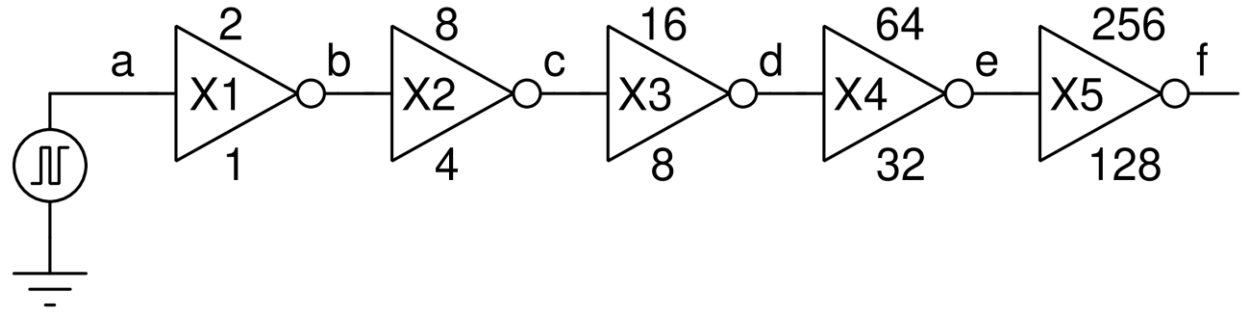
The circuit was modified according to the question and transient analysis was done to get the graphs and delay value.

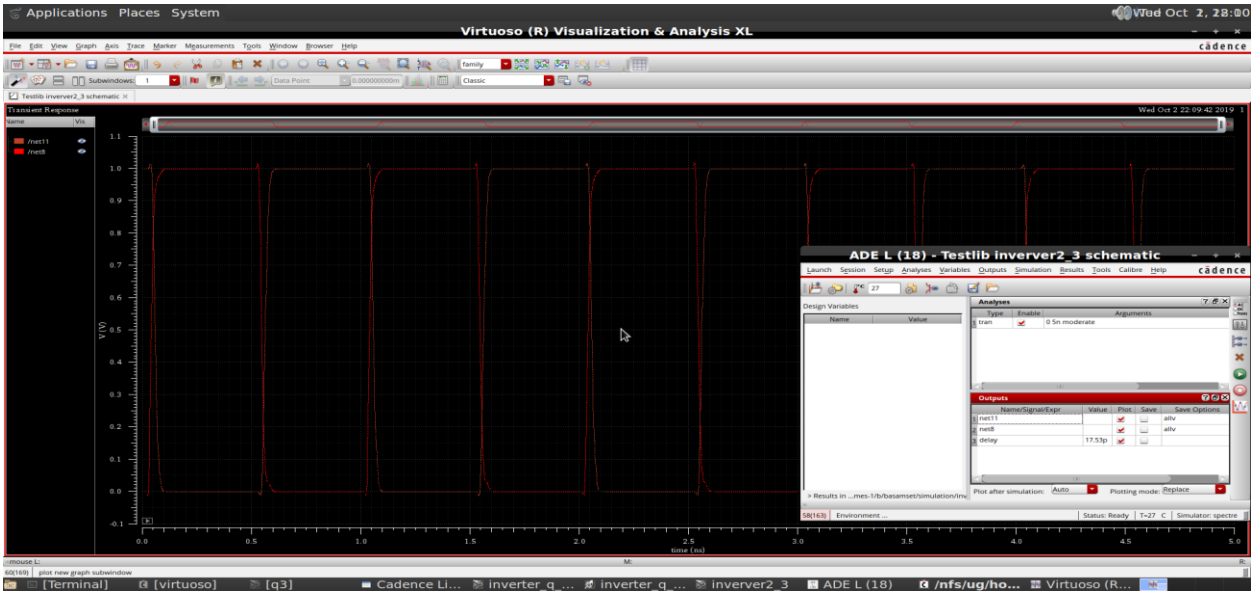
Delay in Question 2.1 is 16.63Ps

Calculation of percentage dealay: (16.63-16.61)/16.61*100= 1.926%

Q2.4

The circuit was modified as shown by changing the Wp and Wn values as in below figure

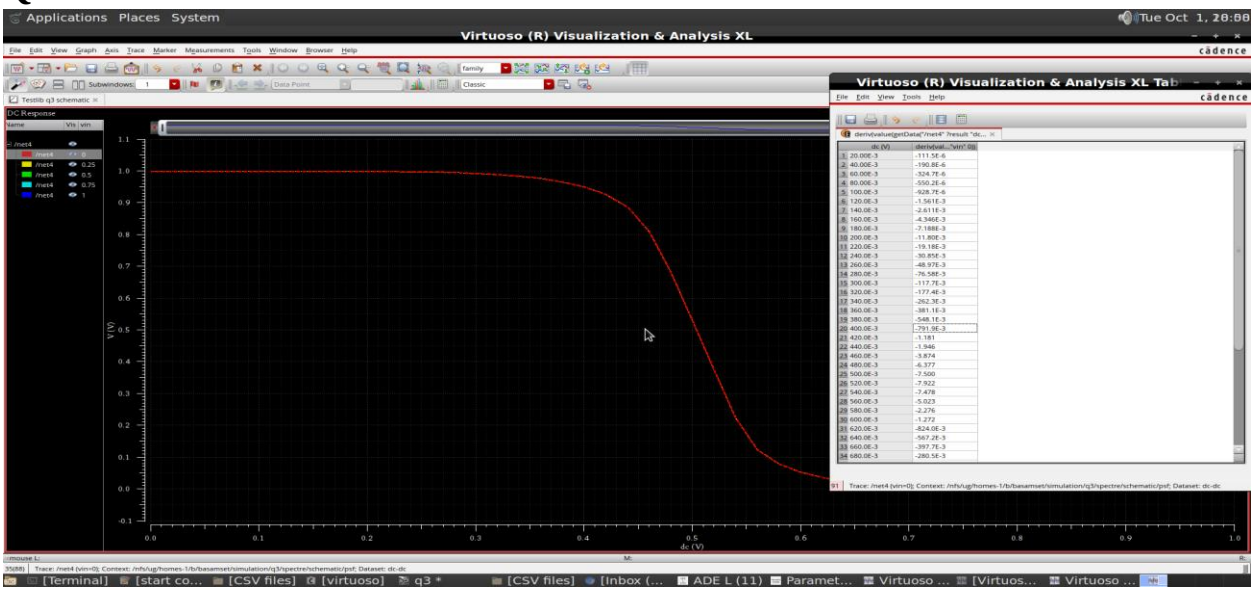




The delay for the 64/32 inverter was found to be 17.53ps and the percentage delay between the delay in question 2.1 and question 2.4 is **5.1%.**

Calculation of percentage delay= (17.53-16.63)/17.53*100=5.1%

Q 3.1



The transfer characteristics of an inverter are plotted by using parametric analysis(i.e VGS=0 to 1V and VDD=1V). The slope for the curve was found using the derivative function in the cadence calculator. The corresponding Y-axis values were found. (VIL=420mV, VOL=53.3275mV, VIH= 600mV, VOH=926.697mV)

The noise margins were calculated using the following formulas

$$N_{ML}=V_{IL}-V_{OH}\,(420mV-53.3275mV)$$

$$N_{MH}=V_{OH}-V_{IH}\,(926.697mV-600mV)$$

On substituting the values we get

High Noise Margin(NMH)=366.6795mV

Low Noise Margin(LMH)=326.697mV

Q 3.2

After a trial and error analysis of making the high noise margin and low noise margin equal, the best value for Wp was found to be 45 where the noise margins were found to be 348.342 and 346.92

Iteration 1:

Wp=50

VIL=420mV, VOL= 58.393 mV, VIH= 580 mV ,VOH= 901.935mV

High Noise Margin(NMH)=375.0223mV

Low Noise Margin(LMH)= 312.535mV

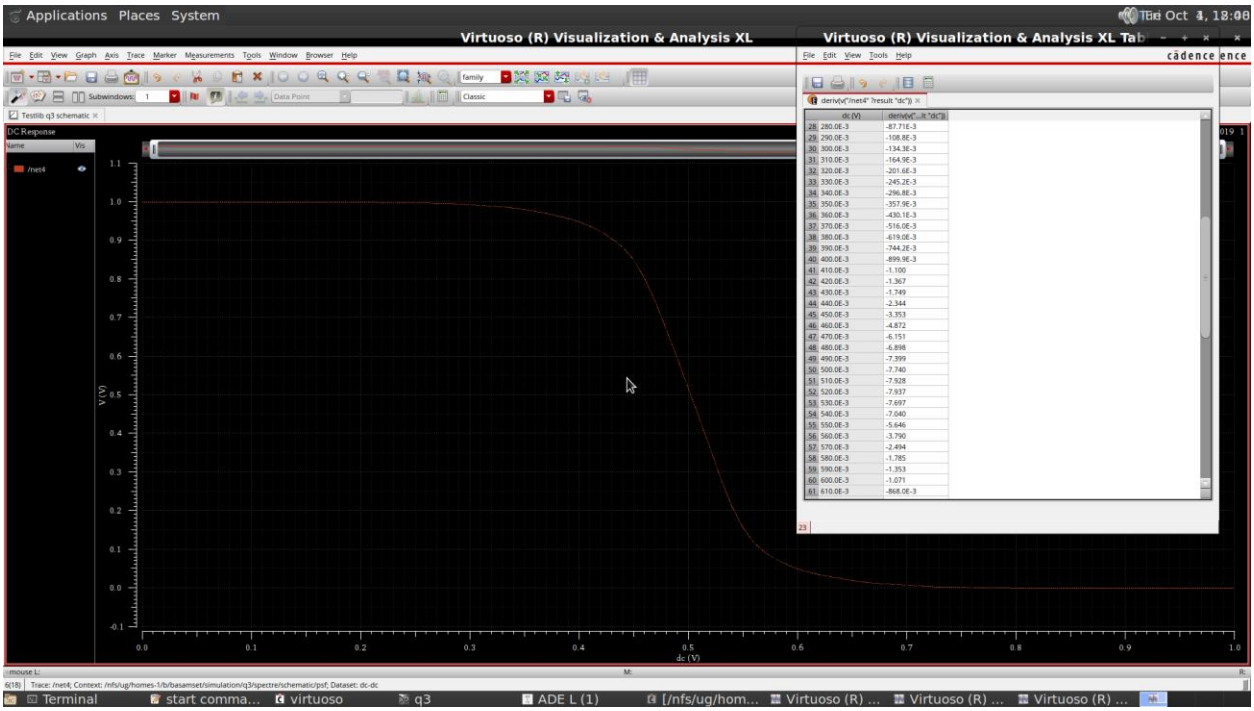
Iteration 2:

Wp=64

VIL=400mV, VOL= 51.4365 mV, VIH= 948.57 mV ,VOH= 600mV

High Noise Margin(NMH)=348.46mV

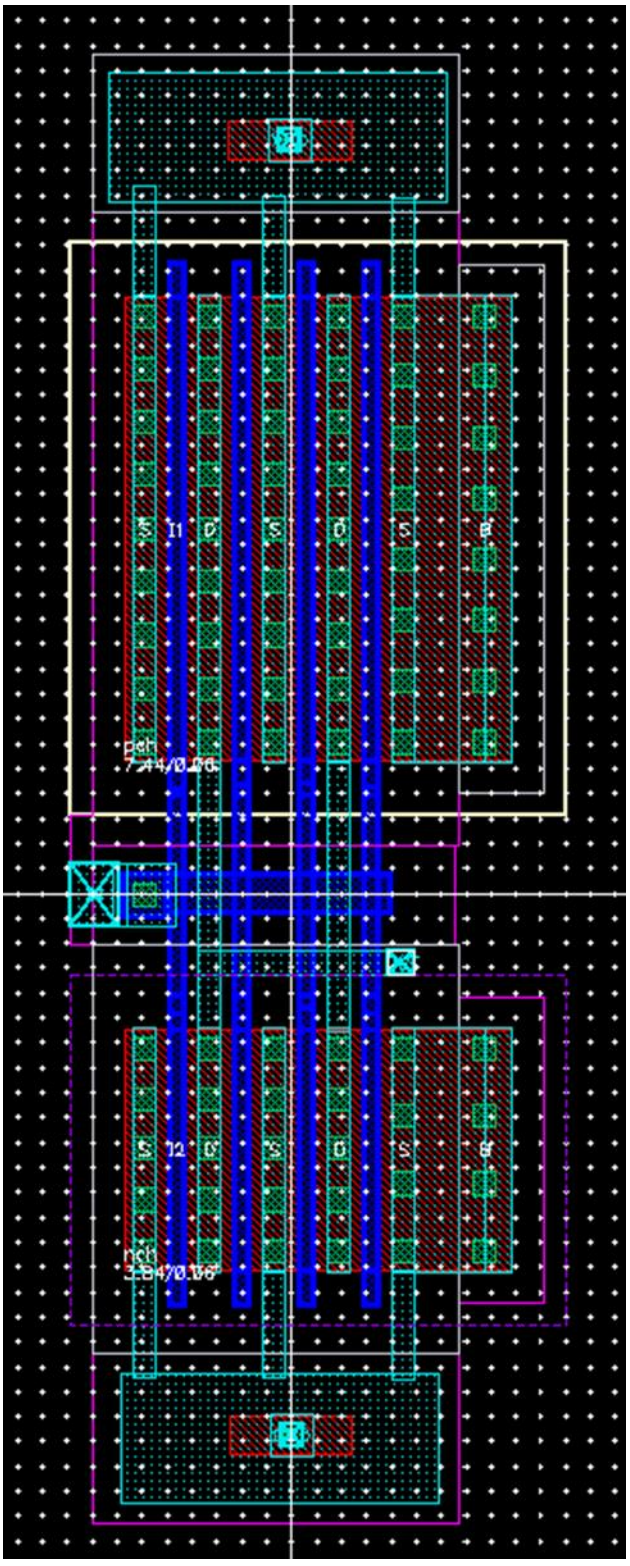
Low Noise Margin(LMH)= 338.57mV



For Wp=64 the values of high noise margin and low noise margins are almost equal.

Q 3.3

From Q 3.2 the wp is found to be 64 and wn=32. So in the layout



LVS report

```
################################################
##                                            ##
##      C A L I B R E   S Y S T E M           ##
##                                            ##
##         L V S   R E P O R T                ##
##                                            ##
################################################
```

REPORT FILE NAME: **inverter_q_3_3.lvs.report**

LAYOUT NAME: **/nfs/ug/homes-1/b/basamset/IC6CRN65GP/./CalibreLVS/inverter_q_3_3.sp ('inverter_q_3_3')**

SOURCE NAME: **/nfs/ug/homes-1/b/basamset/IC6CRN65GP/./CalibreLVS/inverter_q_3_3.src.net ('inverter_q_3_3')**

RULE FILE: **/nfs/ug/homes-1/b/basamset/IC6CRN65GP/./CalibreLVS/_calibre.lvs_**

CREATION TIME: **Fri Oct 4 17:27:20 2019**

CURRENT DIRECTORY: **/nfs/ug/homes-1/b/basamset/IC6CRN65GP/CalibreLVS**

USER NAME: **basamset**

CALIBRE VERSION: **v2014.3_35.26 Wed Oct 1 13:01:36 PDT 2014**

OVERALL COMPARISON RESULTS

CELL COMPARISON RESULTS (TOP LEVEL)

```
   #    ###################    _ _
  #     #         #    * *
 # #     #   CORRECT   #     |
```

LAYOUT CELL NAME: inverter_q_3_3
SOURCE CELL NAME: inverter_q_3_3

INITIAL NUMBERS OF OBJECTS

	Layout	Source	Component Type
Ports:	4	4	
Nets:	4	4	
Instances:	4	1 *	MN (4 pins)
	4	1 *	MP (4 pins)
Total Inst:	8	2	

NUMBERS OF OBJECTS AFTER TRANSFORMATION

	Layout	Source	Component Type
Ports:	4	4	
Nets:	4	4	
Instances:	1	1	_invv (4 pins)
Total Inst:	1	1	

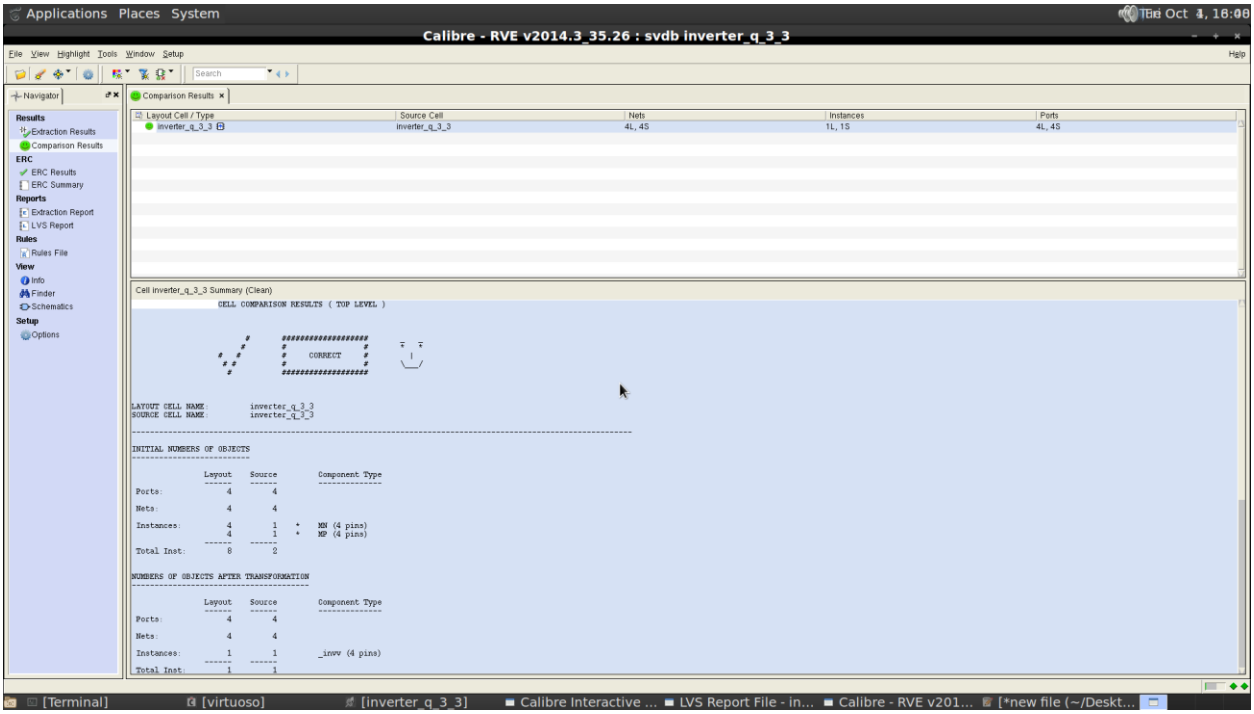
* = Number of objects in a layout different from the number in source.

****
****

INFORMATION AND WARNINGS

****

	Matched Layout	Unmatched Source	Unmatched Layout	Unmatched Source	Component Type
Ports:	4	4	0	0	
Nets:	4	4	0	0	
Instances:	1	1	0	0	_invv
Total Inst:	**1**	**1**	**0**	**0**	



##

##

C A L I B R E S Y S T E M

##

C I R C U I T E X T R A C T I O N R E P O R T

##

##

REPORT FILE NAME: **inverter_q_3_3.lvs.report.ext**

LAYOUT NAME: **inverter_q_3_3.calibre.db ('inverter_q_3_3')**

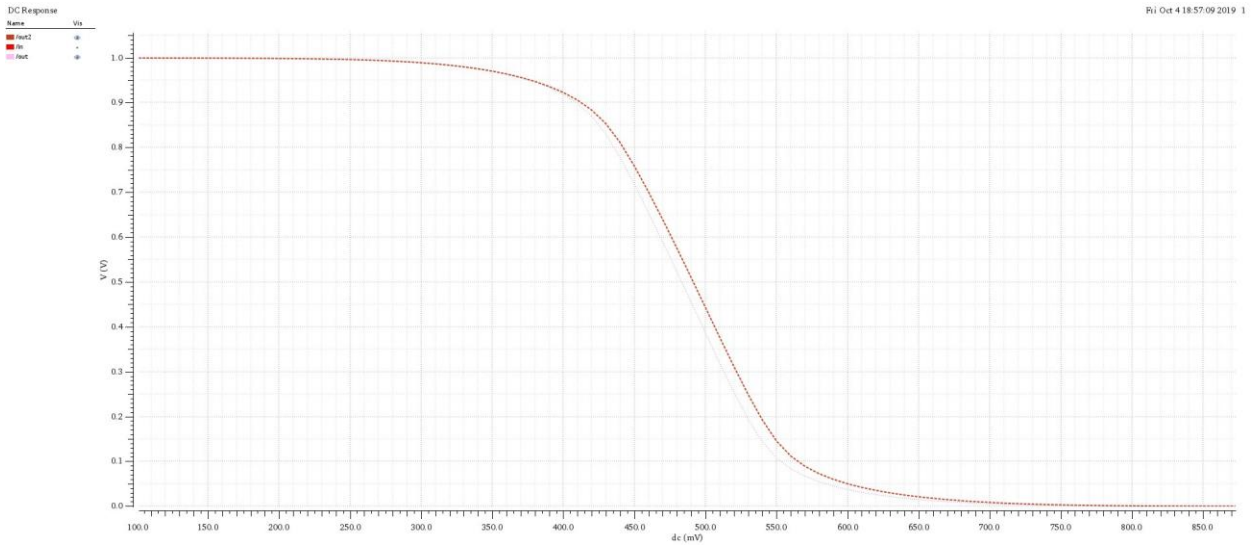
CREATION TIME: **Fri Oct 4 16:47:25 2019**

CURRENT DIRECTORY: **/nfs/ug/homes-1/b/basamset/IC6CRN65GP/CalibreLVS**

USER NAME: **basamset**

CALIBRE VERSION: **v2014.3_35.26 Wed Oct 1 13:01:36 PDT 2014**

Extracted layout



The values of extracted layout were found as Vil=390mv, Vol=55.1099, Vih570mv, Voh= 936.669, 580mv

Low Noise Margin (LMH) 300.38mV

High Noise Margin (NMH)=366.66mV

And the values from question 3.1 are

High Noise Margin(NMH)=366.6795Mv

Low Noise Margin(LMH)=326.697mV which are nearly equal.