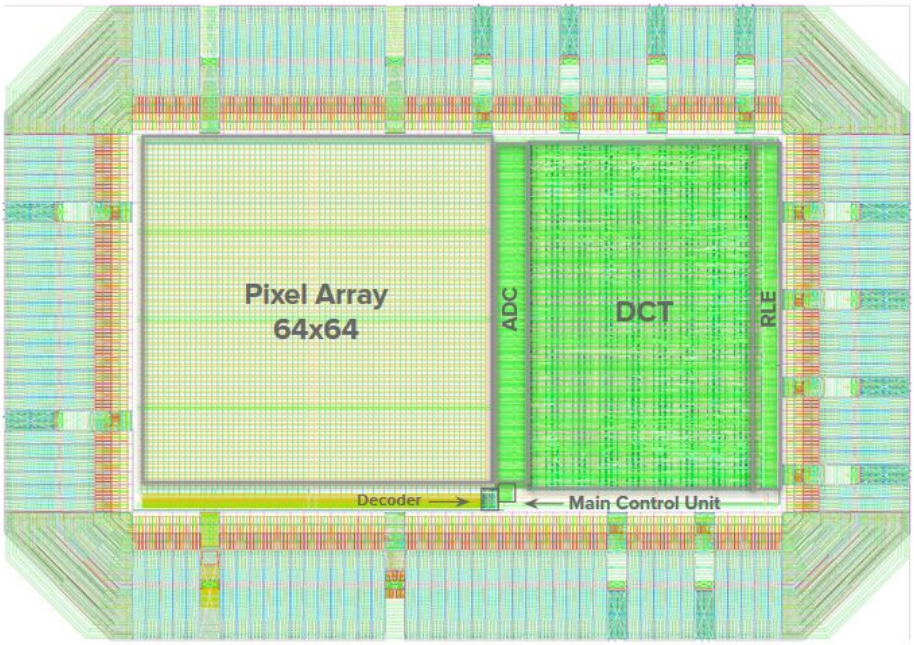
ECE1388H VLSI DESIGN METHODOLOGY

FINAL PROJECT REPORT:
IMAGE CAPTURE AND COMPRESSION FOR WIRELESS ENDOSCOPY



Padframe Layout

Introduction:

Wireless endoscopy, also known as capsule endoscopy was first presented in the famous journal, 'Nature' (edition 405) in the year 2000. The primary use of capsule endoscopy is to examine areas of the gastrointestinal tract which are normally inaccessible by other types of endoscopy such as colonoscopy or EGD. The capsule consists of a small camera, an array of LEDs and its corresponding circuitry. After the patient ingests it, the capsule captures images and transmits them wirelessly to an external receiver worn by the patient.

Objective:

Capsule endoscopy, being wireless in nature, has associated data losses and speed limitations that is inherent. The motivation of the project is that the capsules are limited by their battery life, data acquisition rate, limited visibility from a single camera etc.

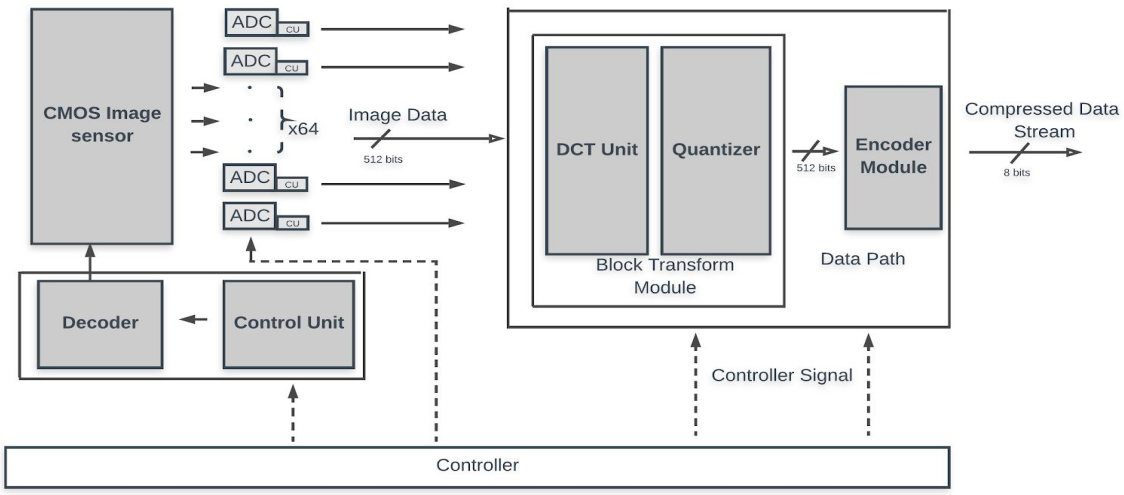
So, our objective in this project is to implement an image compression system that entails the following:

- A CMOS active pixel array to model the acquisition of images by the camera
- A dual slope Analog to Digital Converter (ADC), to convert the analog pixel array values to the digital domain
- A compression module implemented using Discrete Cosine Transform and Run length Encoding.

Specifications:

Parameters	Estimated	Obtained
Power	~1 mW	1.4 mW
Technology	65nm	
Voltage	1 V	
Area	~3 mm^2	0.54 mm^2
Pixel Array Size	64 x 64	64 x 64
Frame Rate	2 fps	20 fps
Compression Ratio	3:1	

System Outline:



System Outline

The figure above depicts the general dataflow of our system.

I. **CMOS image sensor:** Pixel array consisting of 64x64 pixels. The pixel cells in the array consists of a 3-transistor CMOS Active pixel setup. They provide a corresponding analog voltage scaled according to the intensity of the light falling on the photodiode incorporated within the cell.
II. **Decoder:** The information from the pixel array are accessed by selecting the rows using a decoder.
III. **ADC and ADC Control unit:** The output of the CMOS pixel array goes to the ADC module converting them to digital signals. The ADC was implemented using VerilogA code simulating the behaviour of the Dual-slope ADC. The ADC control unit was implemented using state machine logic in Verilog HDL.
IV. **DCT and Quantizer:** This binary image values are then converted from the spatial domain to the frequency domain using Discrete Cosine transform which also includes a quantizer as shown in the diagram.
V. **RLE:** At the end of the data flow, we have the Run Length Encoder, which encodes the data output from the DCT, thus successfully compressing the image. The RLE module was designed using Verilog HDL. The compression ratio of the module was found to be 3.
VI. **Main Control Unit:** All the control signals for the various modules present in the system for efficient and synchronised working is provided by the MCU. This system was implemented using Verilog HDL.

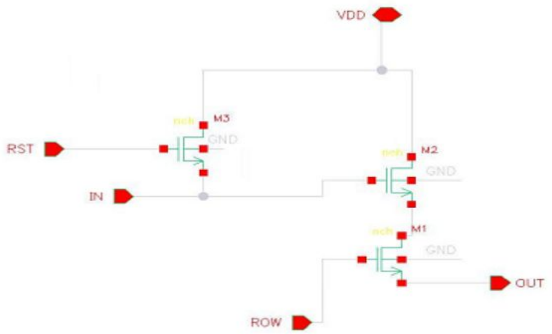
All the systems mentioned above was imported into Cadence Virtuoso and was tested using corresponding test-benches and the result was verified. The schematic, simulated outputs, and the corresponding layouts are provided in the appendix.

Work Distribution:

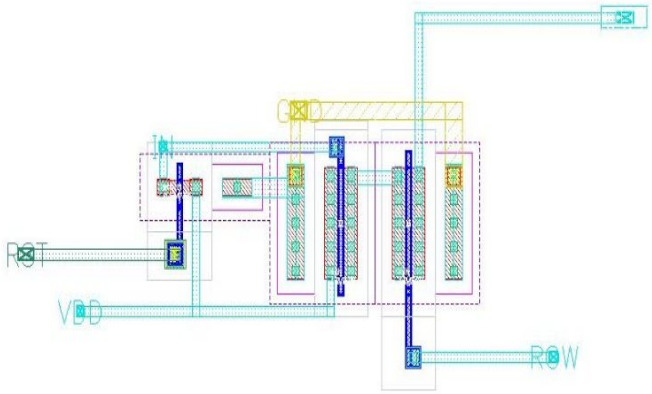
S.No.	Functional Block	Member(s)
1	Pixel Array	Anirudh, Pranav
2	ADC	Pranav, Vimal
3	Decoder	Vimal
4	DCT	Pranav
5	RLE	Anirudh, Vishnu
6	ADC Control Unit	Vishnu
7	Layout in Padframe	Vimal, Anirudh
8	Control Logic Unit	Vishnu, Pranav

Appendix:

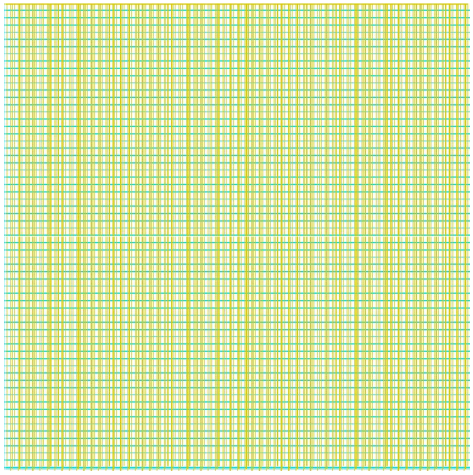
A) CMOS IMAGE SENSOR



Schematic of CMOS Image Sensor

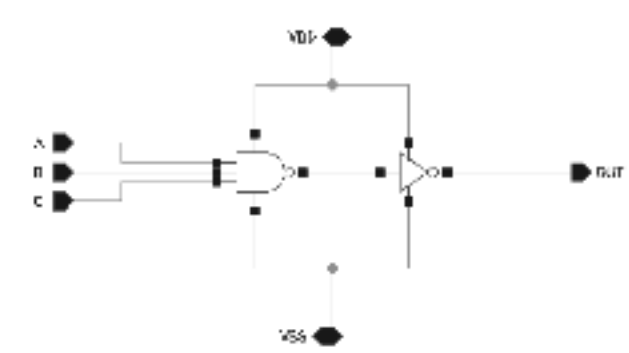


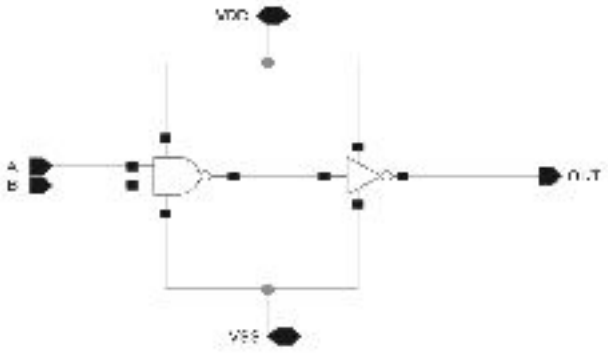
Layout of CMOS Image Sensor

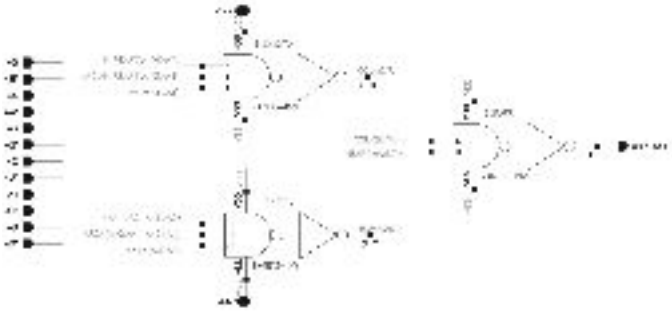


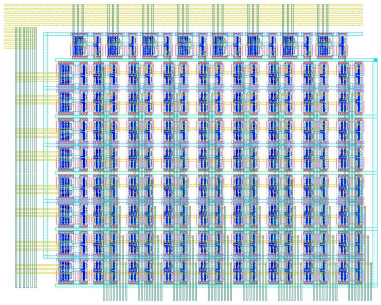
Layout of 64x64 Pixel Array

B) DECODER



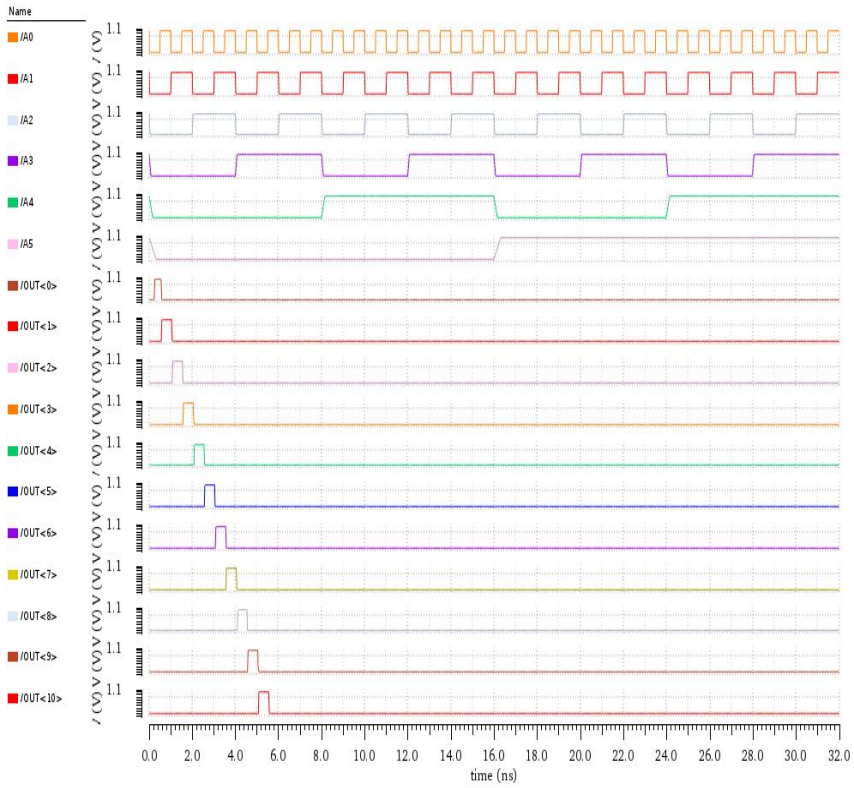






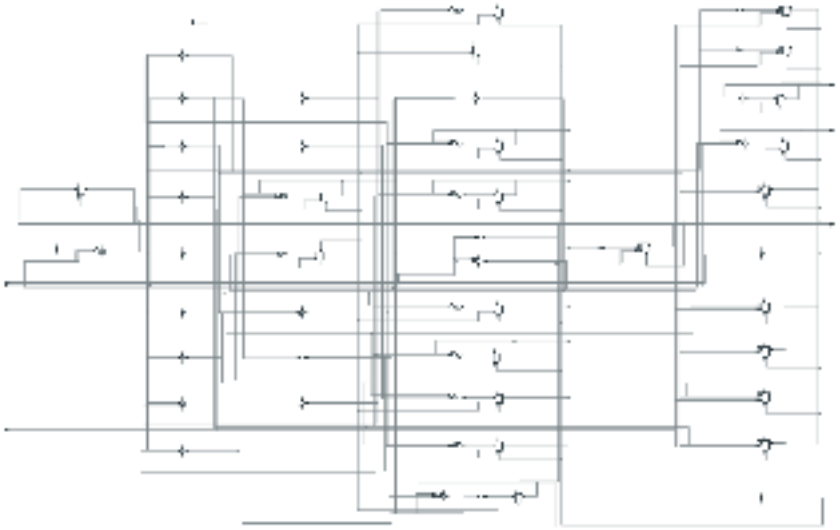
Schematic of Decoder

Layout of Decoder

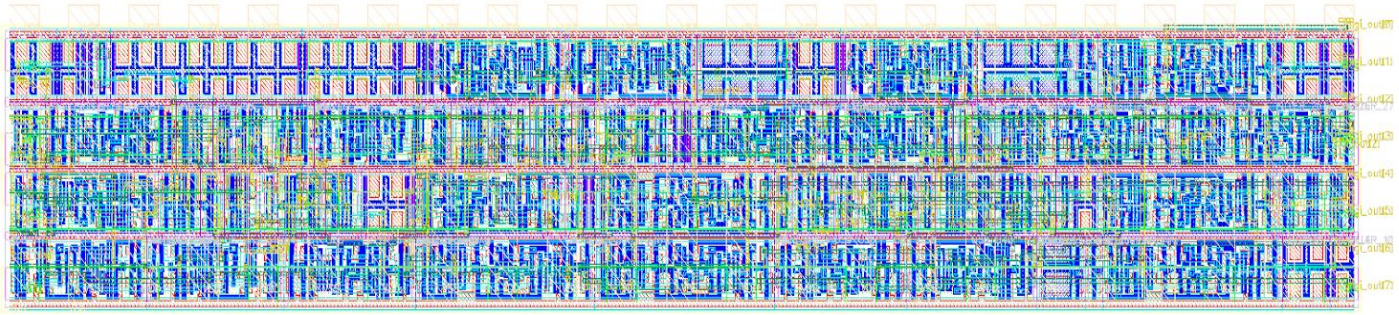


Simulated Output of Decoder

C) ADC CONTROL UNIT MODULE

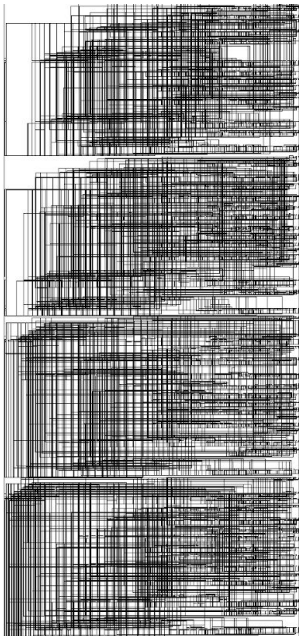


Schematic of ADC Control Unit Module

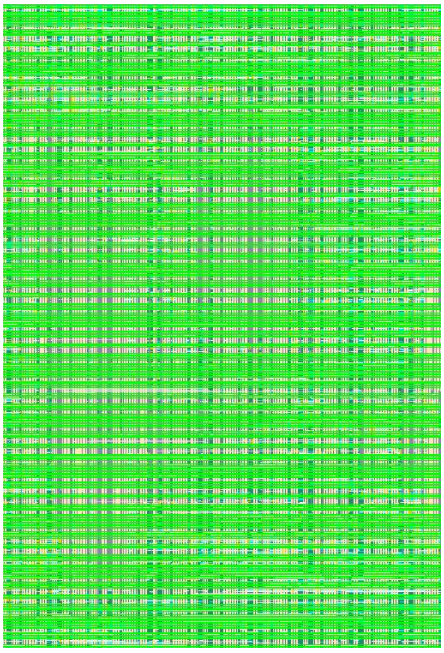


Layout of ADC Control Unit Module

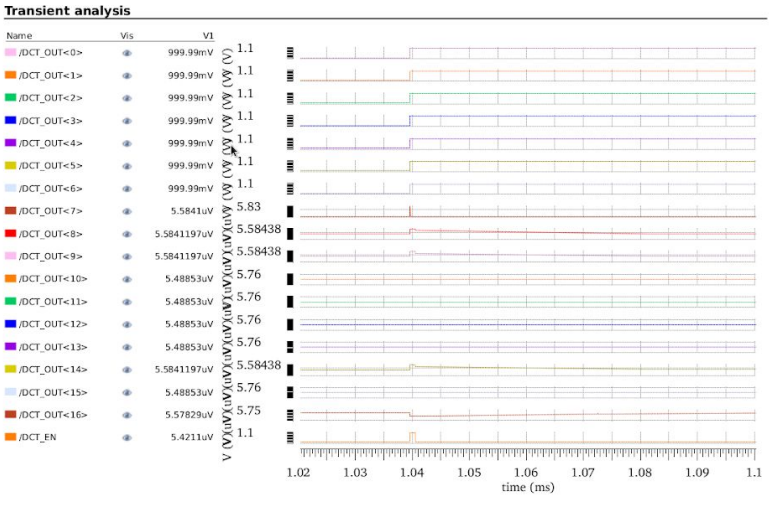
D) DCT MODULE



Schematic Of DCT Module

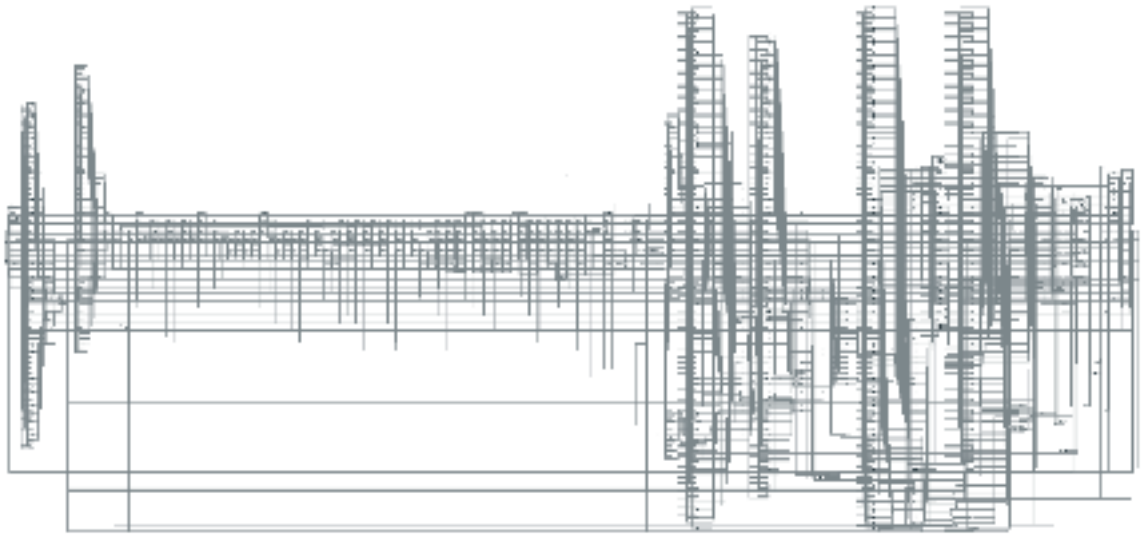


Layout of DCT module

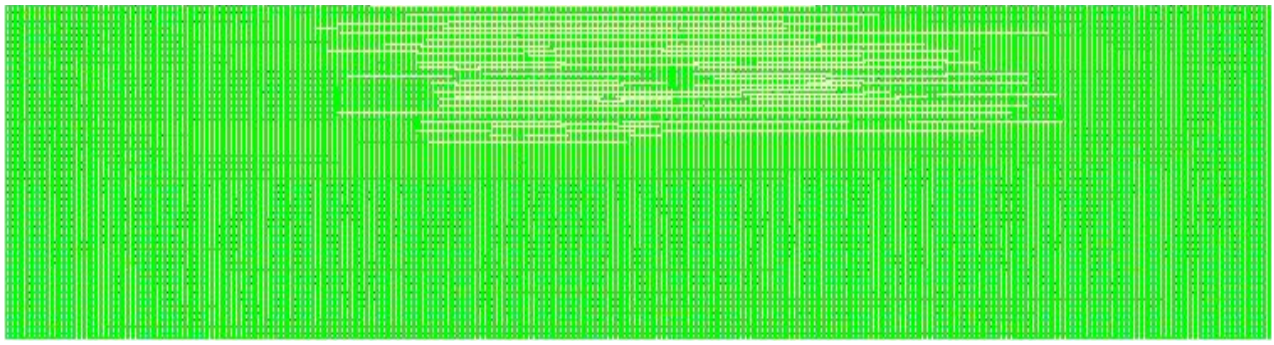


Simulation of DCT module

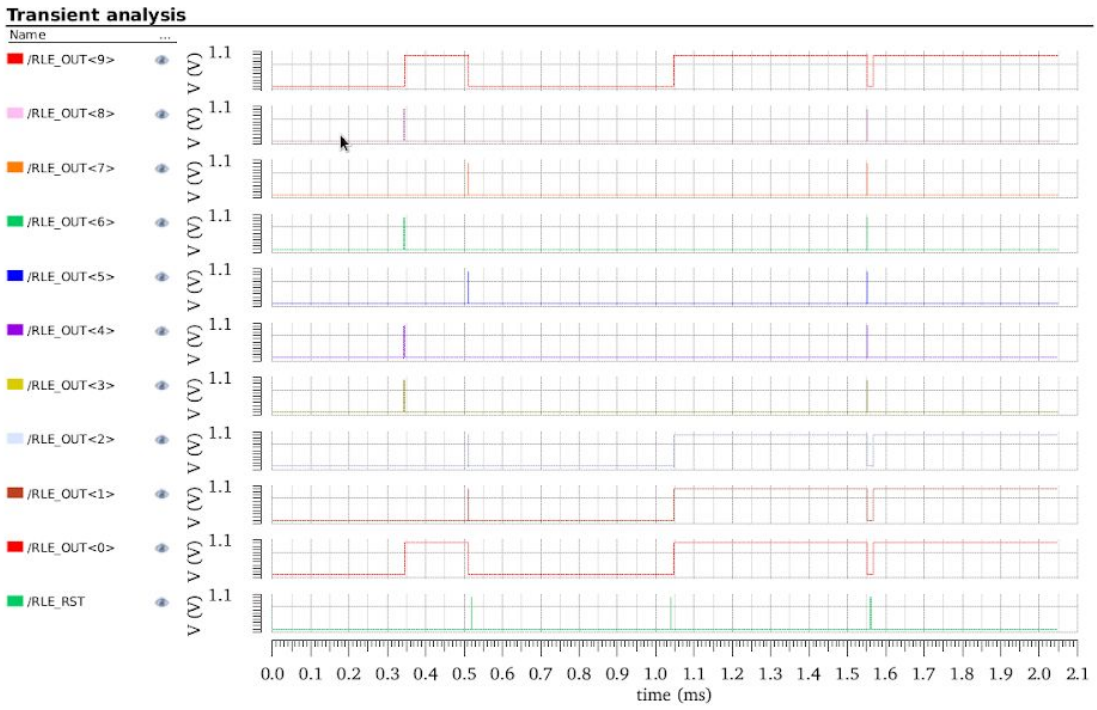
E) RUN LENGTH ENCODER

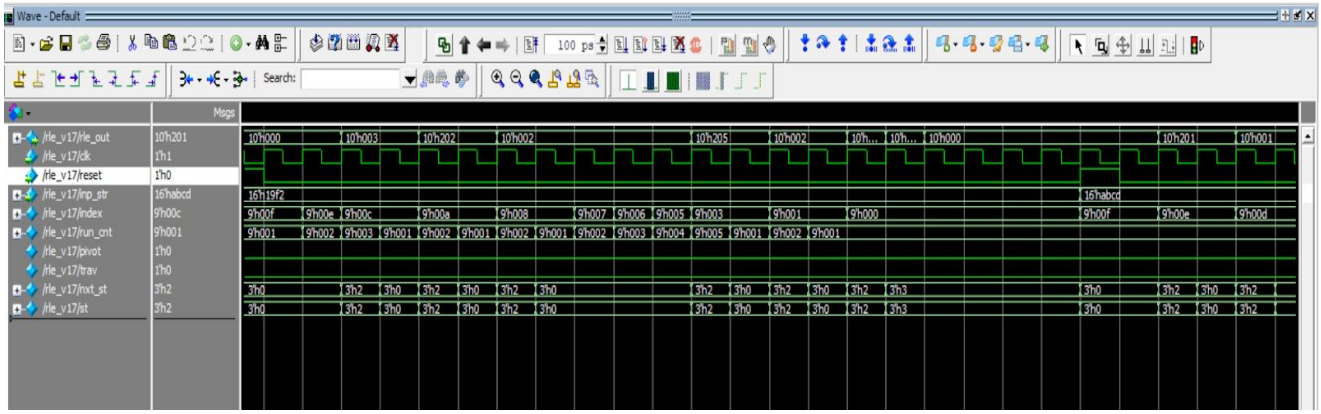


Schematic of RLE



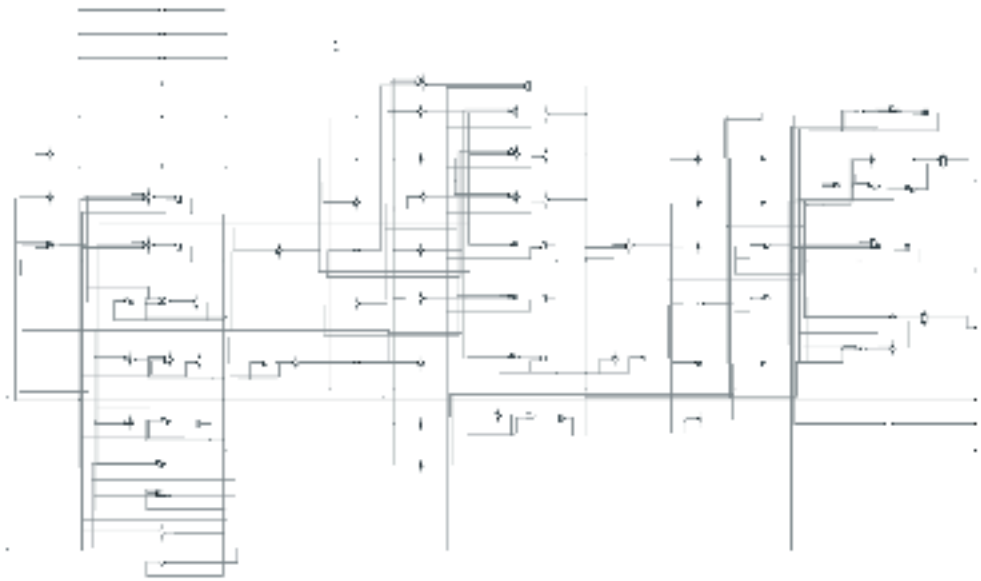
Layout of RLE



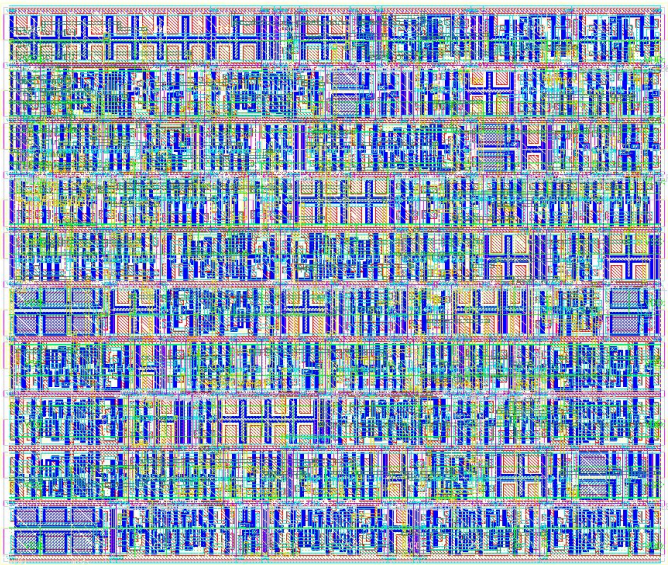


Simulation of RLE module

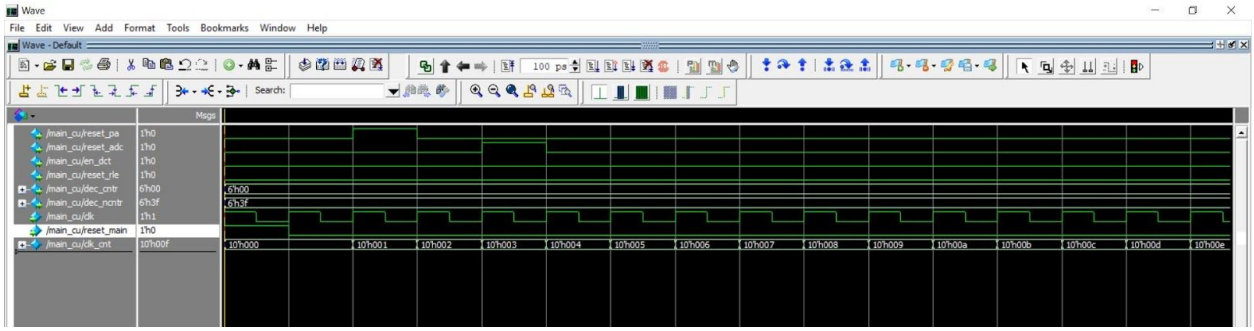
F) MAIN CONTROL UNIT



Schematic of Main Control Unit

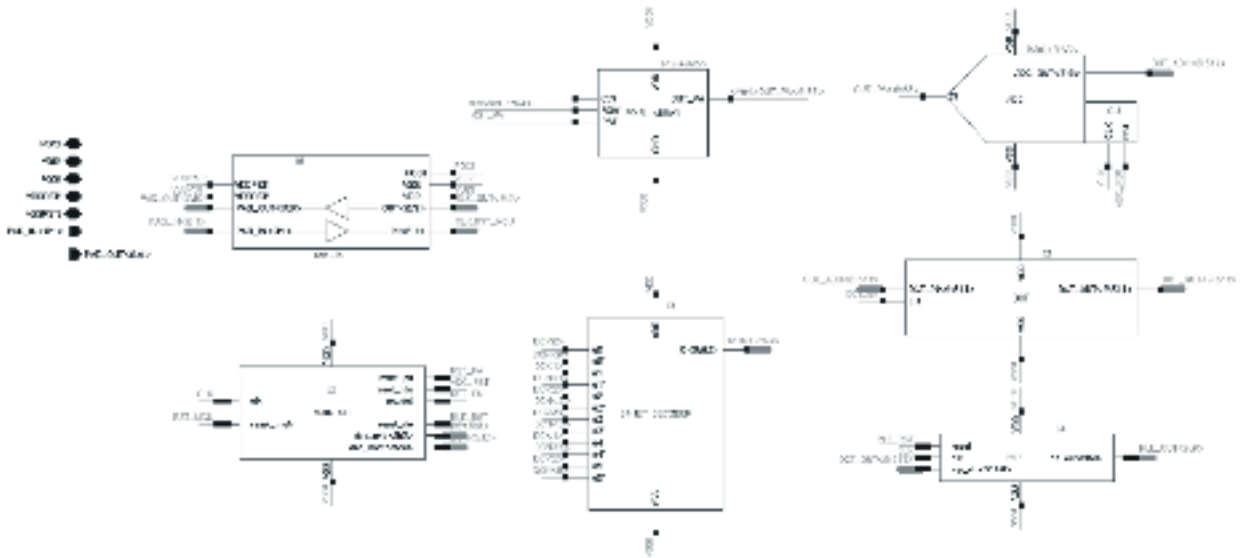


Layout of Main Control Unit

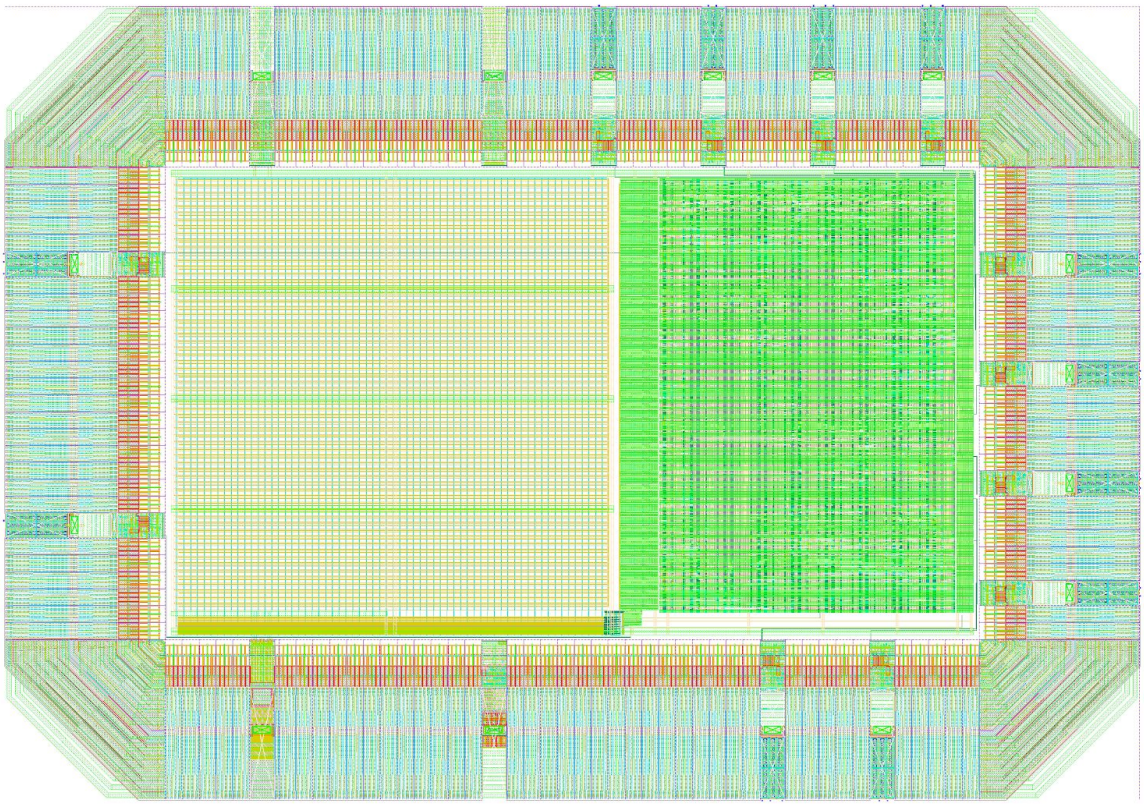


Simulation of Main Control Unit

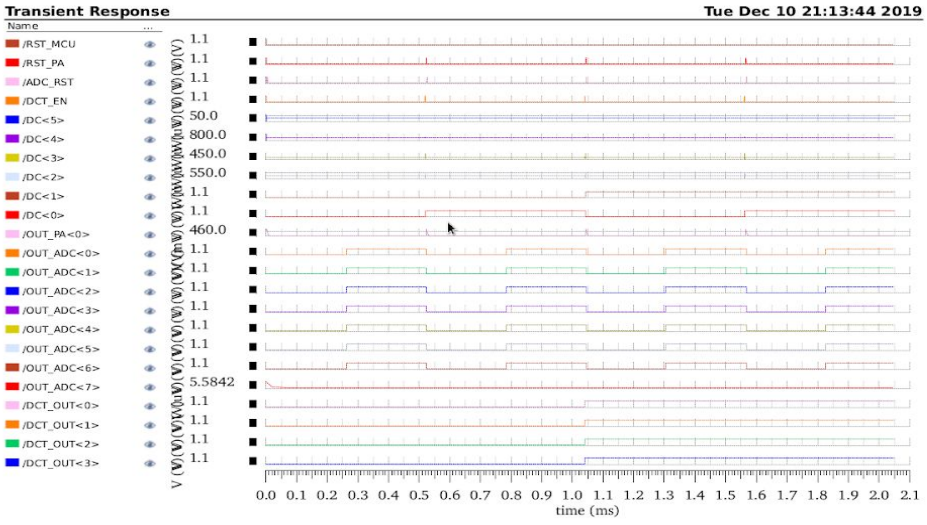
G) INTEGRATED TEST BENCH WITH PAD I/O

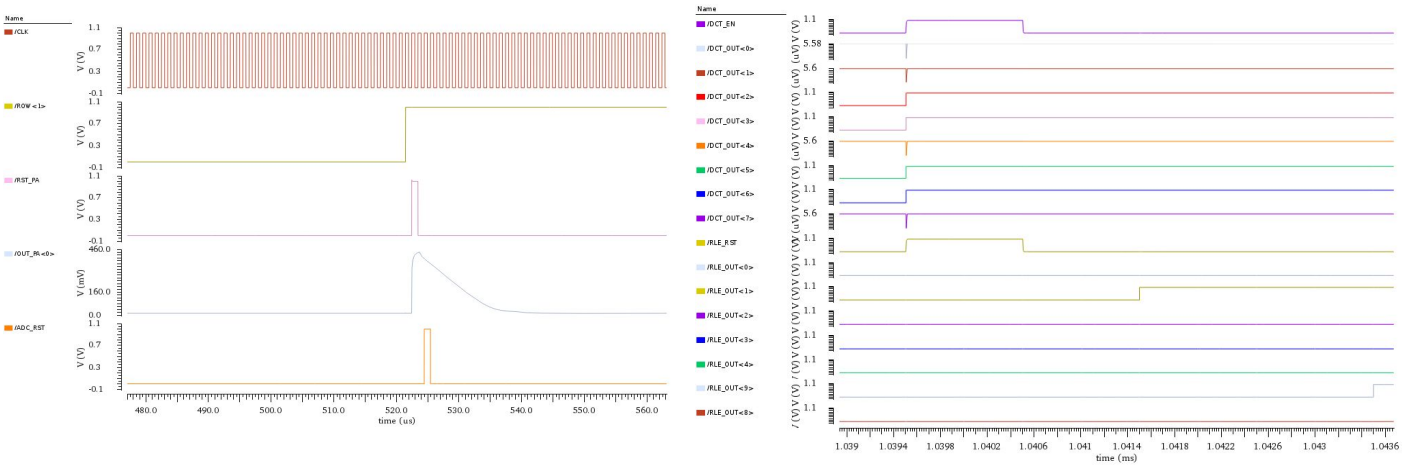


Schematic of Integrated Chip

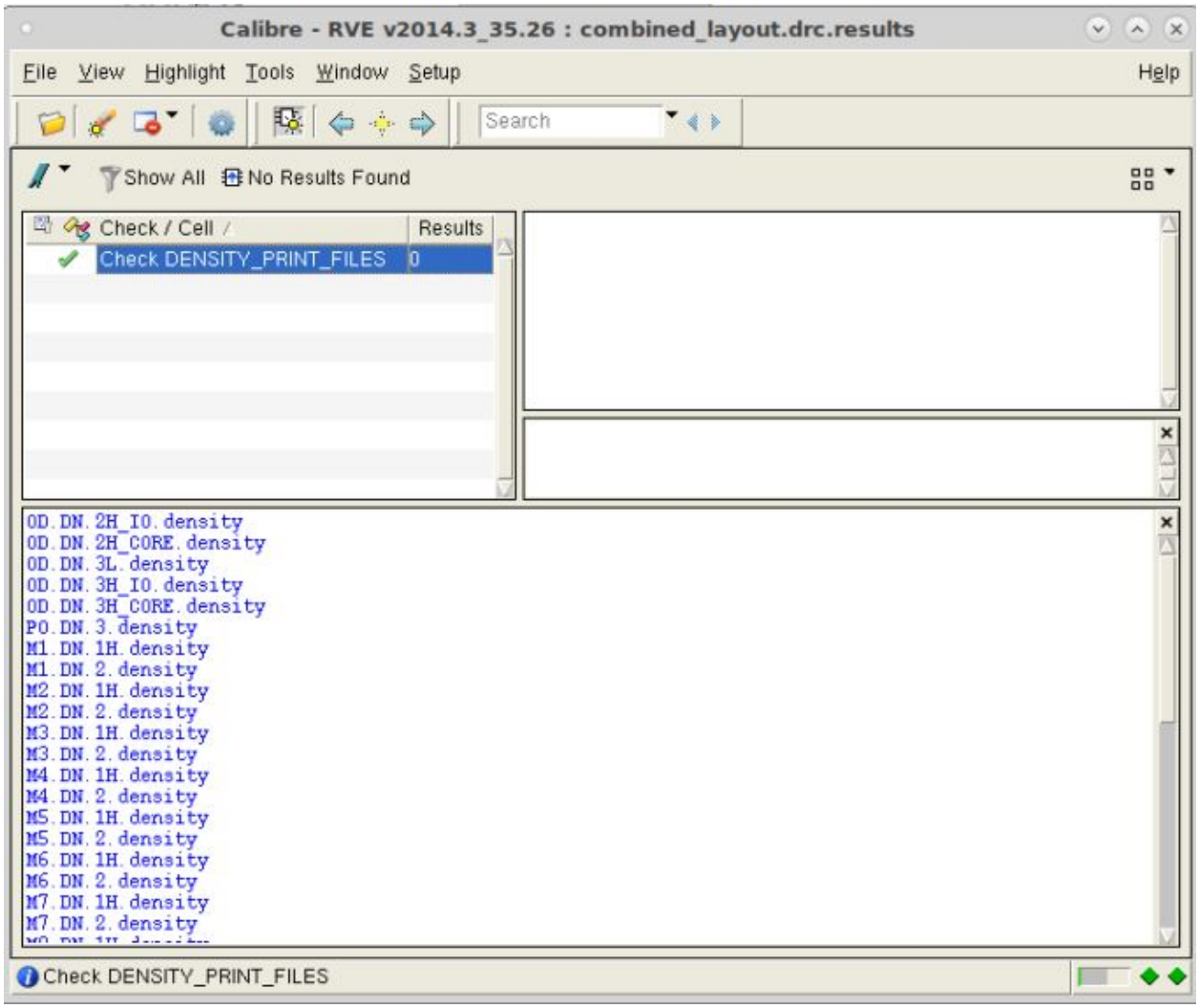


Padframe Layout of Integrated Chip

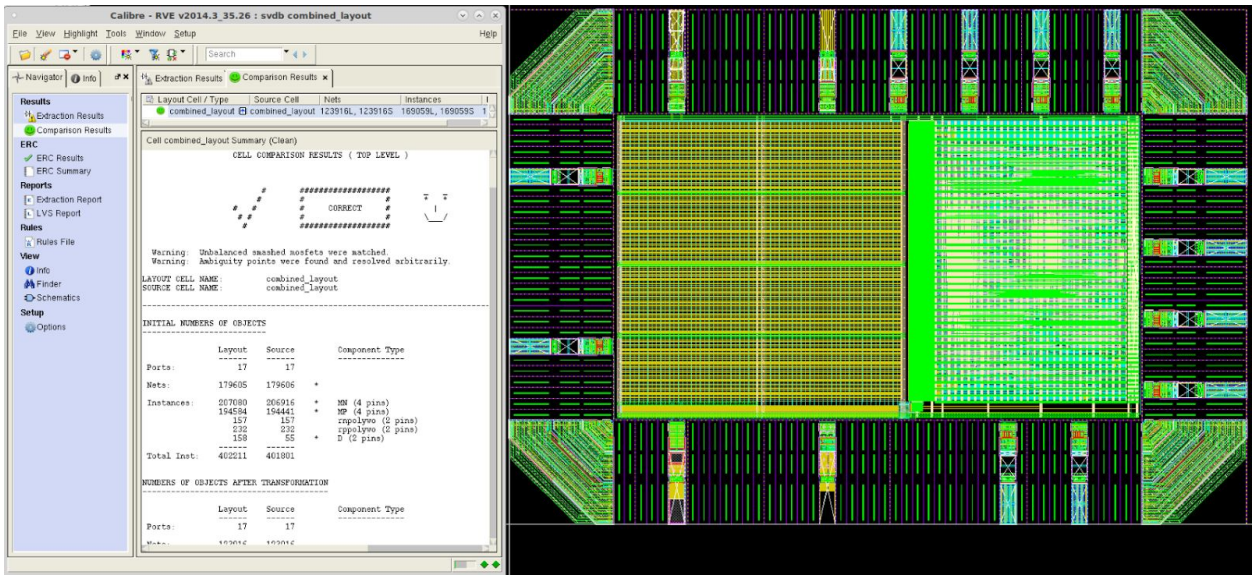




Simulation of Complete Integrated Circuit



DRC Screenshot



LVS Screenshot

Layout v/s Schematic Result:

```
                ##################################################
                ##                                              ##
                ##      C A L I B R E    S Y S T E M            ##
                ##                                              ##
                ##        L V S   R E P O R T                   ##
                ##                                              ##
                ##################################################


REPORT FILE NAME:         combined_layout.lvs.report
LAYOUT NAME:              /nfs/ug/homes-3/v/vargh114/class/final/LVS/combined_layout.sp ('combined_layout')
SOURCE NAME:              /nfs/ug/homes-3/v/vargh114/class/final/LVS/combined_layout.src.net
('combined_layout')
RULE FILE:                /nfs/ug/homes-3/v/vargh114/class/final/LVS/_calibre.lvs_
CREATION TIME:            Mon Dec 23 21:44:02 2019
CURRENT DIRECTORY:        /nfs/ug/homes-3/v/vargh114/class/final/LVS
USER NAME:                vargh114
CALIBRE VERSION:          v2014.3_35.26    Wed Oct 1 13:01:36 PDT 2014


                          OVERALL COMPARISON RESULTS


                    #       ##################        _   _
                  #         #                #        *   *
                #   #       #     CORRECT    #          |
                # #         #                #        \___/
                #           ##################


  Warning:  Unbalanced smashed mosfets were matched.
  Warning:  Ambiguity points were found and resolved arbitrarily.

*************************************************************************************************************
```

```
                                  CELL  SUMMARY
********************************************************************************************************************

  Result         Layout                           Source
  -----------    -----------                      --------------
  CORRECT        combined_layout                  combined_layout


********************************************************************************************************************
                                  LVS PARAMETERS
********************************************************************************************************************


o LVS Setup:

   // LVS COMPONENT TYPE PROPERTY
   // LVS COMPONENT SUBTYPE PROPERTY
   // LVS PIN NAME PROPERTY
   LVS POWER NAME                          "AHVDD" "AHVDDB" "AHVDDG" "AHVDDR" "AHVDDWELL" "AVDD" "AVDDB"
"AVDDBG" "AVDDG" "AVDDR"
                                           "AVDWELL" "DHVDD" "DVDD" "HVDDWELL" "TACVDD" "TAVD33" "TAVD33PST"
"TAVDD" "TAVDDPST"
                                           "VD33" "VDD" "VDD5V" "VDDG" "VDDM" "VDDPST" "VDDSA" "VDWELL" "vdd"
   LVS GROUND NAME                         "AGND" "AHVSS" "AHVSSB" "AHVSSG" "AHVSSR" "AHVSSUB" "AVSS" "AVSSB"
"AVSSBG" "AVSSG"
                                           "AVSSR" "AVSSUB" "DHVSS" "DVSS" "GND" "HVSSUB" "TAVSS" "TAVSSPST"
"VS33" "VSS" "VSSG"
                                           "VSSM" "VSSPST" "VSSUB" "vss"
   LVS CELL SUPPLY                         NO
   LVS RECOGNIZE GATES                     ALL
   LVS IGNORE PORTS                        NO
   LVS CHECK PORT NAMES                    YES
   LVS IGNORE TRIVIAL NAMED PORTS          NO
   LVS BUILTIN DEVICE PIN SWAP             YES
   LVS ALL CAPACITOR PINS SWAPPABLE        YES
   LVS DISCARD PINS BY DEVICE              NO
   LVS SOFT SUBSTRATE PINS                 NO
   LVS INJECT LOGIC                        YES
   LVS EXPAND UNBALANCED CELLS             YES
   LVS FLATTEN INSIDE CELL                 NO
   LVS EXPAND SEED PROMOTIONS              NO
   LVS PRESERVE PARAMETERIZED CELLS        NO
   LVS GLOBALS ARE PORTS                   YES
   LVS REVERSE WL                          NO
   LVS SPICE PREFER PINS                   YES
   LVS SPICE SLASH IS SPACE                YES
   LVS SPICE ALLOW FLOATING PINS           YES
   // LVS SPICE ALLOW INLINE PARAMETERS
   LVS SPICE ALLOW UNQUOTED STRINGS        NO
   LVS SPICE CONDITIONAL LDD               NO
   LVS SPICE CULL PRIMITIVE SUBCIRCUITS   NO
   LVS SPICE IMPLIED MOS AREA              NO
   // LVS SPICE MULTIPLIER NAME
   LVS SPICE OVERRIDE GLOBALS              NO
   LVS SPICE REDEFINE PARAM                NO
   LVS SPICE REPLICATE DEVICES             NO
   LVS SPICE SCALE X PARAMETERS            NO
   LVS SPICE STRICT WL                     NO
   // LVS SPICE OPTION
   LVS STRICT SUBTYPES                     NO
   LVS EXACT SUBTYPES                      NO
   LAYOUT CASE                             YES
   SOURCE CASE                             YES
   LVS COMPARE CASE                        NAMES TYPES
   LVS DOWNCASE DEVICE                     NO
   LVS REPORT MAXIMUM                      50
   LVS PROPERTY RESOLUTION MAXIMUM         65536
   // LVS SIGNATURE MAXIMUM
   // LVS FILTER UNUSED OPTION
   // LVS REPORT OPTION
   LVS REPORT UNITS                        YES
   // LVS NON USER NAME PORT
   // LVS NON USER NAME NET
   // LVS NON USER NAME INSTANCE
   // LVS IGNORE DEVICE PIN

   // Device Type Map
```

```
   LVS DEVICE TYPE                          RESISTOR "rm1" "rm10" "rm2" "rm3" "rm4" "rm5" "rm6" "rm7" "rm8"
"rm9" "rnodl" "rnodl_m"
                                                    "rnods" "rnods_m" "rnodwo" "rnodwo_m" "rnpolyl" "rnpolyl_m"
"rnpolys"
                                                    "rnpolys_m" "rnpolywo" "rnpolywo_m" "rnwod" "rnwod_m"
"rnwsti" "rnwsti_m"
                                                    "rpodl" "rpodl_m" "rpods" "rpods_m" "rpodwo" "rpodwo_m"
"rppolyl" "rppolyl_m"
                                                    "rppolyl_rf" "rppolys" "rppolys_m" "rppolys_rf" "rppolywo"
"rppolywo_m"
                                                    "rppolywo_rf" [ POS=PLUS NEG=MINUS ]  SOURCE LAYOUT

   // Reduction

   LVS REDUCE SERIES MOS                    NO
   LVS REDUCE PARALLEL MOS                  YES
   LVS REDUCE SEMI SERIES MOS               NO
   LVS REDUCE SPLIT GATES                   NO
   LVS REDUCE PARALLEL BIPOLAR              YES
   LVS REDUCE SERIES CAPACITORS             YES
   LVS REDUCE PARALLEL CAPACITORS           YES
   LVS REDUCE SERIES RESISTORS              YES
   LVS REDUCE PARALLEL RESISTORS            YES
   LVS REDUCE PARALLEL DIODES               YES

   LVS REDUCE  rnwsti_m  PARALLEL [ TOLERANCE lr 0 ]
   LVS REDUCE  rnwsti_m  SERIES PLUS MINUS [ TOLERANCE wr 0 ]
   LVS REDUCE  rnwod_m  PARALLEL [ TOLERANCE lr 0 ]
   LVS REDUCE  rnwod_m  SERIES PLUS MINUS [ TOLERANCE wr 0 ]
   LVS REDUCE  rpodwo_m  PARALLEL [ TOLERANCE lr 0 ]
   LVS REDUCE  rpodwo_m  SERIES PLUS MINUS [ TOLERANCE wr 0 ]
   LVS REDUCE  rnodwo_m  PARALLEL [ TOLERANCE lr 0 ]
   LVS REDUCE  rnodwo_m  SERIES PLUS MINUS [ TOLERANCE wr 0 ]
   LVS REDUCE  rpodl_m  PARALLEL [ TOLERANCE lr 0 ]
   LVS REDUCE  rpodl_m  SERIES PLUS MINUS [ TOLERANCE wr 0 ]
   LVS REDUCE  rnodl_m  PARALLEL [ TOLERANCE lr 0 ]
   LVS REDUCE  rnodl_m  SERIES PLUS MINUS [ TOLERANCE wr 0 ]
   LVS REDUCE  rpods_m  PARALLEL [ TOLERANCE lr 0 ]
   LVS REDUCE  rpods_m  SERIES PLUS MINUS [ TOLERANCE wr 0 ]
   LVS REDUCE  rnods_m  PARALLEL [ TOLERANCE lr 0 ]
   LVS REDUCE  rnods_m  SERIES PLUS MINUS [ TOLERANCE wr 0 ]
   LVS REDUCE  rppolys_m  PARALLEL [ TOLERANCE lr 0 ]
   LVS REDUCE  rppolys_m  SERIES PLUS MINUS [ TOLERANCE wr 0 ]
   LVS REDUCE  rnpolys_m  PARALLEL [ TOLERANCE lr 0 ]
   LVS REDUCE  rnpolys_m  SERIES PLUS MINUS [ TOLERANCE wr 0 ]
   LVS REDUCE  rppolyl_m  PARALLEL [ TOLERANCE lr 0 ]
   LVS REDUCE  rppolyl_m  SERIES PLUS MINUS [ TOLERANCE wr 0 ]
   LVS REDUCE  rnpolyl_m  PARALLEL [ TOLERANCE lr 0 ]
   LVS REDUCE  rnpolyl_m  SERIES PLUS MINUS [ TOLERANCE wr 0 ]
   LVS REDUCE  rppolywo_m  PARALLEL [ TOLERANCE lr 0 ]
   LVS REDUCE  rppolywo_m  SERIES PLUS MINUS [ TOLERANCE wr 0 ]
   LVS REDUCE  rnpolywo_m  PARALLEL [ TOLERANCE lr 0 ]
   LVS REDUCE  rnpolywo_m  SERIES PLUS MINUS [ TOLERANCE wr 0 ]
   LVS REDUCE  rppolyl_rf  PARALLEL NO
   LVS REDUCE  rppolyl_rf  SERIES PLUS MINUS NO
   LVS REDUCE  rppolys_rf  PARALLEL NO
   LVS REDUCE  rppolys_rf  SERIES PLUS MINUS NO
   LVS REDUCE  rppolywo_rf  PARALLEL NO
   LVS REDUCE  rppolywo_rf  SERIES PLUS MINUS NO
   LVS REDUCTION PRIORITY                   PARALLEL

   LVS SHORT EQUIVALENT NODES               NO

   // Trace Property

   TRACE PROPERTY  lddp(pch_hv25_spw)  l l 0
   TRACE PROPERTY  lddp(pch_hv25_spw)  w w 0
   TRACE PROPERTY  lddn(nch_hv25_sdnw)  l l 0
   TRACE PROPERTY  lddn(nch_hv25_sdnw)  w w 0

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CELL COMPARISON RESULTS (TOP LEVEL)

Warning: Unbalanced smashed mosfets were matched.
Warning: Ambiguity points were found and resolved arbitrarily.

LAYOUT CELL NAME: combined_layout
SOURCE CELL NAME: combined_layout

INITIAL NUMBERS OF OBJECTS

	Layout	Source	Component Type
Ports:	17	17	
Nets:	179605	179606	*
Instances:	207080	206916	* MN (4 pins)
	194584	194441	* MP (4 pins)
	157	157	rnpolywo (2 pins)
	232	232	rppolywo (2 pins)
	158	55	* D (2 pins)
Total Inst:	402211	401801	

NUMBERS OF OBJECTS AFTER TRANSFORMATION

	Layout	Source	Component Type
Ports:	17	17	
Nets:	123916	123916	
Instances:	12419	12419	MN (4 pins)
	7988	7988	MP (4 pins)
	35	35	rnpolywo (2 pins)
	60	60	rppolywo (2 pins)
	52	52	D (2 pins)
	4608	4608	SMN2 (4 pins)
	512	512	SMP2 (4 pins)
	375	375	SPMN_2_1 (5 pins)
	4	4	SPMN_2_1_1 (6 pins)
	15	15	SPMN_2_2 (6 pins)
	2	2	SPMN_2_2_1 (7 pins)
	15	15	SPMN_2_2_2 (8 pins)
	1	1	SPMN_3_1 (6 pins)
	12	12	SPMN_3_2 (7 pins)
	1760	1760	SPMP_2_1 (5 pins)
	5	5	SPMP_2_1_1 (6 pins)
	772	772	SPMP_2_2 (6 pins)
	10	10	SPMP_2_2_1 (7 pins)
	116	116	SPMP_3_1 (6 pins)
	2	2	SPMP_3_2 (7 pins)
	29129	29129	_invb (6 pins)
	64836	64836	_invv (4 pins)
	10160	10160	_invx2v (4 pins)
	6	6	_mx2v (6 pins)
	5449	5449	_nand2v (5 pins)
	21	21	_nand3v (6 pins)
	196	196	_nand4v (7 pins)
	471	471	_nor2v (5 pins)
	119	119	_nor3v (6 pins)
	125	125	_nor4v (7 pins)

```
                41        41        _pmn2v (4 pins)
                10        10        _pmp2b (5 pins)
                4         4         _pmp2v (4 pins)
                12        12        _smn2b (5 pins)
                9747      9747               _smn2v (4 pins)
                1354      1354               _smn3v (5 pins)
                7967      7967               _smp2v (4 pins)
                13        13        _smp3v (5 pins)
                7219      7219               _tgmb (7 pins)
                1         1         _xnor2v (5 pins)
                2815      2815               _xr2v (5 pins)
                601       601       _xra2v (5 pins)
                ------    ------
 Total Inst:    169059    169059

        * = Number of objects in layout different from number in source.


****************************************************************************************************************
                                INFORMATION AND WARNINGS
****************************************************************************************************************

                Matched   Matched   Unmatched          Unmatched          Component
                Layout    Source              Layout             Source   Type
                -------   -------   ---------          ---------          ---------
   Ports:                 17        17                 0                  0

   Nets:        123916    123916              0                  0

   Instances:   12232     12232               0                  0        MN(nch)
                          137       137                0                  0        MN(nch_25od)
                          1         1                  0                  0        MN(nch_hvt)
                          49        49                 0                  0        MN(nch_na25)
                7828      7828                0                  0        MP(pch)
                          160       160                0                  0        MP(pch_25od)
                          35        35                 0                  0        rnpolywo
                          60        60                 0                  0        rppolywo
                          35        35                 0                  0        D(ndio)
                          1         1                  0                  0        D(ndio_25od)
                          12        12                 0                  0        D(ndio_esd)
                          2         2                  0                  0        D(pdio)
                          2         2                  0                  0        D(pdio_25od)
                4608      4608                0                  0        SMN2
                          512       512                0                  0        SMP2
                          375       375                0                  0        SPMN_2_1
                          4         4                  0                  0        SPMN_2_1_1
                          15        15                 0                  0        SPMN_2_2
                          2         2                  0                  0        SPMN_2_2_1
                          15        15                 0                  0        SPMN_2_2_2
                          1         1                  0                  0        SPMN_3_1
                          12        12                 0                  0        SPMN_3_2
                1760      1760                0                  0        SPMP_2_1
                          5         5                  0                  0        SPMP_2_1_1
                          772       772                0                  0        SPMP_2_2
                          10        10                 0                  0        SPMP_2_2_1
                          116       116                0                  0        SPMP_3_1
                          2         2                  0                  0        SPMP_3_2
                29129     29129               0                  0        _invb
                64836     64836               0                  0        _invv
                10160     10160               0                  0        _invx2v
                          6         6                  0                  0        _mx2v
                5449      5449                0                  0        _nand2v
                          21        21                 0                  0        _nand3v
                          196       196                0                  0        _nand4v
                          471       471                0                  0        _nor2v
                          119       119                0                  0        _nor3v
                          125       125                0                  0        _nor4v
                          41        41                 0                  0        _pmn2v
                          10        10                 0                  0        _pmp2b
                          4         4                  0                  0        _pmp2v
                          12        12                 0                  0        _smn2b
                9747      9747                0                  0        _smn2v
                1354      1354                0                  0        _smn3v
                7967      7967                0                  0        _smp2v
                          13        13                 0                  0        _smp3v
```

```
                7219     7219            0               0       _tgmb
                         1        1              0               0       _xnor2v
                2815     2815            0               0       _xr2v
                         601      601            0               0       _xra2v
                -------  -------  ---------      ---------
   Total Inst:  169059   169059          0               0


o Statistics:

   4749 layout mos transistors were reduced to 1212.
        3537 mos transistors were deleted by parallel reduction.
   4222 source mos transistors were reduced to 992.
        3230 mos transistors were deleted by parallel reduction.

   339 series/parallel layout resistors were reduced to 45.  2 connecting nets were deleted.
   339 series/parallel source resistors were reduced to 45.  2 connecting nets were deleted.

   126 parallel layout diodes were reduced to 20.
   6 parallel source diodes were reduced to 3.

   101 nets and 51 instances were matched arbitrarily.


o Initial Correspondence Points:

   Ports:       VSS! VDD! VSSPST! VDDPST! PAD_OUT<9> PAD_OUT<8> PAD_OUT<7> PAD_OUT<6>
                PAD_OUT<5> PAD_OUT<4> PAD_OUT<0> PAD_OUT<1> PAD_OUT<2> PAD_OUT<3> PAD_IN<1>
                PAD_IN<0> POC!


o Ambiguity Resolution Points:

        (Each one of the following objects belongs to a group of indistinguishable objects.
        The listed objects were matched arbitrarily by the Ambiguity Resolution feature of LVS.
        Arbitrary matching may be prevented by assigning names to these objects or to adjacent nets).

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. X10266/X25/M1(295.900,113.815)                        XI5/XI8/MM_121
        ** missing smashed mosfet **                            XI5/XI8/MM_111
        ** missing smashed mosfet **                            XI5/XI8/MM_113
        ** missing smashed mosfet **                            XI5/XI8/MM_115
        ** missing smashed mosfet **                            XI5/XI8/MM_123

        X10227/X10/X13/X1/M0(566.795,66.095)                    XI5/XI7/MM_71
        X10227/X10/X17/X1/M0(588.235,66.095)                    XI5/XI7/MM_73
        X10227/X10/X16/X1/M0(582.875,66.095)                    XI5/XI7/MM_75
        X10227/X10/X15/X1/M0(577.515,66.095)                    XI5/XI7/MM_77
        X10227/X10/X14/X1/M0(572.155,66.095)                    XI5/XI7/MM_72
        ** missing smashed mosfet **                            XI5/XI7/MM_74
        ** missing smashed mosfet **                            XI5/XI7/MM_79
        ** missing smashed mosfet **                            XI5/XI7/MM_80
        ** missing smashed mosfet **                            XI5/XI7/MM_78
        ** missing smashed mosfet **                            XI5/XI7/MM_76


****************************************************************************************************************
                                        SUMMARY
****************************************************************************************************************

Total CPU Time:  8 sec
Total Elapsed Time:  9 sec
```

Design Path: /nfs/ug/homes-3/v/vargh114/class/final/comb