Project-3 Report
VLSI DESIGN METHODOLOGY

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Answer 1

1.1)

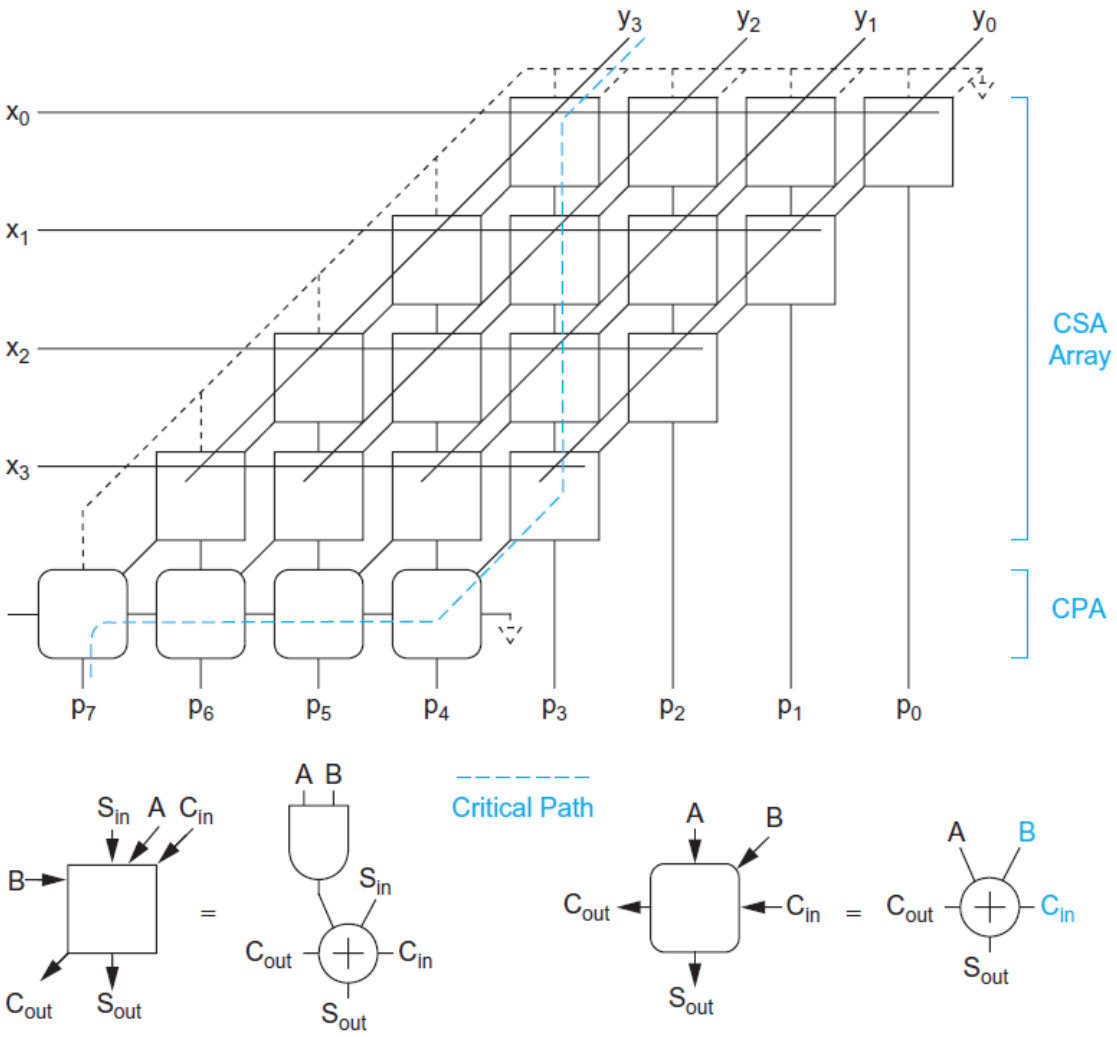


Figure 1 shows the digital logic of an unsigned array multiplier to calculate the unsigned product of two unsigned 4-bit numbers

The following is the verilog code to calculate the calculate the unsigned product of two unsigned 4-bit numbers

Verilog Code:

```
`timescale 1ns/1ps

module multiplier(a,b,p);//Multiplier

//inputs
```

```
input [3:0]a,b;
//outputs
output [7:0]p;
//wires
wire S0[0:3], S1[0:3], S2[0:3], S3[0:3], C0[0:3], C1[0:3], C2[0:3], C3[0:3],Cinp_p[0:4];
APS APS00(a[0],b[0],1'b0,1'b0,S0[0],C0[0]);
APS APS01(a[1],b[0],1'b0,1'b0,S0[1],C0[1]);
APS APS02(a[2],b[0],1'b0,1'b0,S0[2],C0[2]);
APS APS03(a[3],b[0],1'b0,1'b0,S0[3],C0[3]);
APS APS04(a[0],b[1],S0[1],C0[0],S1[0],C1[0]);
APS APS05(a[1],b[1],S0[2],C0[1],S1[1],C1[1]);
APS APS06(a[2],b[1],S0[3],C0[2],S1[2],C1[2]);
APS APS07(a[3],b[1],1'b0,C0[3],S1[3],C1[3]);
APS APS08(a[0],b[2],S1[1],C1[0],S2[0],C2[0]);
APS APS09(a[1],b[2],S1[2],C1[1],S2[1],C2[1]);
APS APS10(a[2],b[2],S1[3],C1[2],S2[2],C2[2]);
APS APS11(a[3],b[2],1'b0,C1[3],S2[3],C2[3]);
APS APS12(a[0],b[3],S2[1],C2[0],S3[0],C3[0]);
APS APS13(a[1],b[3],S2[2],C2[1],S3[1],C3[1]);
APS APS14(a[2],b[3],S2[3],C2[2],S3[2],C3[2]);
APS APS15(a[3],b[3],1'b0,C1[3],S3[3],C3[3]);
MNA MNA0 (S3[0],1'b0,1'b0,p[3],Cinp_p[1]);
MNA MNA1 (S3[1],C3[0],Cinp_p[1],p[4],Cinp_p[2]);
MNA MNA2 (S3[2],C3[1],Cinp_p[2],p[5],Cinp_p[3]);
MNA MNA3 (S3[3],C3[2],Cinp_p[3],p[6],Cinp[4]);
assign p[7]=Cinp_p[4];
assign p[0]=S0[0];
assign p[1]=S1[0];
assign p[2]=S2[0];
endmodule
```

```
module APS (a,b,Sin,Cin,Sout,Cout); //Carry Save Adder
input a,b,Sin,Cin;
output Sout, Cout;
wire pp;
assign pp=a&b; //pp stands for partial product
assign Sout=Sin^Cin^pp;
assign Cout=(pp&Sin)|(Cin&(pp^Sin));
endmodule
module MNA (Sin, Cin, Cinp_p, Sout, Cout);//Carry Propagation Adder
//inputs
input Sin,Cin,Cinp_p;
//outputs
output Sout, Cout;
assign Sout=Sin^Cin^Cinp_p;
assign Cout=(Sin&Cin)|(Cinp_p&(Sin^Cin));
endmodule
```

1.2 NC verilog Testbench:

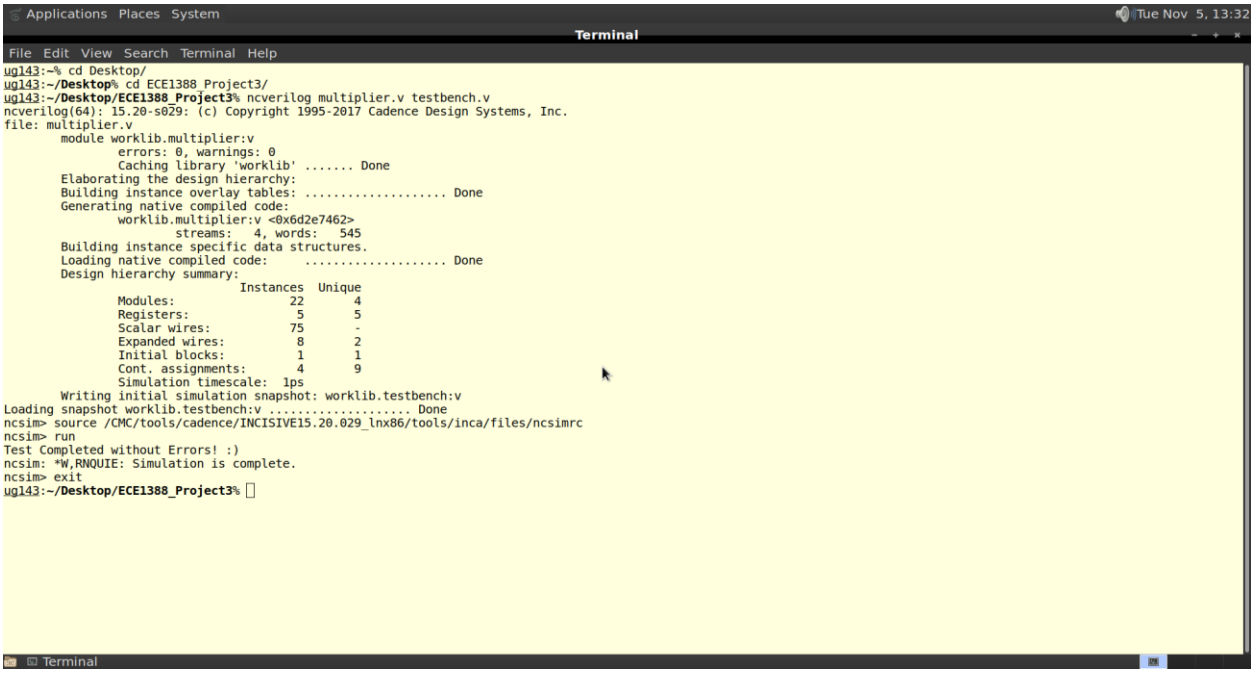


Figure 2 shows the output of NC verilog testbench

ug146:~/Desktop/ECE1388_Project3_1% ncverilog multiplier.v testbench.v

ncverilog(64): 15.20-s029: (c) Copyright 1995-2017 Cadence Design Systems, Inc.

Loading snapshot worklib.testbench:v ..... Done

ncsim> source /CMC/tools/cadence/INCISIVE15.20.029_lnx86/tools/inca/files/ncsimrc

ncsim> run

Test Completed without Errors! :)

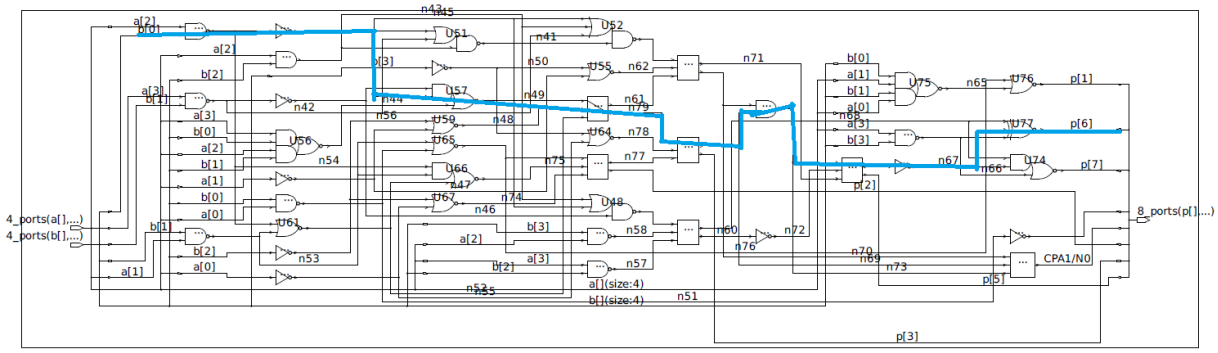
ncsim: *W,RNQUIE: Simulation is complete.

ncsim> exit

Answer 2:

2.1 Schematic with highlighted critical path:

b[0] to p[6] was found to be the critical path from the timing report



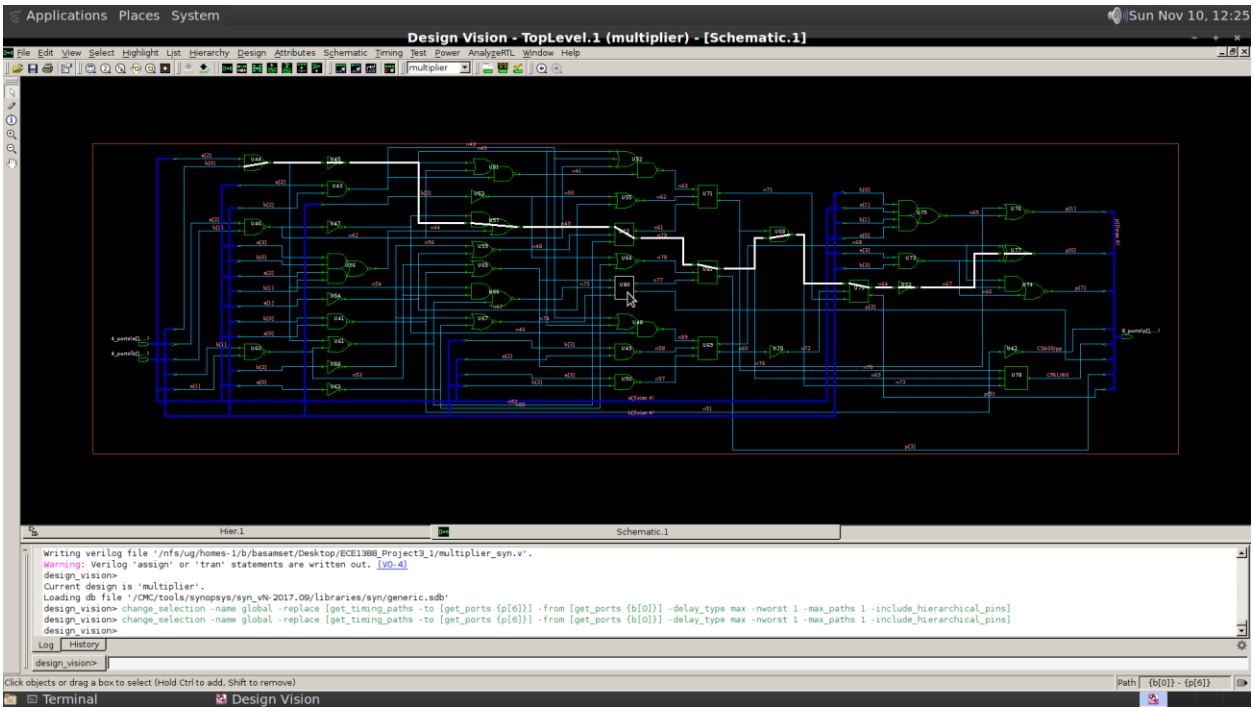


Figure 3 shows Schematic of multiplier with critical path

2.2 Area report:

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Report : area

Design : multiplier

Version: N-2017.09

Date : Sat Nov 9 14:15:28 2019

****

Library(s) Used:

tcbn65gpluswc (File: /CMC/kits/tsmc_65nm_libs/tcbn65gplus/TSMCHOME/digital/Front_End/timing_power_noise/NLDM/tcbn65gplus_140b/tcbn65gpluswc.db)

Number of ports: 16

Number of nets: 55

Number of cells: 41

Number of combinational cells: 41

Number of sequential cells: 0

Number of macros/black boxes: 0

Number of buf/inv: 9

Number of references: 11

Combinational area: 115.200002

Buf/Inv area: 9.720000

Noncombinational area: 0.000000

Macro/Black Box area: 0.000000

Net Interconnect area: undefined (Wire load has zero net area)

Total cell area: **115.200002**

Total area: undefined

1

Timing Report:

****

Report : timing

-path full

-delay max

-max_paths 1

Design : multiplier

Version: N-2017.09

Date : Sat Nov 9 14:15:28 2019

****

Operating Conditions: WCCOM Library: tcbn65gpluswc

Wire Load Model Mode: segmented

Startpoint: b[0] (input port)

Endpoint: p[6] (output port)

Path Group: (none)

Path Type: max

Des/Clust/Port	Wire Load Model	Library
multiplier	ZeroWireload	tcbn65gpluswc

Point	Incr	Path
input external delay	0.00	0.00 f
b[0] (in)	0.00	0.00 f
U44/ZN (CKND2D0)	0.04	0.04 r
U45/ZN (INVD0)	0.04	0.08 f
U57/ZN (AOI21D0)	0.06	0.14 r
U62/S (FA1D0)	0.17	0.31 f
U81/CO (FA1D0)	0.16	0.47 f
U68/Z (CKAN2D0)	0.07	0.54 f
U79/CO (FA1D0)	0.16	0.70 f
U72/ZN (INVD0)	0.04	0.73 r
U77/ZN (XNR3D0)	0.17	0.90 r
p[6] (out)	0.00	0.90 r
data arrival time		0.90

(Path is unconstrained)

Results:

The total area was found to be 115.200002 um^2

The total delay was found to be 0.90 ns

The clock frequency is 1.11Ghz

2.3 NC Verilog Test bench:

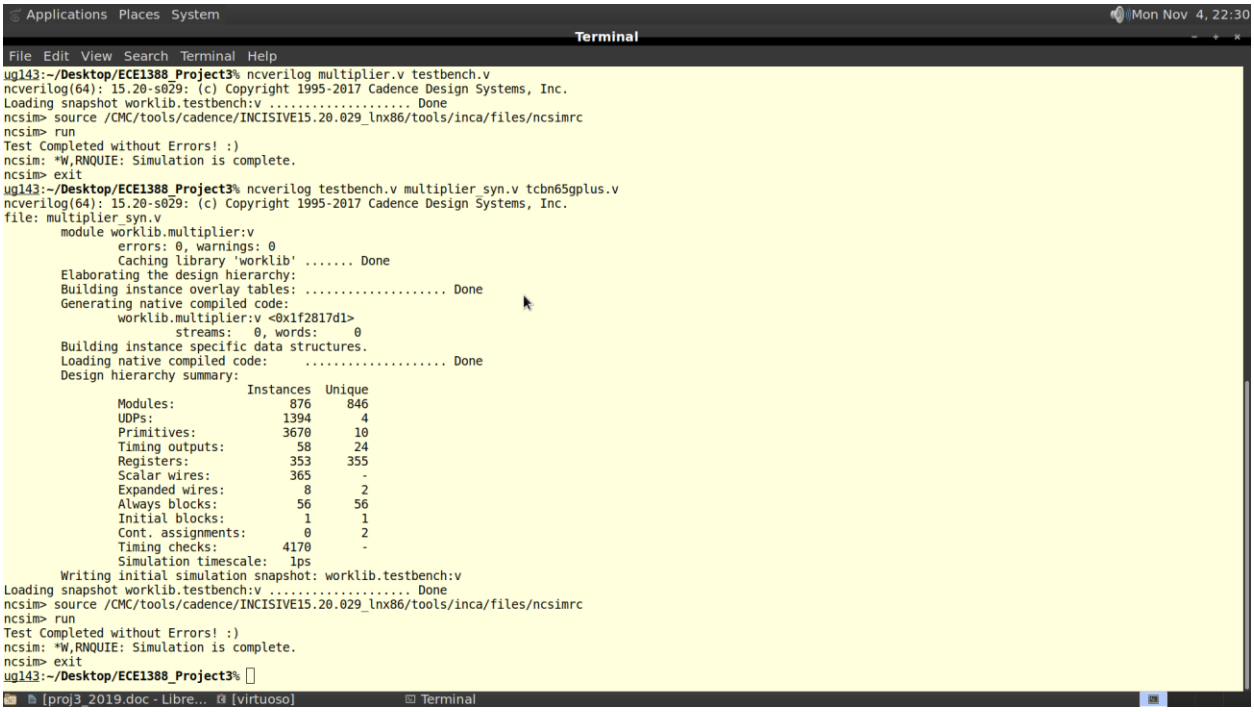


Figure 4 shows the output of NC verilog testbench

ug146:~/Desktop/ECE1388_Project3_1% ncverilog multiplier.v testbench.v

ncverilog(64): 15.20-s029: (c) Copyright 1995-2017 Cadence Design Systems, Inc.

Building instance specific data structures.

Loading native compiled code: ..... Done

Design hierarchy summary:

	Instances	Unique
Modules:	**876**	**846**
UDPs:	**1394**	**4**
Primitives:	**3670**	**10**
Timing outputs:	**58**	**24**

Registers: 353 355

Scalar wires: 365 -

Expanded wires: 8 2

Always blocks: 56 56

Initial blocks: 1 1

Cont. assignments: 0 2

Timing checks: 4170 -

Simulation timescale: 1ps

Writing initial simulation snapshot: worklib.testbench:v

Loading snapshot worklib.testbench:v ..... Done

ncsim> source /CMC/tools/cadence/INCISIVE15.20.029_lnx86/tools/inca/files/ncsimrc

ncsim> run

Test Completed without Errors! :)

ncsim: *W,RNQUIE: Simulation is complete.

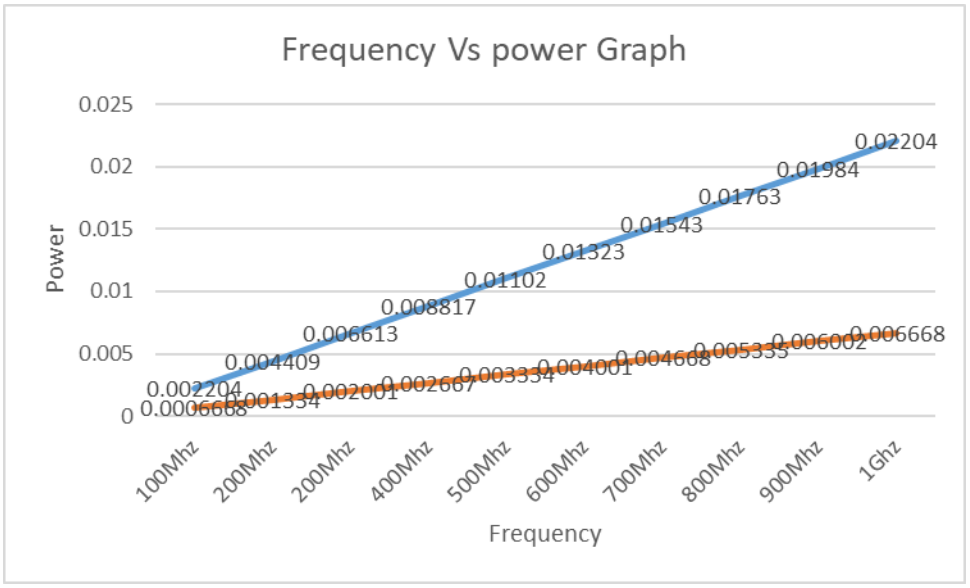
ncsim> exit

Answer 3:

3.6 Power analysis:

Frequency	Internal Power	Switching Power
100Mhz	0.002204	0.000667
200Mhz	0.004409	0.001334
200Mhz	0.006613	0.002001
400Mhz	0.008817	0.002667
500Mhz	0.01102	0.003334
600Mhz	0.01323	0.004001
700Mhz	0.01543	0.004668
800Mhz	0.01763	0.005335
900Mhz	0.01984	0.006002
1Ghz	0.02204	0.006668

The above table shows Frequency vs Internal and switching power values



The above graph represents frequency vs Internal power(blue) and switching power(Orange)

3.7 Area:

Total area of Standard cells: 166.320 um^2

Total area of Standard cells(Subtracting Physical Cells): 115.200 um^2

Total area of Macros: 0.000 um^2

Total area of Blockages: 0.000 um^2

Total area of Pad cells: 0.000 um^2

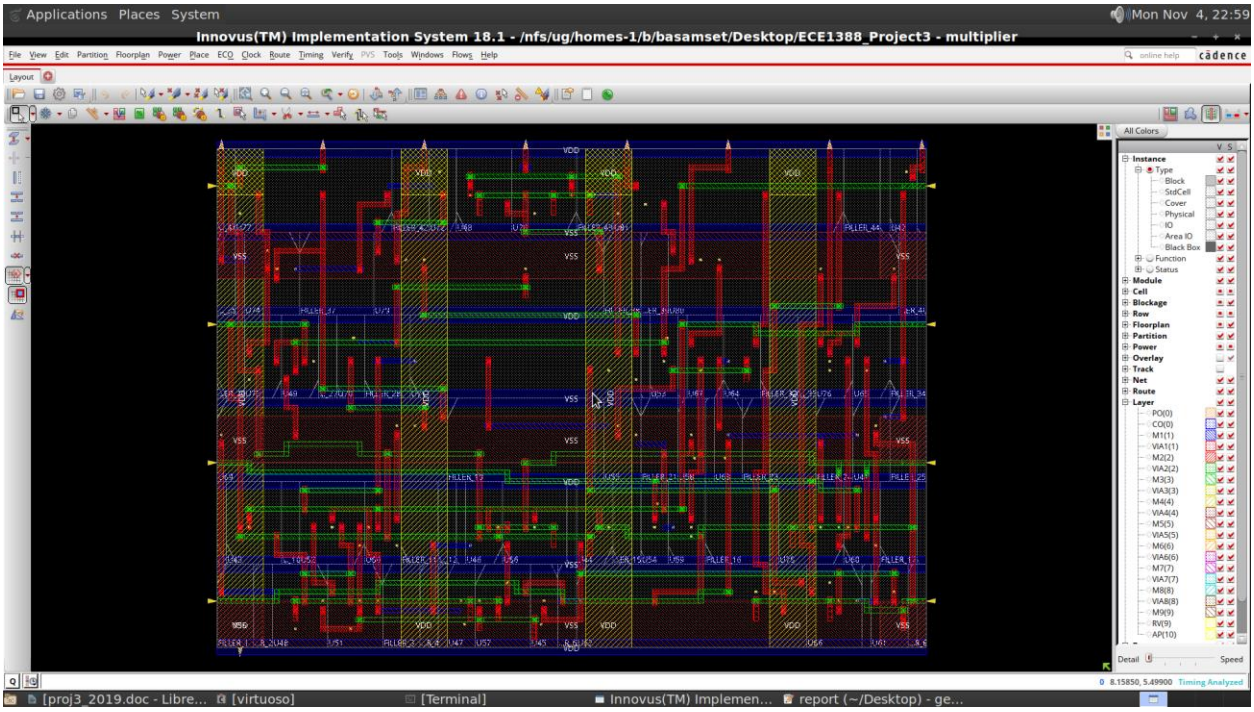
Total area of Core: 166.320 um^2

Total area of Chip: 166.320 um^2

Total area of Core: 166.320 um^2

The difference is about 51.11 um^2 due to the extra area added due to physical cells. All cells of a standard cell library have the same height. Some standard cells contain more (or larger) transistors than others, which requires more area. These cells are wider than others which in turn results in more area consumption.

3.8 Screen capture of your placed & routed design in Cadence Encounter



3.9 NC Verilog testbench report

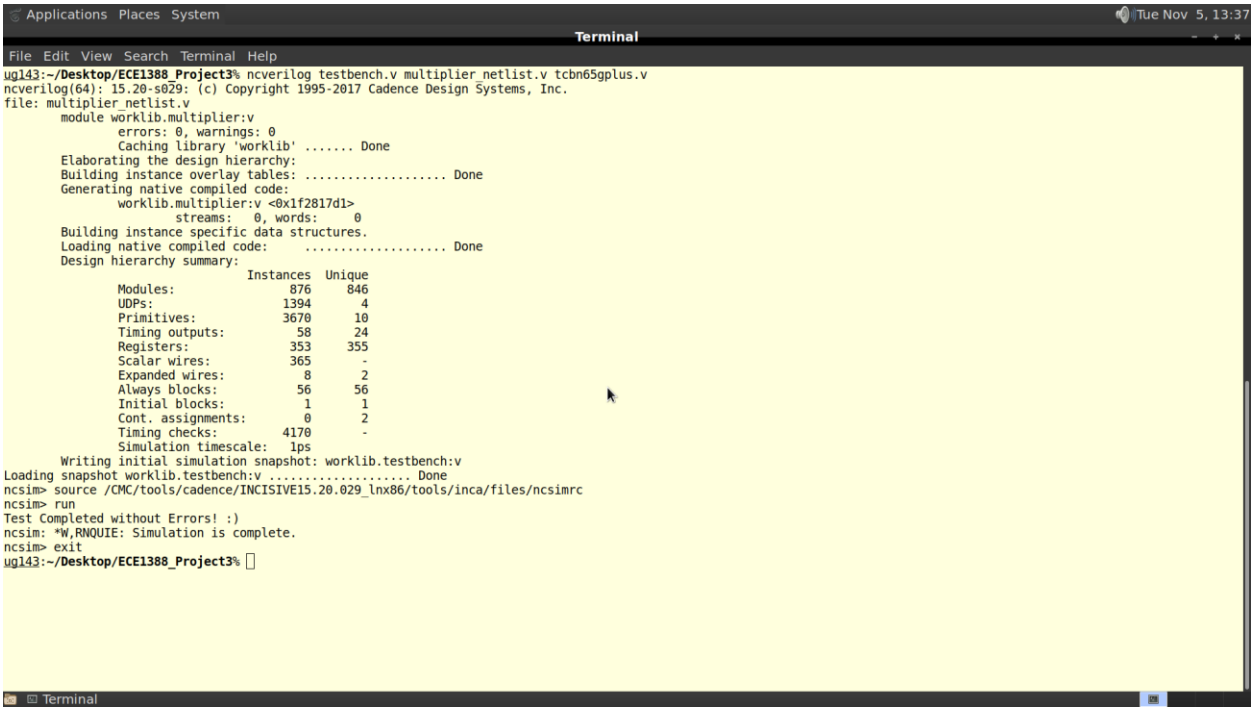


Figure shows the output of NC verilog testbench

ug146:~/Desktop/ECE1388_Project3_1% ncverilog testbench.v multiplier_netlist.v tcbn65gplus.v

ncverilog(64): 15.20-s029: (c) Copyright 1995-2017 Cadence Design Systems, Inc.

Loading snapshot worklib.testbench:v ..... Done

ncsim> source /CMC/tools/cadence/INCISIVE15.20.029_lnx86/tools/inca/files/ncsimrc

ncsim> run

Test Completed without Errors! :)

ncsim: *W,RNQUIE: Simulation is complete.

ncsim> exit