EXPERIMENT- 5
Verilog Switch Level Modeling

Objective:

To study switch level modeling style of Verilog with examples.

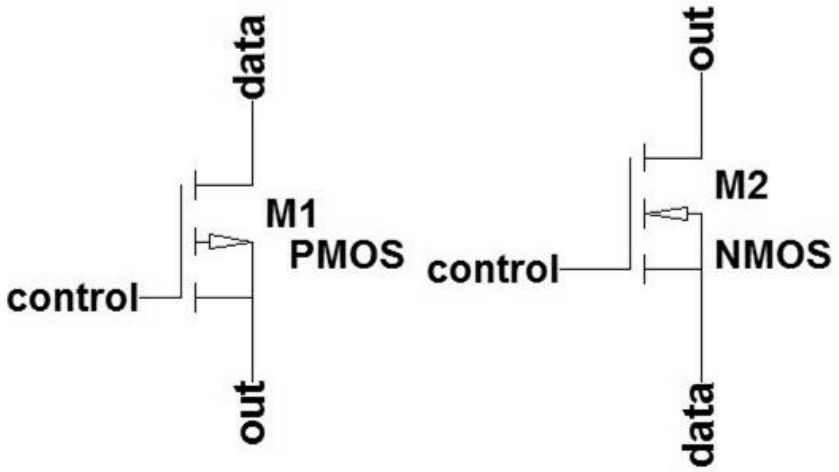
Theory:

Usually, transistor level modeling is referred to modeling hardware structures using transistor models with analog input and output signal values. On the other hand, gate level modeling refers to modeling hard- ware structures using gate models with digital input and output signal values. Between these two modeling schemes is what is referred to as switch level modeling. At this level, a hardware component is described at the transistor level, but transistors only exhibit digital behavior and their input, and output signal values are only limited to digital values. At the switch level, transistors behave as on-off switches. Verilog uses a 4-value logic value system, so Verilog switch input and output signals can take any of the four 0, 1, Z, and X logic values.

Syntax

```
nmos n1(out, data, control ) ;
pmos p1(out, data, control ) ;
```

Two types of MOS switches, nmos is used to model NMOS transistor, pmos is used to model PMOS transistors. The symbols for NMOS and PMOS switches are shown in below given figure.



Symbol for NMOS and PMOS transistor

Exercise Problems

1. **Write the Verilog code for a 3 input CMOS NAND gate and $F = \overline{E(A + BCD)}$ with test benches.**

CMOS NAND

Source Code

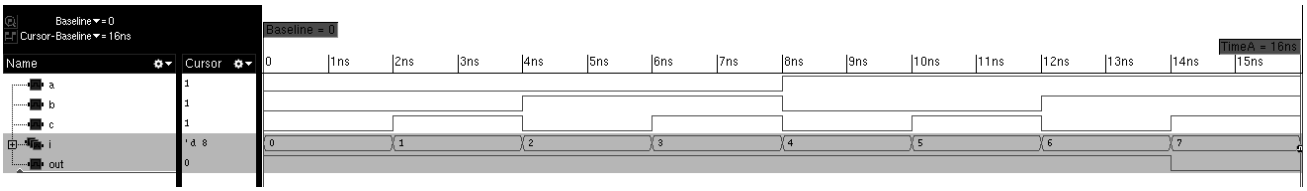
```
module cmosnand(a,b,c,out);
  input a,b,c;
  output out;
  supply1 vdd;
  supply0 gnd;
  pmos p1(out,vdd,a);
  pmos p2(out,vdd,b);
  pmos p3(out,vdd,c);
  nmos n1(out,w1,a);
  nmos n2(w1,w2,b);
  nmos n3(w2,gnd,c);
endmodule
```

Testbench

```
module tb();
  reg a,b,c;
  wire out;
  integer i;
  cmosnand uut (.a(a), .b(b), .c(c), .out(out));
  initial
  begin
    $monitor($time," | a = %b | b = %b | c = %b | out = %b", a, b, c,
out);
    a=0;
    b=0;
    c=0;
    for(i=0;i<=7;i=i+1)
    begin
      {a,b,c}=i;
      #2;
```

```
    end
    $finish;
  end
endmodule
```

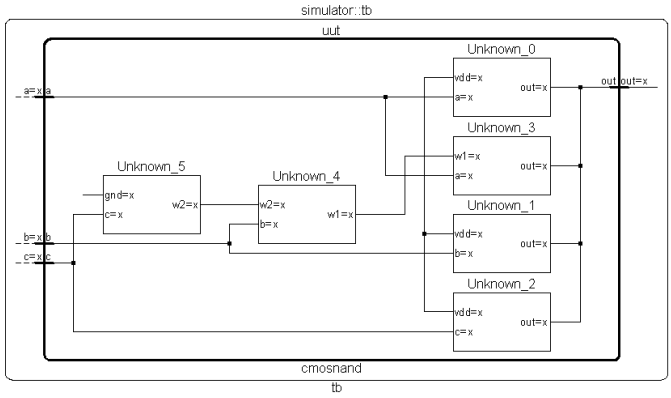
Waveform



Console

```
ncsim>
ncsim> source /home/install/INCISIVE152/tools/inca/files/ncsimrc
ncsim> run
                 0 | a = 0 | b = 0 | c = 0 | out = 1
                 2 | a = 0 | b = 0 | c = 1 | out = 1
                 4 | a = 0 | b = 1 | c = 0 | out = 1
                 6 | a = 0 | b = 1 | c = 1 | out = 1
                 8 | a = 1 | b = 0 | c = 0 | out = 1
                10 | a = 1 | b = 0 | c = 1 | out = 1
                12 | a = 1 | b = 1 | c = 0 | out = 1
                14 | a = 1 | b = 1 | c = 1 | out = 0
Simulation complete via $finish(1) at time 16 NS + 0
./cmos_nand_tb.v:14 $finish;
ncsim>
```

Schematic



$$F = \overline{E(A + BCD)}$$

Source Code

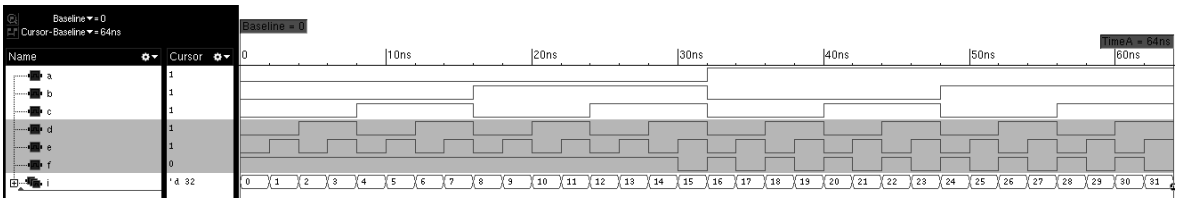
```
module function1(f,a,b,c,d,e);
  output f;
  input a,b,c,d,e;
  supply1 vdd;
  supply0 gnd;
  wire f;
  pmos m1(w1,vdd,b);
  pmos m2(w1,vdd,c);
  pmos m3(w1,vdd,d);
  pmos m4(f,w1,a);
  pmos m5(f,vdd,e);
  nmos m6(f,w2,b);
  nmos m7(w2,w3,c);
  nmos m8(w3,w4,d);
  nmos m9(f,w4,a);
  nmos m10(w4,gnd,e);
endmodule
```

Testbench

```
module tb();
  reg a,b,c,d,e;
  wire f;
  integer i;
  function1 uut (.f(f), .a(a), .b(b), .c(c), .d(d), .e(e));
  initial
  begin
    $monitor($time," | a = %b | b = %b | c = %b | d = %b | e = %b | f =
%b", a, b, c, d, e, f);
    a=0;
    b=0;
    c=0;
    d=0;
    e=0;
    for(i=0;i<=31;i=i+1)
```

```
    begin
      {a,b,c,d,e}=i;
      #2;
    end
    $finish;
  end
endmodule
```

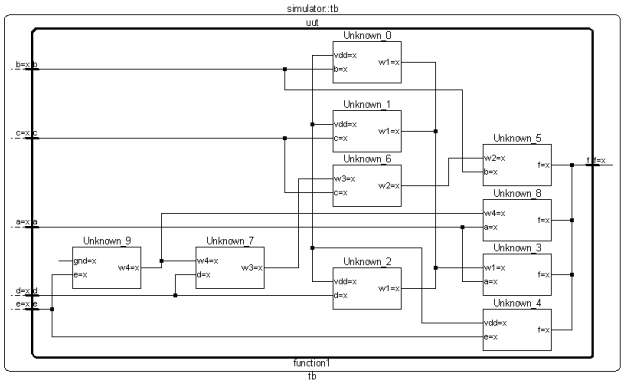
Waveform



Console

```
ncsim> source /home/install/INCISIVE152/tools/inca/files/ncsimrc
ncsim> run
                   0 | a = 0 | b = 0 | c = 0 | d = 0 | e = 0 | f = 1
                   2 | a = 0 | b = 0 | c = 0 | d = 0 | e = 1 | f = 1
                   4 | a = 0 | b = 0 | c = 0 | d = 1 | e = 0 | f = 1
                   6 | a = 0 | b = 0 | c = 0 | d = 1 | e = 1 | f = 1
                   8 | a = 0 | b = 0 | c = 1 | d = 0 | e = 0 | f = 1
                  10 | a = 0 | b = 0 | c = 1 | d = 0 | e = 1 | f = 1
                  12 | a = 0 | b = 0 | c = 1 | d = 1 | e = 0 | f = 1
                  14 | a = 0 | b = 0 | c = 1 | d = 1 | e = 1 | f = 1
                  16 | a = 0 | b = 1 | c = 0 | d = 0 | e = 0 | f = 1
                  18 | a = 0 | b = 1 | c = 0 | d = 0 | e = 1 | f = 1
                  20 | a = 0 | b = 1 | c = 0 | d = 1 | e = 0 | f = 1
                  22 | a = 0 | b = 1 | c = 0 | d = 1 | e = 1 | f = 1
                  24 | a = 0 | b = 1 | c = 1 | d = 0 | e = 0 | f = 1
                  26 | a = 0 | b = 1 | c = 1 | d = 0 | e = 1 | f = 1
                  28 | a = 0 | b = 1 | c = 1 | d = 1 | e = 0 | f = 1
                  30 | a = 0 | b = 1 | c = 1 | d = 1 | e = 1 | f = 0
                  32 | a = 1 | b = 0 | c = 0 | d = 0 | e = 0 | f = 1
                  34 | a = 1 | b = 0 | c = 0 | d = 0 | e = 1 | f = 0
                  36 | a = 1 | b = 0 | c = 0 | d = 1 | e = 0 | f = 1
                  38 | a = 1 | b = 0 | c = 0 | d = 1 | e = 1 | f = 0
                  40 | a = 1 | b = 0 | c = 1 | d = 0 | e = 0 | f = 1
                  42 | a = 1 | b = 0 | c = 1 | d = 0 | e = 1 | f = 0
                  44 | a = 1 | b = 0 | c = 1 | d = 1 | e = 0 | f = 1
                  46 | a = 1 | b = 0 | c = 1 | d = 1 | e = 1 | f = 0
                  48 | a = 1 | b = 1 | c = 0 | d = 0 | e = 0 | f = 1
                  50 | a = 1 | b = 1 | c = 0 | d = 0 | e = 1 | f = 0
                  52 | a = 1 | b = 1 | c = 0 | d = 1 | e = 0 | f = 1
                  54 | a = 1 | b = 1 | c = 0 | d = 1 | e = 1 | f = 0
                  56 | a = 1 | b = 1 | c = 1 | d = 0 | e = 0 | f = 1
                  58 | a = 1 | b = 1 | c = 1 | d = 0 | e = 1 | f = 0
                  60 | a = 1 | b = 1 | c = 1 | d = 1 | e = 0 | f = 1
                  62 | a = 1 | b = 1 | c = 1 | d = 1 | e = 1 | f = 0
Simulation complete via $finish(1) at time 64 NS + 0
./function1_tb.v:14 $finish;
ncsim>
```

Schematic



2. Write Verilog code for the following combinational logic function using CMOS logic, $F = \overline{(ABC + DE)}$

Source Code

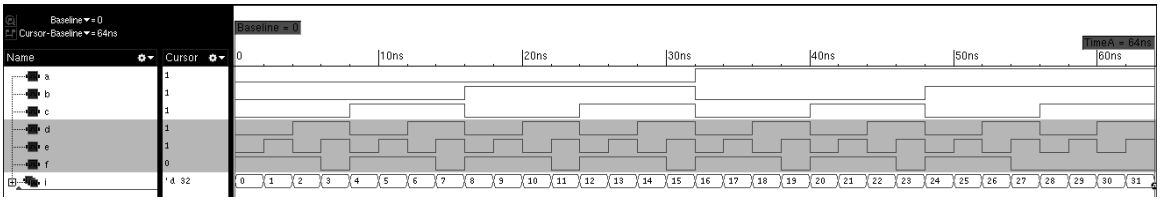
```
module function2(f,a,b,c,d,e);
  output f;
  input a,b,c,d,e;
  supply1 vdd;
  supply0 gnd;
  wire f;
  pmos m1(w1,vdd,a);
  pmos m2(w1,vdd,b);
  pmos m3(w1,vdd,c);
  pmos m4(f,w1,d);
  pmos m5(f,w1,e);
  nmos m6(f,w2,a);
  nmos m7(w2,w3,b);
  nmos m8(w3,gnd,c);
  nmos m9(f,w4,d);
  nmos m10(w4,gnd,e);
endmodule
```

Testbench

```
module tb();
  reg a,b,c,d,e;
  wire f;
  integer i;
  function2 uut (.f(f), .a(a), .b(b), .c(c), .d(d), .e(e));
  initial
  begin
    $monitor($time," | a = %b | b = %b | c = %b | d = %b | e = %b | f =
%b", a, b, c, d, e, f);
    a=0;
    b=0;
    c=0;
    d=0;
    e=0;
```

```
    for(i=0;i<=31;i=i+1)
    begin
      {a,b,c,d,e}=i;
      #2;
    end
    $finish;
  end
endmodule
```

Waveform



Console

```
ncsim> source /home/install/INCISIVE152/tools/inca/files/ncsimrc
ncsim> run
                   0 | a = 0 | b = 0 | c = 0 | d = 0 | e = 0 | f = 1
                   2 | a = 0 | b = 0 | c = 0 | d = 0 | e = 1 | f = 1
                   4 | a = 0 | b = 0 | c = 0 | d = 1 | e = 0 | f = 1
                   6 | a = 0 | b = 0 | c = 0 | d = 1 | e = 1 | f = 0
                   8 | a = 0 | b = 0 | c = 1 | d = 0 | e = 0 | f = 1
                  10 | a = 0 | b = 0 | c = 1 | d = 0 | e = 1 | f = 1
                  12 | a = 0 | b = 0 | c = 1 | d = 1 | e = 0 | f = 1
                  14 | a = 0 | b = 0 | c = 1 | d = 1 | e = 1 | f = 0
                  16 | a = 0 | b = 1 | c = 0 | d = 0 | e = 0 | f = 1
                  18 | a = 0 | b = 1 | c = 0 | d = 0 | e = 1 | f = 1
                  20 | a = 0 | b = 1 | c = 0 | d = 1 | e = 0 | f = 1
                  22 | a = 0 | b = 1 | c = 0 | d = 1 | e = 1 | f = 0
                  24 | a = 0 | b = 1 | c = 1 | d = 0 | e = 0 | f = 1
                  26 | a = 0 | b = 1 | c = 1 | d = 0 | e = 1 | f = 1
                  28 | a = 0 | b = 1 | c = 1 | d = 1 | e = 0 | f = 1
                  30 | a = 0 | b = 1 | c = 1 | d = 1 | e = 1 | f = 0
                  32 | a = 1 | b = 0 | c = 0 | d = 0 | e = 0 | f = 1
                  34 | a = 1 | b = 0 | c = 0 | d = 0 | e = 1 | f = 1
                  36 | a = 1 | b = 0 | c = 0 | d = 1 | e = 0 | f = 1
                  38 | a = 1 | b = 0 | c = 0 | d = 1 | e = 1 | f = 0
                  40 | a = 1 | b = 0 | c = 1 | d = 0 | e = 0 | f = 1
                  42 | a = 1 | b = 0 | c = 1 | d = 0 | e = 1 | f = 1
                  44 | a = 1 | b = 0 | c = 1 | d = 1 | e = 0 | f = 1
                  46 | a = 1 | b = 0 | c = 1 | d = 1 | e = 1 | f = 0
                  48 | a = 1 | b = 1 | c = 0 | d = 0 | e = 0 | f = 1
                  50 | a = 1 | b = 1 | c = 0 | d = 0 | e = 1 | f = 1
                  52 | a = 1 | b = 1 | c = 0 | d = 1 | e = 0 | f = 1
                  54 | a = 1 | b = 1 | c = 0 | d = 1 | e = 1 | f = 0
                  56 | a = 1 | b = 1 | c = 1 | d = 0 | e = 0 | f = 0
                  58 | a = 1 | b = 1 | c = 1 | d = 0 | e = 1 | f = 0
                  60 | a = 1 | b = 1 | c = 1 | d = 1 | e = 0 | f = 0
                  62 | a = 1 | b = 1 | c = 1 | d = 1 | e = 1 | f = 0
Simulation complete via $finish(1) at time 64 NS + 0
./function2_tb.v:14 $finish;
ncsim>
```

Schematic