EE517: ANALOG VLSI LAB
COURSE PROJECT

Design a 2-stage Op-amp in 180 nm technology targeting High Gain

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EEE - VLSI & Nanoelectronics

Contents

1 OBJECTIVE

Design a 2-stage Op-amp in 180 nm technology targeting High Gain

1.1 General Specifications:

- Supply voltage (VDD) = 1.8 V
- Reference current source (Iref) = 20 µA
- Slew rate = 1V/µs
- Phase margin >= 60^{o}
- Load Capacitance (CL) = 10pF
- ICMR = 0.6 - 1.4 V

1.2 Design specifications

- DC gain >= 75dB
- GBW >= 10MHz
- P_{diss} <=1mW
- L_{max} <= 2µm

1.3 ANALYSIS

1.3.1 DC Analysis

- Report the schematic of the diff pair with DC OP point annotated: I_d, V_{gs}, V_{ds}, V_{th}, V_{dsat}, g, g_{ds}, g_{mb}, region.
- Check that all transistors operate in saturation.

1.3.2 AC Analysis

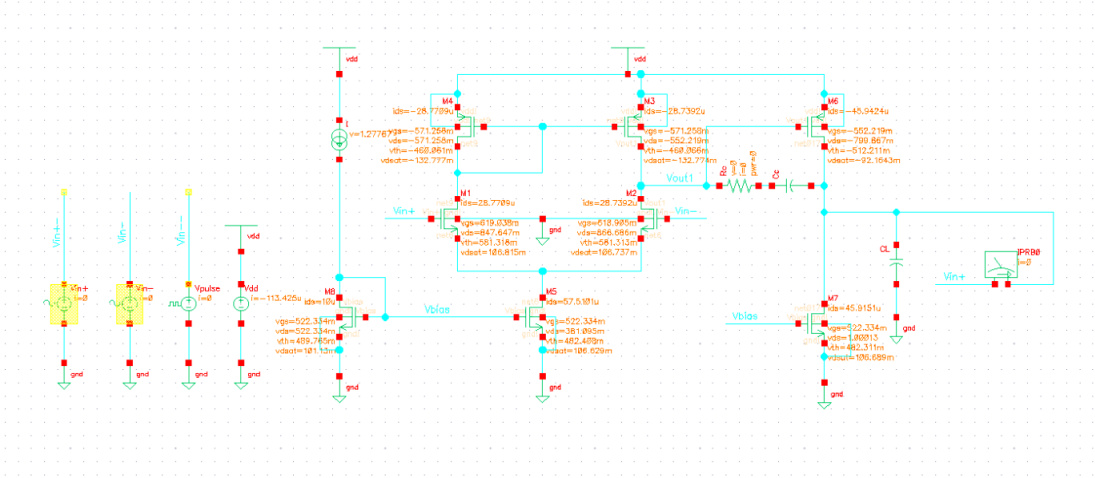
- Observe pole-zero analysis of your circuit.
- Frequency response of your circuit.
- Find Av, PM, Bandwidth, CMRR, PSRR.
- Give a proper reason for selecting any value of any parameter.

1.3.3 Transient Analysis.

- slew rate.
- ICMR, OCMR.

2 THEORY

In analog circuit design, a two-stage operational amplifier, or op-amp, is a popular building component.



generally single stage amplifiers provide less gain compares to practical applications, to overcome this less gain we moved to the use of two-stage op-amps.

In this first stage of amplifier provides the necessary gain and the second stage provides the large voltage swings. that is the reason we have selected second stage as CS amplifier with PMOS transistor as input transistor.

2.1 STRUCTURE

In this two stages are present both of them are cascade connected

First stage is the normal differential amplifier stage with NMOS transistors as input transistors to provide the maximum gain.

second stage is CS amplifier with PMOS transistor as input transistor.

both the stages are biased using current mirror circuits.

2.2 THEORETICAL ANALYSIS

2.3 DC GAIN

In low-frequency applications, one of the most important parameters is the gain. Keep in mind that at low frequencies, compensating capacitor Cc may be viewed as open. first stage gain

$$A_{V1} = -g_{m1}(r_{02}||r_{04}) \tag{1}$$

With a channel active load of Q6s, the second gain stage is essentially a common stage gain stage.It receives its gain from

$$A_{V2} = -g_{m7}(r_{06}||r_{07}) \tag{2}$$

$$Overall - gain(AV) = A_{V1}A_{V2} \tag{3}$$

basic equations of mosfet

$$I_D = \frac{1}{2}K'_n\frac{W}{L}(V_GS - V_t)^2 \tag{4}$$

$$g_m = \sqrt{2K'_n\frac{W}{L}I_D} \tag{5}$$

In order to obtain gain for a two-stage operational amplifier, we have only input voltage Vin, the output voltage of the first stage, which is the input voltage of the second stage V1, and the output voltage of the entire circuit Vo.
then the voltage gain of the amplifier is given as follows:

$$\frac{V_o}{V_{in}} = \frac{V_o}{V_1}X\frac{V_1}{V_{in}} \tag{6}$$

First stage Ro2 || Ro4 output resistance is set to R1, and second stage Ro6 || Ro7 output resistance is set to R2. Additionally, we observe that C1 and C2 CL represent the first and second stage's respective output capacitances. So at last,

$$\frac{V_o}{V_{in}} = \frac{g_{m1}R1 * g_{m2}R2 * (1 - \frac{sC_c}{g_{m2}})}{as^2 + bs + 1} \tag{7}$$

- a = R1R2(C1C2 + C1CL + C2CL)

- b = R2(Cc + C2) + R1(Cc + C1) + Ccgm2R1R2

$$g_{m1} = \sqrt{2K'_p \frac{W_1}{L_1} I_{D1}} \tag{8}$$

$$g_{m2} = \sqrt{2K'_n \frac{W_6}{L_6} I_{D6}} \tag{9}$$

for finding the zeros and poles of the circuit we need to conver the equation in the form as follows

$$\frac{V_o}{V_i} = \frac{A_{dc}(1 - \frac{s}{z1})}{(1 + \frac{s}{p1})(1 + \frac{s}{p2})} \tag{10}$$

then the zero can be written with external zero resistance as follows:

$$z_1 = \frac{1}{C_c(\frac{1}{g_{m2}} - 1)} \tag{11}$$

poles p1 and p2 can approximately written as:

$$p_1 = \frac{1}{C_c g_{m2} R_1 R_2} \tag{12}$$

$$p_2 = \frac{g_{m2} C_c}{C_1 C_2 + C_1 C_L + C_2 C_L} \tag{13}$$

where C1 is very small then p2 can be written as:

$$p_2 = \frac{g_{m2}}{C_1 + C_2} \tag{14}$$

2.4 PHASE MARGIN

The gain bandwidth GBW is given by

$$DCgainp_1 = \frac{g_{m1}}{C_c} \tag{15}$$

phase angle of gain is given by as follows:

$$arctan(\frac{V_o}{V_i n}) = -arctan(\frac{w}{z}) - arctan(\frac{w}{p_1}) - arctan(\frac{w}{p_2})$$

(16)

here we take zero as

$$z = 10 * GBW \tag{17}$$

by substituting in the above equation we get

$$p2 >= 2.2GBW \tag{18}$$

and we get

$$C_c > 0.22C_L \tag{19}$$

in order achieve the phase margin of 60° then we have

$$\frac{g_{m2}}{g_{m1}} <= 10 \tag{20}$$

2.5 SLEW RATE

$$SLEWRATE = \frac{I_5}{C_c} \tag{21}$$

it is generally the rate of change of voltage at the output due to change in the sudden input voltage.

2.6 POWER

$$power = I_{total} * Vdd \tag{22}$$

2.7 Common and differential mode gain:

Once the MOSFETs' parameters have been found, we must examine the output voltage gain. If necessary, we may then need to modify the settings to get the desired common and differential mode voltage gain.

3 CIRCUIT DIAGRAM

3.1 DC ANALYSIS

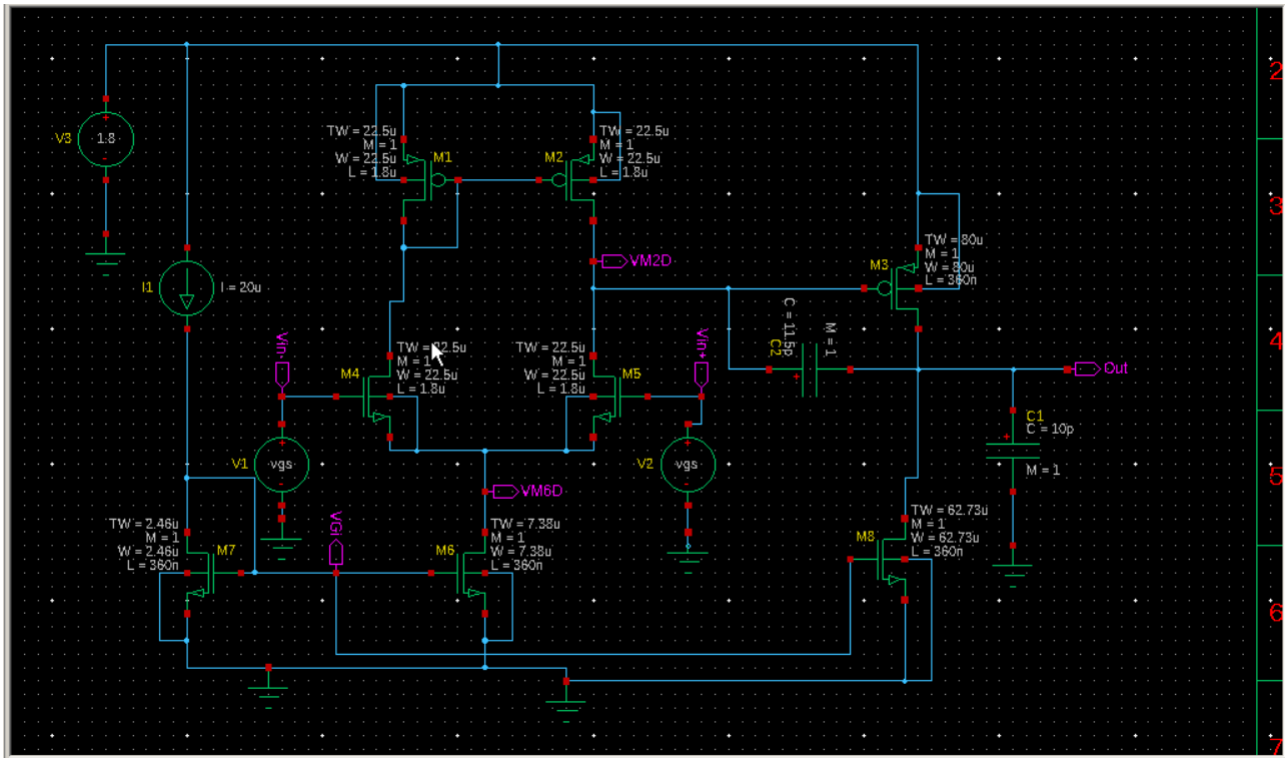


Figure 1: DC analysis schematic of 2-stage op-amp

3.2 AC ANALYSIS

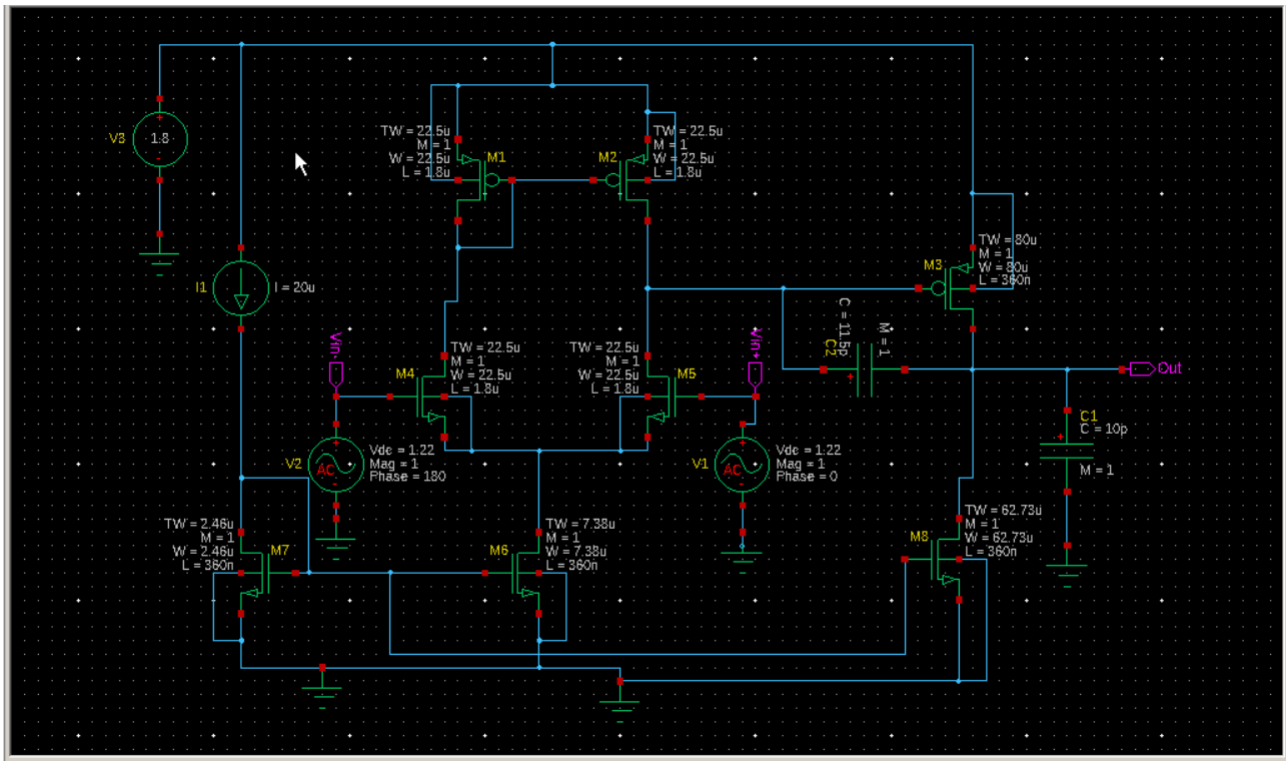


Figure 2: AC analysis schematic of 2-stage op-amp

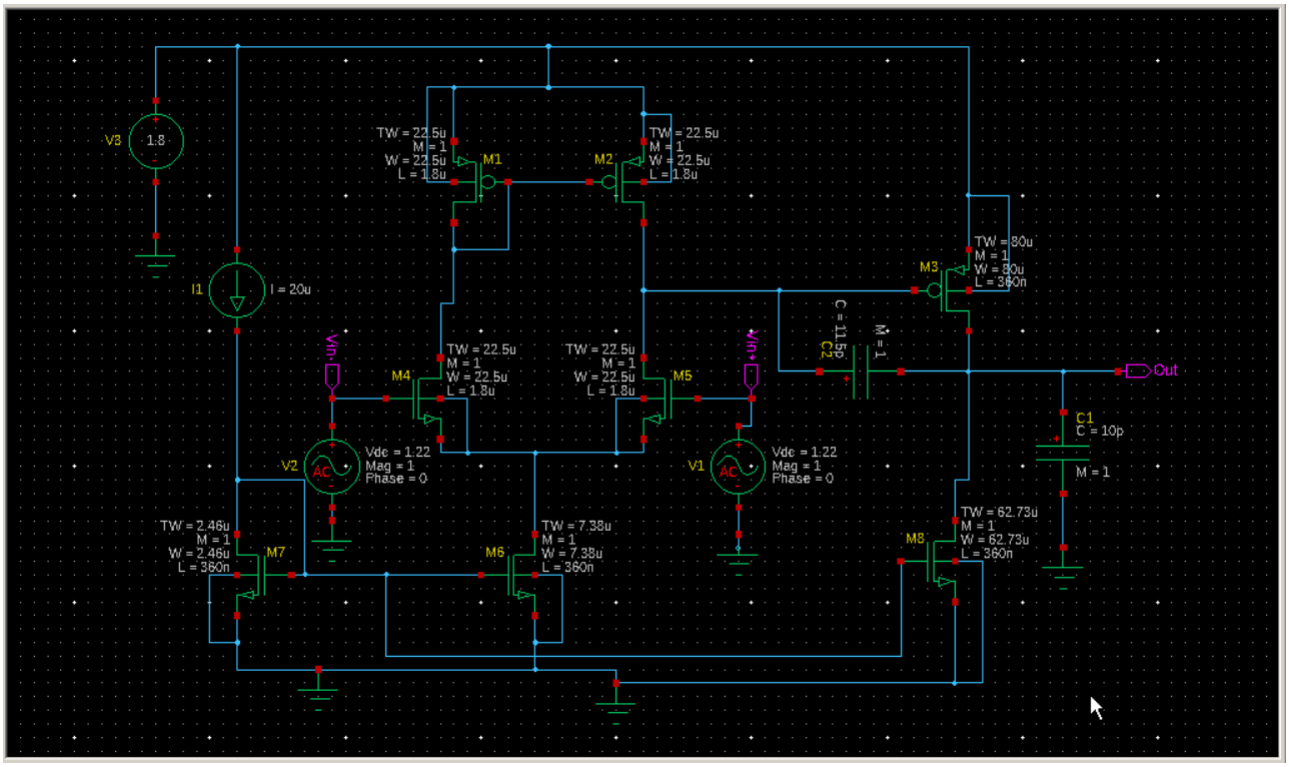


Figure 3: CMRR analysis schematic of 2-stage op-amp

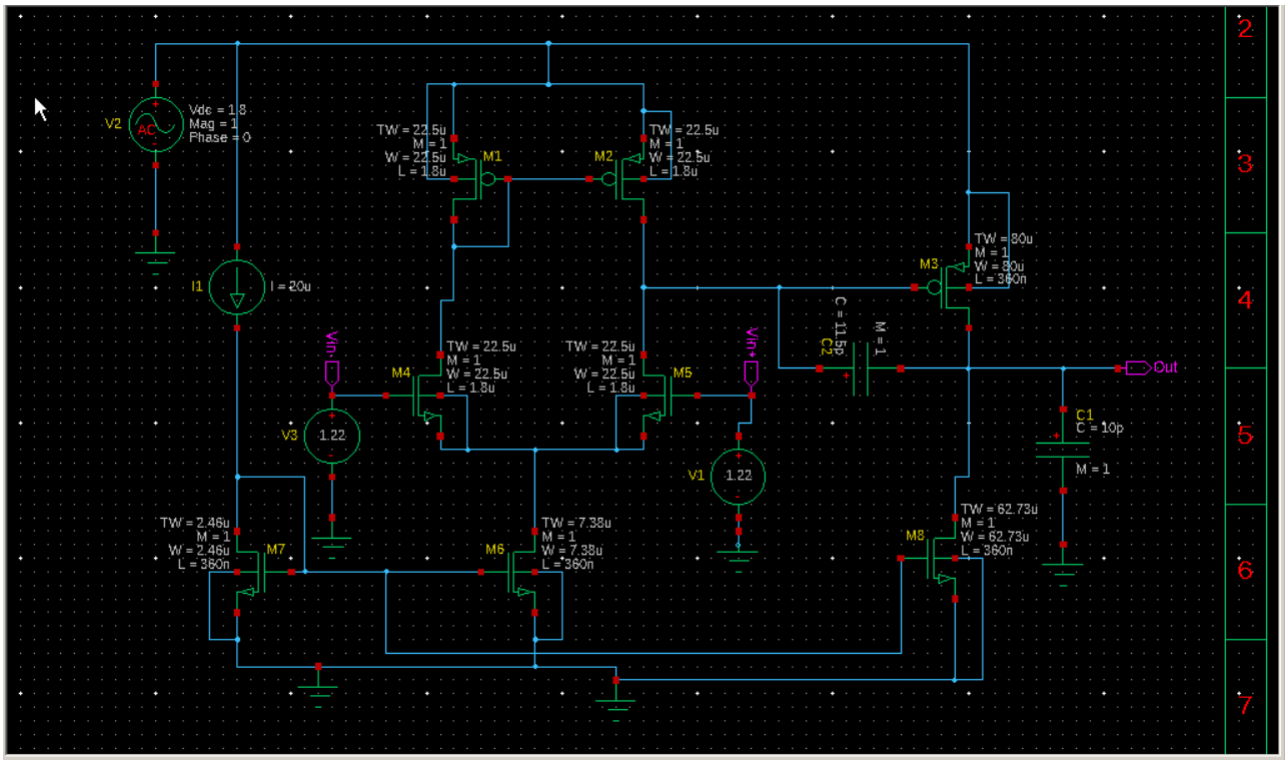


Figure 4: PSRR analysis schematic of 2-stage op-amp

3.3 TRANSIANT analysis

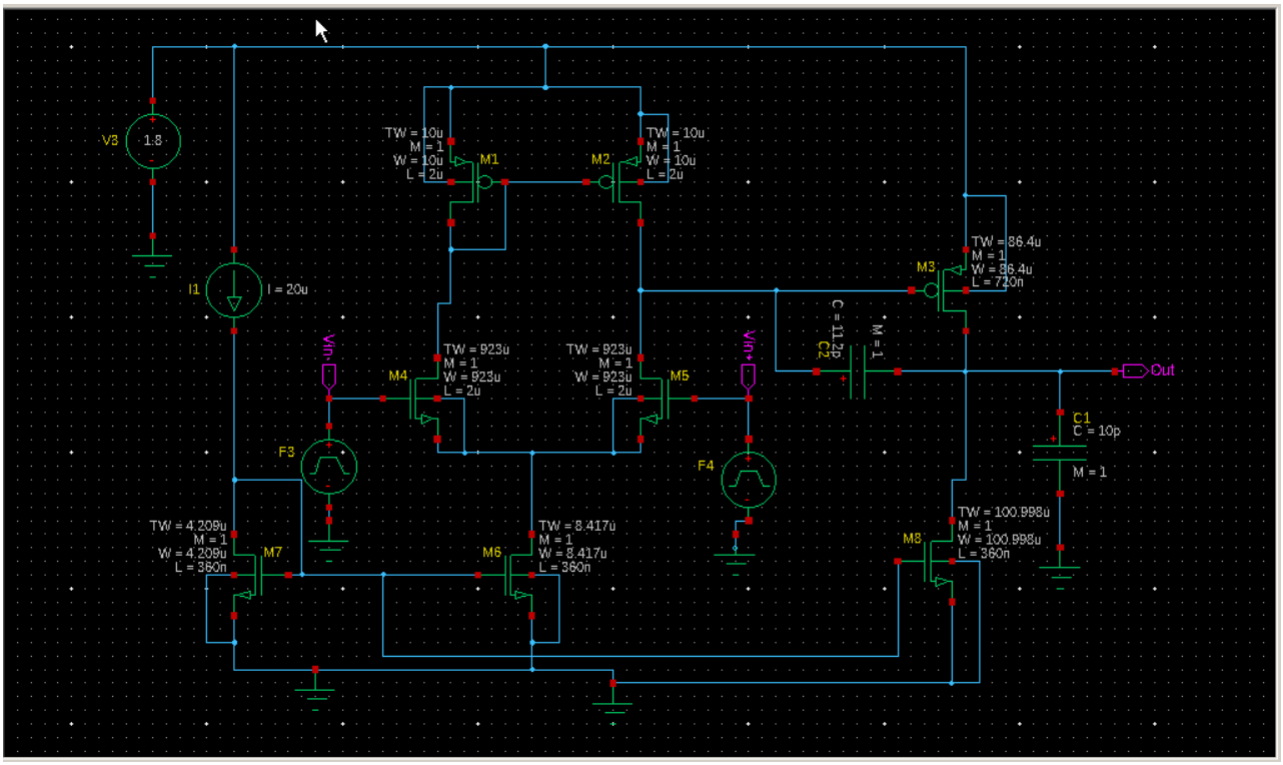


Figure 5: Transient analysis schematic of 2-stage op-amp

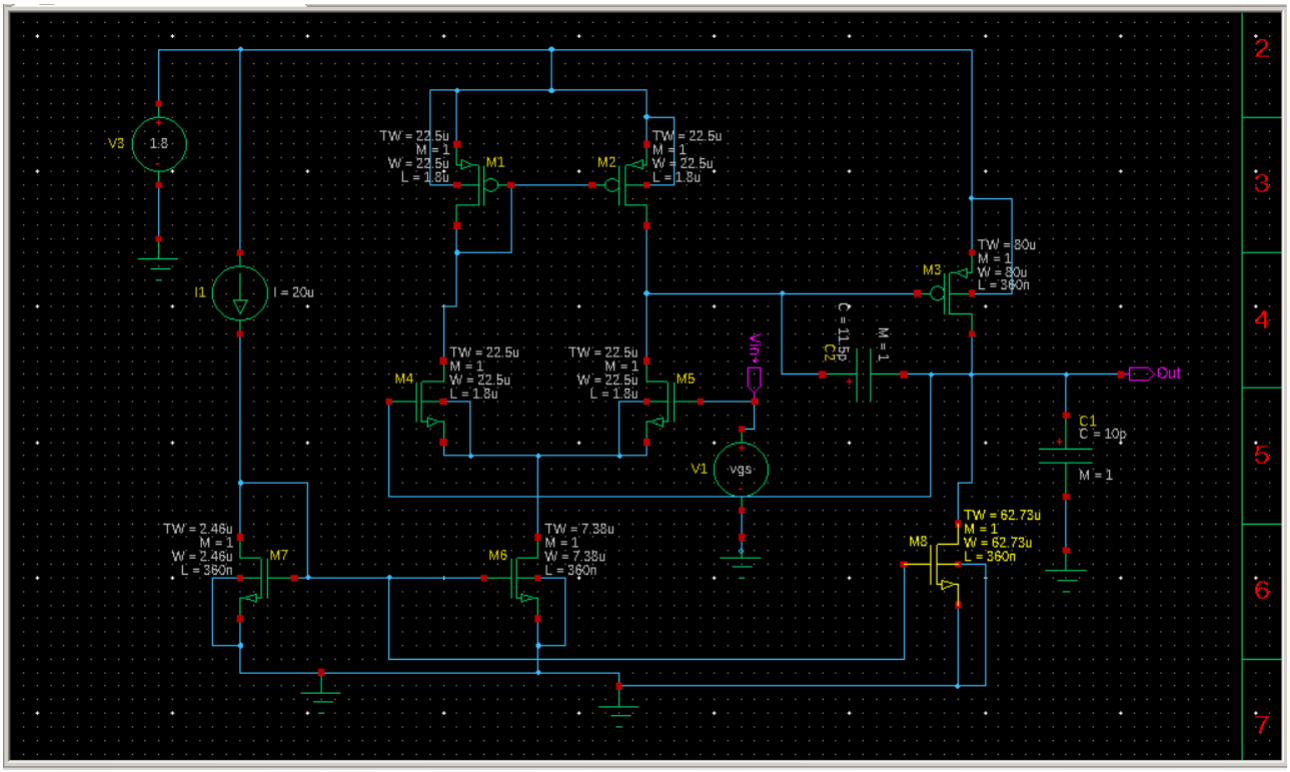


Figure 6: ICMR, OCMR analysis schematic of 2-stage op-amp

4 SIMULATION RESULTS

4.1 DC ANALYSIS

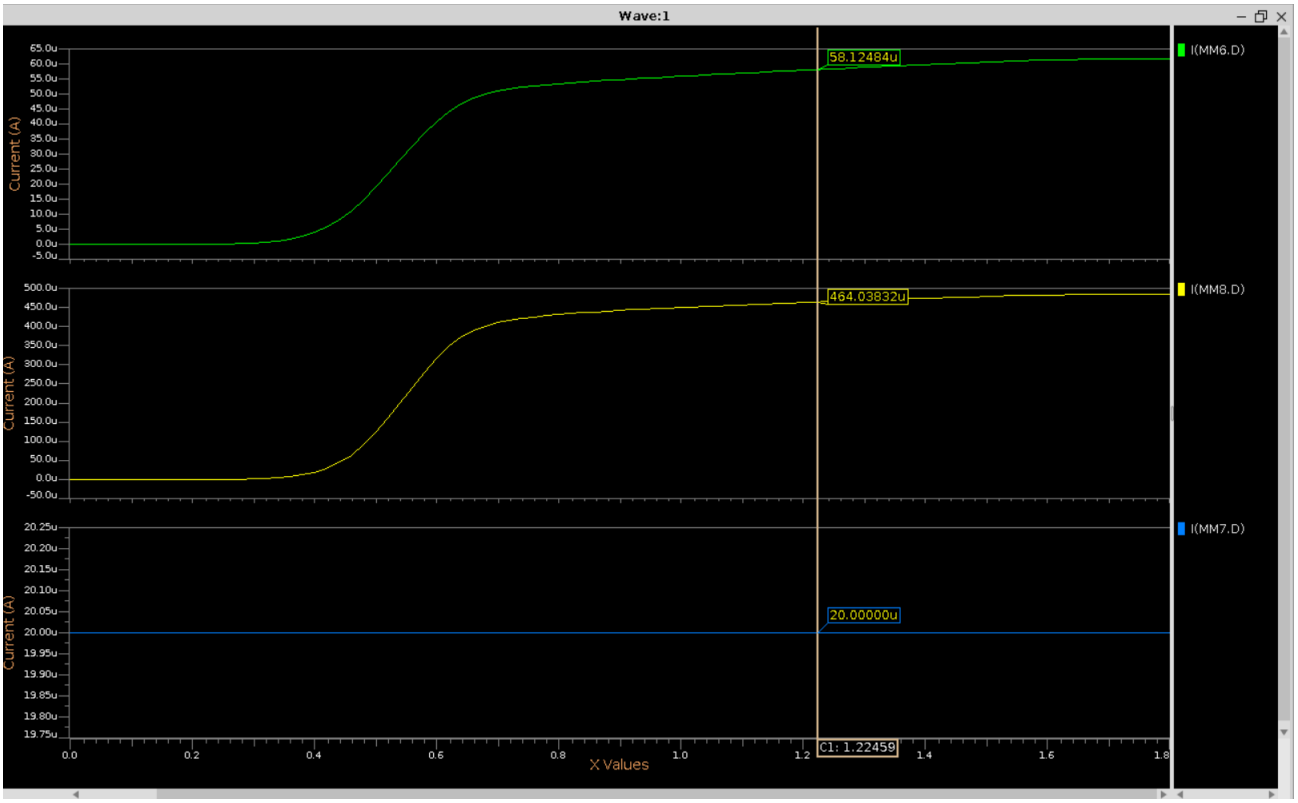


Figure 7: current graph of dc analysis of 2-stage op-amp

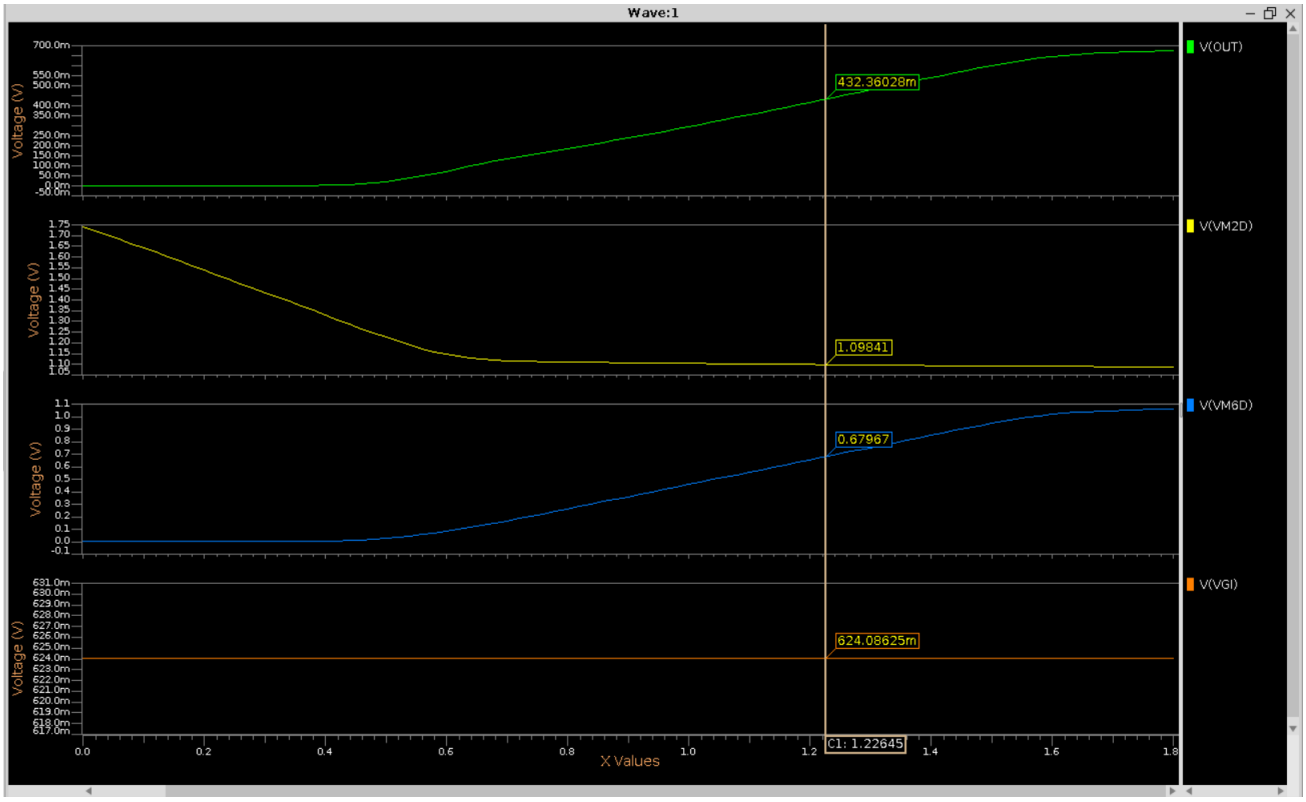


Figure 8: voltage graph of dc analysis of 2-stage op-amp

4.1.1 AC analysis

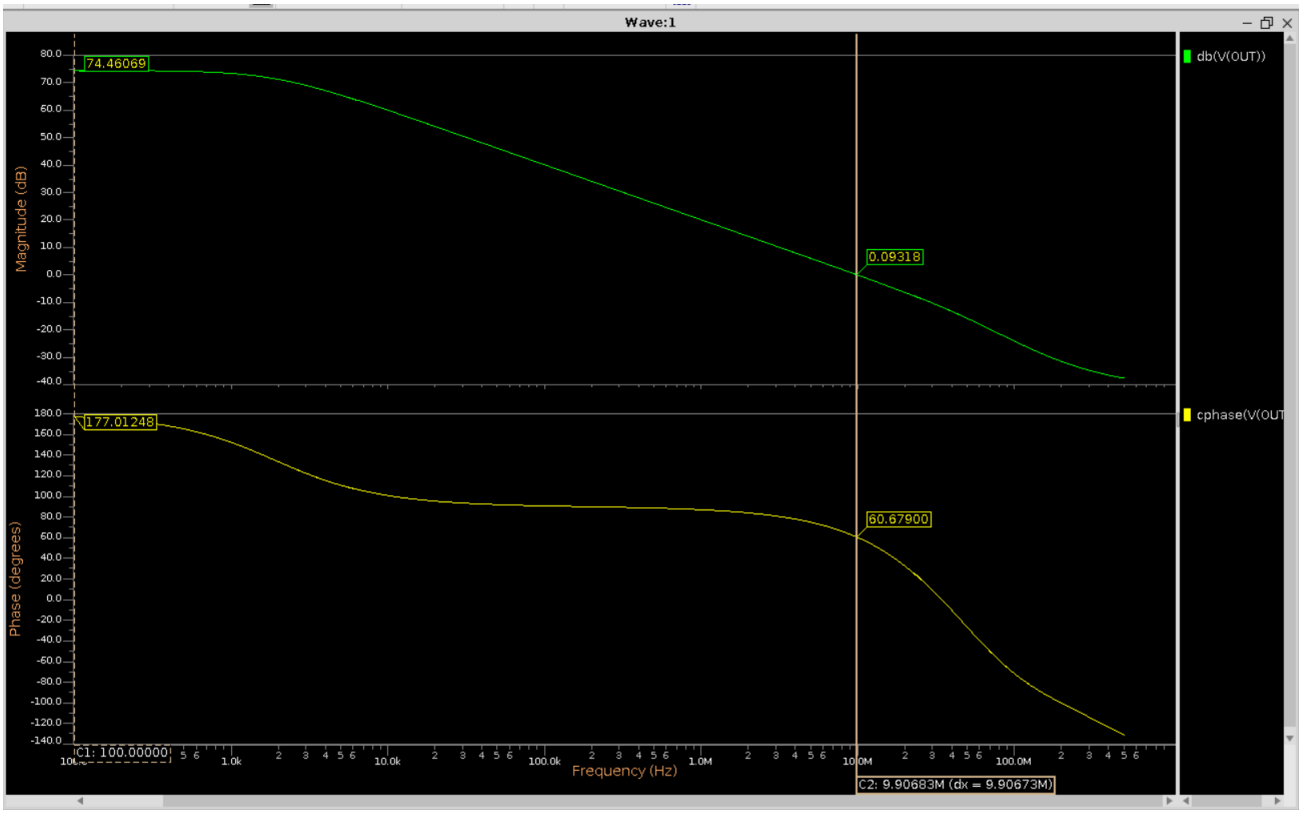


Figure 9: gain bandwidth graph of ac analysis of 2-stage op-amp

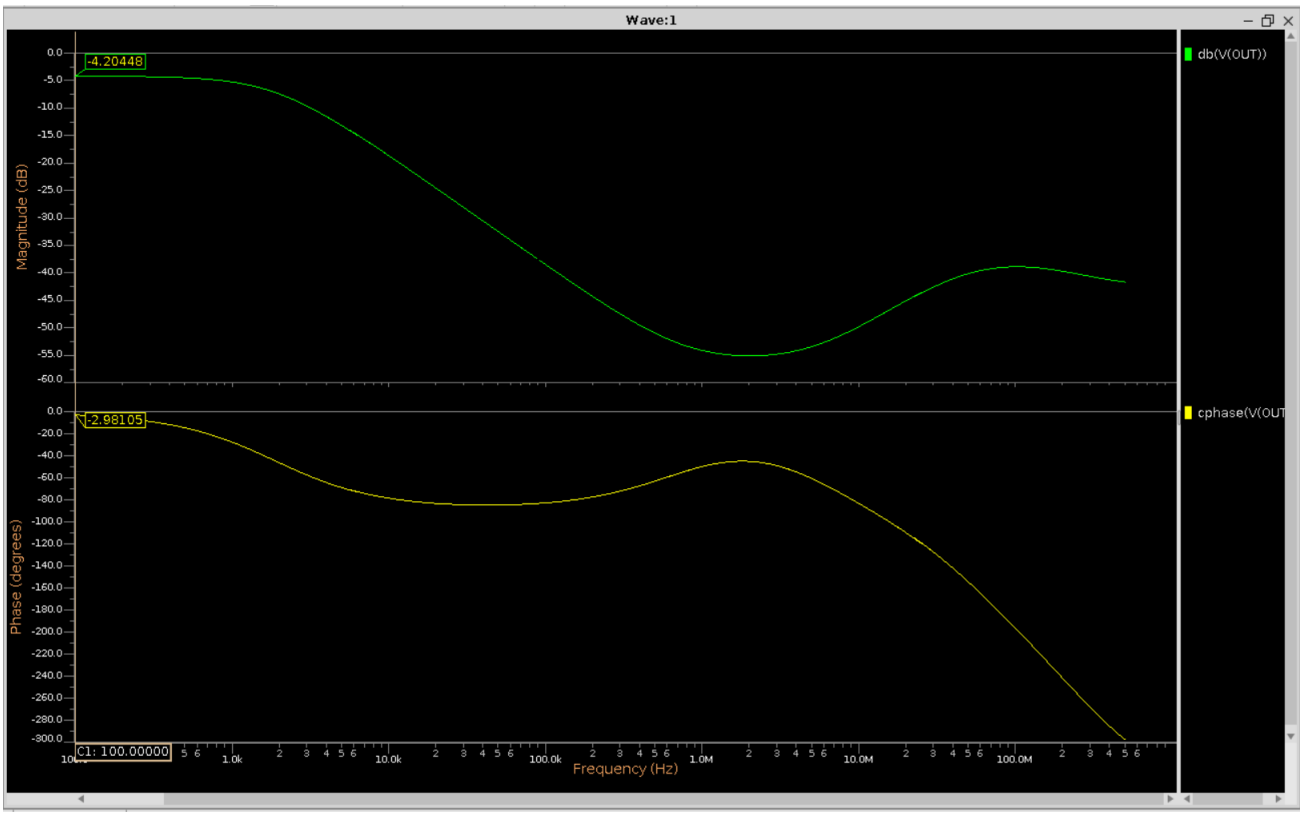


Figure 10: CMRR analysis graph of 2-stage op-amp

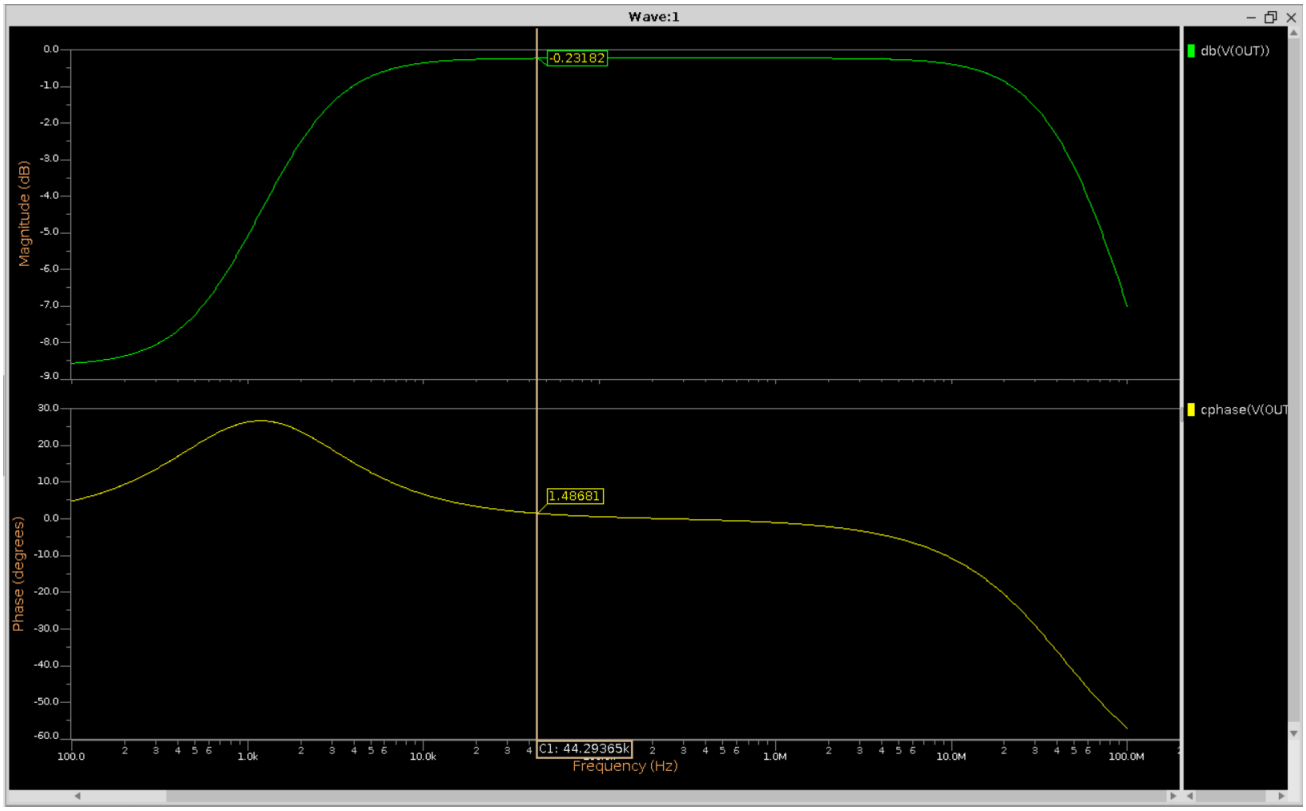


Figure 11: PSRR analysis graph of 2-stage op-amp

4.2 TRANSIENT analysis

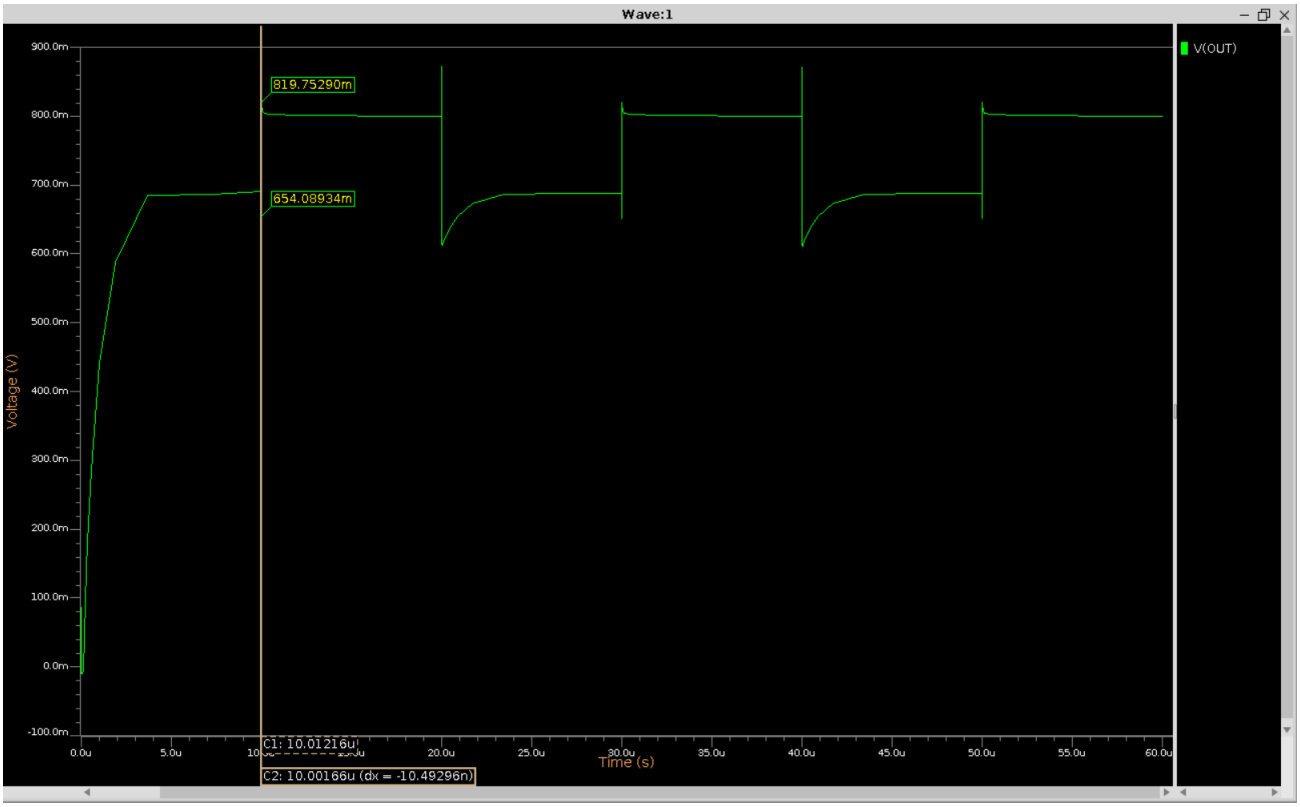


Figure 12: SLEW RATE graph of 2-stage op-amp

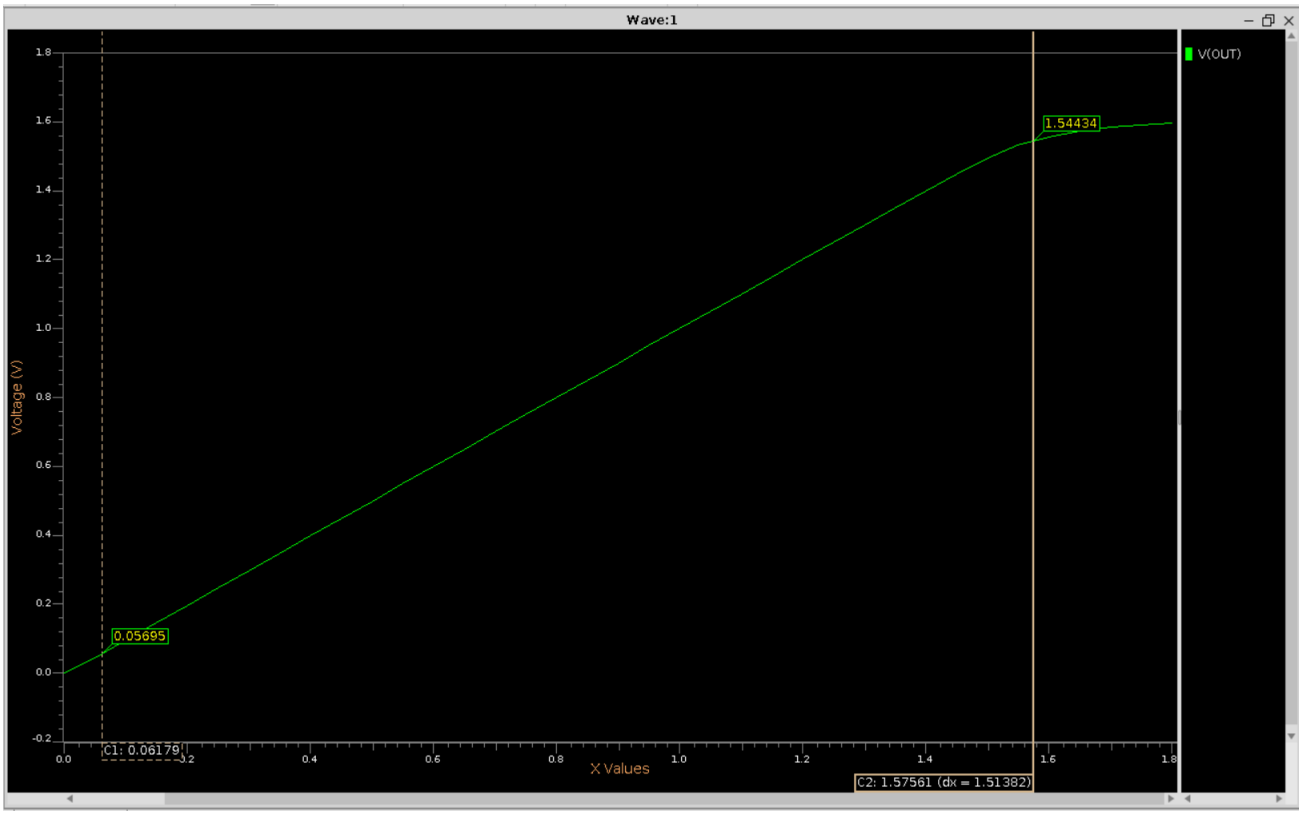


Figure 13: ICMR OCMR graph of 2-stage op-amp

5 CALCULATIONS

here we are considering $\mu_n C_{ox} = 342.18\mu(A/v^2)$, $\mu_p C_{ox} = 120\mu(A/v^2)$
V_{tp} = -0.5v, V_{tn} = 0.5v
Step by step calculations are as follows:

1. consider the minimum length as 180nm.
2. consider the following equation

$$C_c >= 0.22C_L \tag{23}$$

   here we are given with C_L as 10pf, hence C_c must be greater than 2.2pf, here we are considering current it to be 60uA.

3. we know that SLEW RATE is given by

$$SLEWRATE = \frac{I_5}{C_c} \tag{24}$$

   hence we get C_c as greater than 6pF, so we take C_c as 11.5pF.

4. from the equation of gainbandwidth multiplication we get

$$g_{m4} = GBW * C_c * 2\pi \tag{25}$$

   in such a way get g_{m1} approximately as $510\mu(A/V)$

5. by using below equation we can find $(W/l)_{4,5}$:

$$g_{m4} = \sqrt{2K'_p \frac{W_1}{L_1} I_{D1}} \tag{26}$$

   in such a way we get $(W/l)_{4,5}$ as 12.675 and we equate it to 12.5 then for L of 1800nm we get W as 22.5um.

6. from the below equation we can find $(W/l)_{1,2}$:

$$ICMR_{\max} = V_D D - \sqrt{\frac{2I_{D1}}{\mu_p \frac{W}{L}}} - |V_{tp}|_{max} + V_{tnmin} \tag{27}$$

   in such a way $(W/l)_{1,2}$ we get as 12.5 and then for L of 1800nm we get W as 22.5um.

7. from the below equation we can find V_{DS5} saturation value :

$$V_{DS6} = ICMR_{min} - \sqrt{\frac{2I_{D4}}{\mu_n \frac{W_4}{L_4}}} - V_{tn} \tag{28}$$

in such a way we get V_{DS5} as 0.131v by using below equation we can find $(W/L)_6$

$$I_D = \frac{1}{2} K'_n \frac{W}{L} (V_G S - V_t)^2 \tag{29}$$

in such a way $(W/l)_6$ as 20.29 we equate it to 20.5 and then for L of 360nm we get W as 7.38um.

8. we are doing for 60^o phase margin then by using below equation we get g_{m3}

$$\frac{g_{m3}}{g_{m4}} >= 10 \tag{30}$$

we know g_{m4} we get g_{m3} as $5100\mu(A/V)$

9. To get (W/L)3 we need to get g_{m2}
by using g_m equation we can calculate g_{m2} , we can get it as $300\mu(A/V)$

$$\frac{W_3}{L_3} = \frac{g_{m3}}{g_{m2}} \frac{W_2}{L_2} \tag{31}$$

we can get then by using g_m we can find $(W/l)_3$ as 212.5. for length of 360nm we get width as 76.5um.

10. by using below eqution we can find IDS3

$$I_{DS3} = \frac{\frac{W_3}{L_3}}{\frac{W_2}{L_2}} I_{DS2} \tag{32}$$

we get IDS3 as 480uA

11. then by using the current mirrror equations we can find the $(W/L)_8$ as

$$\frac{W_8}{L_8} = \frac{I_{DS8}}{I_{DS4}} \frac{W_6}{L_6} \tag{33}$$

in such a way $(W/l)_8$ as 174.25 we equate it to 175 and then for L of 360nm we get W as 62.73um.

12. then by using the below formule we get $(W/l)_7$:

$$\frac{W_7}{L_7} = \frac{I_{DS7}}{I_{DS6}} \frac{W_6}{L_6} \tag{34}$$

in such a way $(W/l)_7$ as 109.87 we equate it to 110.00 and then for L of 360nm we get W as 19800nm.

6 RESULTS

6.1 DC analysis - BIAS VOLTAGES

Transistor	V_G	V_D	V_S	V_{GS}	V_{DS}	V_{OV}
M4	1.22645v	1.09841v	0.67967v	0.54678	0.41874v	0.04678v
M5	1.22645v	1.09841v	0.67967v	0.54678	0.41874v	0.04678v
M1	1.09841v	1.09841v	1.8v	-0.70159v	-0.70159v	-0.20159v
M2	1.09841v	1.09841v	1.8v	-0.70159v	-0.70159v	-0.20159v
M6	0.629v	0.67967v	0v	0.629v	0.67967v	0.129v
M7	0.629v	0.629v	0v	0.629v	0.629v	0.129v
M8	0.629v	0.432v	0v	0.629v	0.432v	0.129v
M3	1.09841v	0.432v	1.8v	-0.70159v	–1.368v	-0.20159v

all the transistors are in the saturation.

6.2 TRANSISTOR SIZES

transistor	width (um)	length (nm)
M4	22.5	180
M5	22.5	180
M1	22.5	180
M2	22.5	180
M6	7.38	360
M7	2.46	360
M8	62.73	360
M3	80	360

6.3 CAPACITOR VALUE

capacitor	value (pf)
C_c	11.5
c_L	10

6.4 AC analysis

parameter	theoretical value	practical value
GAIN	75db	74.49db
GBW	10Mhz	9.906Mhz
PM	>=60	60.679
power	<=1mW	0.94mW
CMRR	–	-4.2084db
PSRR	–	-0.23182db

6.5 Transient analysis

parameter	theoretical value	practical value
SLEW RATE	$\geq 1V/\mu$ s	14.5 V/μ s
ICMR	0.6v - 1.4v	0.06719v - 1.5756v
OCMR	–	0.056v - 1.54v

7 OBSERVATIONS

- in This experiment we have done the analysis of the 2-stage CMOS opamp design parameters, taking into account the results of simulations.
- The results and graphs stated before are also shown above shows the theoretical and practical values.
- with the 2-stage op-amp circuit we have achieved the higher gain value.

8 CONCLUSION

2-STAGE OP-AMP circuit is constructed for higher gain for given specifications and analysis is done using ELDO software.