University of Central Florida

Department of Computer Science

CDA 5106: Fall 2020

Machine Problem 1: Cache Design, Memory Hierarchy Design

by

SAI CHARAN REDDY PANNALA

Honor Pledge: "I have neither given nor received unauthorized aid on this test or assignment."

SAI CHARAN REDDY PANNALA

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Sample cover page for MP1.

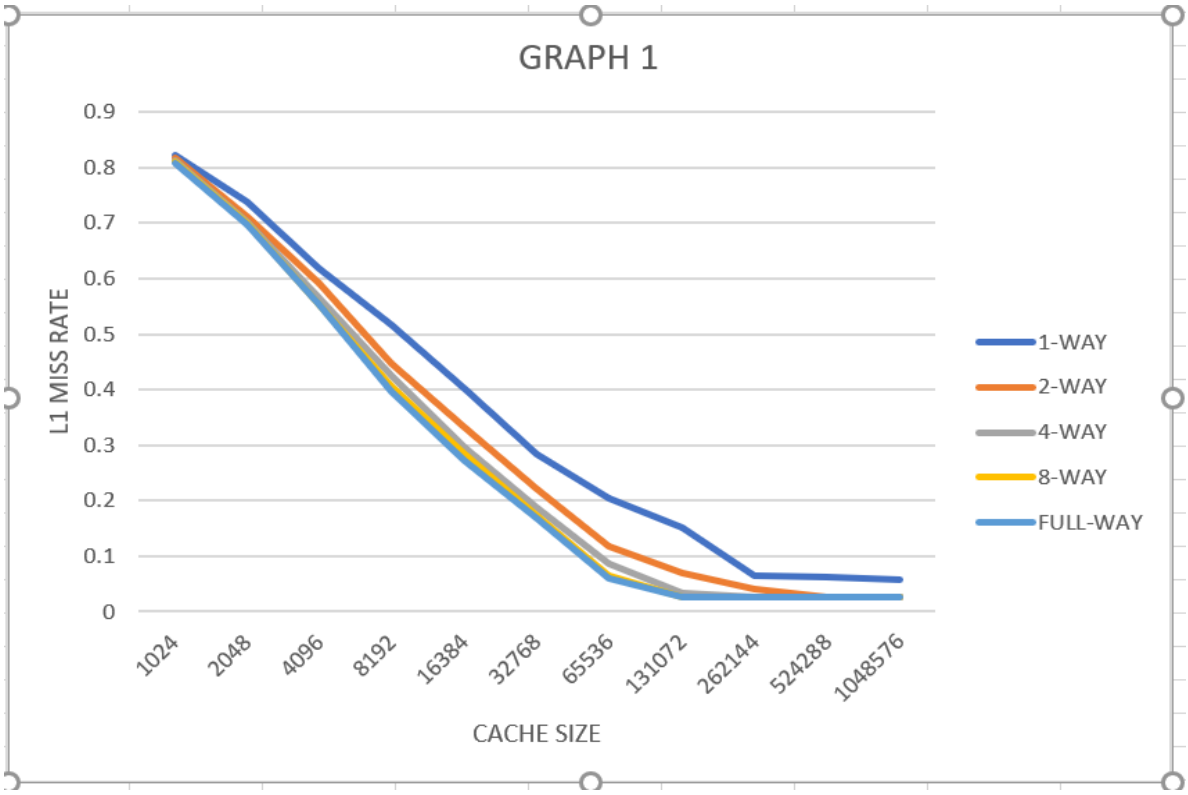
GRAPHS

L1 CACHE EXPLORATION: SIZE AND ASSOC

GRAPH #1

BLOCKSIZE : 32
L1 CACHE SIZE : Varied
L1 ASSOC : Varied
L2 CACHE SIZE : None
L2 ASSOC : None
REPLACEMENT POLICY : LRU
INCLUSION PROPERTY : Non- Inclusive

Plot the between direct-mapped, 2-way set-associative, 4-way associative, 8-way set-associative, and fully associative.graph between L1 Miss rate on Y axis vs L1 CACHE SIZE on the X-axis (10, 11,…20)



LINE GRAPH 1: Plotted between L1 Miss Rate and L1 Cache Size when the cache is direct mapped, 2- way set-associative, 4-way set-associative, 8-way set-associative and fully associative.

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CAHE SIZE	1-way	2-way	4-way	8-way	Full way
1024	0.82278	0.81703	0.8118	0.81007	0.80795
2048	0.73898	0.7116	0.70135	0.7	0.69813
4096	0.61739	0.5905	0.5652	0.55339	0.55198
8192	0.51696	0.44773	0.42561	0.40708	0.39552
16384	0.40052	0.33129	0.29522	0.28328	0.27217
32768	0.28432	0.22179	0.18687	0.17399	0.16708
65536	0.20396	0.11673	0.08588	0.06583	0.05899
131072	0.15164	0.06871	0.03383	0.02726	0.02582
262144	0.06474	0.04193	0.02628	0.02582	0.02582
524288	0.06304	0.02582	0.02582	0.02582	0.02582
1048576	0.05871	0.02582	0.02582	0.02582	0.02582

Figure show the value of the above graph.

1. For a given associativity increasing the cache size there is a decreasing in the Miss Rate in each and every level of associativity. Exclusively for the full way associativity the in better way than the others and it stops at 131072 to 1048576 Bytes be at the same level.
   Effect in Increasing the associativity at each level also decreasing in the Miss Rate. But at certain level like 130172 Bytes there is only slight decrease in the Miss Rate. Increasing the associativity at 1024kb is of not a big change at all.
2. At every level of increasing the cache or increasing in the associativity at certain level all the Miss Rate will be of 0.02582 which is compulsory at some point of Time. So, Here Compulsory miss rate is 2.582%.
3. Conflict miss rate is the difference between the set associative and full way associative of having same cache size. Here the miss rate for 1 way, 2 way, 4 way and 8 way is 0.43397, 0.171925, 0.06429, 0.02163.

GRAPH 2: Average Access Time vs L1 CACHE SIZE

GRAPH #1

BLOCKSIZE : 32
L1 CACHE SIZE : Varied
L1 ASSOC : Varied
L2 CACHE SIZE : None
L2 ASSOC : None
REPLACEMENT POLICY : LRU
INCLUSION PROPERTY : Non- Inclusive

Plot the graph between L1 Average Access Time on Y axis vs L1 CAHE SIZE on the X-axis (10, 11,…20) between direct-mapped, 2-way set-associative, 4-way associative, 8-way set-associative, and fully associative.

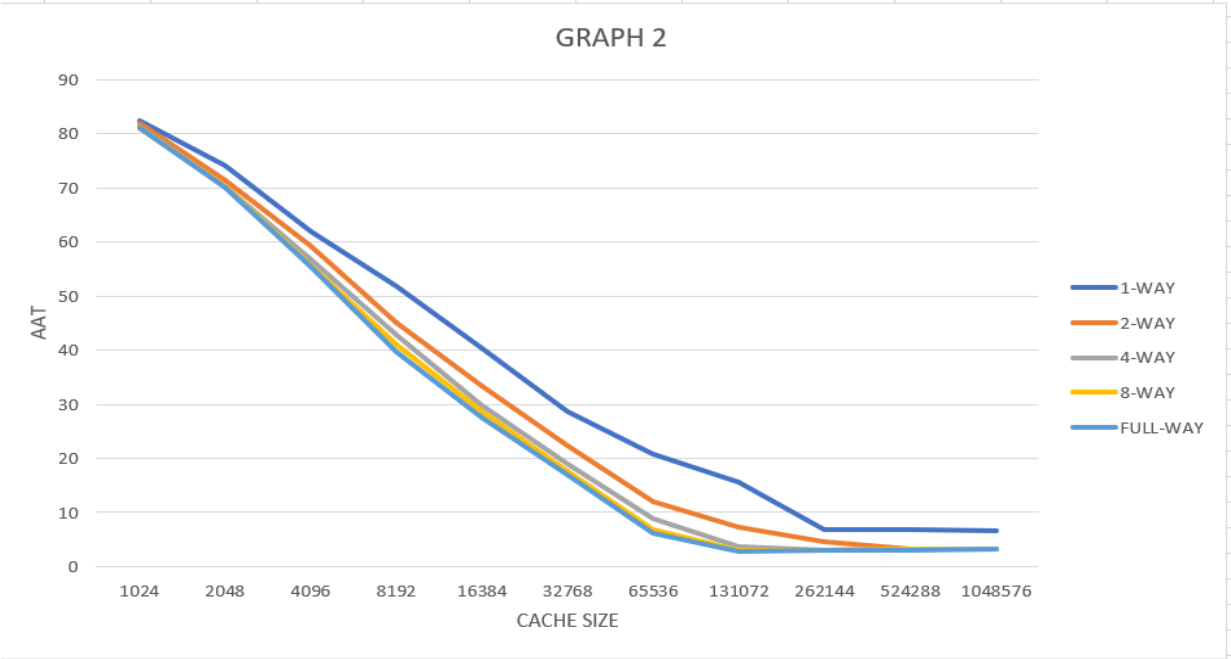

Figure show the line graph between average access time vs l1 cache size for different associativity.

CACHE SIZE	1-WAY	2-WAY	4-WAY	8-WAY	FA=WAY
1024	82.392797	81.843329	81.32682	81.007	80.950484
2048	74.02709	71.321691	70.289496	70.180686	69.989515
4096	61.886005	59.231131	56.705685	55.528065	55.380948
8192	51.85983	44.967195	42.772173	40.918911	39.750581
16384	40.250417	33.352917	29.755936	28.582354	27.422608
32768	28.665353	22.441446	18.95825	17.687511	16.93274
65536	20.690627	11.963727	8.907481	6.924213	6.175281
131072	15.5308	7.245603	3.76328	3.127236	2.904486
262144	6.917812	4.638929	3.085685	3.040925	2.978009
524288	6.847451	3.149744	3.146418	3.160177	3.057728
1048576	6.57038	3.288046	3.281607	3.287819	3.170474

Above figure shows values for the L1 Cache size and AAT for different levels associativity.

1. Lowest AAT occurred for 131072 Bytes (128KB). For all the associativity cache size decreases from low cache size to high form 1KB to 1024KB while in Full way associativity cache size decreased from 1KB to 128KB and then start increasing from 128KB to 1024KB.

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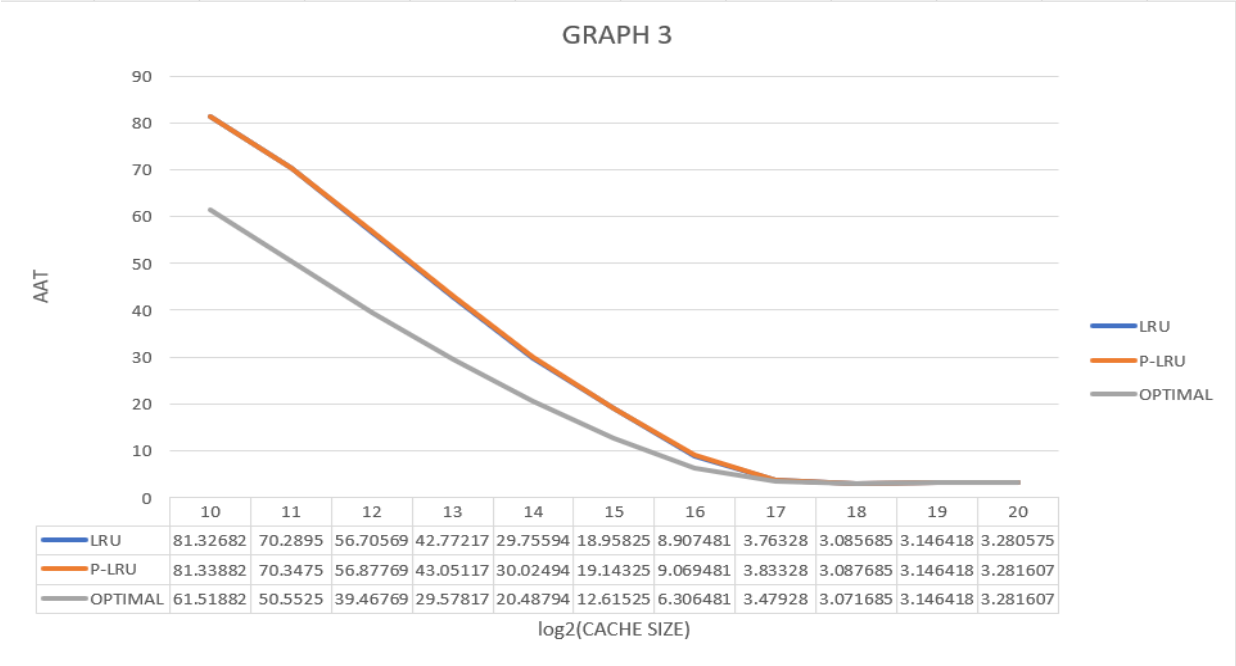
GRAPH 3 : Average Access Time vs Log2(L1 SIZE)

GRAPH #1

BLOCKSIZE : 32
L1 CACHE SIZE : Varied
L1 ASSOC : 4
L2 CACHE SIZE : None
L2 ASSOC : None
REPLACEMENT POLICY : Varied
INCLUSION PROPERTY : Non- Inclusive

Plot the between AAT and log2(l1 cache size) on different Replacement policies.



	10	11	12	13	14	15	16	17	18	19	20
LRU	81.32682	70.2895	56.70569	42.77217	29.75594	18.95825	8.907481	3.76328	3.085685	3.146418	3.280575
P-LRU	81.33882	70.3475	56.87769	43.05117	30.02494	19.14325	9.069481	3.83328	3.087685	3.146418	3.281607
OPTIMAL	61.51882	50.5525	39.46769	29.57817	20.48794	12.61525	6.306481	3.47928	3.071685	3.146418	3.281607

Figure above shows the graph between the different cache sizes of L1 and AAT on different types of policies.

1. Optimal Replacement gives the best (lowest value) AAT for the L1 cache size in between 1KB to 128KB. Whereas after 128KB every replacement policy shows almost equal values.

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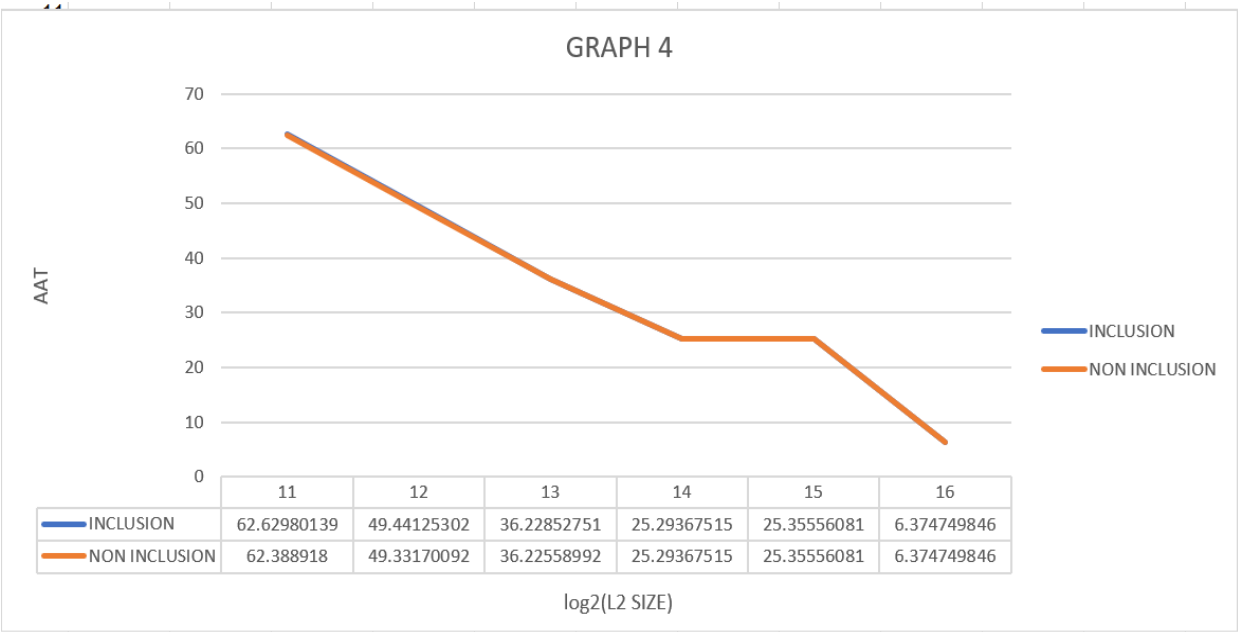
GRAPH 3 : Average Access Time vs Log2(L2 SIZE)

GRAPH #1

BLOCKSIZE : 32
L1 CACHE SIZE : 1024
L1 ASSOC : 4
L2 CACHE SIZE : Varied(1KB to 128KB)
L2 ASSOC : 8
REPLACEMENT POLICY : Varied
INCLUSION PROPERTY : Non- Inclusive

Plot the between AAT and log2(L2 cache size) on Different Inclusion property of LRU.



	11	12	13	14	15	16
INCLUSION	62.62980139	49.44125302	36.22852751	25.29367515	25.35556081	6.374749846
NON INCLUSION	62.388918	49.33170092	36.22558992	25.29367515	25.35556081	6.374749846

1. Graph almost shows the same vales. There is a minute change in the values whereas here Non Inclusive shows the lowest Average Access Time.

   We can see both the properties gives the same value after 8KB. Whereas its different in between 1KB to 8KB.

Sample cover page for MP1.