SAI KIRAN CHERUPALLY

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EDUCATION

- **Ph.D.** **Computer Engineering (Electrical Engineering)** **GPA: 3.81**
  - Arizona State University – Ph.D. advisor: Prof. Jae-sun Seo – Expected Fall 2021/Spring 2022
  - Research focus: In-memory computing, DNN accelerator, biometric/PUF hybrid security engine
- **M.S. (Thesis)** **Electrical and Computer Engineering** **GPA: 3.81**
  - Portland State University – Thesis advisor: Prof. Christof Teuscher – Graduated Fall 2017
  - Research focus: Large-scale reservoir computing with hierarchical random Boolean networks

WORK EXPERIENCE

- **Graduate Technical Intern** **Texas Instruments, Kilby Labs** **Summer '19**
  - **Manager:** Hetul Sanghvi
  - Joined team working on visual cognition in edge devices for autonomous driving applications.
  - Designed and verified energy-efficient digital hardware in SystemVerilog for emulating ternary SRAM IMC array.
  - RTL design of MAC array, pipelined datapath, hazard-free controller.
  - Optimized binary and ternary MobileNets using depth-wise separable computations for edge-computing devices.
- **Graduate Research Associate** **Arizona State University** **Jan. '18 onwards**
  - ECG and SRAM physical unclonable function-based authentication systems for edge deployment
    - Our work published at ISCAS 2019, TBioCAS SI 2020, ASSCC 2019 and JSCC 2020.
  - Leveraging IMC noise for performance improvements in DNNs using PyTorch - Python
    - IMC technologies: XNOR-SRAM, C3-SRAM, XNOR-RRAM
    - Designed and implemented novel IMC hardware noise-aware DNN training methods.
    - Recovered accuracy loss observed in DNNs deployed on IMC hardware.
    - Designed and implemented novel adversarial defense methods using IMC noise.
    - Improved DNN robustness against adversarial input and weight attacks.
- **Graduate Research Assistant** **Portland State University** **May '16 – Dec. '17**
  - Built and evaluated large-scale hierarchical random Boolean network reservoirs using Python

DIGITAL PROJECTS

- **Smart Hardware Security Engine** **Full chip tape-out** **Verilog – EDA Tools**
  - TSMC 65nm low-power full chip tape-out containing on-chip ECG preprocessing, a neural network and an SRAM PUF digital hardware in November 2018.
  - Combined ECG with Heart Rate Variability and SRAM PUF for multi-source authentication.
  - Optimized for low-power consumption via coarse grain sparsity and compression of neural nets.
  - 3-stage pipeline and custom fan-in-fan-out datapath to optimize throughput and latency of fully-connected layers.
  - Achieved 7x reduction in equal error rate of multi-source authentication which consumes 4.04 µW at 0.6V supply.
- **Low-power Binary DNN** **Neuromorphic Hardware Design** **Verilog – EDA Tools**
  - Verilog RTL and APR of digital accelerator for implementing binary feed-forward neural network.
  - Designed Load-Store SIMD architecture and tunable neuron biases to maximize throughput of MNIST inference.
  - Performed Synthesis, APR, and PrimeTime analysis to evaluate accelerator performance.
  - Verified pre-synthesis, post-synthesis, and post-layout RTL for functional correctness using SystemVerilog.
  - Achieved a 3.75nJ, 1.5 µS per image efficiency (second best in the class).
- **2-bit DNN Accelerator** **Neuromorphic Digital Accelerator** **SystemVerilog**
  - Neuromorphic accelerator design and verification in SystemVerilog, optimized for high throughput.
  - Synthesized and verified 3-stage ternary neural network hardware using Mentor Veloce Solo emulator.
  - Designed using 5-stage MIPS-like pipeline with SIMD architecture, data forwarding, and clock gating.
  - Designed a constrained randomizer to generate efficient test vectors to comprehensively cover the test space.
  - Embedded assertions to catch design errors during the accelerator run-time.
  - Verification model based on end-to-end comparison of register states with golden vectors.
- **Cryptographic Processor** **Computer Architecture** **Python**
  - High level implementation of IDEA cipher using multicore, pipelined and custom SIMD architecture.
  - Achieved a throughput of 27.55 Mbps, and a latency of 2.4 µS at 100 MHz clock speed (best in the class).

References available on request

MIXED-SIGNAL PROJECTS

- **Noise-aware Deep Neural Networks In-memory computing (IMC) PyTorch – Python**
  - Studied the effect of IMC noise on inference performance of DNNs deployed on IMC hardware using PyTorch.
    - Recovered up to 17% CIFAR-10 accuracy of low-precision DNNs deployed on XNOR-SRAM (JSSC'20), XNOR-RRAM (DATE '18) and C3SRAM (JSSC'20) IMC prototype chips.
    - PyTorch implementation of IMC partial-sum quantization for accelerated DNN training using of IMC noise.
    - PyTorch implementation of 1-bit and 2-bit input-splitting, and windowed straight-through estimator.
    - Papers under review with IEEE Design and Test and Journal of Semiconductor Science and Technology.
  - Improved the adversarial robustness of DNNs by up to 10.5% and 33.6% against adversarial input and bit-flip weight attacks respectively by using XNOR-SRAM and C3SRAM IMC noise.
    - PyTorch implementation of black-box adversarial input attacks for attacking DNNs with gradient obfuscation.
    - PyTorch implementation of targeted bit-flip adversarial weight attacks for low-precision DNNs.
    - Paper is accepted for publication and presentation at DAC 2021.
- **IMC Peripheral Circuit Design Board-level peripheral circuit design for new RRAMs**
  - Proposed and designed initial prototypes of peripheral circuitry for 4x4 and 16x16 epitaxial RRAM arrays developed by Prof. Jeehwan Kim's group at MIT.

PUBLICATIONS

- **Sai Kiran Cherupally**, Jian Meng, Adnan Siraj Rakin, Shihui Yin, Mingoo Seok, Deliang Fan, and Jae-sun Seo. "Improving DNN Hardware Accuracy by In-Memory Computing Noise Injection," accepted to *IEEE Design and Test*.
- **Sai Kiran Cherupally**, Jian Meng, Adnan Siraj Rakin, Shihui Yin, Injune Yeo, Shimeng Yu, and Jae-sun Seo. "Improving the Accuracy and Robustness of RRAM-based In-Memory Computing Against RRAM Hardware Noise and Adversarial Attacks," *Semiconductor Science and Technology, Special Issue on Neuromorphic Devices and Applications*, under review.
- **Sai Kiran Cherupally**, Adnan Siraj Rakin, Shihui Yin, Mingoo Seok, Deliang Fan, and Jae-sun Seo, "Leveraging Noise and Aggressive Quantization of In-Memory Computing for Robust DNN Hardware Against Adversarial Input and Weight Attacks," *ACM/IEEE Design Automation Conference (DAC)*, 2021, accepted for publication.
- Jyotishman Saikia, Shihui Yin, **Sai Kiran Cherupally**, Bo Zhang, Jian Meng, Mingoo Seok, and Jae-sun Seo, "Modeling and Optimization of SRAM-based In-Memory Computing Hardware Design," *IEEE Design, Automation and Test in Europe (DATE)*, 2021.
- **Sai Kiran Cherupally**, Shihui Yin, Deepak Kadetotad, Chisung Bae, Sang Joon Kim, and Jae-sun Seo. "A Smart Hardware Security Engine Combining Entropy Sources of ECG, HRV, and SRAM PUF for Authentication and Secret Key Generation," *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 55, no. 10, pp. 2680-2690, 2020.
- **Sai Kiran Cherupally**, Gaurav Srivastava, Shihui Yin, Deepak Kadetotad, Chisung Bae, Sang Joon Kim, and Jae-sun Seo. "ECG Authentication Hardware Design with Low-Power Signal Processing and Neural Network Optimization with Low Precision and Structured Compression." *IEEE Transactions on Biomedical Circuits and Systems (TBioCAS)*, vol. 14, no. 2, pp. 198-208, 2020.
- **Sai Kiran Cherupally**, Shihui Yin, Deepak Kadetotad, Chisung Bae, Sang Joon Kim, and Jae-sun Seo, "A Smart Hardware Security Engine Combining Entropy Sources of ECG, HRV, and SRAM PUF for Authentication and Secret Key Generation," *IEEE Asian Solid-State Circuits Conference (ASSCC)*, 2019.
- **Sai Kiran Cherupally**, Shihui Yin, Deepak Kadetotad, Gaurav Srivastava, Chisung Bae, Sang Joon Kim, and Jae-sun Seo. "ECG Authentication Neural Network Hardware Design with Collective Optimization of Low Precision and Structured Compression." *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2019.
- **Sai Kiran Cherupally**, "Hierarchical Random Boolean Network Reservoirs." M.S. Thesis, 2018.

PATENTS

- Jae-sun Seo, Shihui Yin, **Sai Kiran Cherupally**, "Smart Hardware Security Engine Using Biometric Features and Hardware-Specific Features," Patent pending, United States Patent Application No. 16/864,902.

TOOLS & SKILLS

- Verilog, SystemVerilog, Cadence / Synopsis / Mentor EDA tools
- Scan chain insertion, Clock gating, Power gating, Memory interleaving
- Python, PyTorch for deep learning, Bash
- CIFAR-10, CIFAR-100, ImageNet datasets, and several public ECG databases
- SRAM and RRAM based in-memory computing (IMC) technologies
- Proficient in digital hardware design, and functional verification/validation

References available on request