SYS940X

GPIO User Guide

001355 Rev B

July 17, 2013

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Revision history

Revision	Date	Description	Author
1.0	06/December/2011	Initial release	Subramanian H
1.1	09/December/2011	Table 1 and Table 2 name changed	Subramanian H
1.2	24/January/2012	Added Topcliff and Super IO GPIO access	Subramanian H
B	17/July/2013	Document Format Changed	Kavya

Approval Record

Function	Position	Name	Date
Checked By	Project Engineer	Kavya	17/July/2013
Reviewed By	Project Engineer	Kavya	17/July/2013
Approved By	Project Manager	Deveraj P S	17/July/2013

Preface

The purpose of this document is to provide the information about GPIO interfaces, pinouts and interfacing details for users to develop their drivers and other application software's for accessing this interface.

Intended Audience

This document is intended for technically qualified personnel. It is not intended for general audiences.

Intended Use

All Inforce boards are evaluated as Information Technology Equipment (I.T.E.) for use in personal computers (PC) for installation in homes, offices, schools, computer rooms, and similar locations. The suitability of this product for other PC or embedded non-PC applications or other environments, such as medical, industrial, alarm systems, test equipment, etc. may not be supported without further evaluation by Inforce Computing.

Document Organization

The chapters in this document are arranged as follows:

1. Introduction
2. GPIO Architecture
3. Installing System Components
4. Topcliff GPIO driver
5. Super IO
6. Company contact information

Conventions

The following conventions are used in this document:

CAUTION

Cautions warn the user about how to prevent damage to hardware or loss of data.

NOTE

Notes call attention to important information.

Note

This document is subject to change without notice.

Support Information

Every effort has been made to ensure the accuracy of this document. If you have any comments, questions, or ideas regarding this document, Contact technical support: techsupport@inforcecomputing.com

Terminology

The table below gives descriptions to some common terms used in this document.

Term	Description
ASIC	Application Specific Integrated Circuit
BIOS	Basic Input/ Output System
BLDK	Boot Loader Development Kit
DC	Direct Current
GHz	Gigahertz (one billion hertz)
GPIO	General Purpose Input / Output
LPC	Low Pin Count
PCI	Peripheral Component Interconnect
SPI	Serial Peripheral Interface
V	Voltage

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1. INTRODUCTION

The Inforce® SYS940X Portable Computing Platform is a highly-integrated processor system that provides rich and flexible features to embedded and mobile system designers. Based on Intel® Atom™ technology specifically created for ultra-mobile computing, the SYS940X offers outstanding performance in a small form-factor to optimize solutions for a variety of portable and fixed installation applications.

2. GPIO ARCHITECTURE

This chapter briefly describes the GPIO architecture of SYS940X-01 system.

Figure 1: GPIO Architecture

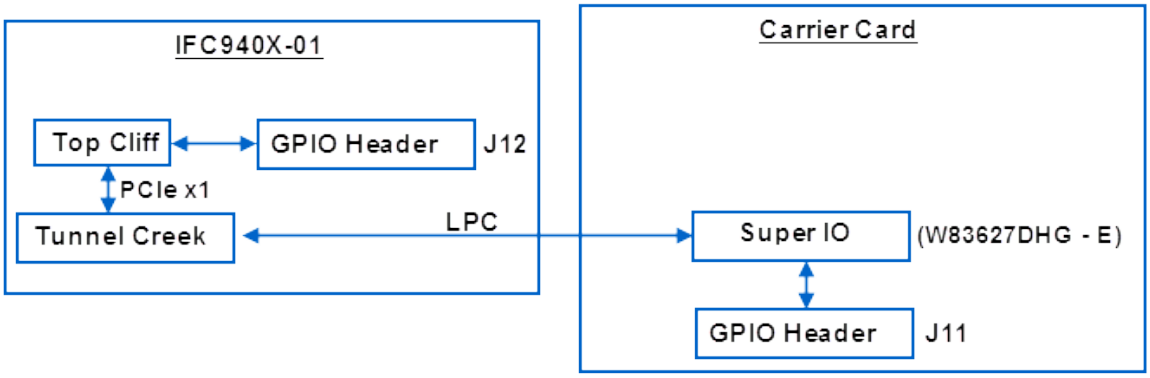


Table 1: Carrier Card (Super IO) GPIO header mapping

Signal Name	Device Location	Pin	Pull Up / Down
LPC GP34	Super IO – Pin # 88	2	2.7K to VCC
LPC GP35	Super IO – Pin # 87	4	2.7K to VCC
LPC GP36	Super IO – Pin # 69	6	2.7K to VCC
LPC GP37	Super IO – Pin # 64	8	2.7K to VCC
LPC GP30	Super IO – Pin # 92	1	2.7K to VCC
LPC GP31	Super IO – Pin # 91	3	2.7K to VCC
LPC GP32	Super IO – Pin # 90	5	2.7K to VCC
LPC GP33	Super IO – Pin # 89	7	2.7K to VCC

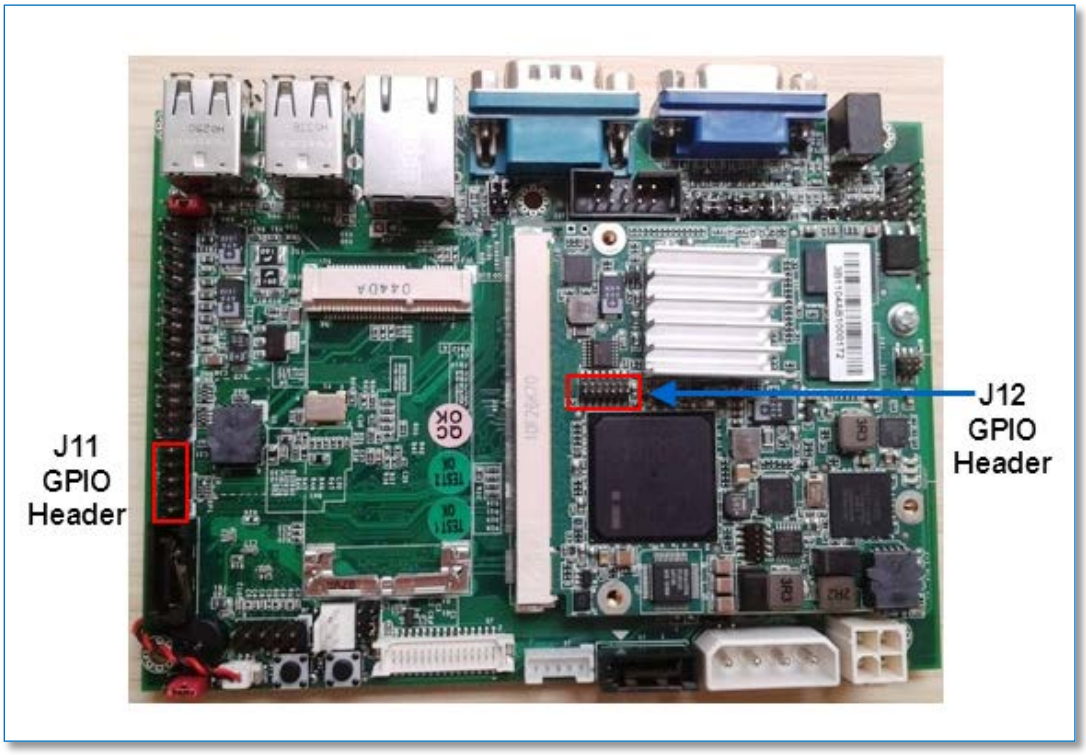
Table 2: IFC940X-01 (Topcliff IOH) GPIO header Mapping

Signal Name	Device Location	Pin	Pull Up / Down
IOH GPIO 0	Top Cliff – Pin AB20	4	None
IOH GPIO 1	Top Cliff – Pin AB19	6	None
IOH GPIO 2	Top Cliff – Pin AB18 & Carrier Card JP5 Connector Pin # 2	8	None
IOH GPIO 3	Top Cliff – Pin AA18	10	None
IOH GPIO 4	Top Cliff – Pin Y18	12	None
IOH GPIO 5	Top Cliff – Pin AB17	14	None
IOH GPIO 7	Top Cliff – Pin Y17	3	None
IOH GPIO 8	Top Cliff – Pin A9	5	None
IOH GPIO 9	Top Cliff – Pin B9	7	None
IOH GPIO 10	Top Cliff – Pin A8	9	None
IOH GPIO 11	Top Cliff – Pin B8	11	None

2.1 SYSTEM COMPONENT OVERVIEW

Figure 1 shows the location of GPIO headers on SYS940X-01.

Figure 2: SYS940X-01 GPIO Header



3. INSTALLING SYSTEM COMPONENTS

This chapter explains about internal headers.

3.1 BEFORE YOU BEGIN

CAUTION

The procedures in this chapter assumes familiarity with the general terminology associated with embedded systems and with the safety practices and regulatory compliance required for using and modifying electronic equipment.

Disconnect the system from its power source and from any telecommunications links, networks, or modems before performing any of the procedures described in this chapter. Failure to disconnect power, telecommunications links, networks, or modems before you open the computer or perform any procedures can result in personal injury or equipment damage. Some circuitry on the system can continue to operate even though the power button is off.

Follow these guidelines before you begin using the SYS940X-01 system:

- Always follow the steps in each procedure in the correct order.
- Set up a log to record information about your system, such as model, serial numbers, installed options, and configuration information.
- Electrostatic discharge (ESD) can damage components. Perform the procedures described in this chapter only at an ESD workstation using an antistatic wrist strap and a conductive foam pad. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the computer chassis.

3.1.1 INSTALLATION PRECAUTIONS

When you install and test the SYS940X-01 system, observe all warnings and cautions in the installation instructions.

To avoid injury, be careful of:

- Sharp pins on connectors or headers
- Sharp pins on printed circuit assemblies
- Rough edges and sharp corners on the chassis
- Hot components (such as voltage regulators and heat sinks)
- Damage to wires that could cause a short circuit

Observe all warnings and cautions that instruct you to refer computer servicing to qualified technical personnel.

3.1.2 PREVENT POWER SUPPLY OVERLOAD

Do not overload the power supply output. To avoid overloading the power supply, make sure that the calculated total current loads of all the modules within the system is less than the output current rating of the power supply.

3.1.3 OBSERVE SAFETY AND REGULATORY REQUIREMENTS

Read and adhere to the instructions in this section and the instructions supplied with the chassis and associated modules. If you do not follow these instructions and the instructions provided by chassis and module suppliers, you increase safety risk and the possibility of noncompliance with regional laws and regulations.

3.2 CONNECTING TO THE INTERNAL GPIO HEADERS

Before connecting cables to the internal headers, observe the precautions in "Before You Begin" on page 4. Figure 3 shows the location of the board's internal headers, Table 3 describes the internal headers identified in Figure 3.

Figure 3: Internal GPIO Headers

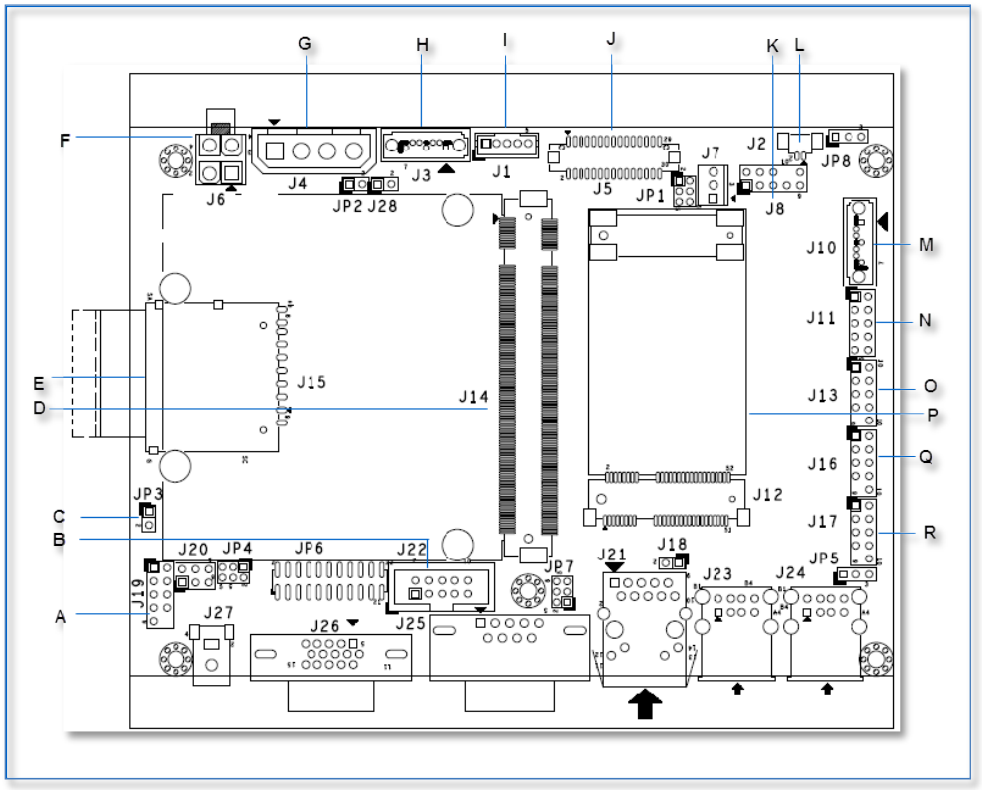


Table 3: Internal GPIO Headers on Carrier Card

Item	Description	Item	Description
A	Front panel control header	B	RS232 header
C	Auto power header	D	Q7 connector
E	SD cord slot	F	Auxiliary power connector
G	SATA power connector	H	SATA data connector 0
I	LVDS back light connector	J	LVDS connector
K	Audio header	L	RTC battery connector
M	SATA data connector 1	**N**	**GPIO header**
O	LPC debug port	P	Mini PCI connector
Q	USB header 0	R	USB header 1

NOTE

Highlighted header is the GPIO header on the Carrier Card

3.3 INTERNAL GPIO HEADER

Table 4: J11 GPIO header (HDR 2x5P 2.54mm) on Carrier Card

Pin	Signal Name	Pin	Signal Name
1	LPC GP30	2	LPC GP34
3	LPC GP31	4	LPC GP35
5	LPC GP32	6	LPC GP36
7	LPC GP33	8	LPC GP37
9	GND	10	VCC

Table 5: J12 GPIO header (HDR 2x7P 1.27mm) on CPU Module

Pin	Signal Name	Pin	Signal Name
1	Reserved	2	V3P3
3	IOH GPIO 7	4	IOH GPIO 0
5	IOH GPIO 8	6	IOH GPIO 1
7	IOH GPIO 9	8	IOH GPIO 2
9	IOH GPIO 10	10	IOH GPIO 3
11	IOH GPIO 11	12	IOH GPIO 4
13	GND	14	IOH GPIO 5

NOTE

V3P3 = 3.3V

VCC = 5V

GND = Ground Reference

NOTE

IOH GPIO 2 is a dual functionality signal as described below

Table 6: JP5 (HDR 1x3P 2.54mm) on Carrier Card

Pin	Signal Name
1	VSB5 (5V)
2	USB HC SEL (IOH GPIO 2)
3	GND

NOTE

1-2 Host (Default) / 2-3 Client

4. TOPCLIFF GPIO DRIVER

The Topcliff EG20T packet hub exposes 12 GPIO pins (from GPIO244 to GPIO255) for the SYS940X board for Inforce Connector on the board – J12. Using systems path in Sysfs, user can access it.
There are three kinds of entry in /sys/class/gpio:
Control interfaces used to get userspace control over GPIOs,GPIOs themselves and GPIO controllers.

- The control interfaces are write-only:

```
sys/class/gpio/
"export" ... Users ask the kernel to export control of  a GPIO to userspace
by writing its number to this file.
"unexport" ... Reverses the effect of exporting to userspace.
```

- GPIO signals have paths like /sys/class/gpio/gpio244/ (for GPIO #244)and have the following read/write attributes:

```
/sys/class/gpio/gpioN/
   "direction" ... reads as either "in" or "out".
   "value" ... reads as either 0 (low) or 1 (high).
   "edge" ... reads as either "none", "rising", "falling", or "both".
   "active_low" ... reads as either 0 (false) or 1 (true).
```

4.1 GPIO ACCESS IN FEDORA CORE 11 TIMESYS VERSION

1. As a root user (use su or sudo), load the module

   ```
   # insmod sch_gpio.ko
   ```

2. Verify that module loaded

   ```
   # lsmod | less
   ```

3. Follow the below example to export the GPIO pins in Fedora Core 14 Timesys version.

4.2 GPIO ACCESS IN FEDORA CORE 14 TIMESYS VERSION

NOTE

By default, the driver is available

A basic example of GPIO usage,

1. As a root, load the following driver.

   ```
   # modprobe sch_gpio
   ```

2. Verify that module loaded:

   ```
   # lsmod | less
   ```

Follow the below example to export the gpio pins.

Export the GPIO pins

1. To export the GPIO number 245

   ```
   # echo 245 > /sys/class/gpio/export
   ```

   This will create a directory gpio245 at /sys/class/gpio/ which contains the interface.

2. Set the direction to be output

   ```
   # echo out > /sys/class/gpio/gpio245/direction
   ```

3. Set to on-state.

   ```
   #echo 1 > /sys/class/gpio/gpio245/value
   ```

4. Set to off-state

   ```
   # echo 0 > /sys/class/gpio/gpio245/value
   ```

5. To remove the directory

   ```
   echo 245 > /sys/class/gpio/unexport
   ```

6. Similarly, you can access other gpio pins.

Test:

7. Test the voltage with multimeter on the board.

5. SUPER IO

Super IO W83627DHG GPIO Test Utility in Linux/Fedora 11 and Fedora 14 for the SYS940X board for Inforce Connector on the carrier card board – J11.This application enables to control the devices using the GPIO interface.

Below are the details for installation of the same.

1. Login as **root** user to run the application.
2. Compile the source file

   ```
   # cc superio_gpio_app.c -o superio_gpio_app
   ```

3. For usage help of read and write operations of gpio functions.

   ```
   #./superio_gpio_app -h
   ```

   Usage: superio_gpio_app write [pin_no] [in/out] [signal_level]

   Usage: superio_gpio_app read [pin_no]

   pin_no: GPIO pin number(available pins:1,2,3,4,5,6,7,8) to select in /out: 1 for input, 0 for output

   signal_level : 1 for high level, 0 for low level

4. Example:

   To write to gpio pin 6

   ```
   #./superio_gpio_app write 6 1 0
   ```

   To read from gpio pin 6

   ```
   #./superio_gpio_app read 6
   ```

5. Test

   Test the voltage with multimeter on the board

6. CONTACT INFORMATION

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