ELEC-336 PROJECT

Differential Amplifier Design And Cascode Load

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1. Objective

The purpose of **differential pair design** in electronics is to eliminate noise and amplify the signal by applying two signals with a 180-degree phase difference on both sides. This results in a higher quality and stronger signal.

Its application areas include sound, video, and internet usage.

The operating principle is shown in Figure 1.

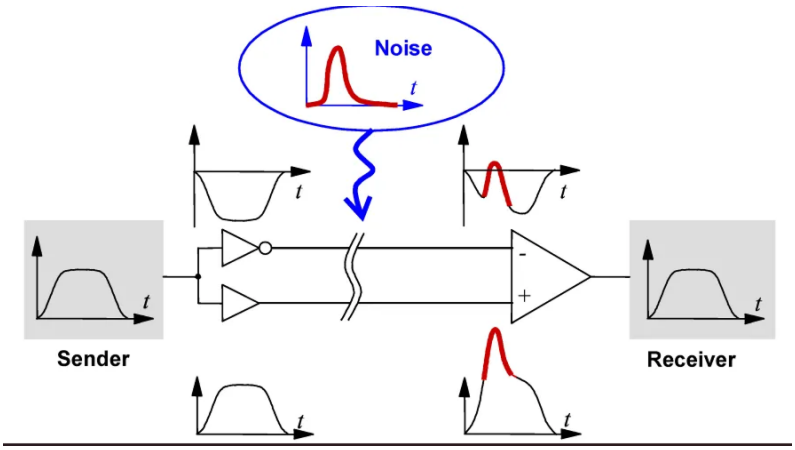


Figure 1.

2.Circuit Design

As required in the project, the LTSpice program has been used. As required in the project, the PMOS and NMOS have been included in LTSpice. These two MOSFETs are manufactured using 180nm technology. According to the code, the values of μCox and Vth have been determined.

	PMOS	**NMOS**
Vth	**0.4 v**	**0.4 v**
μCox (mobility multiplied by oxide capacitance)	**$3x10^{-4}$ A/V^2**	**$3.5x10^{-2}$ A/V^2**

The schematic design essentially consists of two PMOS transistors on the top and two main NMOS transistors on the bottom. The upper part represents the active load section. Below the NMOS transistors, a tail current source for biasing is added.

The DC supply is set to VDD = 1.8V, and the signals are 180 degrees out of phase with an amplitude of 0.1mVpp (0.05mVp) and a frequency of 10kHz. The circuit is shown in Figure 2 in LTspice.

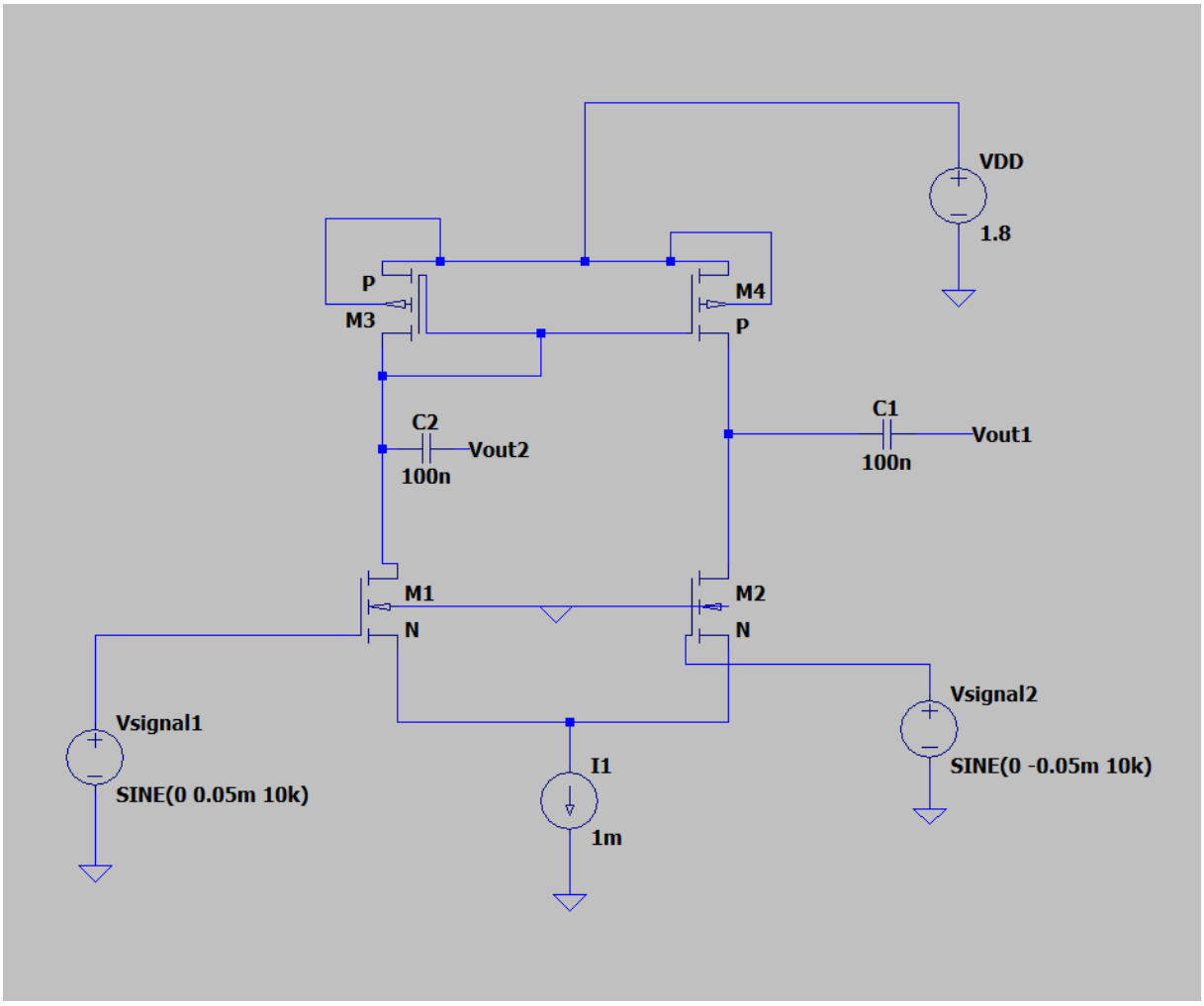
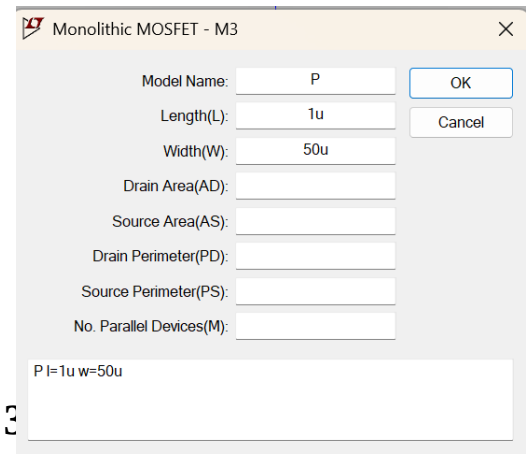
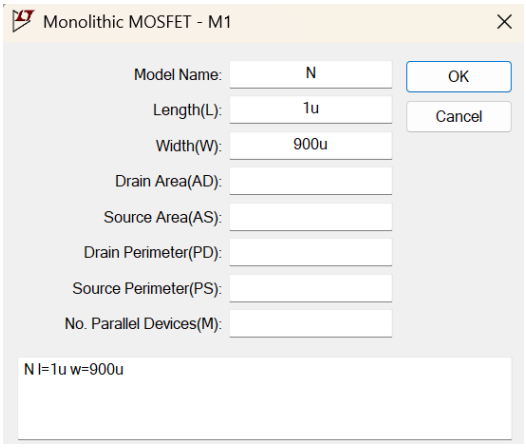


Figure 2.

The W/L ratios of the MOSFETs :

	W	L	W/L
PMOS	50u	1u	50
NMOS	900u	1u	900





3.1 DC ANALYSIS

Before starting the simulation, it is necessary to analytically calculate and test whether the transistor is operating in the saturation region. As shown in Figure 3. , the Isd current should be 0.5mA.

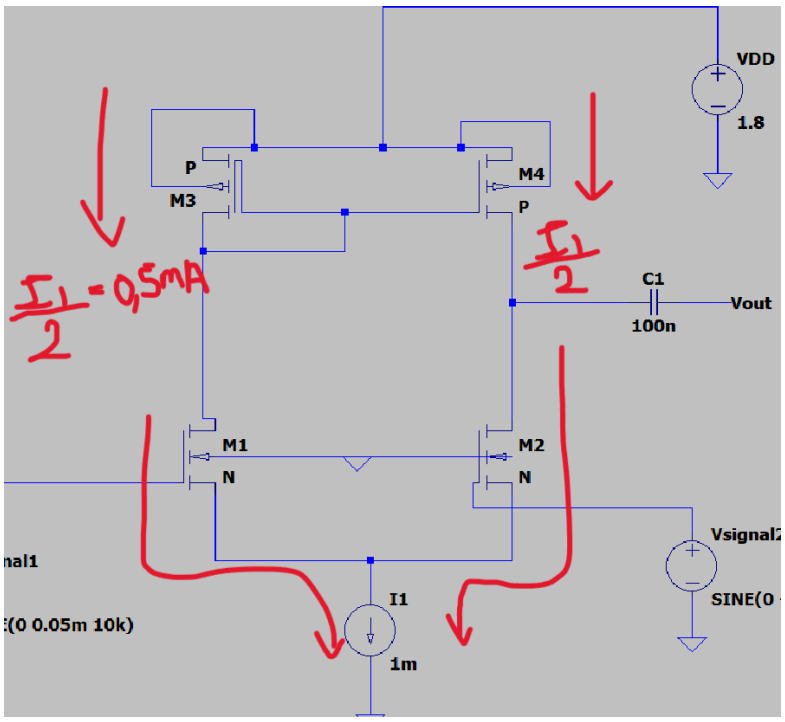


Figure 3.

Then, the Vsg current can be found from the equation of the PMOS operating in the saturation mode.

$$I_{SD} = \frac{1}{2}\mu Cox(\frac{W}{L})(Vsg - Vth)^2$$

$$0.0005 = \frac{1}{2}0.015x130(Vsg - 0.4)^2$$

$$V_{SG} = 0.64v$$

And, it must be $V_{SG}(0.64v) > vth(0.4v)$. Therefore, it is correct for saturation mode and others.

The accuracy of the values has been tested through simulation in LTspice On Figure 3.1.

--- Operating Point ---

V(n002):	0.623818	voltage
V(n001):	1.8	voltage
V(n003):	0.623818	voltage
V(n004):	0	voltage
V(n006):	-0.526793	voltage
V(n005):	0	voltage
V(vout):	6.23818e-008	voltage
Id(M2):	0.000492992	device_current
Ig(M2):	0	device_current
Ib(M2):	7.00759e-006	device_current
Is(M2):	-0.0005	device_current
Id(M1):	0.000492992	device_current
Ig(M1):	0	device_current
Ib(M1):	7.00759e-006	device_current
Is(M1):	-0.0005	device_current
Id(M4):	0.000492992	device_current
Ig(M4):	-0	device_current
Ib(M4):	1.18618e-012	device_current
Is(M4):	-0.000492992	device_current
Id(M3):	-0.000492992	device_current
Ig(M3):	-0	device_current
Ib(M3):	1.18618e-012	device_current
Is(M3):	0.000492992	device_current
I(C1):	-6.23818e-020	device_current
I(I1):	0.001	device_current
I(Vsignal1):	0	device_current
I(Vsignal2):	0	device_current
I(Vdd):	-0.000985985	device_current

Figure 3.1

3.2 AC ANALYSIS

For the AC analysis, the input signal is shown in Figure 3.2.

(0.01m(vpp) = 0.05m(vp)) = (50u(vp))

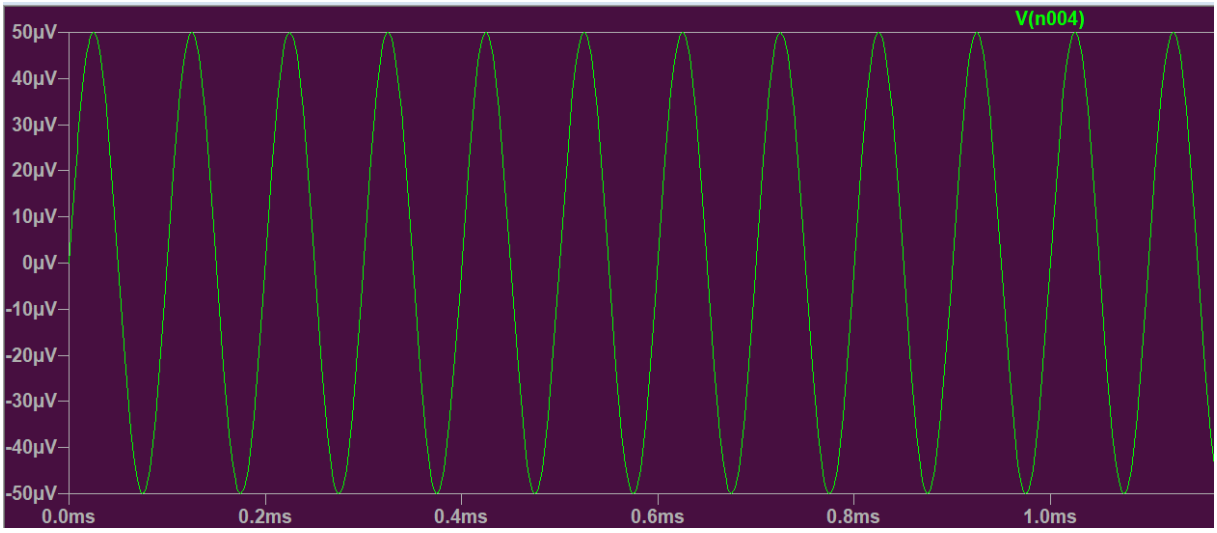


Figure 3.2(V(n004) = vsignal1)

Later, the Vout1 signal is shown in Figure 3.3.

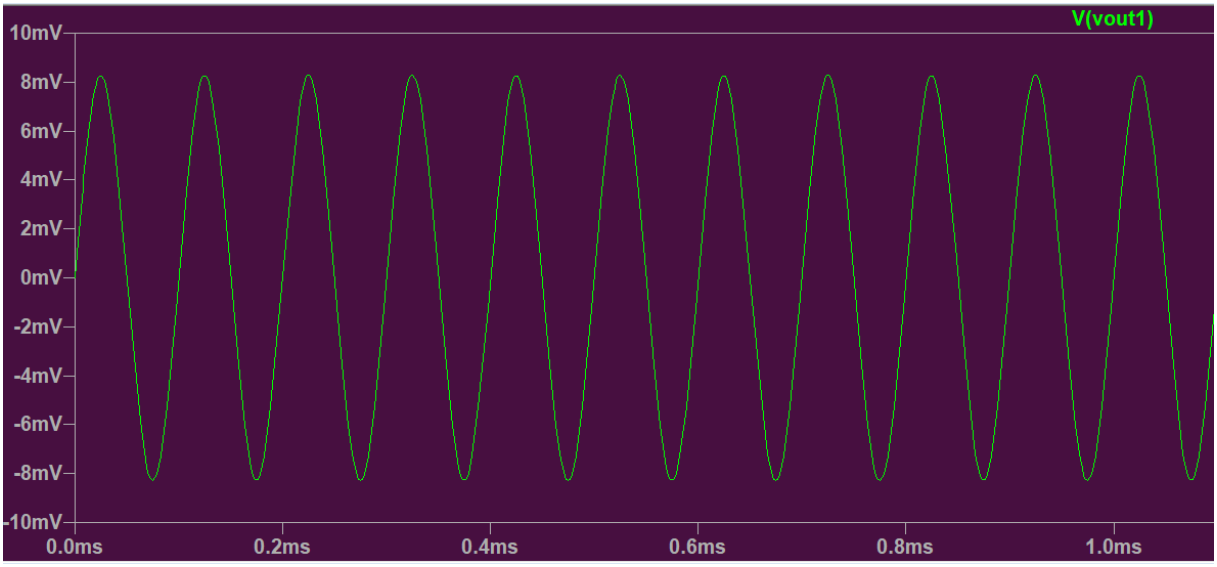


Figure 3.3

Together (Figure 3.4) :

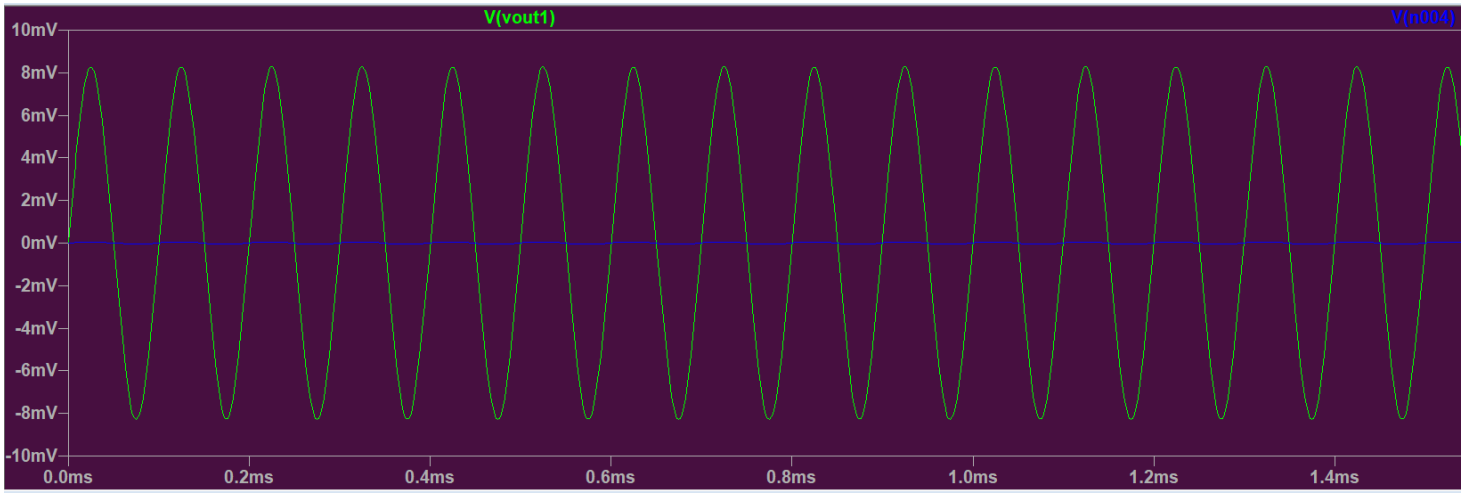


Figure 3.4

The differential gain is given with a phase difference, while the common mode gain is given without a phase difference and is applied to the common signal.

Differential Gain (A_d) :

The parameters :

Difference between vout1 and vout2 is required (Figure 3.5):

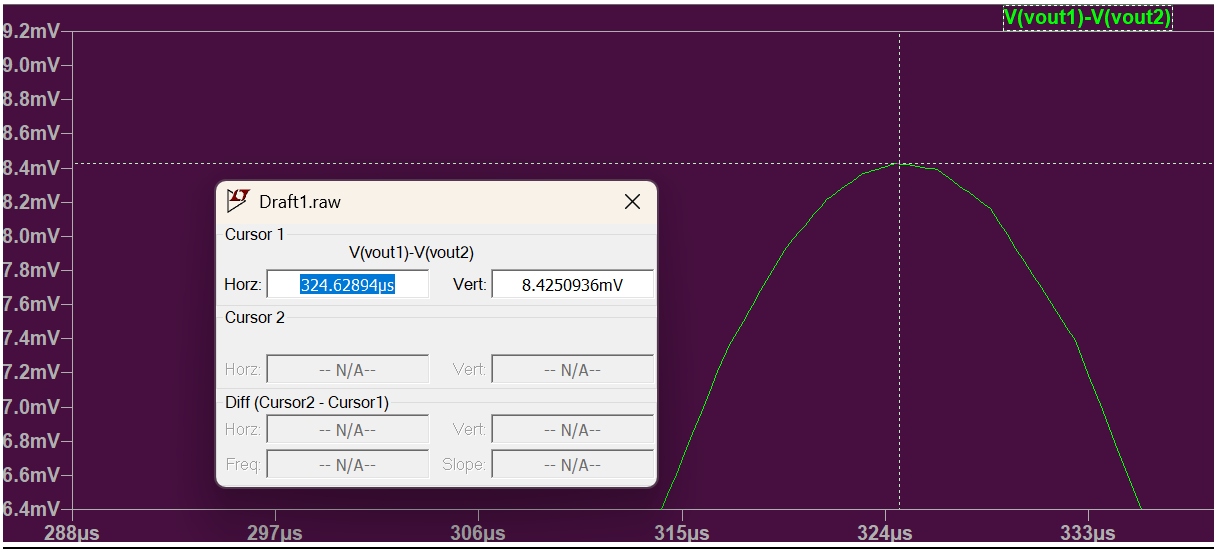


Figure 3.5

Difference between vsignal1 and vsignal2 is required (Figure 3.6):

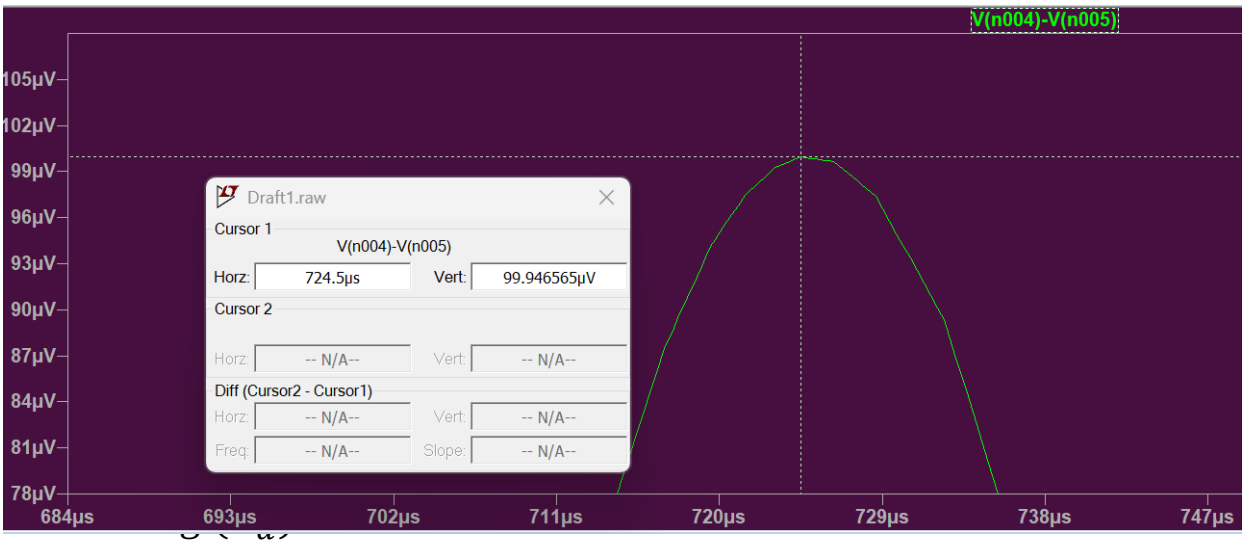


Figure 3.6

$$A_d = \frac{\Delta \text{Vout}}{\Delta \text{Vin}} = \frac{\text{Vout1} - \text{Vout2}}{\text{Vsignal1} - \text{Vsignal2}} = \frac{8.42\text{mv}}{100\text{uv}} = 84.2(v/v)$$

Common-Mode Gain (A_{cm}) :

To calculate the common-mode gain, the 180-degree phase difference between the input sources is removed, and then the average of Vout1 and Vout2 Vout2 is taken. Similarly, the average of V signal1 Vsignal1 and Vsignal2 Vsignal2 is computed. The ratio of the output average to the input average gives the common-mode gain.

The parameters :

For vout, the average of vout1 and vout2 is taken (Figure 3.6) :

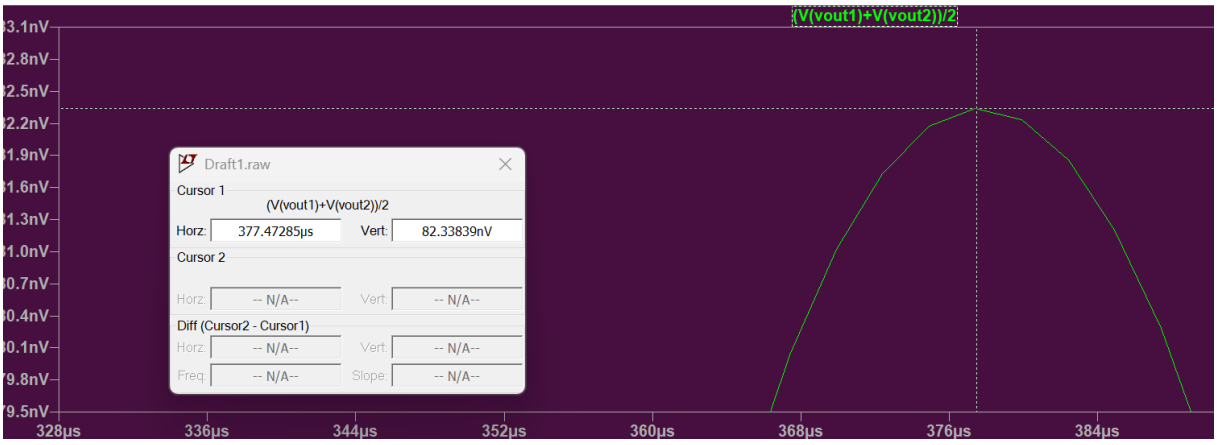


Figure 3.7

For vin, the average of vsignal1 and vsignal2 is taken (Figure 3.8) :

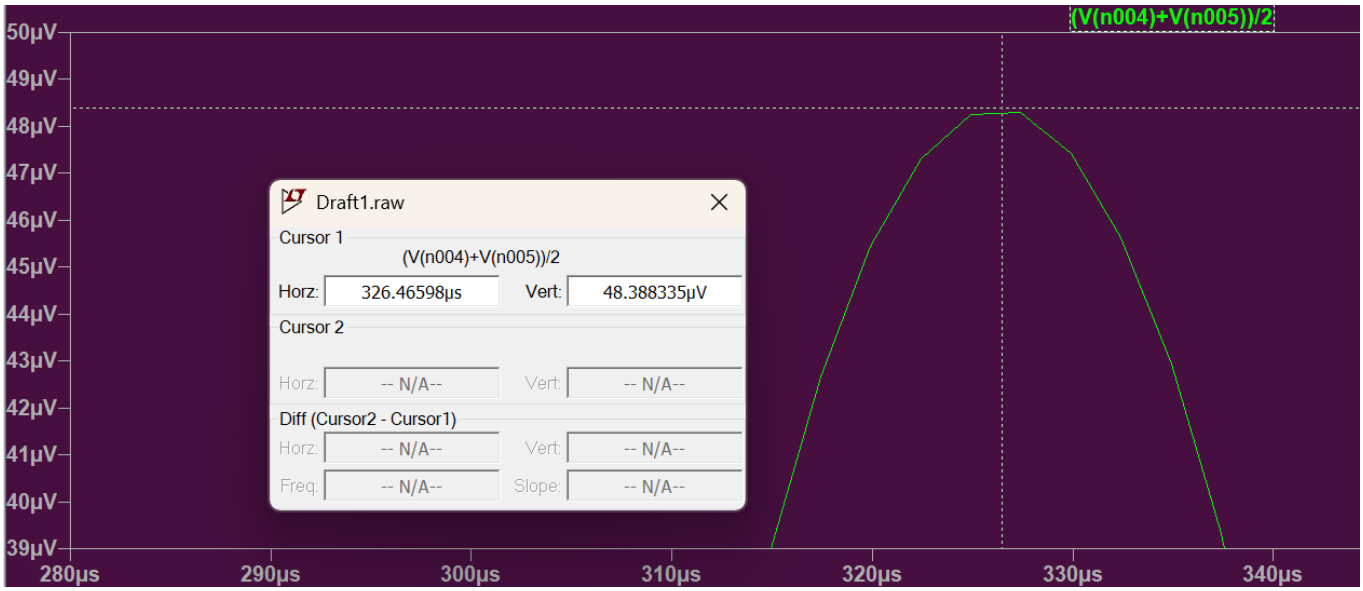


Figure 3.8

Calculating (A_{cm}) :

$$A_{cm} = \frac{\text{Vout(common)}}{\text{Vin(common)}} = \frac{82.34\text{nv}}{48.39\text{uv}} = 0.0017(v/v)$$

Calculation and observing of 3dB Bandwith :

$$A_d = 84.2(v/v)$$

$$A_d(db) = 20\log(A_d) = 20\log(84.2) = 38.5(db)$$ (Figure 3.9 and 3.10)

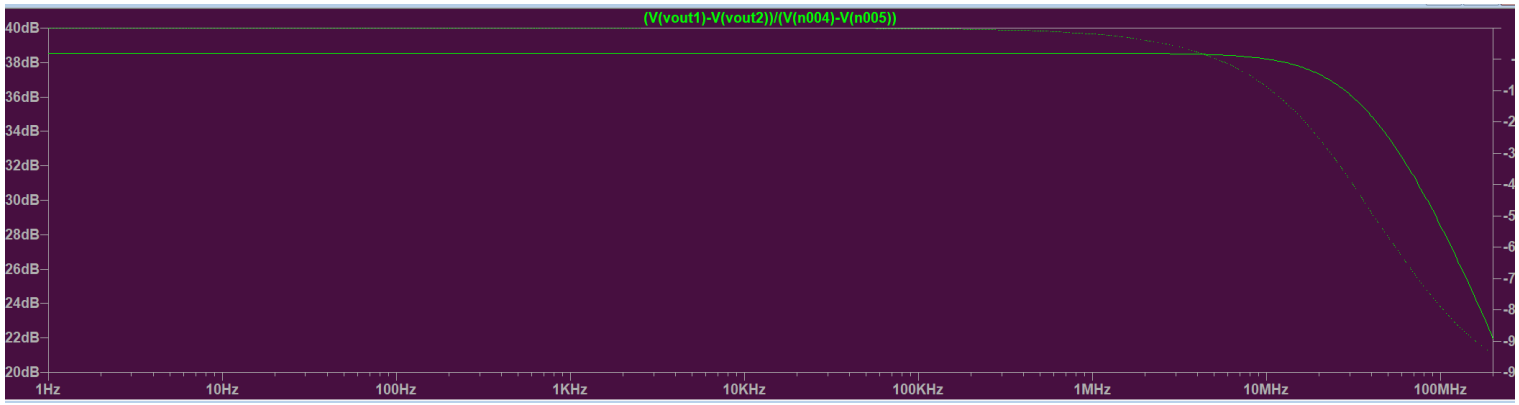


Figure 3.9

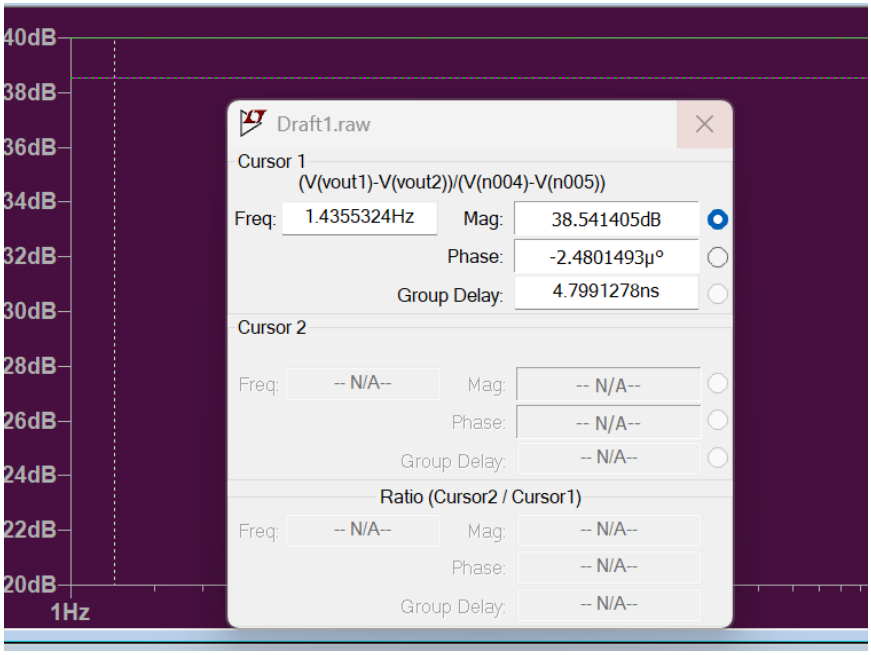


Figure 3.10

As shown in Figures 3.9 and 3.10, the Ad gain is 38.5 dB. To find the 3 dB bandwidth, the frequency at which the gain shows 35.5 dB (which is also 0.7 times the maximum gain) is shown in Figure 3.11

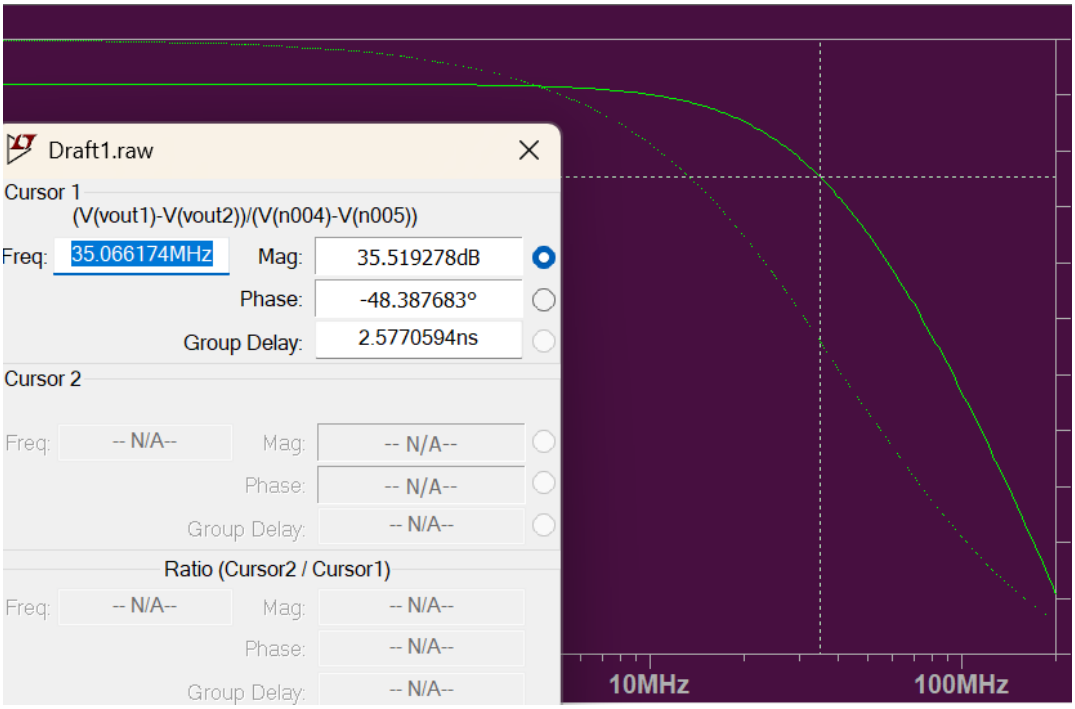


Figure 3.11

The 3 dB bandwidth = 35 MHz.

Unity gain:

it represents a gain of 1, or the 0 dB point (Figure 3.12 and 3.13)

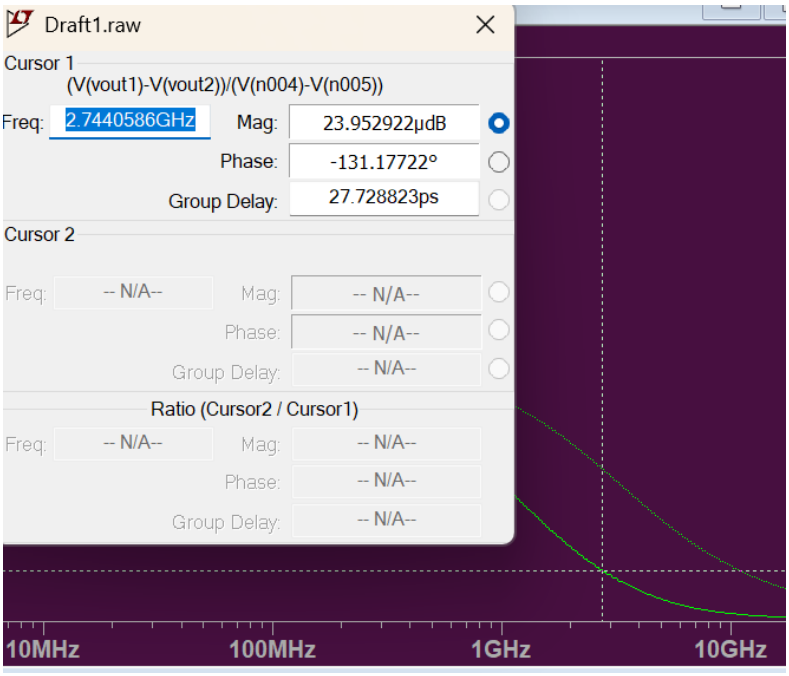


Figure 3.12

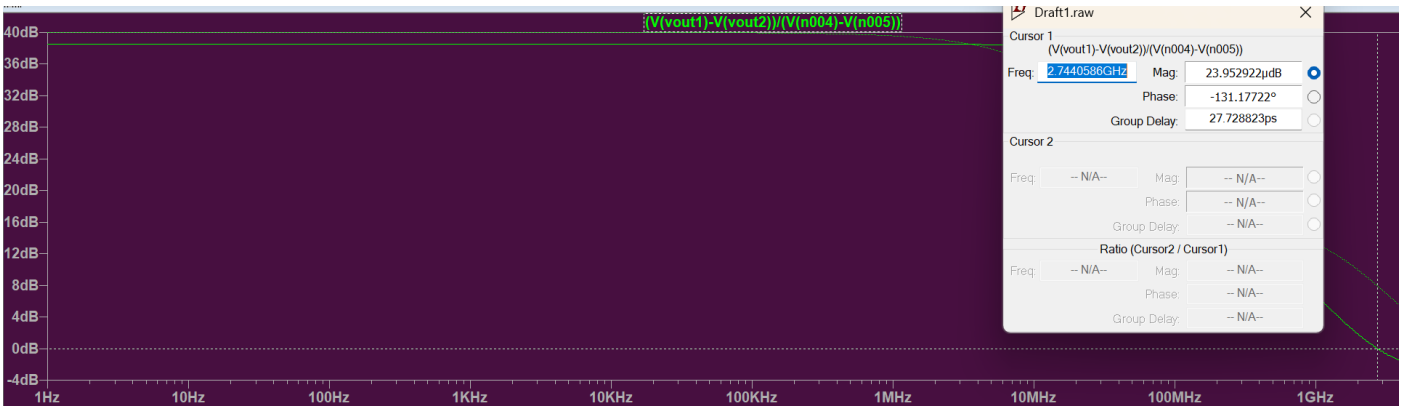


Figure 3.13

unity gain = 2.74Ghz.

Calculating input empedance and output empedance (Z_{in} and Z_{out}) :

When calculating Zin and Zout , Thevenin's theorem is applied, and test voltages Vtest are applied. Then, the current is measured and the ratio is calculated.

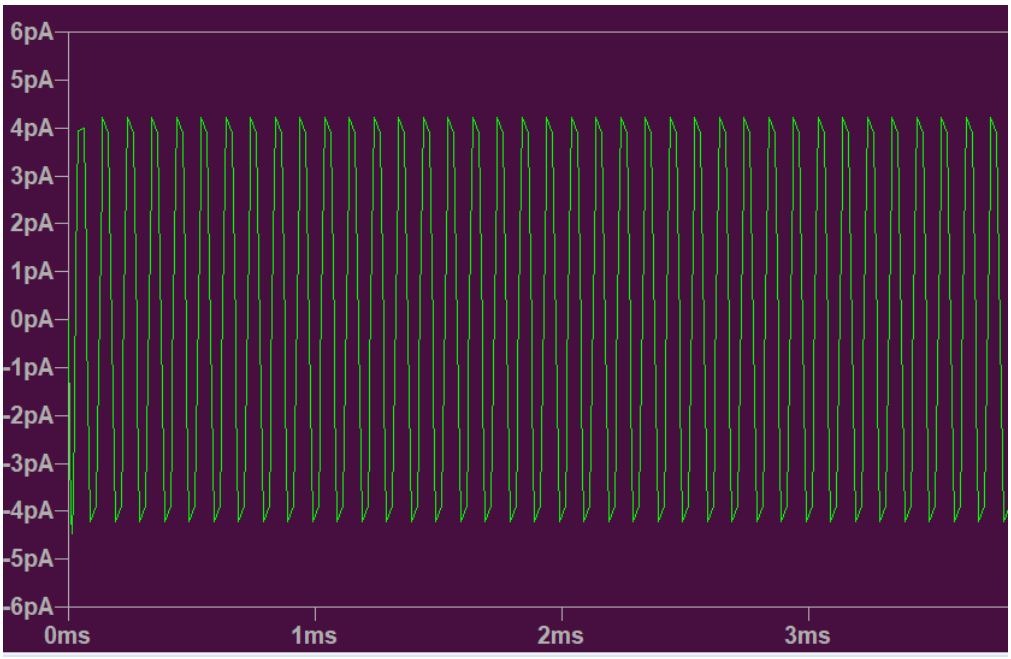


Figure 3.14

$$Z_{in} = \left(\frac{V_{signal}}{I_{in}}\right) = \frac{0.05m(vp)}{4pA} = 12.5M\Omega$$

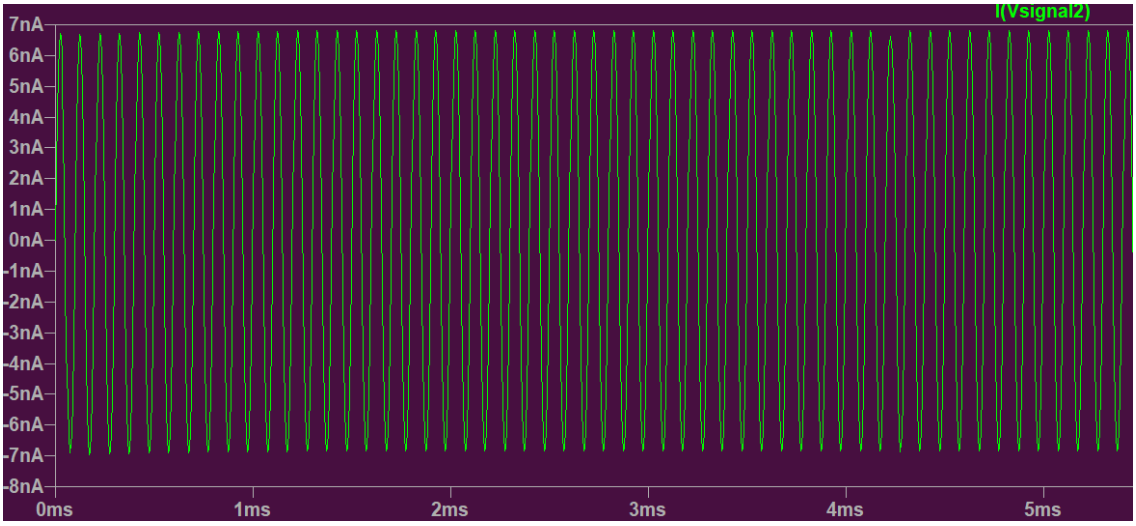


Figure 3.15

$$Z_{out} = \left(\frac{V_{signal}}{I_{out}}\right) = \frac{0.05m(vp)}{7nA} = 7.1k\Omega$$

3.3 Calculating (CMRR) :

CMRR (Common-Mode Rejection Ratio) is a performance parameter that measures the ability of a differential amplifier to suppress common-mode signals

$$\text{CMRR} = 20\log\left(\frac{A_d}{A_{cm}}\right) = \left(\frac{84.2}{0.0017}\right) = 93.9db$$

3.4 Transient Analysis

The input starts at 0.05 mVp and the amplitude is increased step by step. The resulting outputs are presented in Table 2.

Table 2.

	vout	Wave type
0.05m(vp)	8m(vp)	sinusoidal
0.1m(vp)	16m(vp)	sinusoidal
1m(vp)	160m(vp)	sinusoidal
5m(vp)	700m(vp)	sinusoidal
10m(vp)	600m(vp)	Sinusoidal(but voltage drift)

As seen from the values, for 10mV and beyond, the amplifier will distort both the gain and the waveform. A maximum of 10mV should be applied to the input.

4.Design Optimization

In the project, a gain of Ad > 80 v/v is required. Since Ad = 84.2, it is clear that **84.2 >> 80**, and the desired value is achieved.

CMRR > 60dB is required. Since **93.9 >> 60dB**, the desired value is achieved.

The W/L ratio of the MOSFETs, especially the NMOS transistors, was initially high. Later, the W/L ratio was reduced to 100, and the tail current was also reduced to 0.1, which led to the MOSFETs drawing less current. As a result, the MOSFETs consumed less power, and at the same time, the gain increased.

Table 3.

	W	L	W/L
PMOS	50u	1u	50
NMOS	100u	1u	100

Calculating Gain :

Figures 4.0, 4.1, and 4.2 show the voltage values obtained for calculating the Ad gain.

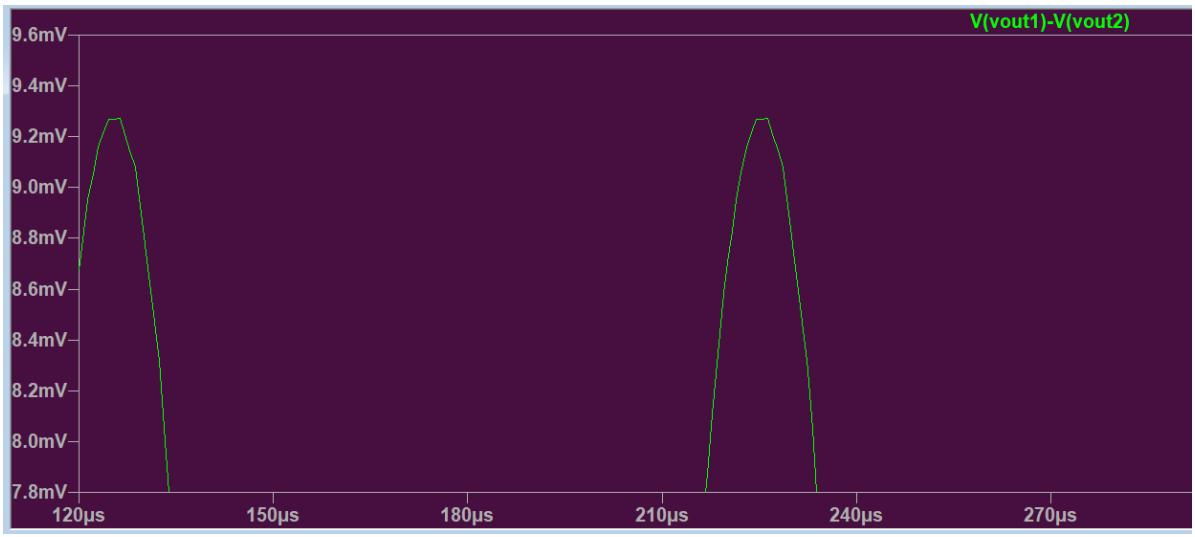


Figure 4.0

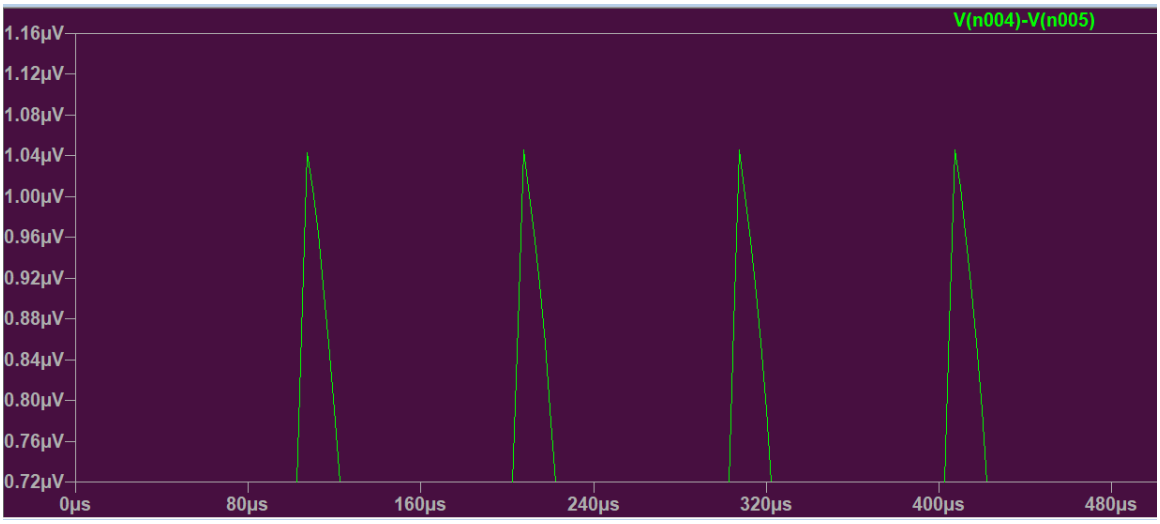


Figure 4.1

Figure 4.2

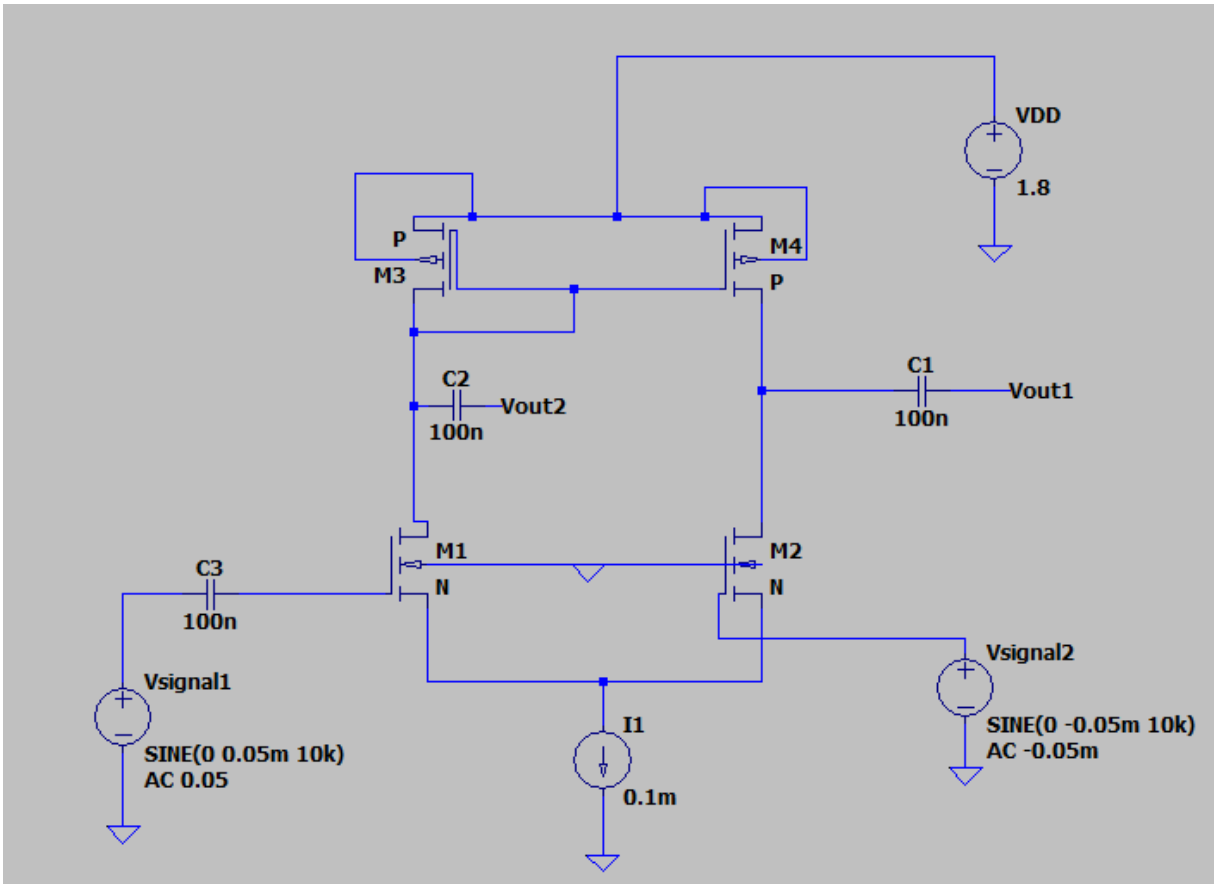
$$A_d = \frac{\Delta\text{Vout}}{\Delta\text{Vin}} = \frac{\text{Vout1} - \text{Vout2}}{\text{Vsignal1} - \text{Vsignal2}} = \frac{9.3\text{mv}}{100\text{uv}} = 93(v/v)$$

$$A_{cm} = \frac{\text{Vout(common)}}{\text{Vin(common)}} = \frac{40\text{nv}}{0.05\text{mv}} = 0.0008(v/v)$$

$$\text{CMRR} = 20\log\left(\frac{A_d}{A_{cm}}\right) = \left(\frac{93}{0.0008}\right) = 101db$$

End of the design (Figure 4.3):

The final version of the circuit is shown in Figure 4.3. The W/L ratios have been reduced, and the tail current has been set to 0.1mA, resulting in an increase in differential gain and CMRR. The main reason for these changes was to achieve power optimization, and thus, the design has been completed.



Figure(4.3)

5.Bonus Challenge(Cascode-Loaded Amplifer):

The cascode load configuration enhances the output impedance and gain of the differential amplifier, ensuring more stable operation and reducing the Miller effect. In this design, PMOS transistors (M5 and M6) are added on top of the active load transistors (M3 and M4) and function as cascode elements.

This structure improves isolation between the output and the load, leading to increased gain and accuracy. Cascode designs offer higher gain and better linearity compared to traditional active load structures. Additionally, the increased output impedance enhances the common-mode rejection ratio (CMRR) and differential gain. However, these benefits often introduce greater circuit complexity and may reduce bandwidth.

The schematic illustrates the circuit where the cascode load is integrated into the differential amplifier. PMOS transistors M5 and

M6 act as cascode elements, while M3 and M4 continue to serve as active loads. The following sections analyze gain, output impedance, CMRR, and bandwidth, and compare them with the active load configuration.

The cascode load amplifier is shown in Figure 5.0.

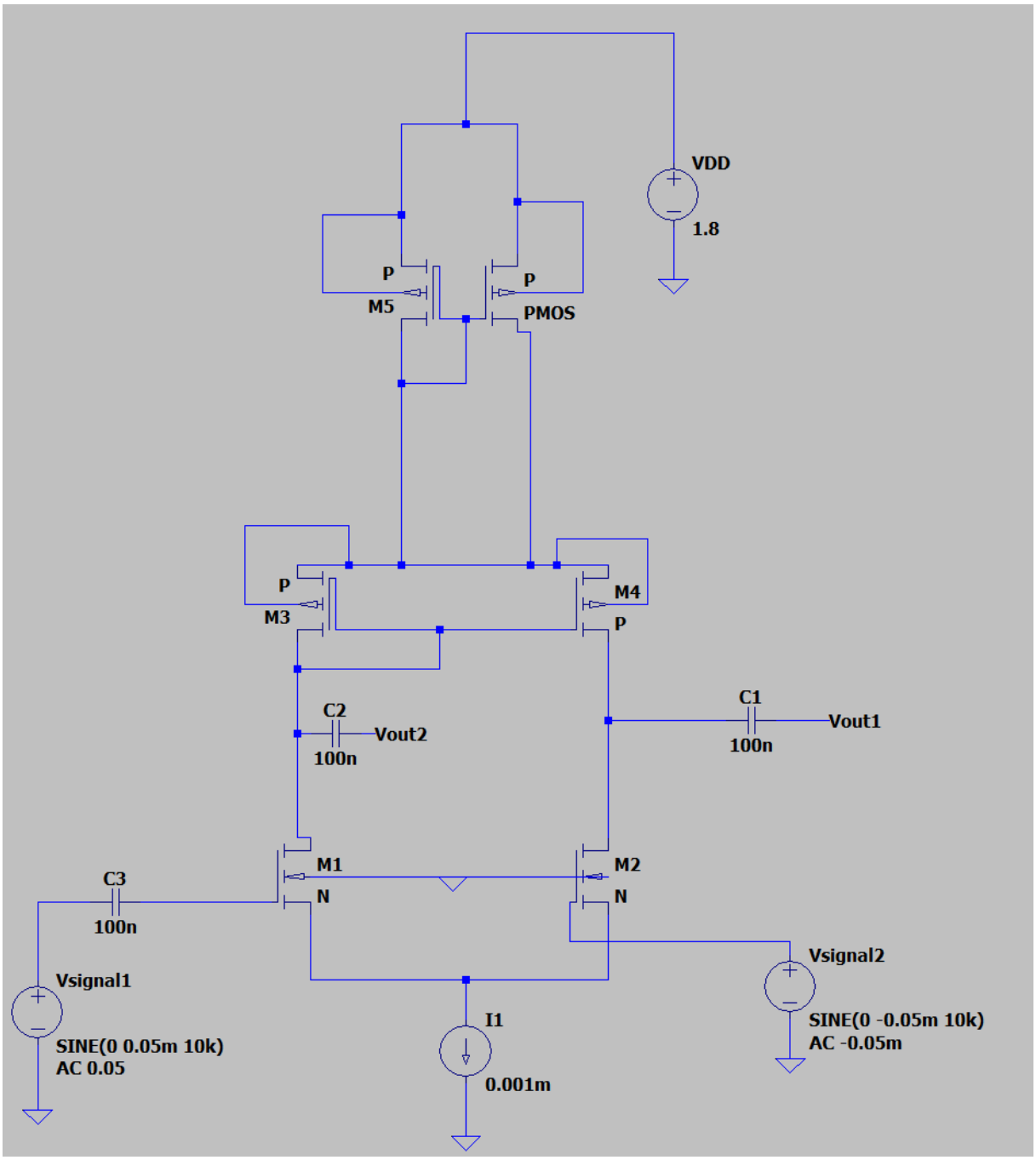


Figure 5.0

Differential gain change (On Figure 5.1) :

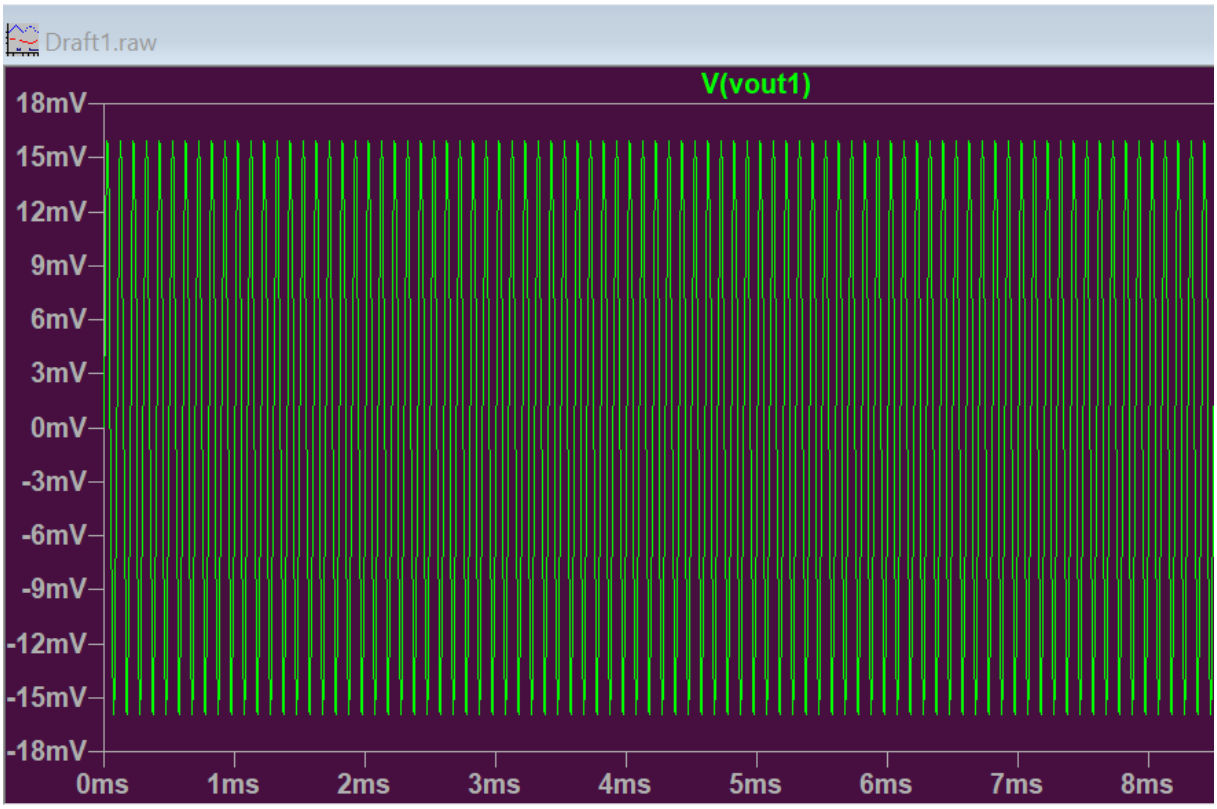


Figure 5.1

The values obtained for the previous circuit have also been determined for the cascode load amplifier and are shown in Table 5.1 and compared basic differential amplifier.

Table 5.1

	Differential Amplifier	Cascode-Load Amp.
A_d	93(v/v)	155(v/v)
CMRR	101dB	136dB
R_{in}	12.5MΩ	14.83MΩ
R_{ou}	7.1kΩ	10.21kΩ
3db bandwith	35Mhz	39Mhz
Unity gain	2.74Ghz	2.81Ghz

By examining Table5.1 , we can see that the cascode load amplifier provides a series of improvements compared to the differential amplifier. The change in each parameter offers important insights into how the design has evolved. Here's the interpretation of the table:

Differential Gain (Ad):

Differential Amplifier: 93 v/v Cascode-Load Amplifier: 155 v/v The cascode structure has increased the gain. The cascode configuration raises the output impedance, thereby enhancing the gain. In this case, the gain has increased by approximately 1.67 times.

CMRR (Common-Mode Rejection Ratio):

Differential Amplifier: 101 dB Cascode-Load Amplifier: 136 dB The cascode structure provides better suppression of common-mode signals. The increase in CMRR ensures the amplifier operates more accurately, as common-mode signals (e.g., noise) are suppressed more effectively. This value has increased by approximately 35 dB.

Input Impedance (Rin):

Differential Amplifier: 12.5 MΩ Cascode-Load Amplifier: 14.83 MΩ The cascode structure has also increased the input impedance. This means less current is drawn, making the amplifier more sensitive.

Output Impedance (Rou):

Differential Amplifier: 7.1 kΩ Cascode-Load Amplifier: 10.21 kΩ The cascode structure has raised the output impedance. This results in better gain and improved accuracy with a higher output impedance.

3 dB Bandwidth:

Differential Amplifier: 35 MHz Cascode-Load Amplifier: 39 MHz A slight increase in bandwidth is observed with the cascode structure. This indicates that the amplifier performs better over a wider frequency range.

Unity Gain Bandwidth:

Differential Amplifier: 2.74 GHz Cascode-Load Amplifier: 2.81 GHz There is also a small increase in unity gain bandwidth. The cascode structure allows the amplifier to operate more effectively at higher frequencies.

Conclusion and Comment:

This project involves the design of a differential amplifier using LTSpice and the implementation of various optimizations. Initially, the gain, common-mode rejection ratio (CMRR), and impedance values of the differential amplifier were determined, and the design was carried out to meet the necessary requirements. The W/L ratios and tail current were optimized, ensuring that the MOSFETs drew less current, which reduced power consumption and allowed the amplifier to operate more efficiently. By adding the cascode load structure, the output impedance and gain of the amplifier were increased, resulting in higher accuracy and stability. The differential gain and CMRR significantly exceeded the targets set at the beginning of the design. Additionally, parameters such as frequency response and bandwidth were also improved. As a result, this project provided valuable insights into basic differential amplifier design and demonstrated how power optimization and high-performance amplifier design can be

achieved. The advantages of the cascode structure led to significant improvements in gain and accuracy, while also increasing the complexity of the design. This project has provided important experience in power optimization and high-efficiency amplifier design using the LTSpice program.

REFERENCES:

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[2]: https://en.wikipedia.org/wiki/Differential_signalling

[3]: https://www.youtube.com/watch?v=ErpKbG7HCG0&t=144s

[4]: https://www.youtube.com/watch?v=_pvlk_SlyDo

[5]: https://www.youtube.com/watch?v=_qKFQ1H_zOI&t=68s

[6]: https://www.youtube.com/watch?v=KvrNSPQ58vA&t=216s

[7]: https://www.youtube.com/watch?v=j4OS3zOqdJg&t=367s