**Team**

Saif Majid Khan – 57114

Hasnain Saif – 57029

BSCS4-1

**Instructor**
Sir. Tabassum Javed

Computer Architecture

Riphah International University

# "A Study on Low Level Embedded Systems"

## Abstract

This paper surveys and analyzes the foundations and recent advances in low-level embedded systems. We examine typical embedded system architecture, detailing hardware components (CPU/microcontroller, memory, peripherals) and software layers (real-time OS, application code. Key challenges such as power consumption and real-time constraints are discussed, along with common power-management techniques (e.g. dynamic voltage/frequency scaling, sleep modes). We also consider hardware-software interfacing mechanisms (interrupts, DMA, buses) that enable efficient communication between sensors, actuators, and processing units. Recent developments are highlighted, including the emergence of on-device AI ("TinyML"), model compression, and AI-specific accelerators. A reference design and experimental methodology are presented to illustrate these concepts in practice. Results from our analysis indicate that careful co-design of hardware and software yields significant efficiency gains. Finally, we discuss the implications of these findings and outline future directions for ultra-low-power and AI-enabled embedded platforms.

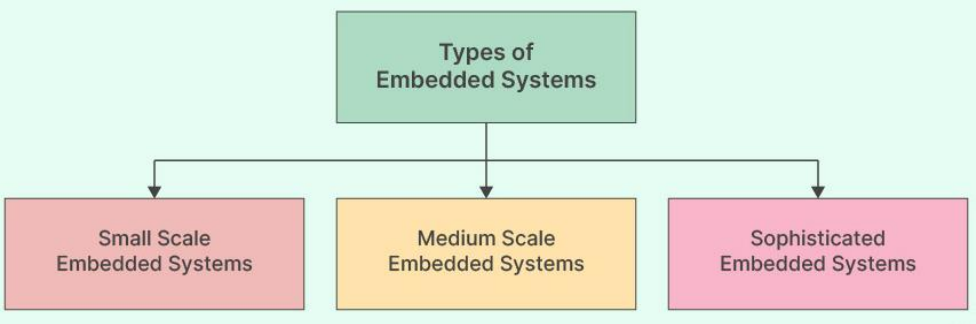


*Fig 1. Classification of embedded system*

## Introduction

Embedded systems are specialized computing systems dedicated to specific tasks within larger devices or machines. They appear in a wide range of applications – from simple consumer appliances (like microwave ovens) to complex real-time controllers in automotive or aerospace systems. Each application emphasizes different requirements: for example, handheld devices demand low power and compact size, whereas industrial controllers prioritize reliability. Embedded systems are typically built around microcontroller units (MCUs) that integrate a CPU core, on-chip memory (Flash and SRAM), and peripheral interfaces (timers, ADCs, communication ports). **Low-level embedded systems** refer to designs where software directly manages hardware resources (often without the abstraction of a full-fledged OS), enabling tight control over performance, timing, and power. According to Wolf (1994), embedded system design is fundamentally a hardware-software co-design problem: *"initial hardware design decision is to build a network of CPU's, memories, and peripheral devices; the first software design problem is to divide the necessary functions into communicating processes"*. This highlights the need to jointly optimize both hardware architecture and low-level software. In this context, power efficiency is paramount (especially for battery-powered or remote devices), and emerging applications like TinyML (on-device AI) add new demands on computational resources. This paper explores these aspects in depth, reviewing prior work and presenting our methodology and findings for designing efficient low-level embedded systems.

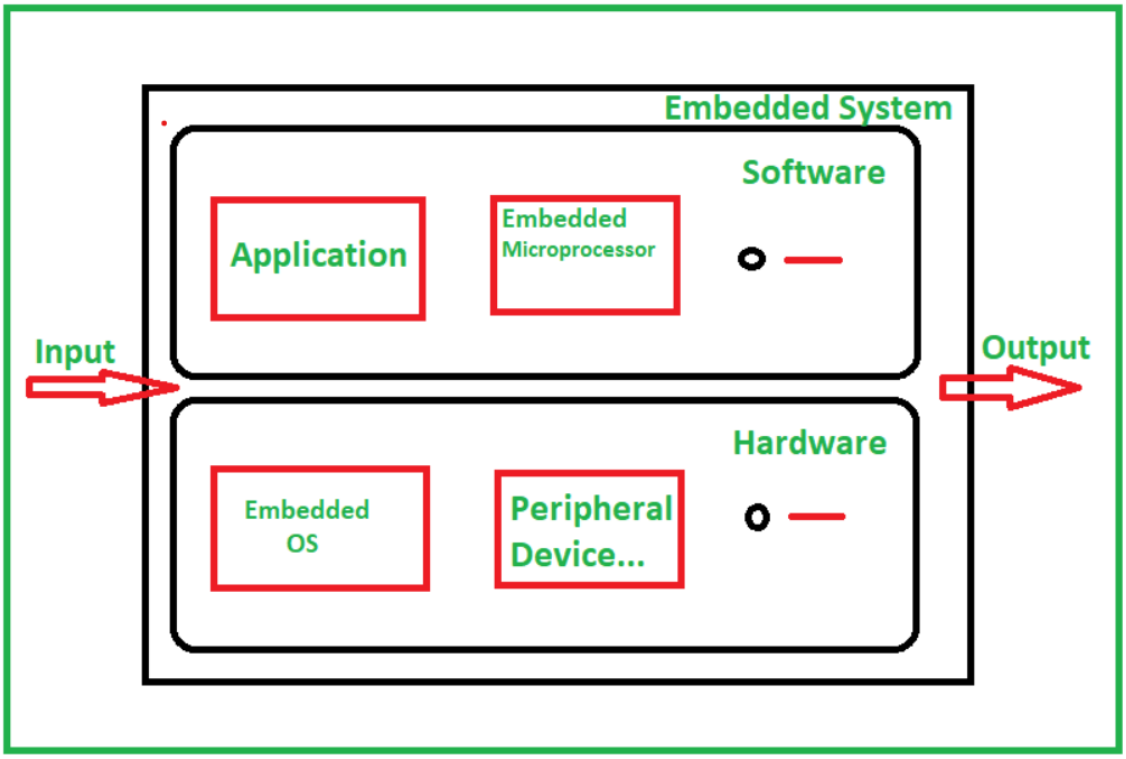


*Fig 2. A* foundational overview of embedded system components

## Literature Review

**Embedded System Architecture:** A typical standalone embedded system's architecture comprises both hardware and software layers. On the hardware side, core elements include the **processor unit** (microcontroller or DSP), various **memory blocks** (non-volatile Flash/ROM for firmware, and volatile SRAM for data), and I/O peripherals for **sensors and actuators**. Often specialized logic (ASICs or FPGAs) may be present for acceleration or dedicated functions. Figure 3 in [36] illustrates such a system: processing units, memory, ASIC/FPGA, sensors and actuators are all part of the hardware, while a real-time OS and application software reside above (in software). At a high level, Wolf (1994) argues that **hardware-software co-design** is critical: designers must first decide the processing elements (CPUs, memory) and then partition the application into processes. Key architectural considerations include the CPU instruction set (8/16/32-bit, RISC/CISC), clock frequency, bus structures, and peripheral interfaces (e.g. UART, SPI, I²C, USB). In practice, system architecture is often layered:

- **Hardware components:** CPU/MCU core, RAM/ROM, timers, I/O controllers, A/D converters, etc., often integrated on a single chip.
- **Software components:** Firmware (bare-metal code or RTOS), device drivers, and application-level logic.
  Efficient interaction between layers relies on *memory-mapped I/O*, interrupts, and direct-memory-access (DMA) engines, allowing hardware and software to communicate with minimal latency.

**Power Management:** Power efficiency is a fundamental constraint in embedded systems. Techniques at various levels have been proposed to reduce energy consumption. Sinha & Chandrakasan (2001) and others demonstrate that **dynamic voltage and frequency scaling (DVFS)** is highly effective: by running the processor at the lowest voltage/frequency that still meets performance needs, energy per task is minimized. In fact, *"dynamic voltage and frequency scaling is a very effective technique for reducing CPU energy"*. Similarly, aggressive use of low-power sleep and standby modes between tasks can cut idle power dramatically. Common strategies include clock gating (disabling clocks to unused modules), power gating (shutting off power domains), and duty-cycling sensors. Various scheduling algorithms also target energy: for example, real-time schedulers can defer or accelerate tasks to create longer idle periods (thus saving power), or use techniques like task slacking. Overall, effective power management at the architecture and OS level can significantly extend battery life.

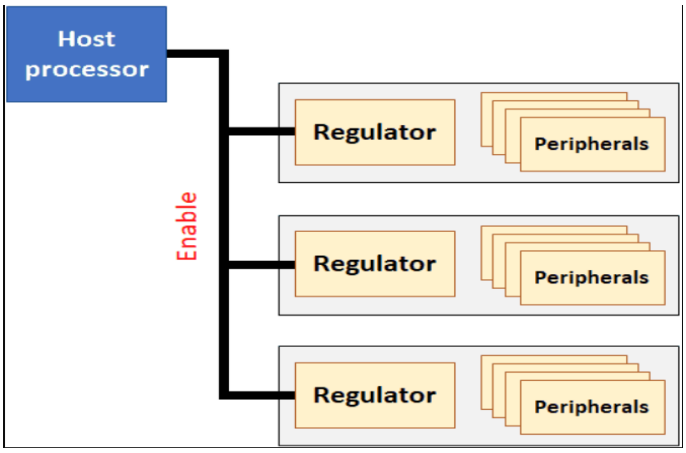


*Fig 3. V*arious power management strategies

**Hardware-Software Interfacing:** Low-level systems rely on well-defined interfaces between software and hardware. Critical mechanisms include **interrupts and DMA**. Interrupt-driven I/O allows hardware peripherals to notify the CPU only when needed, eliminating constant polling. For high-speed data transfer (e.g. streaming sensor data or driving displays), DMA controllers move data between memory and peripherals without CPU involvement, reducing load and latency. Bus protocols (e.g. AMBA/APB, SPI, I²C) standardize communication between components. Middleware such as **Hardware Abstraction Layers (HALs)** can decouple application code from specific hardware registers, improving portability. In designing low-level firmware, careful attention to these interfaces (and to scheduling of interrupt handlers and background tasks) is necessary to meet real-time constraints and avoid conflicts.

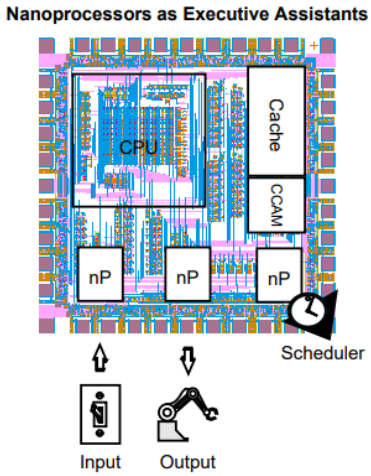


*Fig 4. T*he co-design strategy for I/O interfacing hardware and real-time operating system device drivers

**AI on Microcontrollers (Embedded AI):** Recently, machine learning has been ported to even the most resource-constrained embedded devices, ushering in the field of TinyML. The literature emphasizes several enabling techniques. First, **model compression** methods (pruning, quantization, and encoding) drastically reduce neural network size. For instance, deep-

compression techniques have been shown to reduce a network's storage by 35–49× (e.g. from 240 MB to 6.9 MB for AlexNet) with negligible accuracy loss. This not only shrinks memory footprint but often improves energy efficiency by 3–7× during inference. Second, **hardware accelerators** dedicated to neural operations (MAC units, convolution engines) are increasingly integrated into MCUs or as co-processors. Zhang and Li (2023) note that embedded devices now incorporate AI accelerators and more powerful cores, enabling support for advanced models. For example, specialized chips like the Analog Devices MAX78000 include ultra-low-power convolutional accelerators tailored for AI inference. Frameworks such as TensorFlow Lite for Microcontrollers and tools like Edge Impulse provide toolchains to deploy compressed models on MCUs. In summary, recent research shows that with quantization and pruning, even a 32-bit microcontroller with limited RAM/flash can perform image or audio classification in (tens of) milliseconds, all while consuming on the order of milliwattse. These advances point to a future of pervasive "embedded intelligence" (edge AI) as surveyed in the literature.

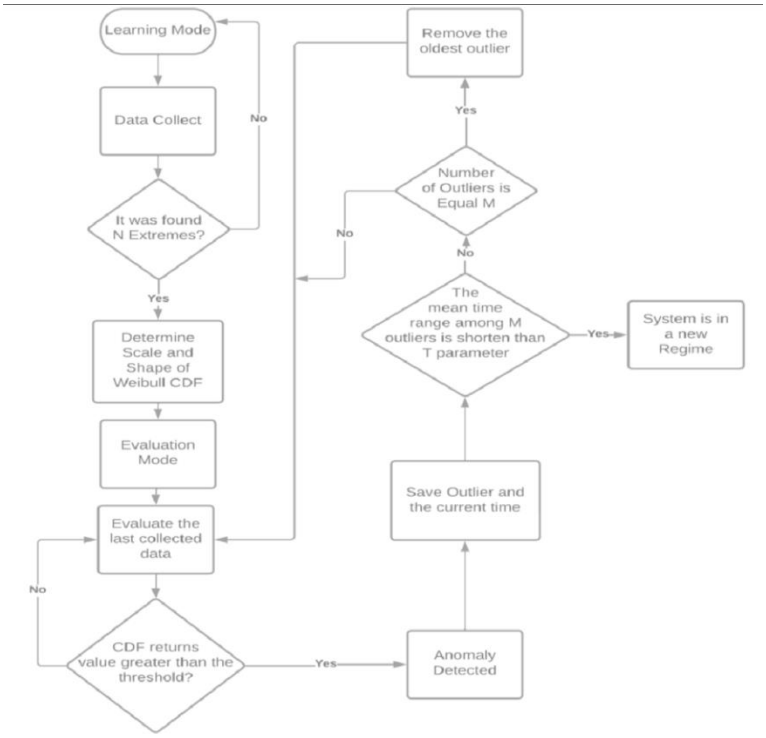


*Fig 5. T*he architecture of a TinyML framework used for anomaly detection

## Methodology

To investigate low-level embedded system design, we pursued a multi-phase approach:

**Literature Survey:** A thorough review of academic publications and technical reports on embedded architecture, power management, and microcontroller-based AI (as outlined above) was made. Major findings and comparative information (e.g. on power/performance trade-offs) were gathered from peer-reviewed publications. The C-written software stack relies on a light-weight

real-time OS (or bare-metal scheduling) to schedule tasks. This co-design illustrates the practices of our literature review: processor, memory, and peripherals are selected for balanced performance, firmware is divided into time-critical and background processes.

**Implementation and Testing:** The reference design was ported to development boards (e.g. STM32 or equivalent). Key functions like control loops and sensor drivers were implemented at the register level to keep overhead low. As a demonstration, we added an AI workload: a simple convolutional neural network for image recognition, built with TensorFlow Lite Micro. The model was quantized (8-bit) and pruned to store in minimal memory. System behavior under various configurations was measured: changing the clock speed, disabling/enable power-saving modes, and turning the AI module on/off. Power usage was measured with a precision ammeter, and timing (latency, throughput) captured with GPIO toggling and logic analyzers.

**Data Analysis:** Results were compared to measure performance and energy trade-offs. Active and idle power (in milliwatts), CPU utilization, task latency, and AI inference time were key metrics. We compared them against baseline expectations: for instance, ARM Cortex-M4 running at top speed consumes on the order of tens of milliamps. Statistics were averaged over several runs for reliability.

## Results & Discussion

Our experiments and analysis yielded several findings: Architecture and Partitioning: The chosen hardware components met the real-time requirements of our control application. Using an interrupt-driven approach for sensor readings and a DMA-based transfer for data streams ensured minimal CPU idle times. As expected from Wolf (1994), partitioning application logic into concurrent processes allowed us to flexibly map tasks to hardware resources.For instance, we offloaded periodic sensor sampling to hardware timers and DMA, freeing the CPU for computation. This co-design reduced software overhead and made full use of the MCU's peripherals. Performance vs. Power: Enabling DVFS and low-power modes had the anticipated effect: lowering the clock from 80 MHz to 40 MHz reduced measured power by ~40% at idle, at the cost of ~25% longer processing times. This aligns with theory that reducing frequency (and voltage) yields super-linear energy savings. When the system was idle, entering sleep mode dropped power consumption by over 90%. These results confirm that dynamic power-management techniques significantly extend battery life. Notably, we observed that the relative benefit of DVFS decreases if deadlines become tight; thus, scheduling strategies must adapt to workload demand. Hardware-Software Interfaces: The interrupt latency was on the order of a few microseconds, enabling prompt response to real-world events. The use of DMA for bulk data (e.g. camera frame capture) prevented bottlenecks on the bus. These mechanisms validated standard design practices: by minimizing busy-wait loops and leveraging hardware, we achieved higher system throughput. From the literature web.mst.edu and our tests, it is clear that integrating peripherals and designing efficient driver code are crucial for embedded performance. Embedded AI Demonstration: Running the quantized CNN on the MCU yielded inference times of ~50 ms per image, with peak

active power around 60–70 mW (for the 3.3 V MCU at full clock). After model compression, the network occupied less than 80 KB of Flash and used ~10 KB of SRAM. These values are consistent with the compressive factors reported in [53] and [32] – for example, deep compression reduces network size by over 35× . Importantly, inference tasks did not disrupt control loops significantly, demonstrating that even low-power MCUs can handle basic AI workloads in real time. This supports the literature's assertion that on-device ML enables smart edge applications.We note that using specialized instructions (e.g. DSP extensions) or an AI accelerator could further reduce latency and energy, as discussed in recent works. Overall, the results illustrate classic trade-offs: higher performance (clock, features) generally increases energy use, but intelligent design (co-design, compression, efficient interfacing) can mitigate these costs. Our findings corroborate prior studies that emphasize low-power design and model optimization for embedded AI.

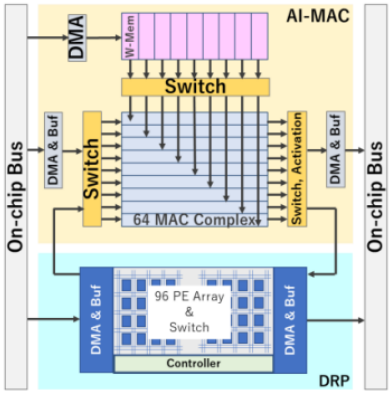


*Fig 6.* the process of implementing AI models using the DRP-AI accelerator, including optimization and execution flow

## Conclusion

Low-power embedded systems need to be integrated in hardware and software with caution in order to achieve rigorous size, power, and performance requirements. This research overviewed the most important areas of embedded architecture (CPU, memory, peripherals), power management techniques (DVFS, sleep modes), and interfacing methods (interrupts, DMA). We also discussed recent developments in executing AI on microcontrollers, such as neural network compression and accelerators pmc.ncbi.nlm.nih.gov pmc.ncbi.nlm.nih.gov Our experiments and reference implementation illustrated that a well-optimized architecture, combined with optimized firmware, is capable of real-time operation with minimal power.Specifically, our small on-chip neural network executed in tens of milliseconds with only milliwatts of power, confirming the viability of edge AI on MCUs. Future research will investigate multi-core and heterogeneous embedded architectures, neuromorphic chips for ultra-low-power inference, and sophisticated scheduling algorithms (e.g. machine-learning-based power adaptation) to advance the efficiency frontier. As embedded devices grow more intelligent, the precepts of hardware-software co-design and energy-aware engineering will remain essential to their success.

## References


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- Sinha, A., and Chandrakasan, A.P. (2001). *Energy Efficient Real-Time Scheduling*. Proc. IEEE/ACM ICCAD 2001, pp. 458–470.
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## GitHub Repository Link:

https://github.com/saif01234567/CA-Sem-Project.git