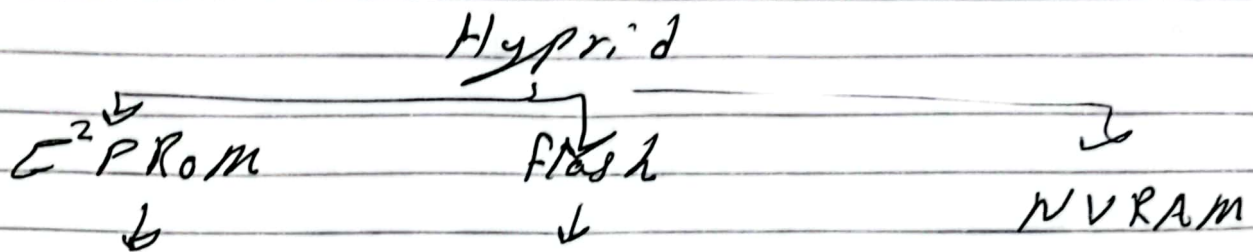
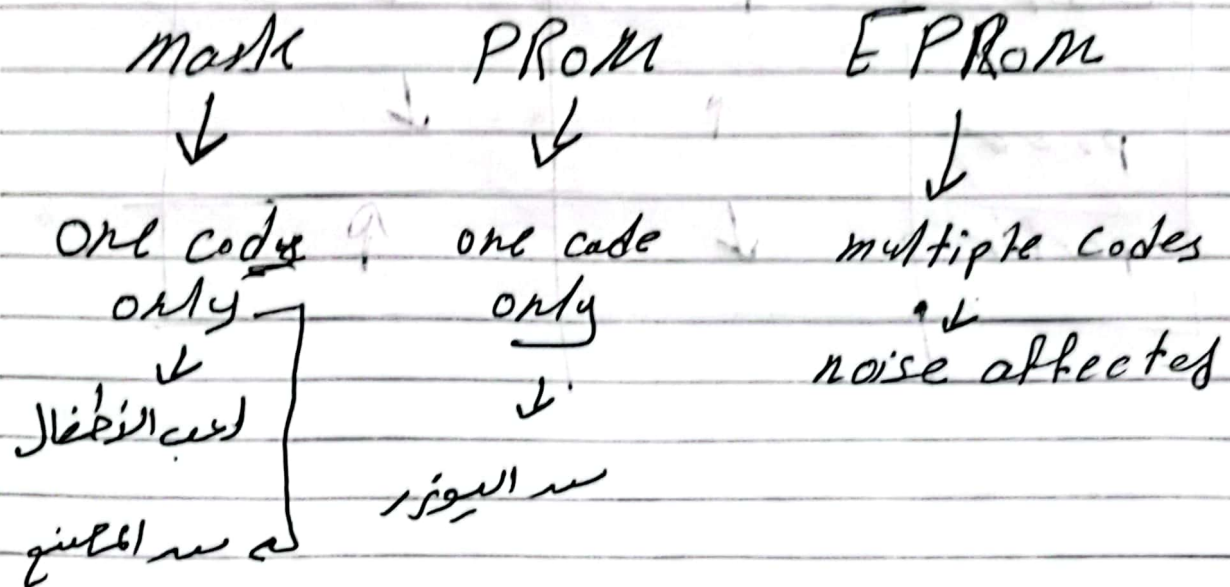


ROM  $\rightarrow$  Read only (Code in there)

$\rightarrow$  Floating gate memory



Electric	$\rightarrow$ more speed	SRAM + Battery
Endurance		SRAM + E²PROM
High cost	- Block access Sector by Sector	+ Battery
	- Low cost	

cache  $\rightarrow$  levels

Register > cache > RAM > HDD  
files

size  $\rightarrow$   
 $\leftarrow$  speed increase

- FPU  $\rightarrow$  floating point unit
- MPU  $\rightarrow$  Memory protection unit
- MMU  $\rightarrow$  Memory management unit

ARCH

Von-Neumann

Harvard



memory mapped

Support  
pipeline

doesn't support  
pipeline

Port  
mapped

One memory  
system

Date : \_\_\_\_\_

No: \_\_\_\_\_

	RC	CR	CO
cost	↓	—	↓
Accuracy	↓	—	↓
Temp	↓	↑	↑
Gmi	↓	↑	↑
vibr	↑	↓	↓
Setting time	↑	—	↓