Saif Khattak

Overview

2 years of full-time experience working on industry-strength compilers.
Seeking opportunities to tackle challenging problems in the efficient planning of highly parallel workloads.

Work Experience

June 2024 - Ongoing
SQL Compiler Engineer, *Snowflake*, San Mateo CA
Compiler Platform Team

- Maintained and improved the quality of Snowflake's **SQL compiler**, which executes over 6 billion queries a day. Participated in a support rotation that involved triaging and resolving customer issues.
- Overhauled dozens of **compiler optimization passes** using a new internal compiler framework as part of a multi-quarter effort to improve compilation time and reduce the rate of hard-to-diagnose errors.
- Diagnosed query planning issues that resulted in poor performance in Snowflake's **parallel execution architecture**, such as cardinality misestimation or late filtering.
- Designed a mechanism to serialize query metadata into a **Protobuf** message as part of a project to create an API for the compiler, with the aim of improving extensibility.

Data Governance Team

- Led a project to design **new SQL syntax** enabling the application of multiple policies on a table, eliminating boilerplate code and reducing likelihood of human error when applying privacy constraints.
- Designed algorithms to enforce Join Policy semantics on the parse tree of a SQL query, reducing the manual effort required to sanitize data before sharing.
- Designed optimizations on query execution plans to increase the query flexibility while maintaining privacy guarantees, reducing the amount of rewriting required for a query to satisfy constraints.

Aug 2023 - June 2024
FPGA Compiler Engineer, *Intel*, Toronto ON

- Enabled users to generate an Avalon-based **RTL** interface for compute kernels specified in **SYCL**.
- Created an FPGA-specific **LLVM** optimization pass in **C++** that improved performance by 15% on a standard **OpenCL** benchmark suite, by using scalar evolution analysis to narrow induction variables.
- Debugged complex issues across the hardware-software boundary, including investigating compiled binaries, LLVM IR, OpenCL runtime libraries, Quartus compilation pipelines, Modelsim simulations, and HAL functionality.

Jan 2022 - Apr 2022
ML Compiler Engineer (Co-op), *Groq*, Toronto ON

- Increased neural network inference throughput by up to 20% by designing algorithms in **C++** to efficiently utilize hardware resources for common tensor operations (e.g. convolutions).
- Created optimization passes in **C++** using the **MLIR** compiler framework to manipulate neural networks described in **ONNX** format.
- Created machine learning models in **PyTorch** to run end-to-end compiler tests and measure cycle-accurate performance when run on custom neural network accelerator hardware.

Education

Sep 2018 - Apr 2023
University of Waterloo, *Computer Engineering B.A.Sc*, Waterloo ON
Graduated with distinction.

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