Saif Khattak

Overview

2+ years of experience in the acceleration of SQL queries and FPGA compilation.

Aiming to bridge the gap between the theoretically and practically computable.

Work Experience

June 2024 - Ongoing

SQL Compiler Engineer, *Snowflake*, San Mateo CA

Compiler Platform Team
- Architected migration of 20+ compiler stages to new expression framework, enabling feature teams to focus on **what** optimizations to implement rather than **how** to integrate them, improving compilation performance by 10-15% and reducing system incident rate by 100x across 6B daily queries.
- Served as cross-functional technical consultant, democratizing access to compiler expertise across teams previously blocked by low-level framework complexity.
- Participated in quarterly support rotation, triaging and resolving 40-50 customer issues weekly in 3-person team covering query performance degradation, correctness bugs, and compilation failures across the full execution stack.

Data Governance Team
- Led a project to design **new SQL syntax** enabling the application of multiple policies on a table, eliminating boilerplate code and reducing likelihood of human error when applying privacy constraints.
- Designed algorithms to enforce Join Policy semantics on the parse tree of a SQL query, reducing the manual effort required to sanitize data before sharing.
- Designed optimizations on query execution plans to increase the query flexibility while maintaining privacy guarantees, reducing the amount of rewriting required for a query to satisfy constraints.

Aug 2023 - June 2024

FPGA Compiler Engineer, *Intel*, Toronto ON

- Enabled domain experts to describe compute kernels in high-level **SYCL** while automatically generating optimized **RTL** interfaces, democratizing access to reconfigurable hardware acceleration.
- Created an FPGA-specific **LLVM** optimization pass in **C++** that improved performance by 15% across standard **OpenCL** benchmarks by using scalar evolution analysis to narrow induction variables.
- Debugged complex issues across the hardware-software boundary, building expertise in the full compilation stack from high-level code to hardware implementation.

Jan 2022 - Apr 2022

ML Compiler Engineer (Co-op), *Groq*, Toronto ON

- Bridged the gap between ML researchers' high-level **ONNX** models and specialized hardware execution, enabling 20% throughput improvements through automated resource utilization algorithms for tensor operations.
- Created optimization passes in **C++** using the **MLIR** compiler framework, applying cross-domain compilation techniques to neural network acceleration.
- Built end-to-end validation pipeline in **PyTorch**, enabling rapid iteration between algorithmic improvements and hardware performance measurement.

Education

Sep 2018 - Apr 2023

University of Waterloo, *Computer Engineering B.A.Sc*, Waterloo ON
Graduated with distinction.