Work Experience

Aug 2023 - FPGA Compiler Engineer, Intel, Toronto ON

- Ongoing O Designed a feature to generate Avalon-based RTL interface for compute kernels that includes registers to control and monitor hardware interrupts, ensuring usability for customers developing device drivers by engaging with FAEs for early feedback
 - Created and troubleshooted FPGA-specific LLVM loop optimization passes in C++ to improve throughput and area usage for user designs written in SYCL and OpenCL, improving performance by 15% on a user benchmark suite
 - Debugged complex issues across the hardware-software boundary, including investigating compiled binaries, LLVM IR, OpenCL runtime libraries, Quartus compilation pipelines, Modelsim simulations, and HAL functionality

Sep 2022 - Software Engineering Co-op, Snowflake, San Mateo CA

- Dec 2022 O Developed data privacy features at the SQL query engine level for Snowflake's cloud database platform
 - O Added rules to an ANTLR 3 grammar to enable managing data aggregation policies in SQL, enabling customers to share data while maintaining their users' privacy
 - O Implemented compiler changes in Java to parse and generate code for applying policies to a table
 - Implemented changes to a custom FoundationDB layer to store information about policies

Jan 2022 - Compiler Engineering Co-op, Groq, Toronto ON

- Apr 2022 O Increased neural network inference throughput by up to 20% by designing algorithms in C++ to efficiently utilize hardware resources for common tensor operations (e.g. convolutions)
 - Created optimization passes in C++ using the MLIR compiler framework to manipulate neural networks described in **ONNX** format
 - O Created machine learning models in PyTorch to run end-to-end compiler tests and measure cycleaccurate performance when run on custom neural network accelerator hardware

Jan 2020 - Software Engineering Co-op, RadComm Systems, Oakville ON

- Aug 2020 O Researched cutting-edge radiation analysis techniques using GNU Octave and Python for data visualization to assess development options
 - Implemented algorithms in C# to analyze radiation patterns using the ReactiveX library to handle real-time data emitted by an embedded device, processing energy histograms every 100ms
 - Automated the device calibration process using C# to allow parallel setup of many devices

Projects

May 2022 - Bayesian Network Inference Accelerator, Scala — Chisel — Python — Verilog

- Dec 2022 O Created a compiler in Scala to convert Bayesian network specifications into a Verilog module that can answer queries on the network with real-time evidence based on Markov-Chain Monte-Carlo techniques
 - Created Protobuf-based specifications for model description and elaboration
 - Created language for expressing Bayesian networks parsed using an ANTLR 4 grammar
 - O Utilized Chisel to construct hardware modules dynamically and generate RTL for various backends

Feb 2022 - CHIP-8 Emulator, C++ — SDL2 — ImGUI

- Mar 2022 O C++ interpreter for CHIP-8 instruction set, runs publicly available ROMs
 - Includes graphical and audio interface using the SDL2 library
 - Implemented an assembler and disassembler to enable troubleshooting
 - Designed live debugger using ImGUI to inspect memory dumps and processor state

Education

Sep 2018 - University of Waterloo, Computer Engineering B.A.Sc, Waterloo ON

Apr 2023 Cumulative average 92%

- O Degree honours: Dean's honours list, graduated with distinction
- Scholarships and awards
 - President's Research Award
 - Savvas Chamberlain Scholarship