# Saif Khattak

## Work Experience

Jan. 2022 - Apr. 2022 **Compiler Engineering Intern**, *Groq Inc.*, Mississauga ON (remote)
- Designed and implemented algorithms to efficiently utilize hardware resources for common tensor operations (e.g. convolutions), increasing inference throughput by up to 40%
- Created optimization passes in **C++** using the **MLIR** compiler framework to manipulate neural networks described in the **ONNX** format
- Created machine learning models in **PyTorch** to run end-to-end compiler tests and measure cycle-accurate performance when run on custom hardware

Jan. 2020 - Aug. 2020 **Software Engineering Co-Op**, *RadComm Systems*, Oakville ON
- Researched cutting-edge radiation detection techniques using **GNU Octave** and **Python** for data visualization to assess development options
- Implemented algorithms in **C#** to analyze radiation patterns using the **ReactiveX** library to handle real-time data emitted by an embedded device
- Automated device calibration process using **C#** to allow parallel setup of many devices

Sep. 2020 - Dec. 2020 **Undergraduate Research Assistant**, *University of Waterloo*, Waterloo ON
- Wrote **C** implementation of novel post-quantum cryptographic algorithms
- Implemented cache-aware optimizations resulting in 60% speed improvement
- Created custom boolean matrix library for use in cryptographic algorithms

May 2019 - Aug 2019 **Secure Software Developer**, *ESCRYPT*, Waterloo ON
- Implemented asynchronous process in **C++** for periodically provisioning digital certificates on-vehicle, improving anonymity in the system by enabling certificate swapping
- Wrote ETSI-compliant tests using **GoogleTest** framework to prove functionality

## Projects

May 2022 - Aug. 2022 **Bayesian Network Accelerator**, Python — VHDL — Chisel
- Created hardware design for inference over a Bayesian network leveraging parallelism, efficient discrete sampling algorithms, and Markov-Chain Monte-Carlo methods (e.g. likelihood weighting)
- Created **protobuf**-based specifications for model description and elaboration
- Implemented compiler in **Python** to analyze models and emit VHDL for accelerator

Feb. 2022 - Mar. 2022 **CHIP-8 Emulator**, C++ — SDL2 — ImGUI
- **C++** interpreter for CHIP-8 instruction set, runs publicly available ROMs
- Includes graphical and audio interface using **SDL2**
- Designed live debugger using **ImGUI** to inspect memory dumps and processor state

Dec. 2021 - Jan. 2022 **3D Rasterized Render System**, C++ — CMake — OpenGL
- 3D rasterized rendering system written with **OpenGL 3.3** in **C++17**
- Implements mesh generation, texture loading and phong lighting shaders
- Allows model loading from common file types based on the **Assimp** library

Sep. 2021 - Nov. 2021 **Pipelined 32-Bit RISC-V Core**, Verilog — Verilator
- Implements RV32I spec; written from scratch in **Verilog**, simulated using **Verilator**
- Wrote **Python** script to run standardized RV32I instruction and benchmark tests

## Education

Sep. 2019 - Apr. 2023 (expected) **University of Waterloo**, *Candidate for Computer Engineering B.A.Sc*, Waterloo ON

Relevant coursework and projects in:

- Computer Architecture
- FPGAs
- ARM & RISC-V ISAs
- Operating Systems
- Compilers
- Reinforcement Learning
- Digital VLSI
- Computer Security
- Digital Signal Processing

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