
Overview

2+ years of experience optimizing highly parallel workloads across databases, FPGAs, and ML accelerators.

Work Experience

June 2024 - **SQL Compiler Engineer**, *Snowflake*, San Mateo CA

Ongoing *Compiler Platform Team*

- Rearchitected 20+ compiler stages that are collectively run by 17M+ daily queries as part of a migration to a new expression framework.
- Engineered large-scale workload validation strategies to roll out migrated compiler stages, ensuring zero regressions across all 6B+ daily customer queries.
- Resolved 40-50 customer escalations per week during support rotations, triaging and resolving issues with query performance degradation, correctness bugs, and compilation failures across the full stack.

Data Governance Team

™Led design of new SQL syntax enabling multiple policies on a table, reducing boilerplate and preventing errors in applying privacy constraints. Designed algorithms to enforce Join Policy semantics on the parse tree of a SQL query, enabling data sharing for over 3000 tables while preserving sensitive information. Designed optimizations on query execution plans to increase query flexibility while maintaining privacy guarantees provided by aggregation policies, which protect over 80,000 tables in production.

Aug 2023 - **FPGA Compiler Engineer**, *Intel*, Toronto ON

- June 2024
- Enabled the compilation of compute kernels in high-level **SYCL** code to pipelined **RTL** implementations for Intel FPGAs.
 - Created an FPGA-specific **LLVM** optimization pass in **C++** that improved performance by 15% across standard **OpenCL** benchmarks by using scalar evolution analysis to narrow induction variables.
 - Debugged complex issues across the hardware-software boundary, building expertise in the full compilation stack from high-level code to hardware implementation.

Jan 2022 - **ML Compiler Engineer (Co-op)**, *Groq*, Toronto ON

- Apr 2022
- Designed optimizations for the execution of **ONNX** models on custom hardware, enabling up to 20% throughput improvements by efficient packing of tensor operations.
 - Created optimization passes in **C++** using the **MLIR** compiler framework, applying cross-domain compilation techniques to neural network acceleration.
 - Built end-to-end validation pipeline in **PyTorch**, enabling rapid iteration between algorithmic improvements and hardware performance measurement.

Education

Sep 2018 - **University of Waterloo**, *Computer Engineering B.A.Sc*, Waterloo ON

Apr 2023 Graduated with distinction.