

## Work Experience

- Aug 2023 - **FPGA Development Tools Engineer**, *Intel PSG*, Toronto ON  
Ongoing
  - test
  - test
  - test
- Sep 2022 - **Software Engineering Intern**, *Snowflake*, San Mateo CA  
Dec 2022
  - Added rules to **ANTLR 3** grammar to enable managing data privacy policies in SQL
  - Implemented compiler changes in **Java** to parse and generate code for applying policies to a table
  - Implemented changes to custom **FoundationDB** layer to store information about policies
- Jan 2022 - **Compiler Engineering Intern**, *Groq*, Toronto ON  
Apr 2022
  - Increased neural network inference throughput by up to 40% by designing algorithms in **C++** to efficiently utilize hardware resources for common tensor operations (e.g. convolutions)
  - Created optimization passes in **C++** using the **MLIR** compiler framework to manipulate neural networks described in **ONNX** format
  - Created machine learning models in **PyTorch** to run end-to-end compiler tests and measure cycle-accurate performance when run on custom neural network accelerator hardware
- Jan 2020 - **Software Engineering Co-Op**, *RadComm Systems*, Oakville ON  
Aug 2020
  - Researched cutting-edge radiation analysis techniques using **GNU Octave** and **Python** for data visualization to assess development options
  - Implemented algorithms in **C#** to analyze radiation patterns using the **ReactiveX** library to handle real-time data emitted by an embedded device, processing energy histograms every 100ms
  - Automated the device calibration process using **C#** to allow parallel setup of many devices

## Projects

- May 2022 - **Bayesian Network Acceleration Compiler**, Scala — Chisel — Python — Verilog  
Dec 2022
  - Created compiler in **Scala** to convert Bayesian network specifications into a **Verilog** module that can answer queries on the network with real-time evidence based on Markov-Chain Monte-Carlo techniques
  - Created **Protobuf**-based specifications for model description and elaboration
  - Created language for expressing Bayesian networks parsed using an **ANTLR 4** grammar
  - Utilized **Chisel** to construct hardware modules dynamically and generate various RTL backends
- Feb 2022 - **CHIP-8 Emulator**, C++ — SDL2 — ImGUI  
Mar 2022
  - **C++** interpreter for CHIP-8 instruction set, runs publicly available ROMs
  - Includes graphical and audio interface using the **SDL2** library
  - Designed live debugger using **ImGUI** to inspect memory dumps and processor state
- Dec 2021 - **3D Rasterized Render System**, C++ — CMake — OpenGL  
Jan 2022
  - 3D rasterized rendering system written with **OpenGL 3.3** in **C++17**
  - Implemented mesh generation, texture loading and Phong lighting shaders
  - Enabled loading models from common file types based on the **Assimp** library

## Education

- Sep 2018 - **University of Waterloo**, *Candidate for Computer Engineering B.A.Sc*, Waterloo ON  
Apr 2023 Cumulative average **92%**. Relevant coursework and projects in:
  - Computer Architecture
  - Operating Systems
  - Digital VLSI
  - FPGAs
  - Compilers
  - Computer Security
  - ARM & RISC-V ISAs
  - Reinforcement Learning
  - Digital Signal Processing