National University of Sciences & Technology (NUST)
School of Electrical Engineering and Computer Science (SEECS)
Department of Electrical Engineering

Computer Architecture and Organization

Course Code:	EE-321	**Semester:**	Spring 2015
Credit Hours:	3+1	**Prerequisite Codes:**	Digital Logic Design
Instructor:	Taufique-ur-Rehman	**Discipline:**	Electrical Engineering
Office:	Room: A-206, Faculty Block	**Telephone:**	+92 (0)51-9085-2160
Lectures: **Labs:**	Monday, Tuesday, Wednesday Thursday	**E-mail:**	taufique.rehman@seecs.edu.pk
Class Room:	CR-5 SEECS	**Consulting Hours:**	Section A Wednesday 1500-1600, Section B Monday 1000-1100
Knowledge Group:	DSSP	**Updates on LMS:**	Every Week

Course Description:

This course will focus on the principles, current practices, and issues in computer architecture and organization. Students will be introduced to the understanding of computer organization: roles of processors, main memory, and input/ output devices. Understanding simple data path and control designs for processors. Understanding memory organization, including cache structures and virtual memory schemes. Understanding parallel processing and multi-core computers.

Course Objectives:

- A complete understanding of program execution
- Understanding of computer functional components, their characteristics, their performance and their interactions
- Understanding of computer architecture so to run programs more efficiently
- Practical use of microcontroller for embedded systems

Course Learning Outcomes (CLO)

	Upon successful completion of this course the students will be able to demonstrate the following:-	PLO	BT LEVEL*
1	**Understand** the function of major components of computer systems.	1	C-2,3
2	**Analyze** the internal architecture and organization of the processor.	2	C-4
3	**Validate** the underlying theoretical concepts of computer architecture and organization through simulation	5	P-4
* BT=Bloom's Taxonomy, C=Cognitive domain, P=Psychomotor domain, A=Affective domain			

Mapping of CLOs TO Program Learning Outcomes

PLOs/ CLOs	Level of Emphasis of PLO (1: High 2:Medium 3: Low)	CLO-1	CLO-2	CLO-3	CLO-4	CLO-5
PLO 1 (Engineering Knowledge)	2	√	√		√	
PLO 2 (Problem Analysis)	1			√		
PLO 3 (Designing/Development of Solutions)	3					
PLO 4 (Investigation)	3					
PLO 5 (Modern tool usage)	1					√
PLO 6 (The Engineer and Society)	3					
PLO 7 (Environment and Sustainability)	3					
PLO 8 (Ethics)	3					
PLO 9 (Individual and Team Work)	3					
PLO 10 (Communication)	3					
PLO 11 (Project Management)	3					
PLO:12 (Lifelong Learning)	3					

Mapping of CLOs to Assessment Modules and Weight ages (in accordance with NUST statutes)

To be filled in at the end of the course

CLOs\PLOs	CLO-1	CLO-2	CLO-3	CLO-4	CLO-5
Quizzes: (9%)					
Assignments: (4.5%)					
Class Participation: (1.5%)					
OHT-1: (12%)					
OHT-2: (12%)					
Labs: (17.5%)					
Lab Test: (7.5%)					
End Semester Exam: (36%)					
Total: 100%					

Books:

Text Book: William Stallings, Computer Organization and Architecture, Eighth/Ninth Edition, Prentice Hall.

Reference Books:

1. *Computer System Architecture* Third edition By M. Morris Mano
2. *The Intel Microprocessors* Sixth Edition By Barry B. Brey
3. *Computer Architecture : A Quantitative approach* fifth Edition By Hennessy, Patterson
4. *Computer Organization and Design The Hardware/Software interface* Fourth edition By Hennessy, Patterson

Main Topics to be Covered:

1 – Introduction
2 – Computer Evolution/Performance
3 – Computer Memories, Cache Memory, Internal Memory, External Memory
4 – Instruction Sets: Addressing modes, Formats, Functions
5 - Processor Structure & Function : Instruction cycle, pipelining
6 - RISC
7 - Instruction Level Parallelism and Superscalar Processors
8 - Parallel Processing
9 - Multicore Computers

Lecture Breakdown:

Week No	Lecture	Topics	Text Book Reference	Other References	Remarks
1.	**1.**	Introduction to title of course and Faculty's experience	1.1		
	2.	Introduction and Motivation to the course			
	3.	Course Policies and Computer Structure		.	
	Lab 01	LabVolt Trainer Familiarization			
2.	4.	Top Level view of Computer Function	1.2		
	5.	Instruction Cycle, Interrupts	3.2		
	6.	Input Output Function	3.2		
	Lab 02	LabVolt Trainer Familiarization			
3.	**7.**	Elements of Bus Design	3.4		
	8.	QPI, PCIe bus	3.5, 3.6		
	9.	PCIe bus, Cache Memory	3.6, 4.1		
	Lab 03	Bus Operations			

4.	10	Memory Heirarchy	4.2		
	11	Cache Memory Direct Mapping	4.3		
	12.	Cache Memory Direct Mapping	4.3		
	Lab 04	Read and Write Cycles			
5.	13.	Cache Memory Mapping Fully Associated and Set Associative mapping	4.3		
	14.	Replacement Algorithms, Other Cache characteristics	4.3		
	15.	Other Cache characteristics, Pentium and ARM CPU architecture	4.4, 4.5		
	Lab 05	Declaration and Manipulation of Variables in Assembly Language			
6.	**OHT-1**				
7.	16.	Internal Memory	5.1		
	17.	Internal Memory Organization	5.1		
	18.	Correction Codes, Advanced Memory Architectures	5.2		
	Lab 06	Flag and Jump Commands in Assembly Language			
8.	19.	External Memory	6.1		
	20.	RAID System	6.2		
	21.	SSD, Optical drives and Tapes	6.3		
	Lab 07	Write a program for searching a data within an array			
9.	22.	I/O Modules, Programmed I/O	7.1, 7.2, 7.3		
	23.	Interrupt Driven I/O	7.4		
	24.	Direct Memory Access	7.5		

	Lab 08	Write a program to make a simple calculator program			
10.	25.	I/O Channels and Processors	7.6		
	26.	Thunderbolt and Infiniband	7.7		
	27.	Machine Instructions	12.1		
	Lab 09	Write a program to display the input number on the standard display without using the library integer display procedure			
11.	28.	Type of Operands and Operations	12.2, 12.3		
	29.	Addressing Modes	13.1		
	30.	Processor Organization, Register Organization	14.1, 14.2		
	Lab 10	Floating Point Numbers			
12.	**OHT-2**				
13.	31.	Instruction Cycle	14.3		
	32.	Instruction Pipelining	14.4		
	33.	Pipelining Hazards	14.4		
	Lab 11	Array sorting of Floating Point Numbers			
14.	34.	Pipelining Design	14.4		
	35.	MIPS Processor Organization	15.6		
	36.	MIPS Datapath Design	15.6		
	Lab 12	Write a program for 8051 microcontroller that turns on LEDs			
15.	37.	MIPS Control Design	15.6		
	38.	Instruction Level Parallelism	16.1		
	39.	Instruction Level Parallelism Design Issues	16.2		
	Lab 13	Write a program for 8051 microcontroller			

		that turns on an LEDs using interrupt			
16.	40.	Multiple Processor Organizations	17.1, 17.2		
	41.	Cache Coherence and MESI Protocol	17.3		
	42.	Hardware and Software Issues	18.1, 18.2		
	Lab 14 : Lab Test				
17.		Multicore Organization	18.3		
		Revision			
		Revision			
	Lab 15 : Lab Test				
18.	**End Semester Exam**				

Lab Experiments:
Lab 1 &2 : LabVolt Trainer Familiarization
Lab 3: Bus Operations
Lab 4: Read and Write Cycles
Lab 5: Declaration and Manipulation of Variables in Assembly Language
Lab 6: Declaration and Manipulation of Variables in Assembly Language
Lab 7: Write a program for searching a data within an array
Lab 8: Write a program for searching a data within an array
Lab 9: Write a program to display the input number on the standard display without using the library integer display procedure
Lab 10: Floating Point Numbers
Lab 11: Array sorting of Floating Point Numbers

Lab 12: Write a program for 8051 microcontroller that turns on LEDs
Lab 13: Write a program for 8051 microcontroller that turns on an LEDs using interrupt
Lab 14 & 15 : Lab Tests

Grading Policy:	
Quizzes Policy	The quizzes are a mandatory component of the overall assessment. The purpose of quizzes is to keep the students up-to-date with the lecture material and test basic understanding of the course concepts. There will be at least **6** unannounced quizzes conducted in the class any time during the lecture. Each quiz will consist of questions that target specific topics from the most recent as well as previous week lectures.
Assignments	In order to give sufficient practice and comprehensive understanding of the subject assignments will be given, on submitting you have to declare that which questions you attempted yourself. The evaluated assignment is an individual effort and no hints will be posted on forum. Only declared questions by individual student will be evaluated. If the declared question done by you is found a copy of other then you may loose all the marks in assignments and get zero in assignments category. The questions in assignments will be challenging to give students the confidence and enable them to prepare for the exams well. Home works will be submitted at the beginning of class on the due date. The students are advised to do the assignment themselves. Copying of assignment is highly discouraged, taken as cheating case and dealt accordingly. Late submissions will also loose marks.
Conduct of Labs	The labs will be conducted for three hours each week. For the conduct of lab the students will be divided into groups with 2 students per group. A lab handout comprising pre-lab, in-lab, and post-lab report parts will be provided to students for study and analysis during the week preceding each lab session. The students are expected to complete pre-lab work before lab starts and also come prepared for the lab. Any student failing to complete pre-lab will not be allowed to attend lab session. The students will be evaluated during each lab on the basis of demonstration, oral viva, and lab report submitted by them individually on completion of lab work. The students are required to be punctual in the lab; latecomers will not be allowed in the lab. No make-up provisions for the missed labs. Each lab is evaluated by Lab Engineer by taking a Lab Quiz and lab report. A comprehensive lab test will be arranged during closing weeks of semester and students will be individually evaluated accordingly.
Other Matters	
Academic Honesty and Plagiarism	Plagiarism is the unacknowledged use of other's work, including the copying of Assignments and laboratory results from the other students. Plagiarism is considered a serious offence by the university and severe penalties apply. Therefore, all the students must display originality of efforts and avoid plagiarism in any form.
Classroom Etiquettes	It is the collective responsibility of all the students to make the class environment conducive for learning. To create and maintain a friendly atmosphere, the following standards of class room behavior will be observed:-

	1. Students will be punctual for the class. The teacher considers late comers disrespectful of those who manage to be on time. 2. If a student decides to attend the class, he or she will not disrupt class by leaving before the lecture has ended. 3. All the cell phones must be switched OFF prior to entering the class room.
Tools / Software Requirement:	
	1. The Microsoft Macro Assembler (MASM) is used for programming in assembly language. Microcontroller 8051 is used for implementation. 2. Control System lab will be used for hands on practice.

Forum for Communication and Addressing any Questions & Answers:

- **For online discussions among students and Faculty Piazza forum is used. The students are encouraged to ask any questions related to the course for better learning value of the subject. Following link is used for the forum.**
- **https://piazza.com/seecs.edu.pk/spring2015/ee321/home**
- **The students are required to register on above link and use it for addressing any question or discussion or for polling for an opinion.**
- **Please participate on course discussion forum. Your participation in the forum will be evaluated.**

Facebook Group Page for more interactivity

- **Enable you to give question/answers or share any material with the group members. Following link is used for the group page.**
- **https://www.facebook.com/groups/386103158236151/**
- **You may opt to participate on course discussion group.**

Online Consultation through Skype

- **You can discuss any question related to the course in allocated online consultation hours. Besides the consultation hours you can take an appointment through email.**
- **Skype ID : teacher.nasir**

Online Consultation through google hangout

- **You may interact and discuss any question or clarify your concepts by hosting a google hangout meeting with your teacher or class mates.**
- **Faculty email : nasirm15@gmail.com**

BEST OF LUCK FOR INDEPTH LEARNING OF THE SUBJECT KNOWLEDGE