National University of Sciences & Technology (NUST)
School of Electrical Engineering and Computer Science (SEECS)
Department of Electrical Engineering

Digital Logic Design

Course Code:	EE221	**Semester:**	Spring 2015
Credit Hours:	3+1	**Pre-requisites:**	Nil
Instructor:	Dr. Ammar Hasan	**E-mail:**	arshad.nazir@seecs.edu.pk
Office:	Room A-215, Faculty Block	**Telephone:**	+92 (0)51 9085 2112
Students Batch:	BESE-5B	**Discipline/Year:**	Computer Science/First
Lecture/Lab Days:	**Mon, Wed, Thur** Lab on Tuesday	**Consulting Hours:**	**Open door policy**
Lab Engr:	Asma Majeed	**E-mail:**	asma.majeed@seecs.edu.pk
Knowledge Group:	Digital Systems and Signal Processing	**Updates on LMS:**	on required basis

Course Description:

Digital Logic Design is a one-semester course taken by Computer Science students during first year of their engineering program. This course introduces the logic operators and gates to lay the framework for strengthening the basic understanding of computer building blocks. Both combinational and sequential circuits are studied in this course along with their constituent elements comprising Arithmetic circuits, Comparators, Decoders, Encoders, Multiplexers, as well as latches, flip-flops, counters and registers. It lays down foundations for advanced studies in Computer Architecture.

Course Objectives:

In this course students will learn principles of Digital Logic Design. They will combine classical design methodologies with a series of laboratory assignments in which they will demonstrate their ability to successfully design, implement, and debug digital systems using Computer Aided Design tools and physical prototyping.

Course Learning Outcomes (CLO)

	Upon successful completion of this course the students will be able to demonstrate the following:-	PLO	BT LEVEL*
1	**Describe** number systems, binary codes, complements and **apply** those concepts in computer arithmetic.	1	C-2,3
2	**Explain** different simplification methods i.e Boolean algebra, map method and Quine-McCluskey minimization algorithm in simplifying functions and **practice** them in optimal design of digital circuits using logic gates.	1	C-2,3
3	**Analyze** combinational circuits of moderate complexity from the given circuit diagram, table, equations or timing waveforms.	2	C-4
4	**Design** sequential circuits within given hardware constraints and evaluate their timing behavior.	3	C-2,3,5
5	**Implement**, **test**, and debug prototype digital systems using standard laboratory equipment and also demonstrate basic skills in working with hardware description language (Verilog) in the design and analysis of digital logic circuits.	4,5	P-4
* BT=Bloom's Taxonomy, C=Cognitive domain, P=Psychomotor domain, A=Affective domain			

Mapping of CLOs TO Program Learning Outcomes

PLOs/ CLOs	CLO-1	CLO-2	CLO-3	CLO-4	CLO-5
PLO1 (Engineering Knowledge)	√	√			
PLO2 (Problem Analysis)			√		
PLO3 (Designing/Development of Solutions)				√	
PLO4 (Investigation)					√
PLO5 (Modern tool usage)					√
PLO6 (The Engineer and Society)					
PLO7 (Environment and Sustainability)					
PLO8 (Ethics)					
PLO9 (Individual and Team Work)					
PLO10 (Communication)					
PLO11 (Project Management)					
PLO:12 (Lifelong Learning)					

Mapping of CLOs to Assessment Modules and Weight ages (in accordance with NUST statutes)

To be filled in at the end of the course

CLOs\PLOs	CLO-1	CLO-2	CLO-3	CLO-4	CLO-5
Quizzes: (10.5%)					
Assignments: (4.5%)					
OHT-1: (12%)					
OHT-2: (12%)					
Labs: (17.5%)					
Project: (7.5%)					
End Semester Exam: (36%)					
Total: 100%					

Books:

Text Book: Digital Design(Fourth Edition) by M. Morris Mano and Michael Ciletti

Reference Books:

1. Digital Design(Fifth Edition) by M. Morris Mano and Michael Ciletti
2. Digital Fundamentals (Tenth Edition) by Floyd
3. Logic and Computer Design Fundamentals (Fourth Edition) by M. Morris Mano and Charles R. Kime
4. Fundamentals of Logic Design (Fifth Edition)by Charles H. Roth Jr
5. Digital Systems: Principles and Applications (Tenth Edition) by TocciWidmer
6. Contemporary Logic Design (Second Edition) by Randy H. Katz
7. Verilog HDL: A guide to Digital Design and Synthesis (Second Edition) by Samir Palnitkar
8. Fundamentals of Digital Logic with Verilog Design (Second Edition) by Stephen Brown|Zvonko

Main Topics to be Covered:

1. Digital Systems. Binary Numbers. Number Base Conversions. Octal and Hexadecimal Numbers. Complements. Signed Numbers. Binary Codes.
2. Basic Definitions. Axiomatic Definition of Boolean algebra. Basic Theorems and Properties of Boolean Algebra
3. Boolean Functions. Canonical and Standard Forms. Other Logic Operations. Digital Logic Gates. Integrated Circuits
4. The K-Map Method. Four-Variable Map. Product of Sums and Sum of Products simplifications. Introduction to Five-Variable Map. Quine-McCluskey minimization technique (Tabulation).
5. Don't-Care Conditions. NAND and NOR Implementation. Other Two-Level Implementations
6. Combinational Circuits. Analysis Procedure. Design Procedure. Binary Adder-Subtractor. Decimal Adder. ALU Design using Combinational Circuits.
7. Binary Multiplier. Magnitude Comparator. Decoders. Encoders. Multiplexers
8. Sequential Circuits. Latches and Flip-flops
9. Analysis of Clocked Sequential Circuits.
10. Mealy and Moore FSM. State Reduction and Assignment. Design of clocked sequential circuits.
11. Registers. Shift Registers. Ripple Counters
12. Synchronous Counters. Other Counters

Lecture Breakdown:

Week No	Lecture	Topics	Text Book Reference	Other References	CLO
1.	**1.**	**Introduction**: Digital Systems and motivation for study	1-1		
	2.	Number Systems: Binary, Octal, Decimal and Hexadecimal Numbers and Base Conversions.	1-2,1-3,&1-4	1-2 Ref Book(3)	**C-1**
	3.	Complements: Subtraction of Unsigned Numbers using Complements.	1-5	.	**C-1**
	Lab 01	Familiarization of Basic Gates and Digital ICs			**P-4**
2.	4.	Signed Binary Numbers Arithmetic: Addition and Subtraction of Signed Binary Numbers.	1-6	2-6 Ref Book(2)	**C-1**
	5.	Binary Codes.	1-7		**C-1**
	6.	Binary Storage and Registers. Binary Logic: Definition of Binary Logic and Logic gates.	1-8&1-9		**C-1**
	Lab 02	Introduction to Verilog HDL. Basic language constructs and design entry using Verilog HDL.			**P-4**
3.	**7.**	**Introduction**: Boolean Algebra: Basic and	2-1,2-2, &2-3	2-2 Ref Book(3)	**C-2**

		Axiomatic Definition of Boolean Algebra; Two-Valued Boolean Algebra.			
	8.	Basic Theorems and Properties of Boolean Algebra.	2-4		**C-2**
	9.	Boolean Functions; Canonical and Standard Forms.	2.5 &2-6		**C-2**
	Lab 03	Derivation of Boolean Functions from given logic diagram and its Hardware implementation. Function implementation using Verilog HDL Gate-Level modeling.			**P-4**
4.	10.	Other Logic Operations.	2-7	8-1 Ref Book (5)	**C-2**
	11.	Digital Logic Gates and Integrated Circuits.	2-8&2-9		**C-2**
	12.	**Introduction**: The K-Map Method; Two, and Three -Variable K-Maps.Sum-of-Products (SOP) simplification using Three-Variable K-Map.	3-1 & 3-2	5-2 Ref Book(4)	**C-2**
	Lab 04	Minimization of Boolean Functions and its Hardware implementation.			**P-4**
5.	13.	Sum-of-Products (SOP) simplification using Four-Variable K-Map; Essential and Non-essential Prime Implicants.	3-3	5-3 Ref Book(4) 2.5 Ref Book(3)	**C-2**
	14.	Five-Variable K-Map; Sum-of-Products (SOP) simplification using Map Method.	3-4	5-4 Ref Book(4)	**C-2**
	15.	Product- of- Sums (POS) Simplifications and Don't Care conditions.	3.5&3-6		**C-2**
	Lab 05	Design of Binary-to-Gray/Gray-to-Binary Code Converter using basic gates. Gate-Level Modeling of Combinational Circuits using Verilog HDL.			**P-4**
6.	**OHT-1**				
7.	16.	Quine-MacCluskey Minimization algorithm (Tabulation).		6-1, 6-2 &6.3 Ref Book(4)	**C-2**
	17.	NAND and NOR implementations.	3-7		**C-2**
	18.	Other Two-Level implementations.	3-8		**C-2**
	Lab 06	BCD-to-Seven Segment Decoder Design.			**P-4**
8.	19.	Exclusive-OR function: Parity Generation and Checking.	3-9		**C-2**

	20.	**Introduction**: Combinational Circuits: Design Procedure with Code Conversion Example.	4-1, 4-2 & 4-4		**C-4**
	21.	Combinational Circuits: Analysis Procedure.	4-3		**C-3**
	Lab 07	Design of a 2-bit Magnitude Comparator using Classical design method. Combinational Logic Design using Verilog HDL.			**P-4**
9.	22.	Half and Full Adders: Design of 4-BIT Ripple Carry Adder-Subtractor using Full Adders.	4-5		**C-4**
	23.	Design of 4-Bit Adder-Subtractor with Carry Look-ahead Generator and Overflow.	4-5		**C-4**
	24.	Decimal Adder.	4-6		**C-4**
	Lab 08	Design of a 2-bit Adder/Subtractor Circuit. Combinational Logic Design using Verilog HDL.			**P-4**
10.	25.	Binary Multiplier. Magnitude Comparator.	4-7&4.8		**C-4**
	26.	Decoders/De-multiplexers.	4-9		**C-4**
	27.	Encoders.	4-10		**C-4**
	Lab 09	Design of 4-bit ALU.			**P-4**
11.	28.	Multiplexers and Tri-State Gates.	4-11	4-2-2, 4-2-3 &4-2-4 Ref Book (6)	**C-4**
	29.	**Introduction**: Sequential Circuits and different types of Latches.	5-1&5-2		**C-3**
	30.	Storage Elements: Latches	5-3		**C-4**
	Lab 10	Voting Machine Design.			**P-4**
12.	**OHT-2**				
13.	31.	Storage Elements: Flip-Flops, Other Flip-Flops, Conversion of Flip-Flops.	5-4	11-4,11-5,11-6 &11-7 Ref Book (4)	**C-4**
	32.	Analysis of Clocked-Sequential Circuits; State Equations, State Table, State Diagram, and Flip-Flop input equations.	5-5		**C-3**
	33.	Analysis with D Flip-Flops, JK Flip-Flops, and T Flip-Flops.	5-5		**C-3**

	Lab 11	Memory Elements: Latches and Flip-flops. Design of a positive-edge triggered D flip-flop. Sequential Logic Design using Verilog HDL			**P-4**
14.	34.	Mealy and Moore Models. Mealy-Moore Conversion Procedure.	5-5		**C-3**
	35.	State Reduction using Row Matching and Implication Table Techniques. State Assignment Method.	5-7	15.3 Ref Book(4)	**C-4**
	36.	Design Procedure- Synthesis using D Flip-Flops.	5-8		**C-4**
	Lab 12	Flip-Flop Applications & Proteus Simulation of Digital Circuits			**P-4**
15.	37.	Design Procedure- Synthesis using JK Flip-Flops, and T Flip-Flops.	5-8		**C-4**
	38.	**Introduction**: Registers with Parallel Load.	6-1		**C-3**
	39.	Shift Registers; 4-Bit Shift Register; Serial Transfer and Serial Addition.	6-2		**C-3**
	Lab 13	Sequence Detector Design. Sequential Logic Design using Verilog HDL			**P-4**
16.	40.	4-Bit Universal Shift Register.	6-2		**C-4**
	41.	Ripple Counters; Binary and BCD Ripple Counters.	6-3		**C-4**
	42.	Synchronous Counters: Binary and BCD Counters.	6-4		**C-4**
	Project Progress Presentations/Demonstration				
17.	43.	Other Counters; Counter with unused States.	6-5		
	44.	Other Counters: Counters with unused states, Ring Counters and Johnson Counters.	6-5		
	45.	Revision			
	Project Final Presentations/Demonstration				
18.	**End Semester Exam**				

Lab Experiments:	
Lab 1: Familiarization of Basic Gates and Digital ICs	
Lab 2: Introduction to Verilog HDL. Basic language constructs and design entry using Verilog HDL.	
Lab 3: Derivation of Boolean Functions from given logic diagram and its Hardware implementation.Function implementation using Verilog HDL Gate-Level modeling.	
Lab 4: Minimization of Boolean Functions and its Hardware implementation.	
Lab 5: Design of Binary-to-Gray/Gray-to-Binary Code Converter using basic gates.Gate-Level Modeling of Combinational Circuits using Verilog HDL.	
Lab 6:BCD-to-Seven Segment Decoder Design.	
Lab 7: Design of a 2-bit Magnitude Comparator using Classical design method. Combinational Logic Design using Verilog HDL.	
Lab 8: Design of a 2-bit Adder/Subtractor Circuit.Combinational Logic Design using Verilog HDL.	
Lab 9: Design of 4-bit ALU.	
Lab 10: Voting Machine Design.	
Lab 11: Memory Elements: Latches and Flip-flops. Design of a positive-edge triggered D flip-flop. Sequential Logic Design using Verilog HDL	
Lab 12: Flip-Flop Applications & Proteus Simulation of Digital Circuits	
Lab 13: Sequence Detector Design.Sequential Logic Design using Verilog HDL	

Grading Policy:	
Quizzes Policy	The quizzes are a mandatory component of the overall assessment. The purpose of quizzes is to keep the students up-to-date with the lecture material and test basic understanding of the course concepts. There will be at least **6** unannounced quizzes conducted in the class any time during the lecture. Each quiz will consist of questions that target specific topics from the most recent as well as previous week lectures.
Assignments	In order to give sufficient practice and comprehensive understanding of the subject, a minimum of **5** home assignments will be given to the students. The questions in assignments will be challenging to give students the confidence and enable them to prepare for the exams well. Home works will be submitted at the beginning of class on the due date. The students are advised to do the assignment themselves. Copying of assignment is highly discouraged, taken as cheating case and dealt accordingly. No late submissions will be accepted.
Conduct of Labs	The labs will be conducted for three hours each week. For the conduct of lab the students will be divided into groups with 2 students per group. A lab handout comprising pre-lab, in-lab, and post-lab report parts will be provided to students for study and analysis during the

	week preceding each lab session. The students are expected to complete pre-lab work before lab starts and also come prepared for the lab. Any student failing to complete pre-lab will not be allowed to attend lab session. The students will be evaluated during each lab on the basis of demonstration, oral viva, and lab report submitted by them individually on completion of lab work. The students are required to be punctual in the lab; late comers will be penalized in award of marks.
Design Projects	The students will be allocated course projects during the week preceding mid semester exam and evaluated before final exams based on parameters spelled out in Project Reservation form provided to them. The students will be grouped into syndicates with each syndicate having a maximum strength of 3 students depending upon the complexity level of design. However, any student desirous of carrying out design work individually will be encouraged and graded in the same pretext. The students are advised to select project titles well before their submission schedule.
Other Matters:	
Online Discussions	In this semester we will be using Piazza for class discussions. The system is highly catered to getting you help fast and efficiently from classmates, the lab engineer, and me. Rather than emailing questions to the teaching staff, I encourage you to paste your questions and optimally use this online resource. If you have any problems or feedback for the developers, email **team@piazza.com** Find our class page at: **https://piazza.com/seecs.edu.pk/spring2015/ee221/home**
Academic Honesty and Plagiarism	Plagiarism is the unacknowledged use of other's work, including the copying of assignments and laboratory results from the other students. Plagiarism is considered a serious offence by the university and severe penalties apply. Therefore, all the students must display originality of efforts and avoid plagiarism in any form.
Classroom Etiquettes	It is the collective responsibility of all the students to make the class environment conducive for learning. To create and maintain a friendly atmosphere, the following standards of class room behavior will be observed:- 1. Students will be punctual for the class. The teacher considers late comers disrespectful of those who manage to be on time. 2. If a student decides to attend the class, he or she will not disrupt class by leaving before the lecture has ended. 3. All the cell phones must be switched OFF prior to entering the class room. 4. The students must bring text book and calculators in the class and make lecture notes.
Tools / Software Requirement:	
	1. Verilog Hardware Description Language (Verilog HDL) software and HDL simulator ModelSim version 5.7f will be used for the design and simulation of logic circuits. 2. Digital and Embedded System lab will be used for hands on practice.