North South University
Department of Electrical and Computer Engineering
Fall-2020, CSE 231L Final
CSE 231 Digital Logic Design, Section-8
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Instructor-Md. Anisur Rahman Asif

Total Marks: 50 **Time: 1 Hour 15 minutes**

Instructions:

1. Answer all the questions.
2. Clearly label all the diagrams and truth tables.
3. Write **Page number** and your **Name and ID** on each page.

Questions:

1. Assume I_0, I_1, I_2 and I_3 in the following truth table are the Data Inputs of a 4:1 MUX. Take A and C as the select bits, and find out the values of Data Inputs for the function F(A, B, C) = Σ (0, 2, 6, 7). Show all the steps and fill-up the following table. [5]

A	B	C	F	Data Inputs
0	0	0		I_0 =
0	0	1		
0	1	0		I_1 =
0	1	1		
1	0	0		I_2 =
1	0	1		
1	1	0		I_3 =
1	1	1		

Table: 4:1 Multiplexer

2. Explain why there is a don't care term in K column of JK excitation table. Explain using JK characteristic table.[5]

Q	Q(Next)	J	K
0	0	0	X

Table: JK Flip-flop Excitation table

3. Subtract 1010 from 1100 using 2's compliment rule. Explain with XOR Truth table, how Data input B is subtracted from A for the value M=1. [5+5]

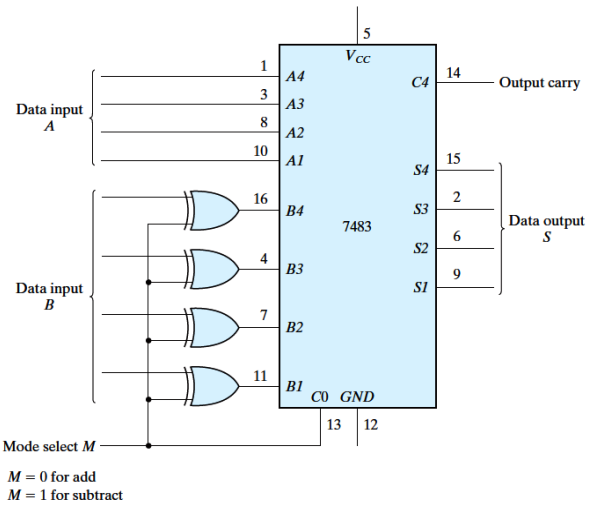

Figure: 4 bit binary adder for Addition and Subtraction

4. How would you add two 8 bit numbers using 4 bit binary adder IC? [5]

5. The given State Diagram represents a circuit that has two Flip-Flops (A and B), one input (X) and one output (Y).

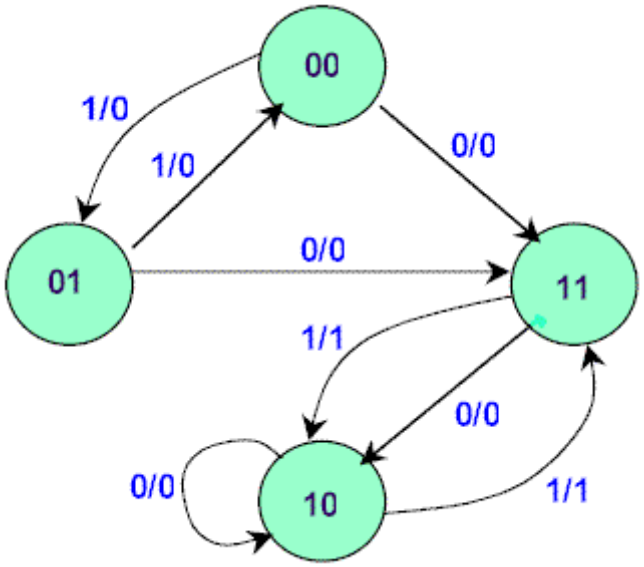

Figure: State Diagram

- Complete the Next State and Output columns of the State Table [5]
- Using the Excitation Table of the JK Flip-Flop, determine the inputs for the two Flip-Flops (J_A, K_A and J_B, K_B) for each state transition [10]
- Use Karnaugh Maps to minimize the functions of the combinational circuit for each Flip-Flop input (J_A, K_A and J_B, K_B) as well as the combinational circuit for the output (Y) [5]
- Draw the diagram for Synchronous Sequential Circuit using JK Flip-Flops and the minimized equations [5]

Present state		Input	Next state		Output	Flip-flop input functions			
A	B	X	A	B	Y	J_A	K_A	J_B	K_B
0	0	0							
0	0	1							
0	1	0							
0	1	1							
1	0	0							
1	0	1							
1	1	0							
1	1	1							

Table: State Table for JK Flip-flops