Digital Logic Design :

Lecture 19

Counter Applications :

The Digital Clock

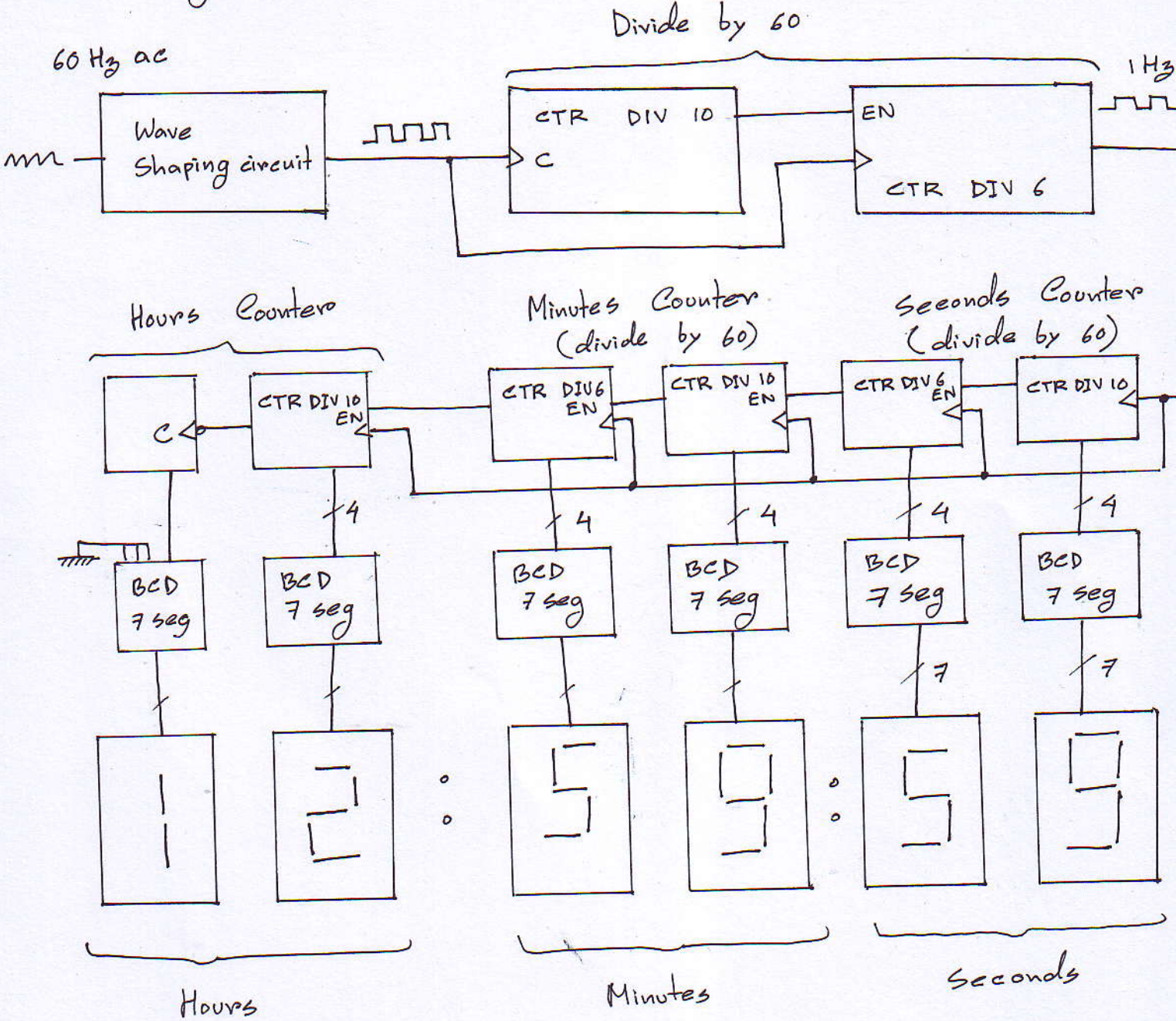
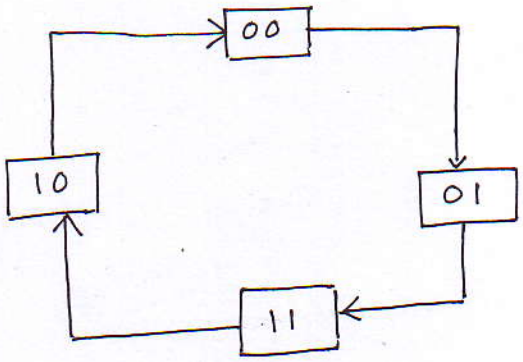


Fig : Simplified logic diagram for a 12-hour digital clock

Design a counter that will count in 2-bit Gray code sequence:



Present State		Next State	
Q_1	Q_0	Q_1	Q_0
0	0	0	1
0	1	1	1
1	1	1	0
1	0	0	0

J_0 Map

Q_1 \ Q_0	0	1
0	1	x
1	0	x

$J_0 = \overline{Q_1}$

K_0 Map

Q_1 \ Q_0	0	1
0	x	0
1	x	1

$K_0 = Q_1$

J_1 Map

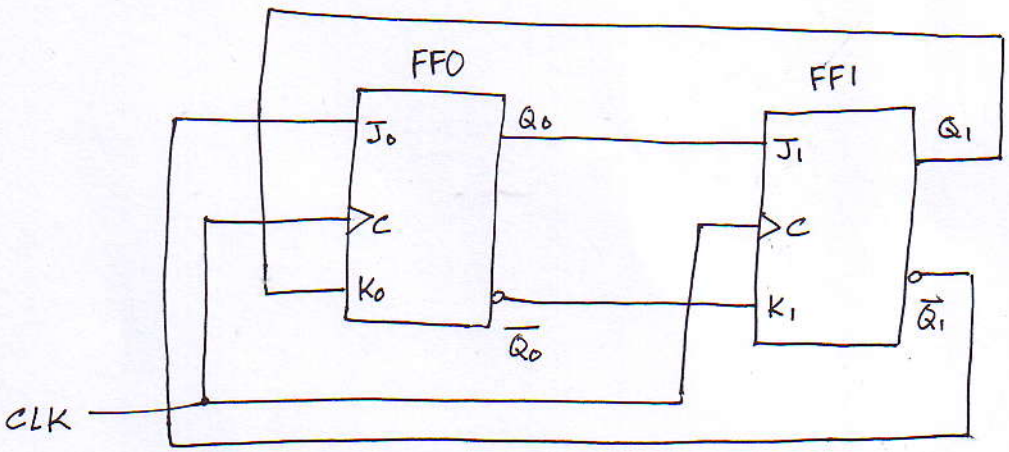
Q_1 \ Q_0	0	1
0	0	1
1	x	x

$J_1 = Q_0$

K_1 Map

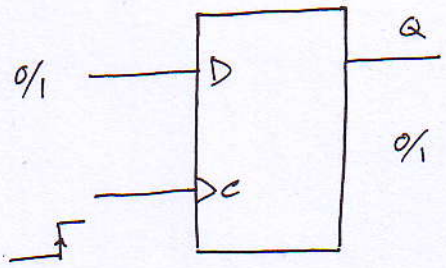
Q_1 \ Q_0	0	1
0	x	x
1	1	0

$K_1 = \overline{Q_0}$



Output Transitions		Flip-flop inputs	
Q_N	Q_{N+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

SHIFT REGISTERS



Serial In / Serial Out shift register :

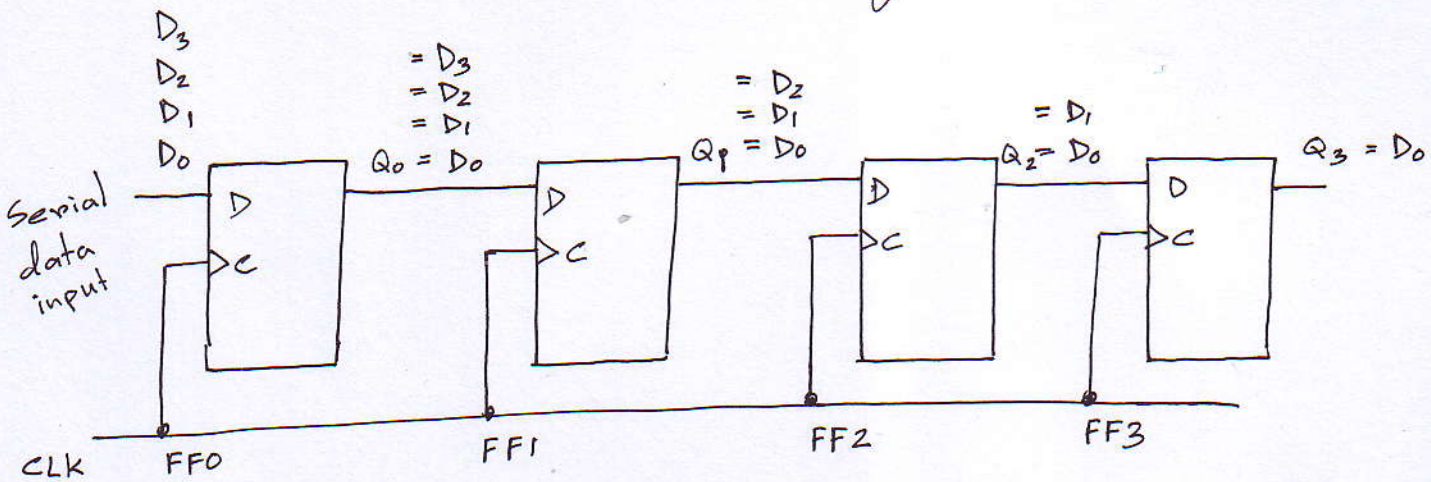
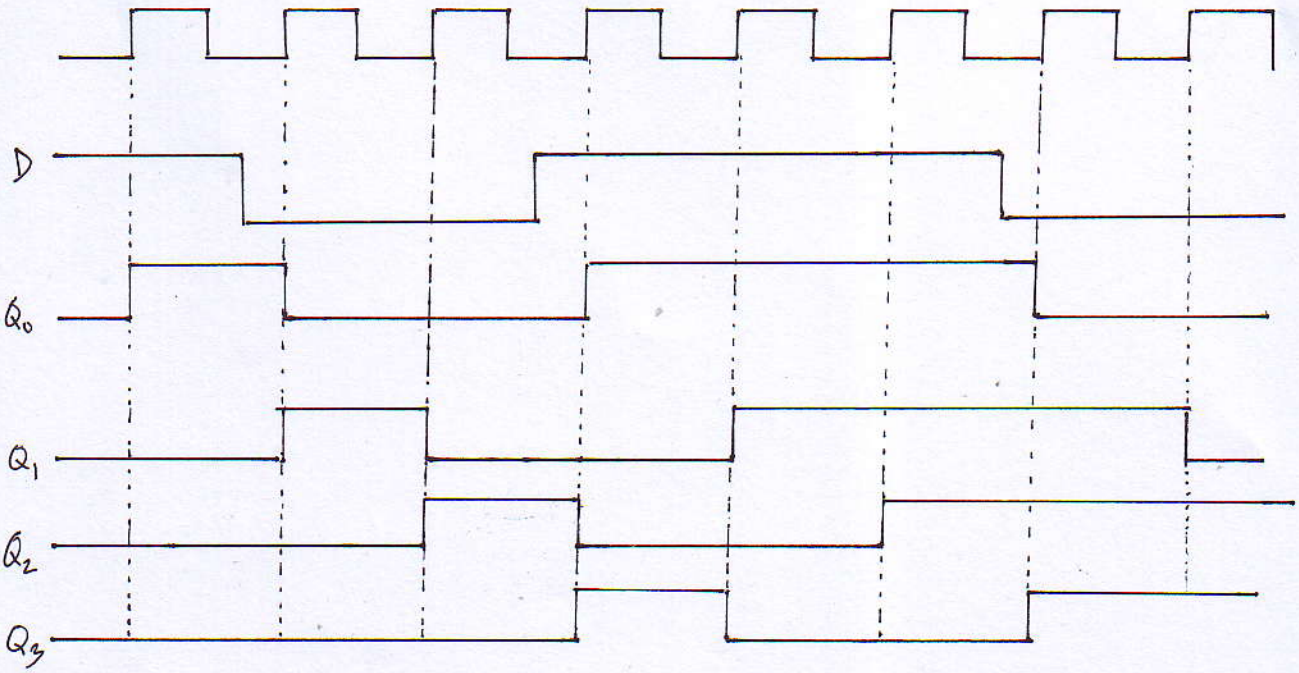
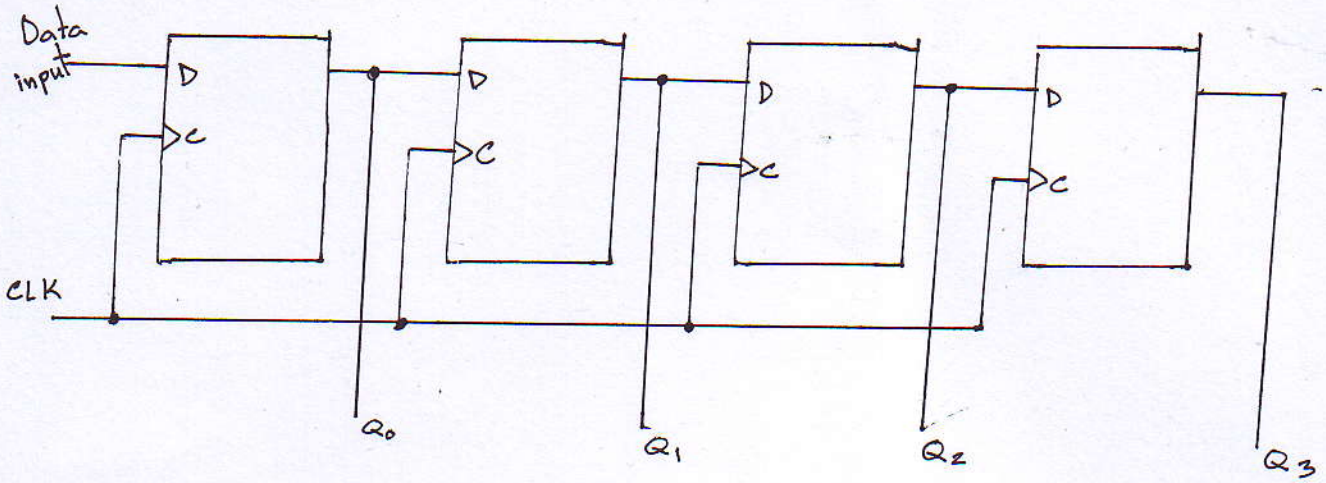


Fig : 4-bit serial in / serial out Shift register

Determine Q_0, Q_1, Q_2 and Q_3 for the following clock and D input :



Serial In / Parallel Out Shift Register :



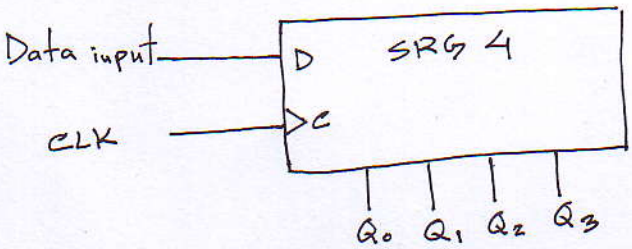


Fig : Logic symbol

Fig : A serial in/parallel out shift register

Parallel In / Serial Out Shift Register :

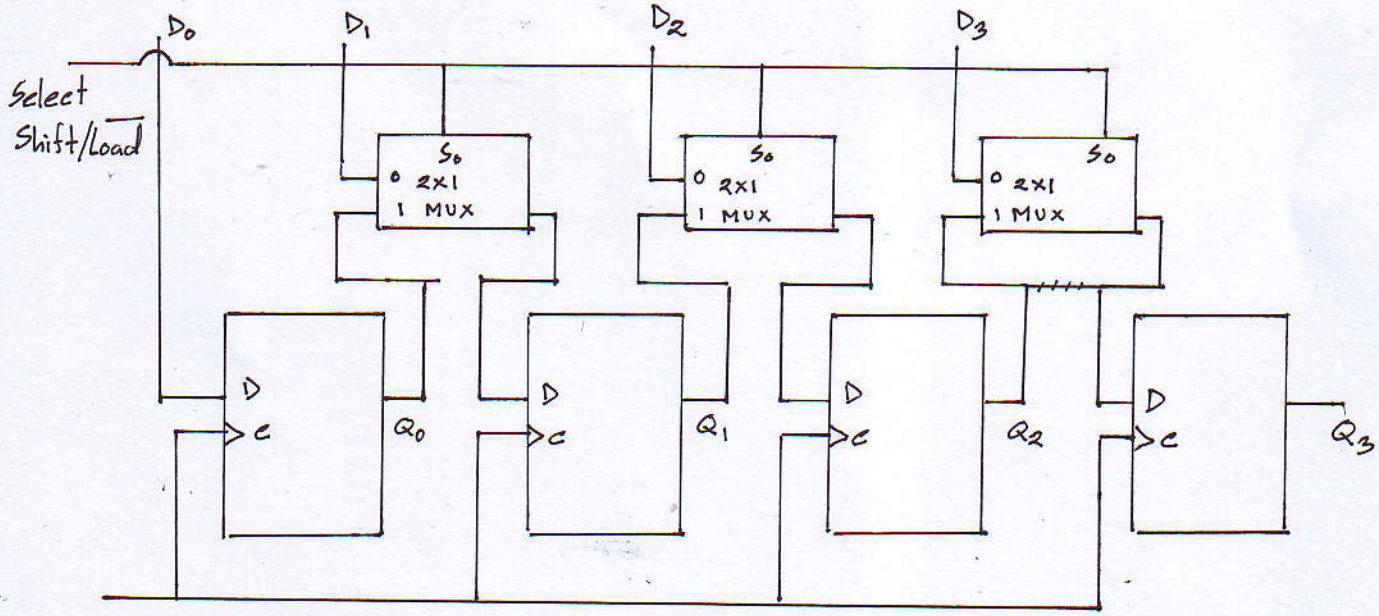


Fig : Four Bit Parallel In Serial Out Shift Register

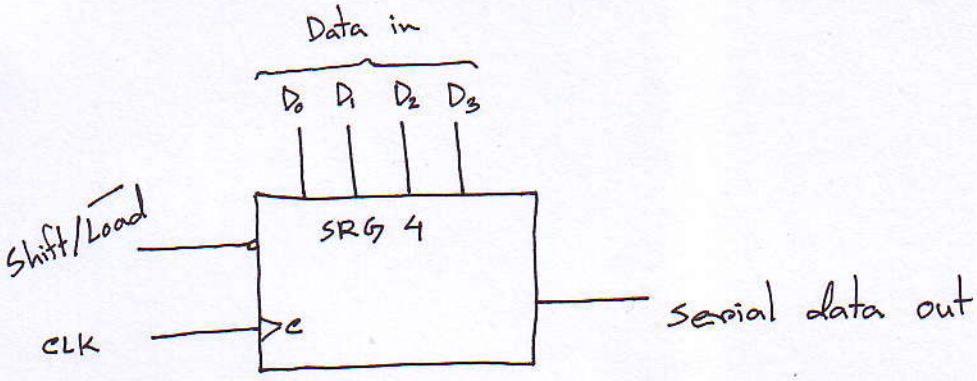
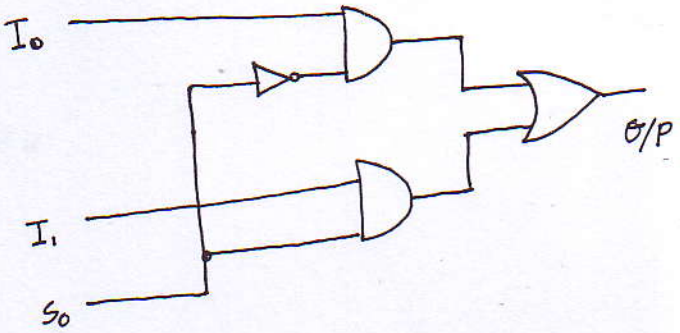


Fig : Logic symbol



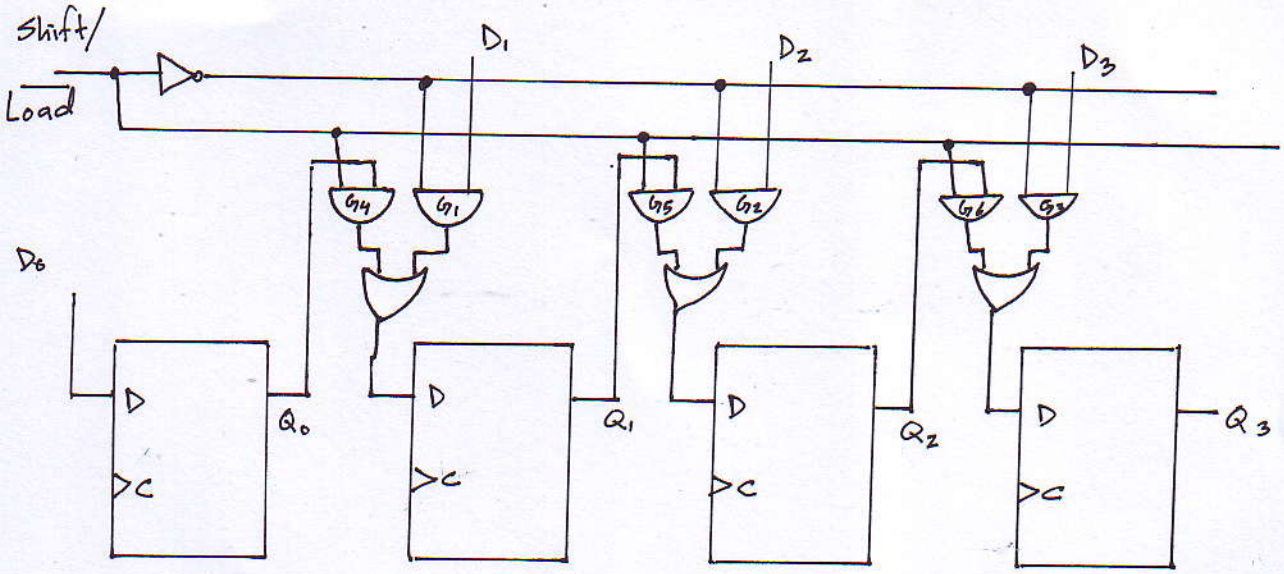


Fig : Four bit Parallel In/ Serial Out Shift Register

Parallel In / Parallel Out Shift Register :

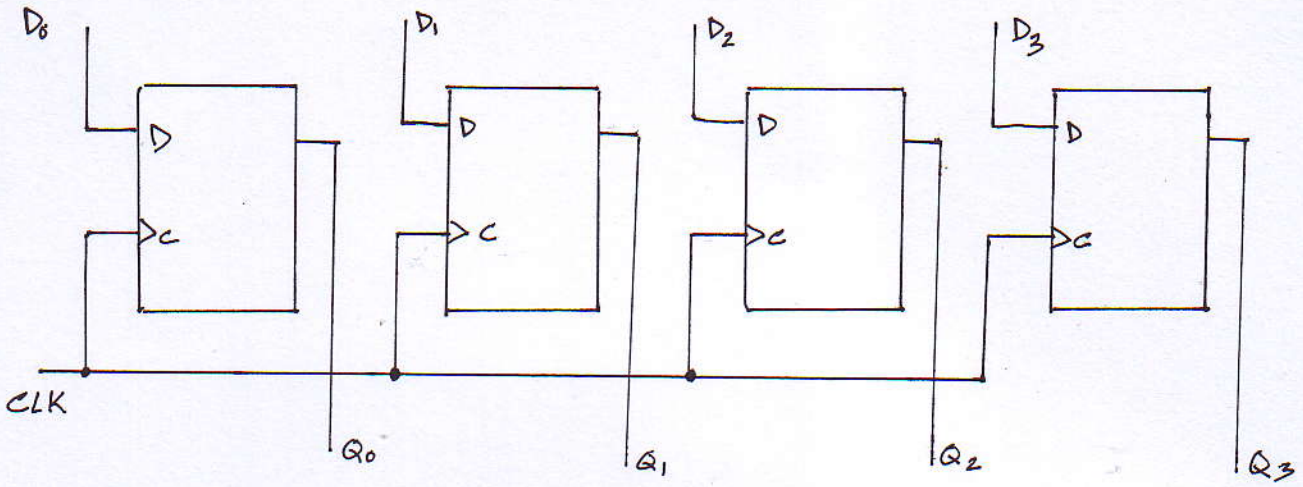


Fig : Four Bit Parallel In / Parallel Out shift Register