North South University

Department of Electrical and Computer Engineering

LAB REPORT-03

Course name: Digital Logic Design

Course Code: 231

Experiment Number: 03

Experiment name: Combinational Logic Design

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Section: 06

Group no: 04

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Remarks:	**Score:**

OBJECTIVE

- Become familiarized with the analysis of combinational logic networks.
- Learn the implementation of networks using the two canonical forms.

THEORY

Min terms and Max terms:

In Boolean algebra, Boolean function can be expressed as Canonical Disjunctive Normal Form known as minterm and some are expressed as Canonical Conjunctive Normal Form known as maxterm.

In Minterm, we look for the functions where the output results in "1" while in Maxterm we look for function where the output results in "0".

We perform Sum of minterm also known as Sum of products (SOP) . We perform Product of Maxterm also known as Product of sum (POS). Boolean functions expressed as a sum of minterms or product of maxterms are said to be in canonical form.

Combinational logic circuit:

Combinational Logic Circuits are memoryless digital logic circuits whose output at any instant in time depends only on the combination of its inputs. The output of combinational circuit at any instant of time, depends only on the levels present at input terminals. The combinational circuit do not use any memory. The previous state of input does not have any effect on the present state of the circuit. A combinational circuit can have an n number of inputs and m number of outputs. Generally, the functions of combinational circuits are specified through Boolean Algebra, Truth Table and Logic gates.

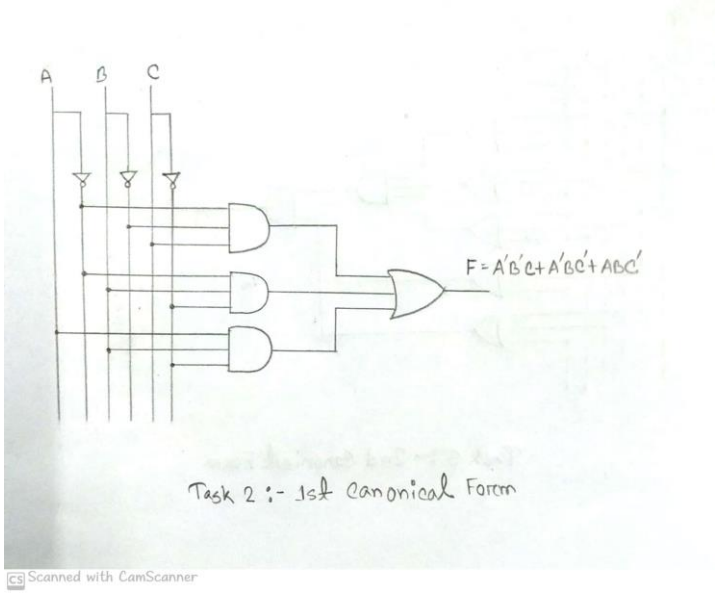
Canonical forms

Each term of Boolean expressions contains all input variables either in true form or in complement form. If there are 'n' input variables, then there will be 2n possible combinations with zeros and ones. So the value of each output variable depends on the combination of input variables. So, each output variable will have '1' for some combination of input variables and '0' for some other combination of input variables.

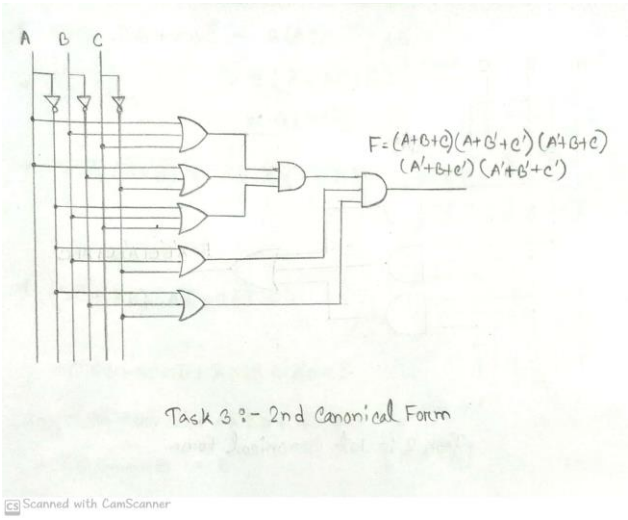
EQUIPMENT LIST

- Trainer Board
- 1 x IC 4073 Triple 3-input AND gates
- 2 x IC 4075 Triple 3-input OR gates
- 1 x IC 7404 Hex Inverters (NOT gates)

CIRCUIT DIAGRAM



F1.1 : *1st Canonical Form (Minterm)*



F1.2 : *2nd Canonical Form(Maxterm)*

Figure F.*1 1st and 2nd canonical circuit diagrams of the combinational circuit of Table F.1*

DATA & TABLE

Input Reference	A	B	C	F	Min Term	Max Term
0	0	0	0	0		A+B+C
1	0	0	1	1	A'B'C	
2	0	1	0	1	A'BC'	
3	0	1	1	0		A+B'+C'
4	1	0	0	0		A'+B+C
5	1	0	1	0		A'+B+C'
6	1	1	0	1	ABC'	
7	1	1	1	0		A'+B'+C'

Table F.1: *Truth table to a combinational circuit*

	Standard Notation	Function
1st Canonical Form	F= Σ(1,2,6)	F = A'B'C+ A'BC'+ ABC'
2nd Canonical Form	F= Π(0,3,4,5,7)	F = (A+B+C).(A+B'+C').(A'+B+C). (A'+B+C').(A'+B'+C')

Table F.2 :*1st and 2nd canonical forms of the combinational circuit of TableF.1*

RESULT ANALYSIS AND DISCUSSION

In this experiment, our goal is to understand the concepts of Combinational Circuits and to be able to design them. We used canonical forms to implement the combinational logic networks. The two canonical forms that we used to design our circuits are Minterm (Sum of Products) and Maxterm (Product of Sum).

Minterm is the sum of the product of outputs where the output results in "1". Constructing a circuit following Minterm will deliver the output "1" whenever the function of Minterm, F equals "1". For example, a circuit constructed from the function, F = A'B'C+ A'BC'+ ABC' will deliver the output "1" for the set of possible combination of 3 variable inputs, that is {(0, 0, 1), (0, 1, 0), (1, 1, 0)}.

Maxterm is the product of the sum of outputs where the output results in "0". Constructing a circuit following Maxterm will deliver the output "0" whenever the function of Maxterm, F equals "0". For example, a circuit constructed from the function,

F = (A+B+C).(A+B'+C').(A'+B+C).(A'+B+C').(A'+B'+C') will deliver the output "0" for the set of possible combinations of 3 variable inputs, that is {(0, 0, 0), (0, 1, 1), (1, 0, 0), (1, 0, 1), (1, 1, 1)}

CONTRIBUTION

NAME	CONTRIBUTION IN
Khalid Bin Shafiq	Result Analysis and Discussion
Rafidul Islam	Circuit Diagram
Rashiqur Rahman Rifat	Theory
Towsif Muhtadi Khan	Data & table, Coordinator

Task 1: Complete the tables

Input Reference	A B C	F	Min term	Max term
0	0 0 0	0		A+B+C
1	0 0 1	1	A'B'C	
2	0 1 0	1	A'BC'	
3	0 1 1	0		A+B'+C'
4	1 0 0	0		A'+B+C
5	1 0 1	0		A'+B+C'
6	1 1 0	1	ABC'	
7	1 1 1	0		A'+B'+C'

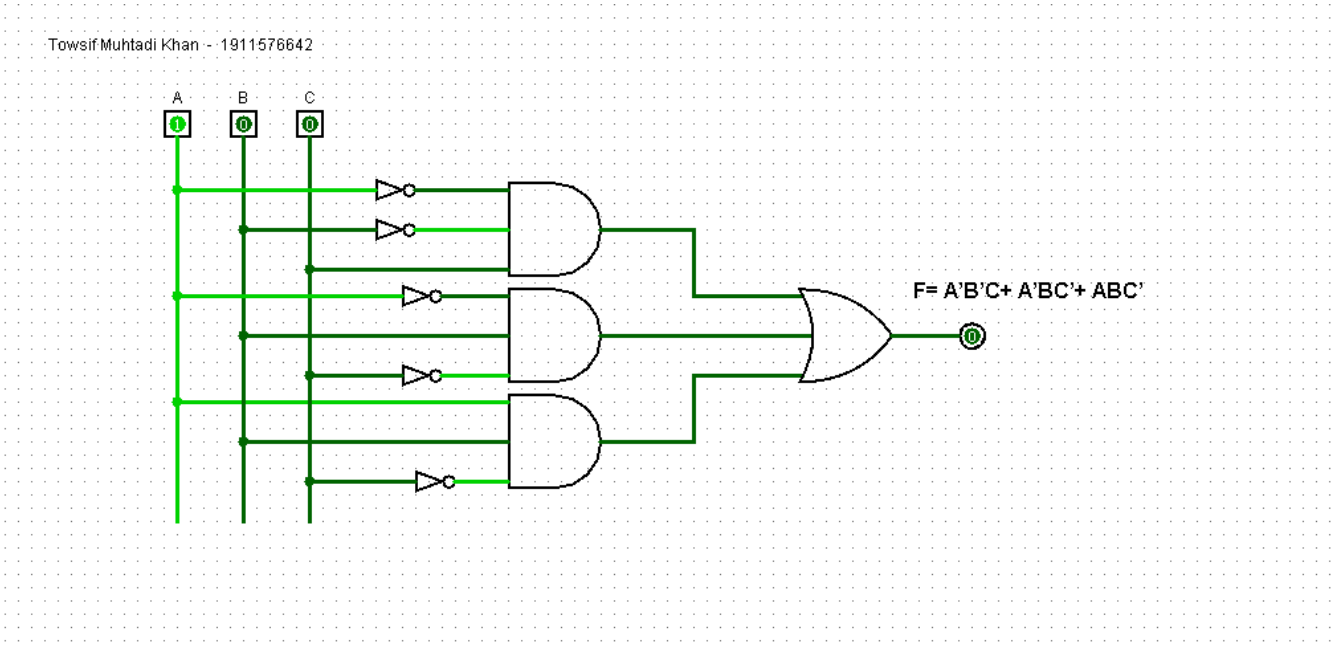
Table C.1 Truth table to a combinational circuit

	Shorthand Notation	Function
1st Canonical Form	F= Σ(1,2,6)	F = A'B'C+ A'BC'+ ABC'
2nd Canonical Form	F= Π(0,3,4,5,7)	F =(A+B+C).(A+B'+C').(A'+B+C).(A'+B+C').(A'+B'+C')

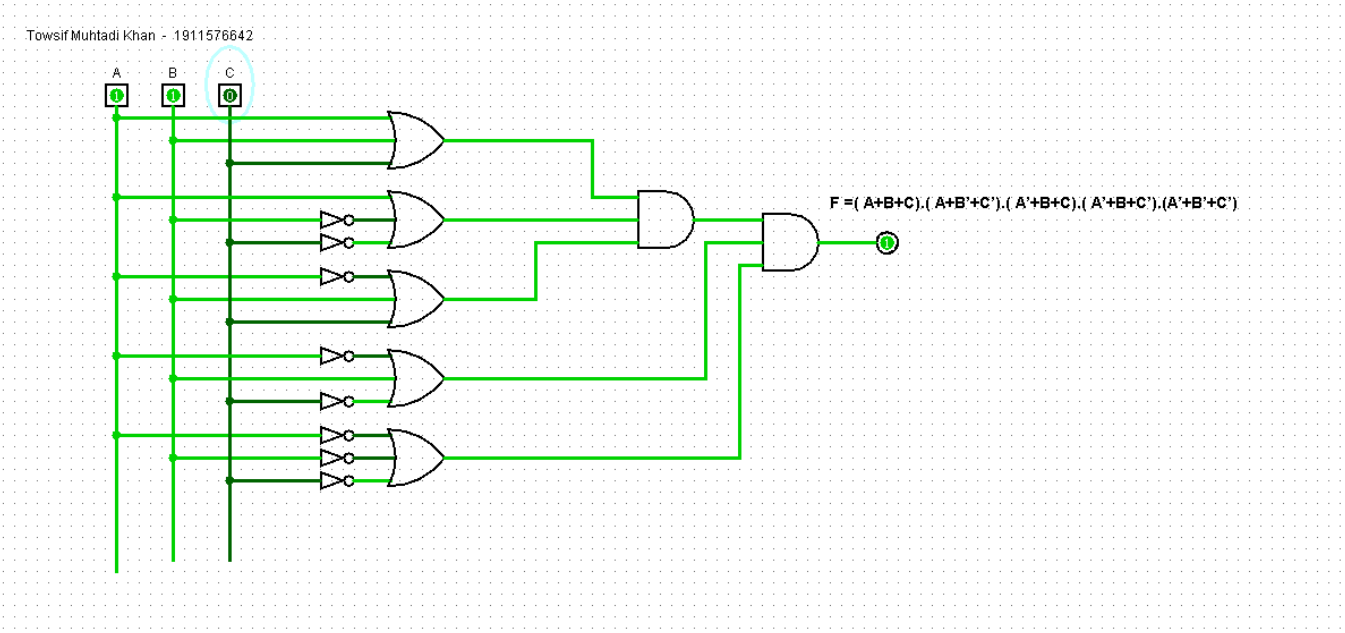
Table C.2 1st and 2ndcanonical forms of the combinational circuit of Table C.1

Task 2: Attach the **1st Canonical Form** circuit diagram of the combinational circuit of Table C.1

Task 3: Attach the **2nd Canonical Form** circuit diagram of the combinational circuit of Table C.1



F1.1 : *1st Canonical Form (Minterm)*



F1.2 : *2nd Canonical Form(Maxterm)*

Figure F.1 1st and 2nd canonical circuit diagrams of the combinational circuit of Table F.1

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