Digital Logic Design :

Lecture 15

The Edge-Triggered J-K Flip-Flop :

The functioning of the J-K flip-flop is identical to that of the S-R flip-flop in the SET, RESET and No change conditions of operation. The difference is that the J-K flip-flop has no invalid states as does the S-R flip-flop.

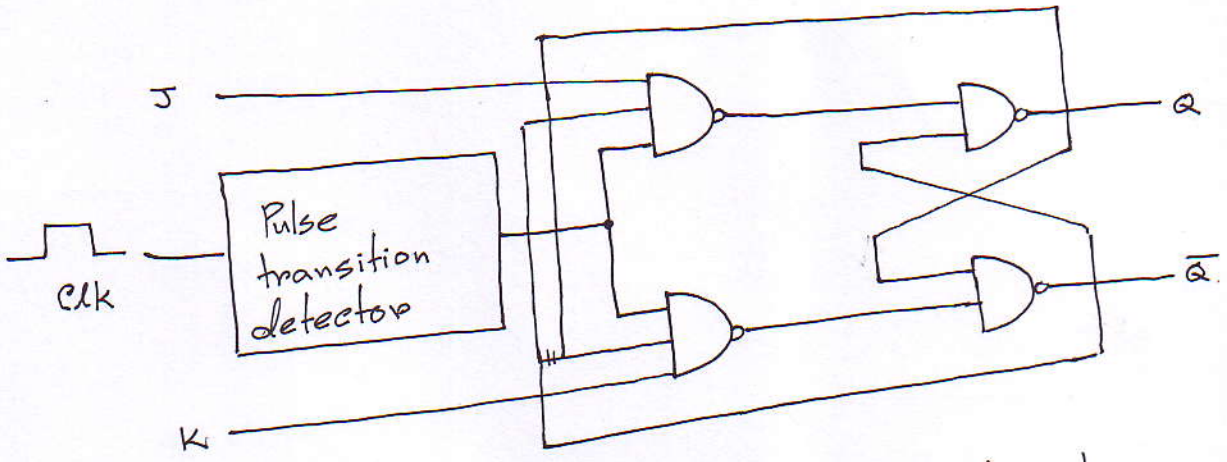
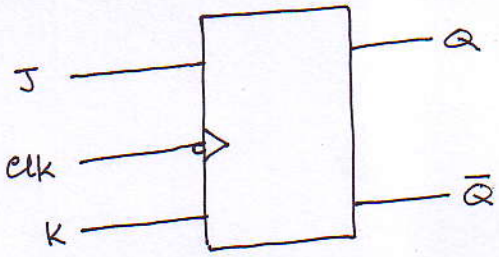
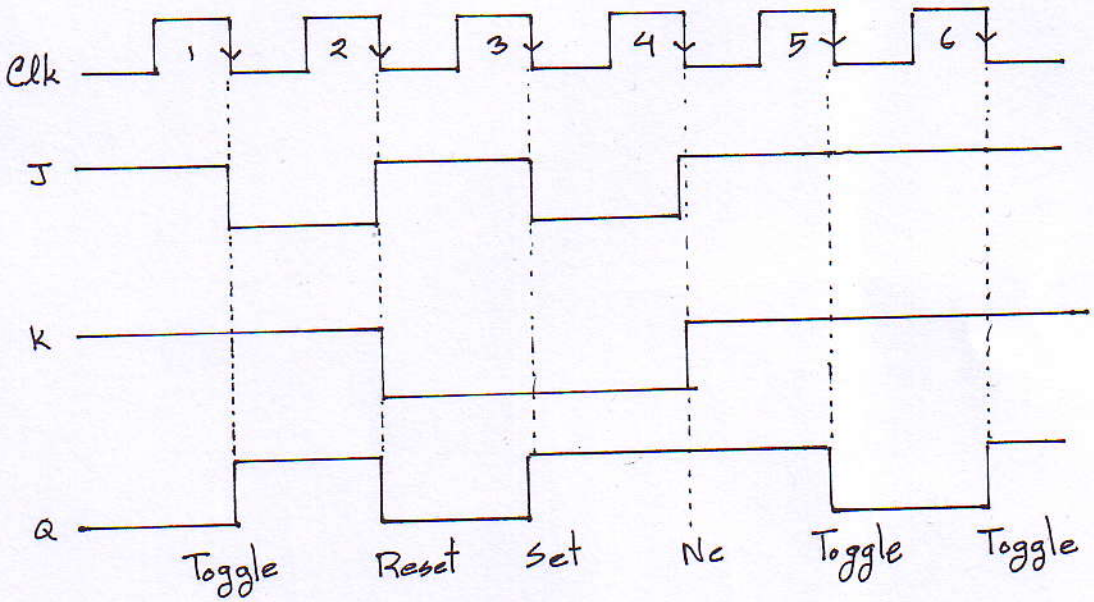


Fig : Logic diagram for a positive edge triggered J-K flip-flop

Inputs			Outputs		Comments
J	K	Clk	Q	$\overline{Q}$	
0	0	↑	Q_0	$\overline{Q_0}$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\overline{Q_0}$	Q_0	Toggle

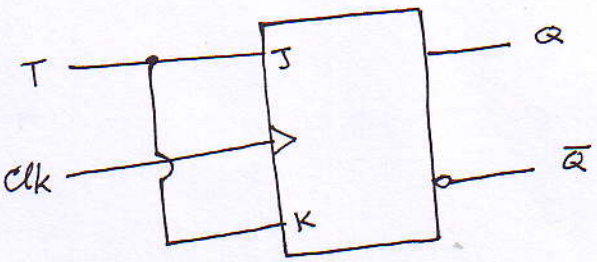
Determine Q output if the J-K flip-flop is initially RESET





T flip-flop :

A J-K flip-flop connected for toggle operation is sometimes called a T flip-flop.



Inputs		Outputs		Comments
T	Clk	Q	$\overline{Q}$	
0	↑	Q_0	$\overline{Q_0}$	No Change
1	↑	$\overline{Q_0}$	Q_0	Toggle mode

The Edge-Triggered D Flip-Flop :

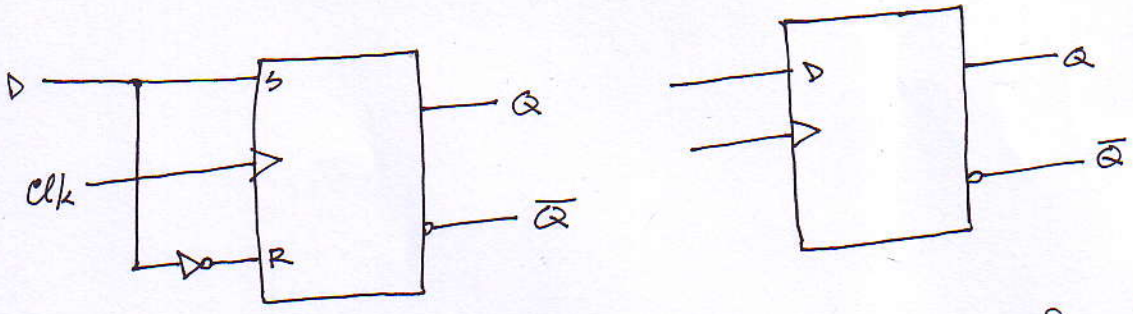


Fig : A positive edge triggered D flip-flop formed with an S-R flip-flop and an inverter

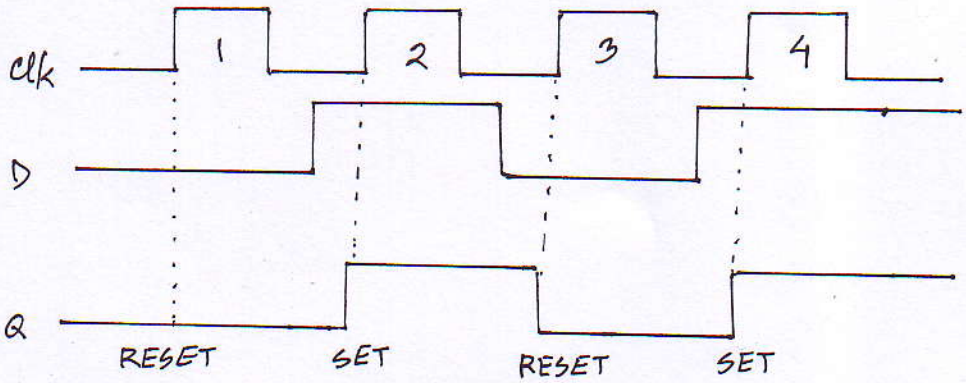
Truth table for positive edge triggered D flip-flop

Inputs		Outputs		Comments
D	Clk	Q	$\overline{Q_0}$	
1	↑	1	0	SET
0	↑	0	1	RESET

The D flip-flop is used to store a single data bit, positive edge triggered flip-flop stores data at the

leading edge of the clock.

Determine Q if the D flip-flop is initially RESET



flip-flop with Asynchronous Inputs

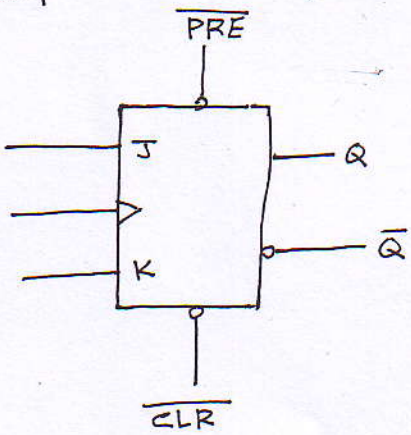
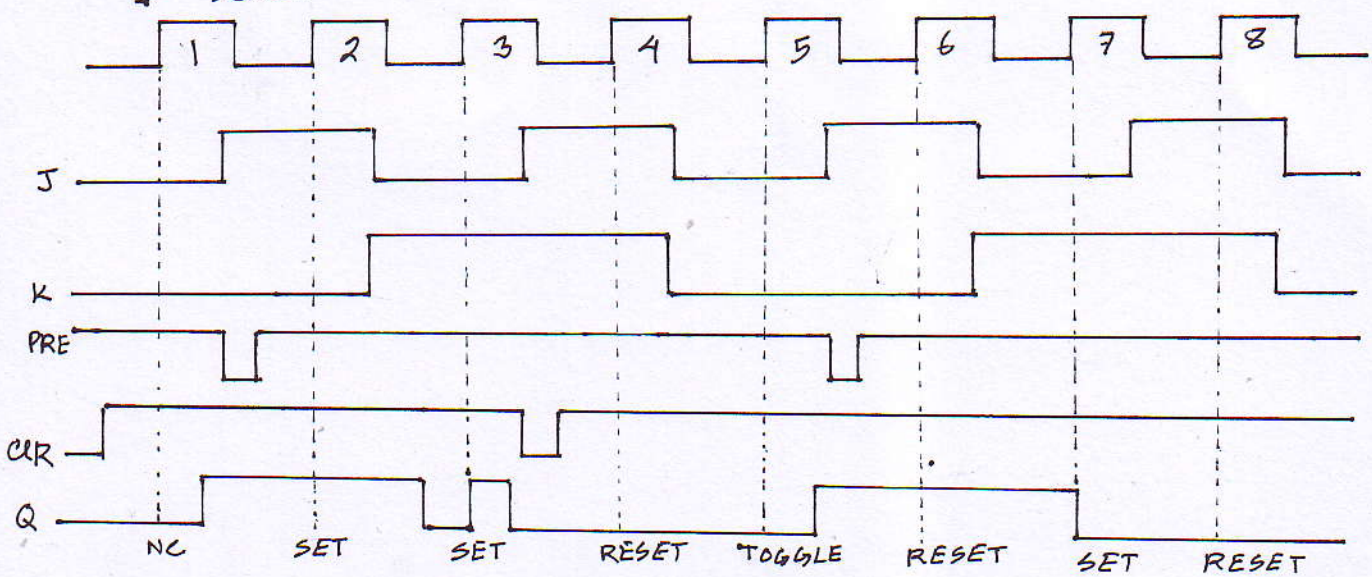


Fig: Logic symbol for a J-K flip-flop with active Low preset and clear inputs.

* Determine Q for the following inputs



MASTER SLAVE FLIP-FLOPS

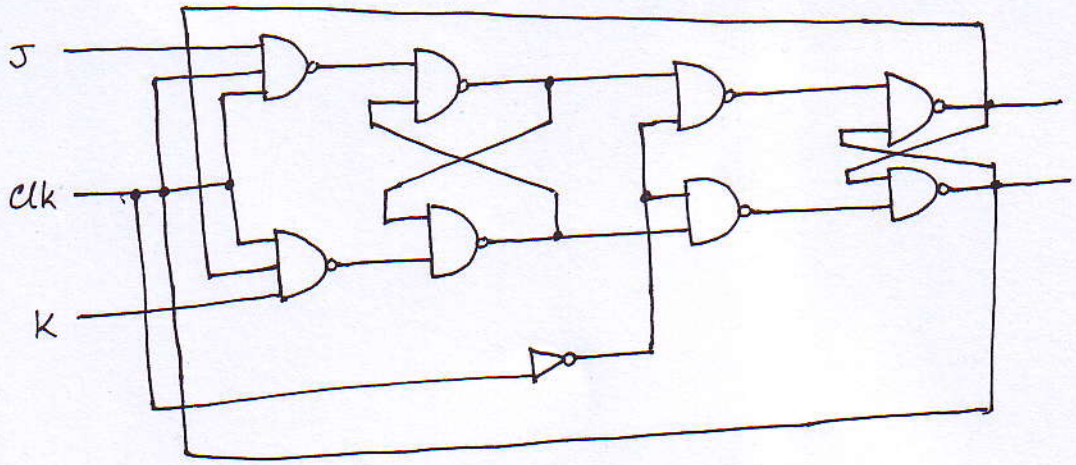
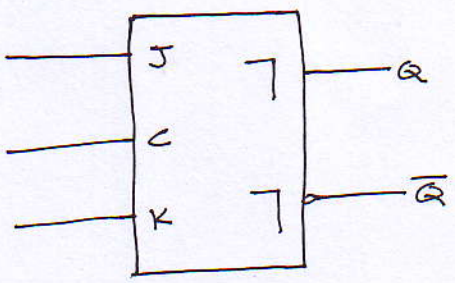


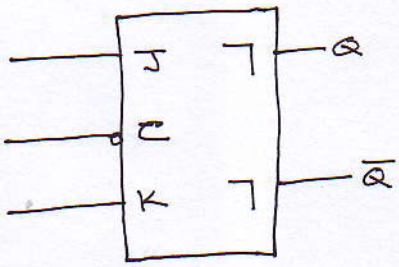
Fig : Logic diagram for a master slave J-K flip-flop

Truth table

Inputs			Outputs		Comments
J	K	clk	Q	$\overline{Q}$	
0	0	⊓	Q_0	$\overline{Q}_0$	No Change
0	1	⊓	0	1	RESET
1	0	⊓	1	0	SET
1	1	⊓	$\overline{Q}_0$	Q_0	Toggle

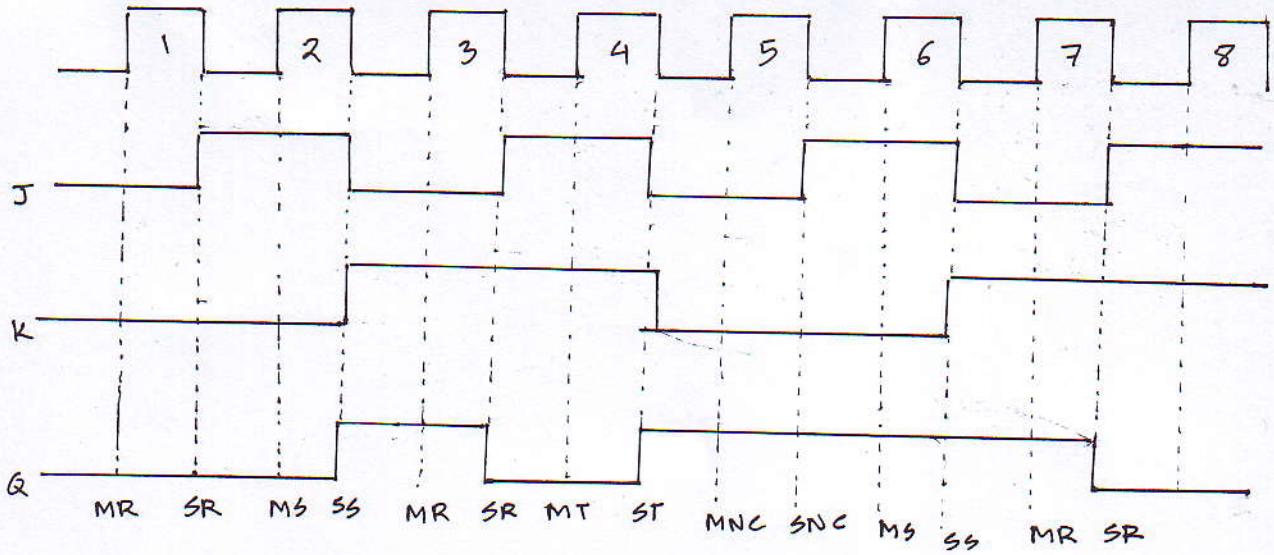


a) Data transferred to the output at the negative edge of the clock pulse



b) Data transferred to the output at the positive edge of the cloc pulse

Fig : Pulse triggered / Master Slave flip-flop



Determine Q if the flip-flop is initially RESET

D type Edge triggered flip-flop without pulse transition detecto

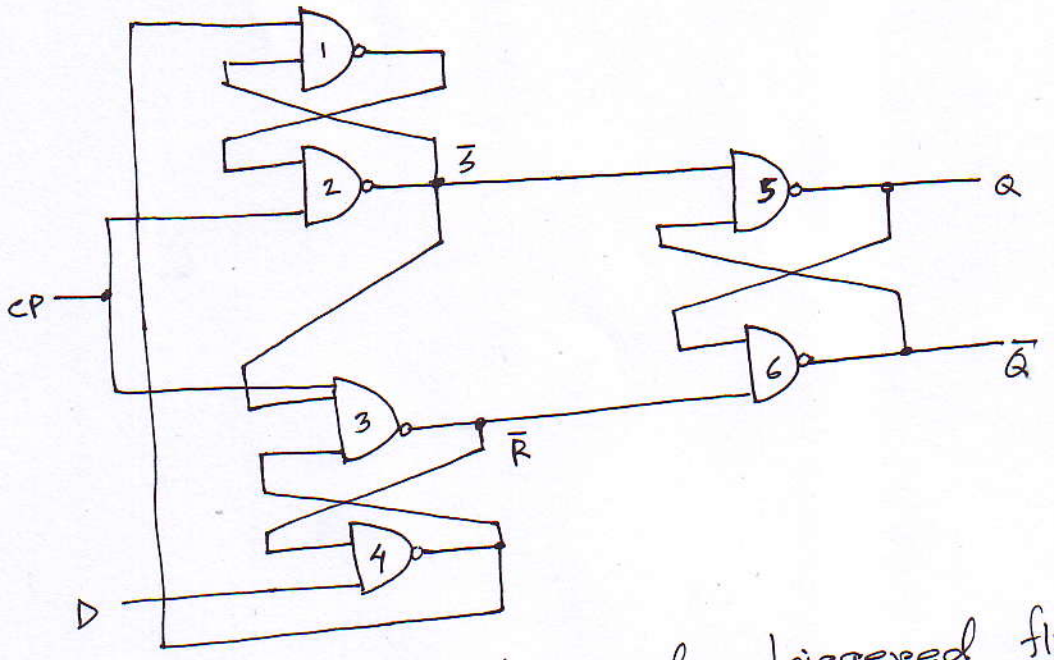


Fig : D type positive edge-triggered flip-flop.

Truth table of $\bar{S}\bar{R}$ latch

$\bar{S}$	$\bar{R}$	Q
0	1	1
1	0	0
0	0	Invalid
1	1	NC

CP	D	$\bar{S}$	$\bar{R}$	G1	G4
0	0	1	1	0	1
1	0→1	1	0	0	1
0	1	1	1	1	0
1	1→0	0	1	1	0→1