North South University

Department of Electrical and Computer Engineering

LAB REPORT-07

Course name: Digital Logic Design Lab

Course Code: 231.L

Experiment Number: 07

Experiment name: Introduction to Multiplexers and Decoders

Experiment Date: 20th April, 2021

Report Submission Date: 27th April, 2021

Section: 06

Group no: 04

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Remarks:	**Score:**

OBJECTIVES:

- Understand the concept of multiplexing in the context of digital logic circuits.
- Learn about the internal logic of digital multiplexers.
- Implement digital logic functions using multiplexers.
- Observe and analyze the operations of the 3 to 8 Line Decoder

THEORY:

Multiplexer:

Multiplexer is a combinational circuit that has maximum of 2^n data inputs, 'n' selection lines and single output line. One of these data inputs will be connected to the output based on the values of selection lines. Since there are 'n' selection lines, there will be 2^n possible combinations of zeros and ones. So, each combination will select only one data input. Multiplexer is also called as MUX. Example- 2:1 MUX, 4:1 MUX and so on.

Decoder:

A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^n out puts lines. One of these outputs will be active High based on the combination of inputs present, when the decoder is enabled. That means decoder detects a particular code. The outputs of the decoder are nothing but the min terms of 'n' input variables lines, when it is enabled. Example- 2x4 Decoder, 3x8 Decoder and so on.

EQUIPMENT LIST:

- Trainer Board
- 1 x IC 7404 Hex Inverter (NOT gates)
- 2 x IC 7411 3-input AND gates
- 1 x IC 7432 2-input OR gates
- IC 74151 (8:1 Multiplexer)
- IC 74138 (3 to 8 Line Decoder)

CIRCUIT DIAGRAM:

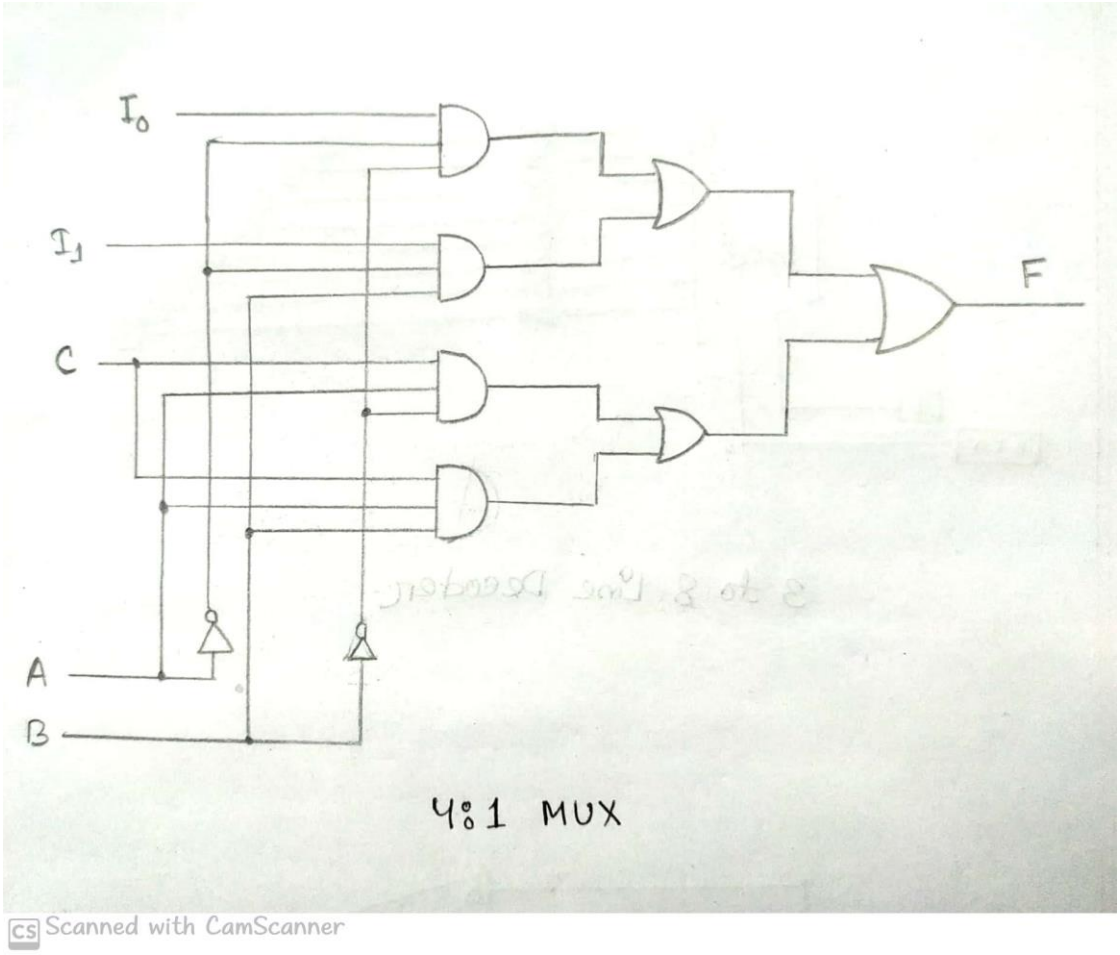

Figure D.1.1 *4:1 Multiplexer*

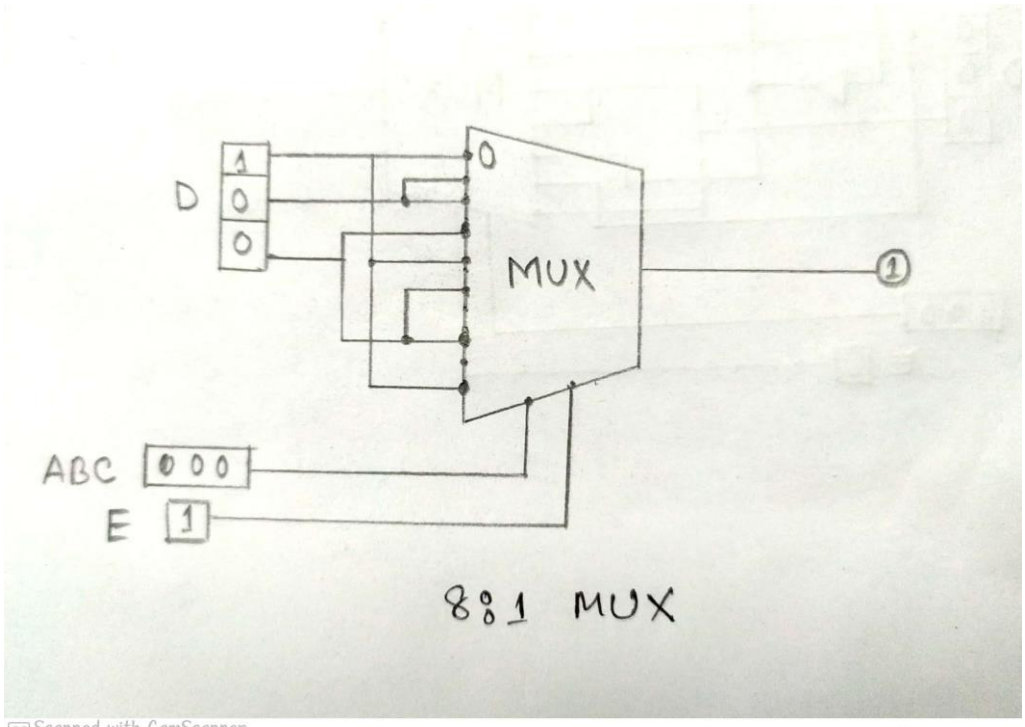

***Figure 2.1**: 8:1 Multiplexer to implement a Boolean function*

F (A, B, C, D) = Σ (0, 1, 3, 5, 8, 9, 14, 15)

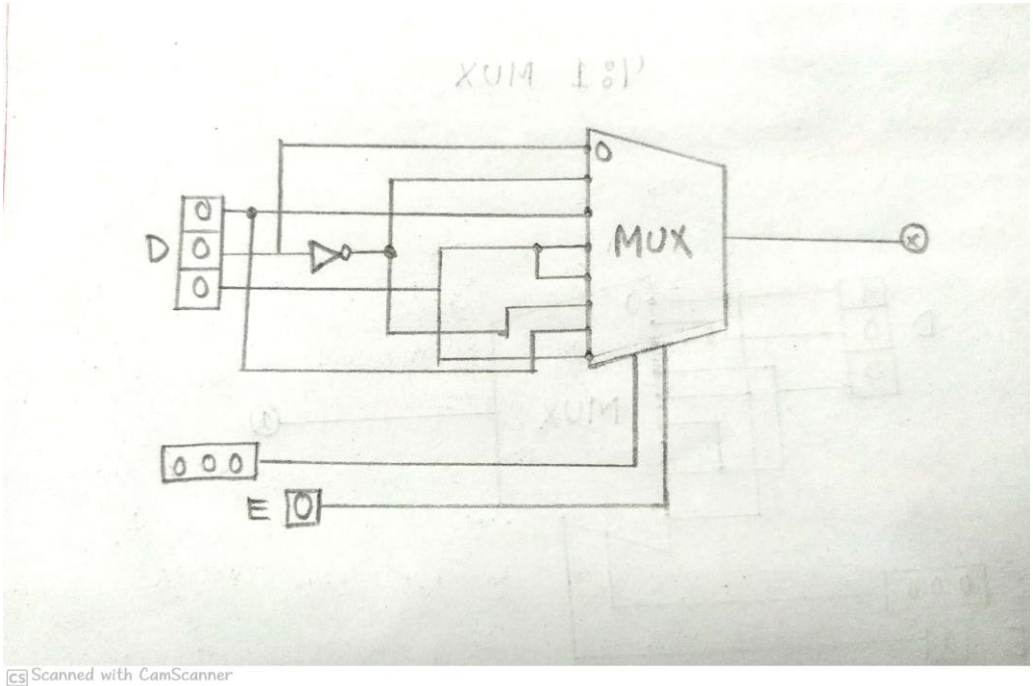

***Figure 2.1**: 8:1 Multiplexer to implement a Boolean function*

F (A, B, C, D) = Σ (1, 2, 4, 5, 10, 12, 13)

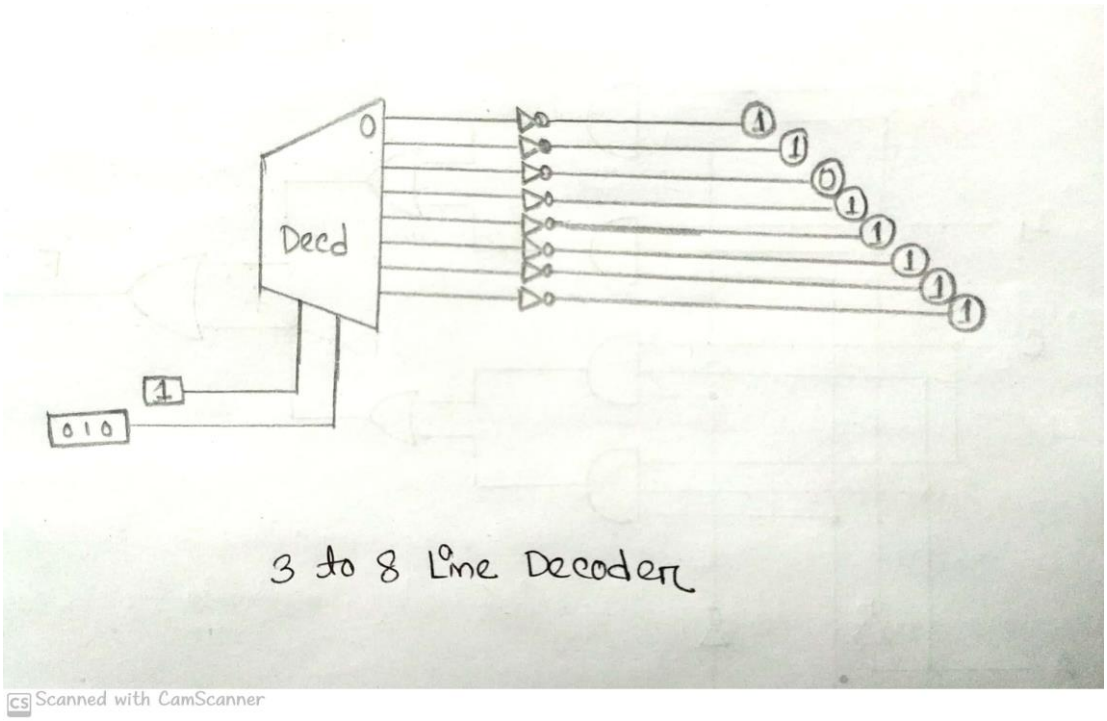

***Figure 3.1**: Implementing a 3 to 8 Line Decoder*

DATA & TABLE:

A	B	C	F (Theoretical)	Data Inputs	F (Practical)
0	0	0	**1**	I_0 = **1**	**1**
0	0	1	**1**		**1**
0	1	0	**0**	I_1 = **0**	**0**
0	1	1	**0**		**0**
1	0	0	**0**	I_2 = **C**	**0**
1	0	1	**1**		**1**
1	1	0	**0**	I_3 = **C**	**0**
1	1	1	**1**		**1**

***Table F.1.1**: Implementing a Boolean function using a 4:1 MUX*

A	B	C	D	F (Theoretical)	Data Inputs	F (Practical)
0	0	0	0	**1**	I_0 = **1**	**1**
0	0	0	1	**1**		**1**
0	0	1	0	**0**	I_1 = **D**	**0**
0	0	1	1	**1**		**1**
0	1	0	0	**0**	I_2 = **D**	**0**
0	1	0	1	**1**		**1**
0	1	1	0	**0**	I_3 = **0**	**0**
0	1	1	1	**0**		**0**
1	0	0	0	**1**	I_4 = **1**	**1**
1	0	0	1	**1**		**1**
1	0	1	0	**0**	I_5 = **0**	**0**
1	0	1	1	**0**		**0**
1	1	0	0	**0**	I_6 = **0**	**0**
1	1	0	1	**0**		**0**
1	1	1	0	**1**	I_7 = **1**	**1**
1	1	1	1	**1**		**1**

F.2.1: *Using an 8:1 MUX to implement a Boolean function*

Enable Inputs		Select Inputs			Outputs							
G_1	**G_2**	**C**	B	A	Y_0	**Y_1**	**Y_2**	**Y_3**	**Y_4**	**Y_5**	**Y_6**	**Y_7**
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	**L**	**H**	**H**	**H**	**H**	**H**	**H**	**H**
H	L	L	L	H	**H**	**L**	**H**	**H**	**H**	**H**	**H**	**H**
H	L	L	H	L	**H**	**H**	**L**	**H**	**H**	**H**	**H**	**H**
H	L	L	H	H	**H**	**H**	**H**	**L**	**H**	**H**	**H**	**H**
H	L	H	L	L	**H**	**H**	**H**	**H**	**L**	**H**	**H**	**H**
H	L	H	L	H	**H**	**H**	**H**	**H**	**H**	**L**	**H**	**H**
H	L	H	H	L	**H**	**H**	**H**	**H**	**H**	**H**	**L**	**H**
H	L	H	H	H	**H**	**H**	**H**	**H**	**H**	**H**	**H**	**L**

F.3.1: *3 to 8 Line Decoder*

A	B	C	D	F (Theoretical)	Data Inputs	F (Practical)
0	0	0	0	**0**	I_0 = **D**	**0**
0	0	0	1	**1**		**1**
0	0	1	0	**1**	I_1 = **D'**	**1**
0	0	1	1	**0**		**0**
0	1	0	0	**1**	I_2 = **1**	**1**
0	1	0	1	**1**		**1**
0	1	1	0	**0**	I_3 = **0**	**0**
0	1	1	1	**0**		**0**
1	0	0	0	**0**	I_4 = **0**	**0**
1	0	0	1	**0**		**0**
1	0	1	0	**1**	I_5 = **D'**	**1**
1	0	1	1	**0**		**0**
1	1	0	0	**1**	I_6 = **1**	**1**
1	1	0	1	**1**		**1**
1	1	1	0	**0**	I_7 = **0**	**0**
1	1	1	1	**0**		**0**

Table: *For function* ***F (A, B, C, D) = Σ (1, 2, 4, 5, 10, 12, 13)***

8:1 MUX implementation ***(report section).***

QUESTIONS:

E.3 Q: Explain the difference between an active-high and an active-low device.

Ans:

Active-High Device:A signal ‘active-high’ means that signal will be performing when its logical value is ‘1’. Active-high device works when the enable input is active high or ‘1’. If the circuit uses "active high" logic, 5 volts represents a digital "1" and 0 volts represents a digital "0".

Active-Low Device: A signal ‘active-low’ means that signal will be performing when its logical value is ‘0’. Active-low device works when the enable input is active low or ‘0’. If the circuit uses "active low" logic, 5 volts represents a digital "0" and 0 volts represents a digital "1".

RESULT ANALYSIS AND DISCUSSION:

The overall lab experiment was about the structures and implementations of multiplexers and decoders.

At the beginning of the experiment, the task was to build a 4:1 MUX. So we designed it using logic gates as well as IC diagram. We needed 4 2-input AND gates and 3 2-input OR gates to design 4:1 MUX. We implemented a function, F (A, B, C) = Σ (0, 1, 5, 7) using 4:1 MUX and completed necessary truth table by drawing Karnaugh Map.

The 2nd experiment was to implement a Boolean function using 8:1 MUX and the function was F(A, B, C, D) = Σ (0, 1, 3, 5, 8, 9, 14, 15). We used A, B, C as selector variables and D as input variable. By drawing Karnaugh Map, we got the required 8 inputs. By completing necessary truth table, we got the expected outputs. And the outputs received from truth table and outputs received from designed circuit were same. Following this same way, we implemented another function, F(A, B, C, D) = Σ (1, 2, 4, 5, 10, 12, 13). Then we did 3 to 8-line decoder for the 3rd experiment. We completed the necessary truth table using enable inputs. The outputs of the truth table show diagonally ‘L’ which means active-low. Rest of the outputs show ‘H’ which means active-high. We drew the circuit diagram then. During the experiments, Logisim worked perfectly. So we didn’t face any issue.

From the experiment, we learned about the internal structures and logical implementations of different types of multiplexers and decoders.

CONTRIBUTION

NAME	CONTRIBUTION IN
Khalid Bin Shafiq	**RESULT ANALYSIS AND DISCUSSION**
Rafidul Islam	**CIRCUIT DIAGRAM**
Rashiqur Rahman Rifat	**THEORY**
Towsif Muhtadi Khan	**DATA & TABLE, COORDINATOR**

F.1 Experimental Data: Implementing a Boolean function using a 4:1 MUX:

A	B	C	F (Theoretical)	Data Inputs	F (Practical)
0	0	0	**1**	I_0 = **1**	**1**
0	0	1	**1**		**1**
0	1	0	**0**	I_1 = **0**	**0**
0	1	1	**0**		**0**
1	0	0	**0**	I_2 = **C**	**0**
1	0	1	**1**		**1**
1	1	0	**0**	I_3 = **C**	**0**
1	1	1	**1**		**1**

Table F.1.1

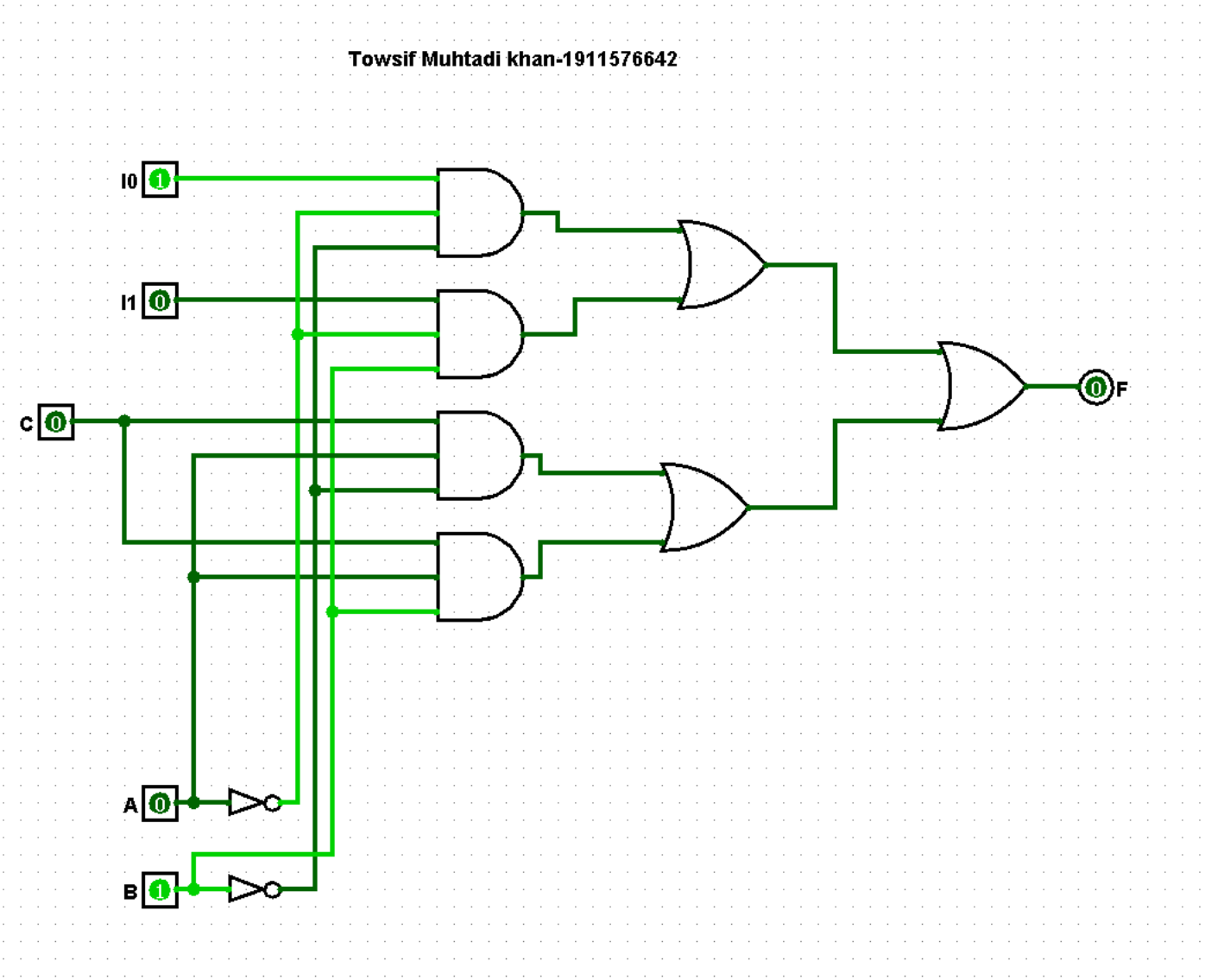

Figure F.1

F.2 Experimental Data: Using an 8:1 MUX to implement a Boolean function:

A	B	C	D	F (Theoretical)	Data Inputs	F (Practical)
0	0	0	0	**1**	I_0 = **1**	**1**
0	0	0	1	**1**		**1**
0	0	1	0	**0**	I_1 = **D**	**0**
0	0	1	1	**1**		**1**
0	1	0	0	**0**	I_2 = **D**	**0**
0	1	0	1	**1**		**1**
0	1	1	0	**0**	I_3 = **0**	**0**
0	1	1	1	**0**		**0**
1	0	0	0	**1**	I_4 = **1**	**1**
1	0	0	1	**1**		**1**
1	0	1	0	**0**	I_5 = **0**	**0**
1	0	1	1	**0**		**0**
1	1	0	0	**0**	I_6 = **0**	**0**
1	1	0	1	**0**		**0**
1	1	1	0	**1**	I_7 = **1**	**1**
1	1	1	1	**1**		**1**

Table F.2.1

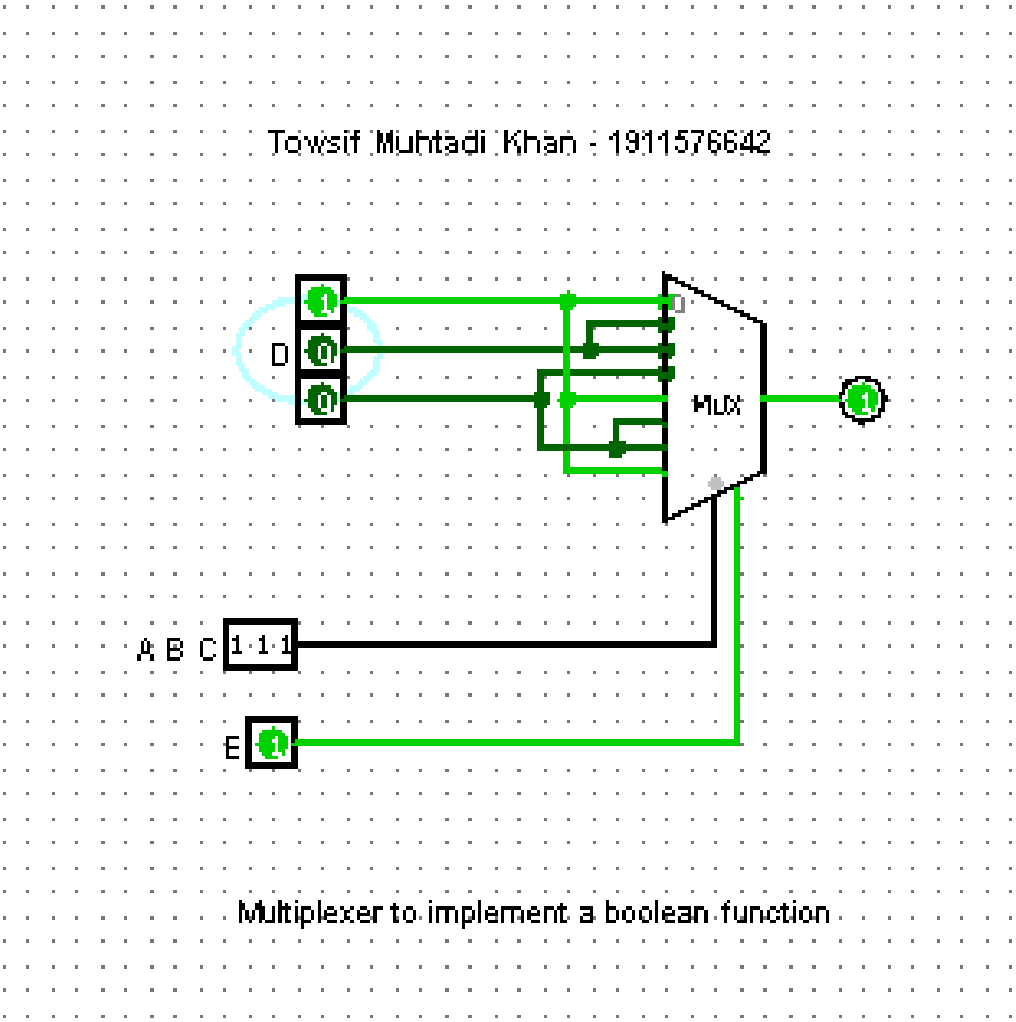

Figure F.2.1

F.3 Experimental Data: 3 to 8 Line Decoder:

Enable Inputs		Select Inputs			Outputs							
G1	G2	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

Table F.3.1

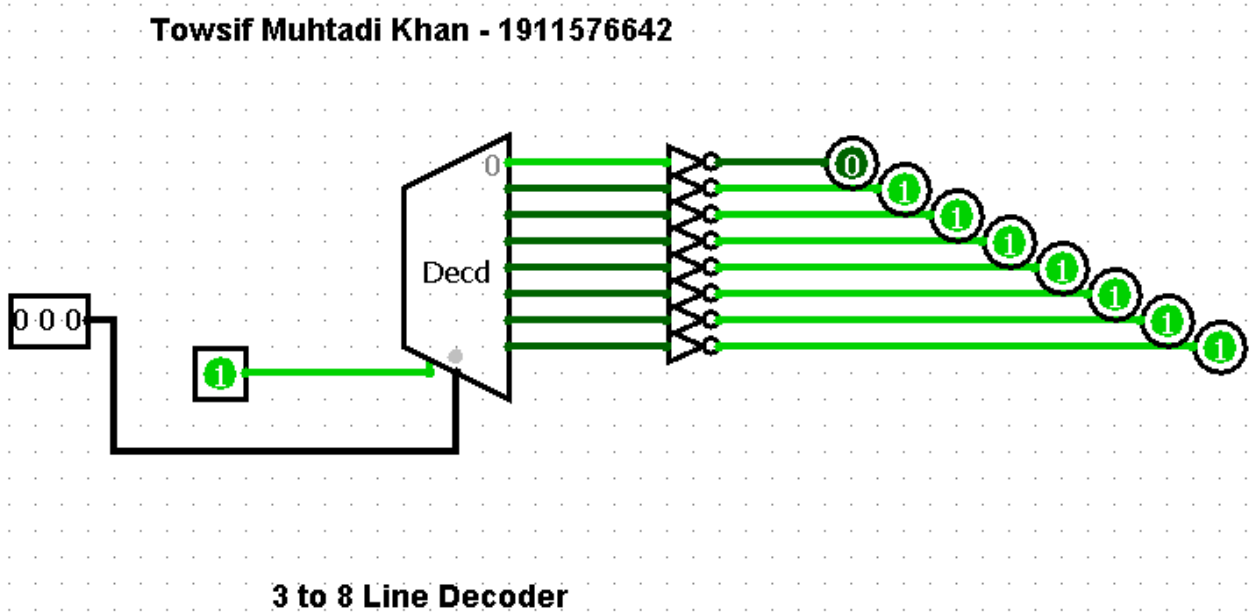

Figure F.3

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