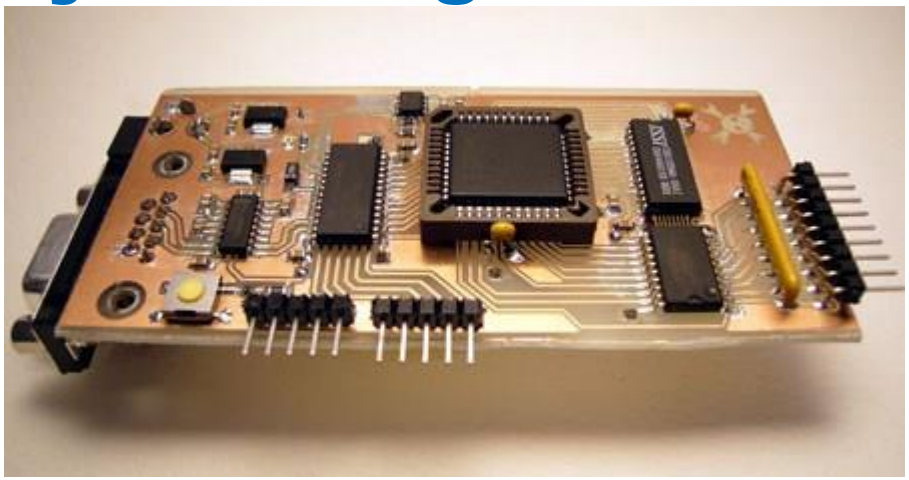
EEE 211/ETE 211
Digital Logic Design

Memory and Programmable Logic



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Introduction

- A memory unit is a device to which binary information is transferred for storage and from which information is retrieved when needed for processing.

- Binary information received from an input device is stored in memory,
- and information transferred to an output device is taken from memory.

- A memory unit is a collection of cells capable of storing a large quantity of binary information.

Introduction

- **There are two types of memories that are used in digital systems:**

  Random-access memory(RAM): perform both the write and read operations.

  Read-only memory(ROM): perform only the read operation.

- **The read-only memory is a programmable logic device (PLD).**
- **Other such units are the programmable logic array(PLA), the programmable array logic(PAL), and the field-programmable gate array(FPGA).**

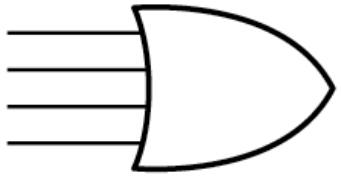
  A PLD is an integrated circuit with internal logic gates connected through electronic paths

Introduction

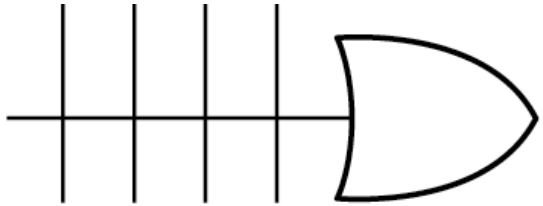
- RAM stores new information for later use.
- The process of storing new information into memory is referred to as a memory *write operation.*
- The process of transferring the stored information out of memory is referred to as a memory *read operation.*
- RAM can perform both write and read operations.
- ROM can perform only the read operation.
- This means that suitable binary information is already stored inside memory and can be retrieved or read at any time.

Array logic

- A typical programmable logic device may have hundreds to millions of gates interconnected through hundreds to thousands of internal paths.
- In order to show the internal logic diagram in a concise form, it is necessary to employ a special gate symbology applicable to array logic.



(a) Conventional symbol



(b) Array logic symbol

Fig. 7-1 Conventional and Array Logic Diagrams for OR Gate

Random-Access Memory

•A memory unit is a collection of storage cells, together with associated circuits needed to transfer information into and out of a device.

- A memory unit stores binary information in groups of bits called words. 1 byte = 8 bits

  1 word = 2 bytes

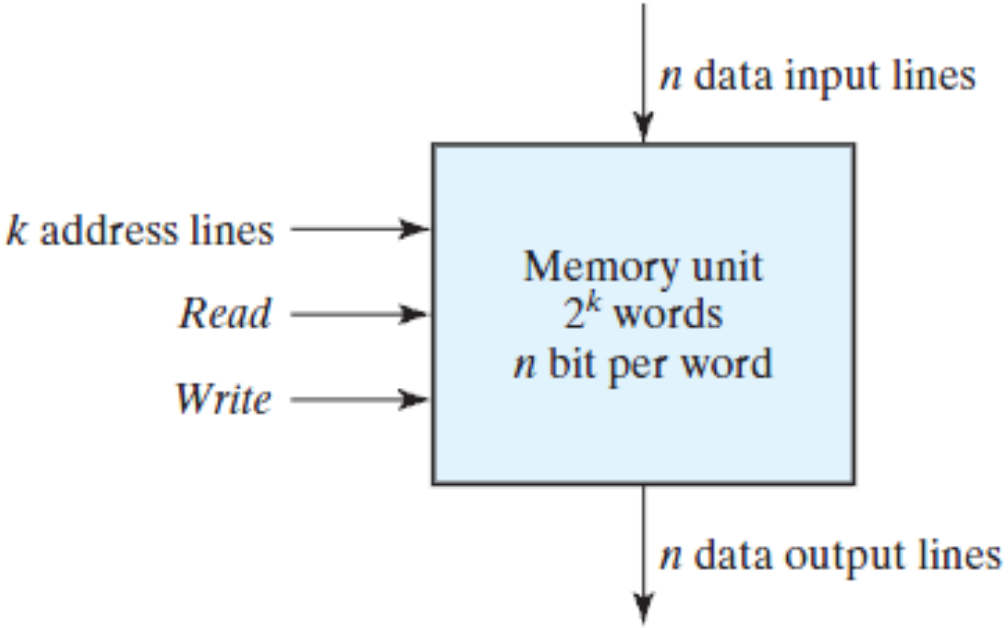
•A memory word is a group of 1's and 0's and may represent a number, an instruction, one or more alphanumeric characters, or any other binary-coded information.

•Most computer memories use words that are multiples of 8 bits in length.

Random-Access Memory

•The capacity of a memory unit is usually stated as the total number of bytes that the unit can store.

- The communication between a memory and its environment is achieved through data input and output lines, address selection lines, and control lines that specify the direction of transfer.

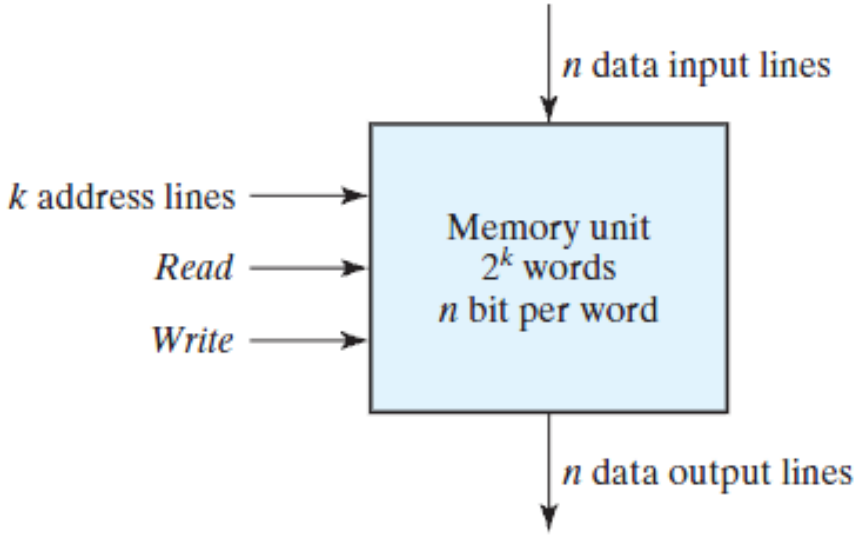


Block diagram of a memory unit

Random-Access Memory

- The *n data input lines* provide the information to be stored in memory, and the *n data output lines supply the* information coming out of memory

- The *k address lines specify the particular word* chosen among the many available.



- The *Write input causes binary data to be transferred into the memory, and*
- the *Read input causes binary data to be transferred out of memory.*

- The address lines select one particular word.

Content of a memory

- Each word in memory is assigned an identification number, called an address, starting from 0 up to 2^k-1, where k is the number of address lines.
- The number of words in a memory with one of the letters K=2^{10}, M=2^{20}, or G=2^{30}.

  64K = 2^{16} 2M = 2^{21}

  4G = 2^{32}

•Memories vary greatly in size and may range from 1,024 words, requiring an address of 10 bits, to 2^{32} words, requiring 32 address bits.

Memory address		Memory contest
Binary	decimal	
0000000000	0	1011010101011101
0000000001	1	1010101110001001
0000000010	2	0000110101000110
⋮	⋮	⋮
1111111101	1021	1001110100010100
1111111110	1022	0000110100011110
1111111111	1023	1101111000100101

Fig. 7-3 Content of a 1024 × 16 Memory

Content of a memory

Consider, for example, a memory unit with a capacity of 1K words of 16 bits each. Since 1K = 1,024 = 2^{10} and 16 bits constitute two bytes, we can say that the memory can accommodate 2,048 = 2K bytes.

Memory address		Memory contest
Binary	decimal	
0000000000	0	1011010101011101
0000000001	1	1010101110001001
0000000010	2	0000110101000110
⋮	⋮	⋮
1111111101	1021	1001110100010100
1111111110	1022	0000110100011110
1111111111	1023	1101111000100101

Fig. 7-3 Content of a 1024 × 16 Memory

- A word in memory is selected by its binary address.
- When a word is read or written, the memory operates on all 16 bits as a single unit.

Content of a memory

- The 1K * 16 memory of Fig. 7.3 has 10 bits in the address and 16 bits in each word.

- As another example, a 64K * 10 memory will have 16 bits in the address (since 64K = 2^{16}) and each word will consist of 10 bits.

Memory address		
Binary	decimal	Memory contest
0000000000	0	1011010101011101
0000000001	1	1010101110001001
0000000010	2	0000110101000110
⋮	⋮	⋮
1111111101	1021	1001110100010100
1111111110	1022	0000110100011110
1111111111	1023	1101111000100101

Fig. 7-3 Content of a 1024 × 16 Memory

Write and Read operations

Transferring a new word to be stored into memory:

1. Apply the binary address of the desired word to the address lines.
2. Apply the data bits that must be stored in memory to the data input lines.
3. Activate the write input.

The memory unit will then take the bits from the input data lines and store them in the word specified by the address lines.

Write and Read operations

- Transferring a stored word out of memory:

1. Apply the binary address of the desired word to the address lines.
2. Activate the read input.

- Commercial memory sometimes provide the two control inputs for reading and writing in a somewhat different configuration

Table 7-1
Control Inputs to Memory Chip

Memory Enable	Read/Write	Memory Operation
0	X	None
1	0	Write to selected word
1	1	Read from selected word

•The steps that must be taken for the purpose of transferring a stored word out of memory

Write and Read operations

- The memory unit will then take the bits from the word that has been selected by the address and apply them to the output data lines.

- The contents of the selected word do not change after the read operation, i.e., the word operation is nondestructive.

Types of memories

- In **random-access memory:**
  - the word locations may be thought of as being separated in space, with each word occupying one particular location.
  - the access time is always the same regardless of the particular location of the word.
- In **sequential-access memory:**
  - the information stored in some medium is not immediately accessible, but is available only certain intervals of time. A magnetic disk or tape unit is of this type.
  - the time it takes to access a word depends on the position of the word with respect to the reading head position; therefore, the access time is variable.

Static RAM (SRAM):

- SRAM consists essentially of internal latches that store the binary information.
- The stored information remains valid as long as power is applied to the unit.
- SRAM is easier to use and has shorter read and write cycles.
- Low density, low capacity, high cost, high speed, high power consumption.

Dynamic RAM (DRAM):

- DRAM stores the binary information in the form of electric charges on capacitors.
- The capacitors are provided inside the chip by MOS transistors.
- The capacitors tends to discharge with time and must be periodically recharged by refreshing the dynamic memory.
- DRAM offers reduced power consumption and larger storage capacity in a single memory chip.
- High density, high capacity, low cost, low speed, low power consumption.

- **Volatile Memory:**
  - units that lose stored information when power is turned off are said to be volatile
  - Both static and dynamic, are of this category since the binary cells need external power to maintain the stored information.
- **Nonvolatile memory:**
  - such as magnetic disk, ROM, retains its stored information after removal of power.

Memory decoding

- The equivalent logic of a binary cell that stores one bit of information is shown below.

  Read/$\overline{\text{Write}}$ = 0, select = 1, input data to S-R latch

  Read/$\overline{\text{Write}}$ = 1, select = 1, output data from S-R latch

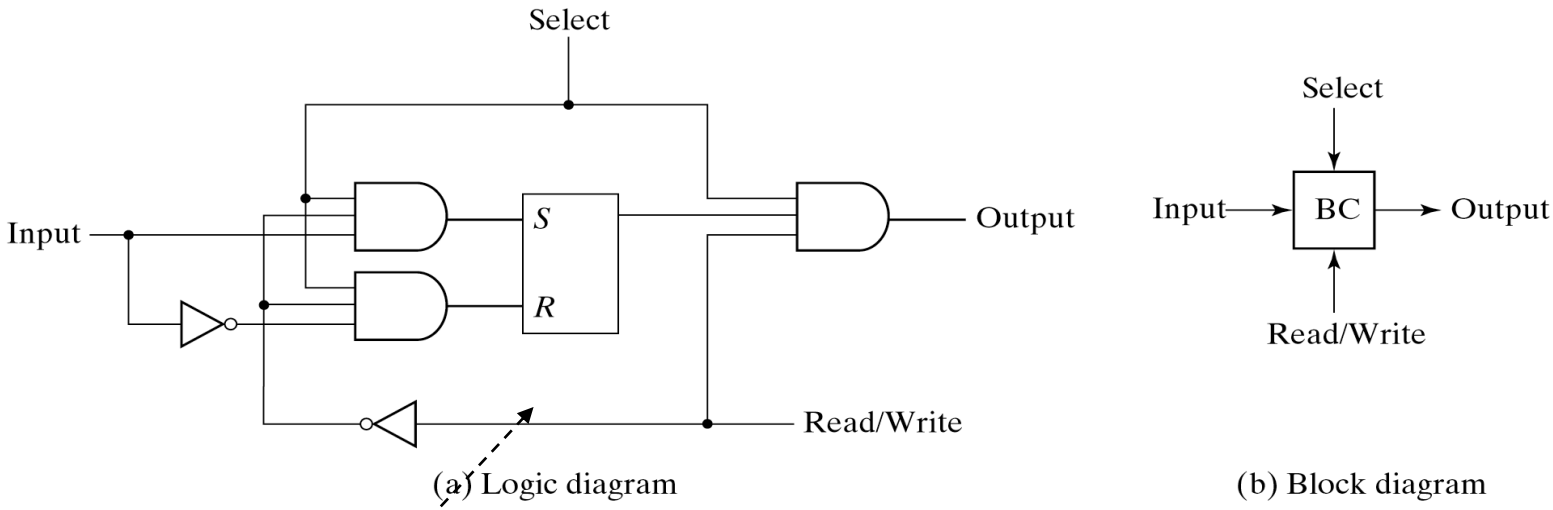


Fig. 7-5 Memory Cell

SR latch with NOR gates

4X4 RAM

- There is a need for decoding circuits to select the memory word specified by the input address.
- During the read operation, the four bits of the selected word go through OR gates to the output terminals.
- During the write operation, the data available in the input lines are transferred into the four binary cells of the selected word.

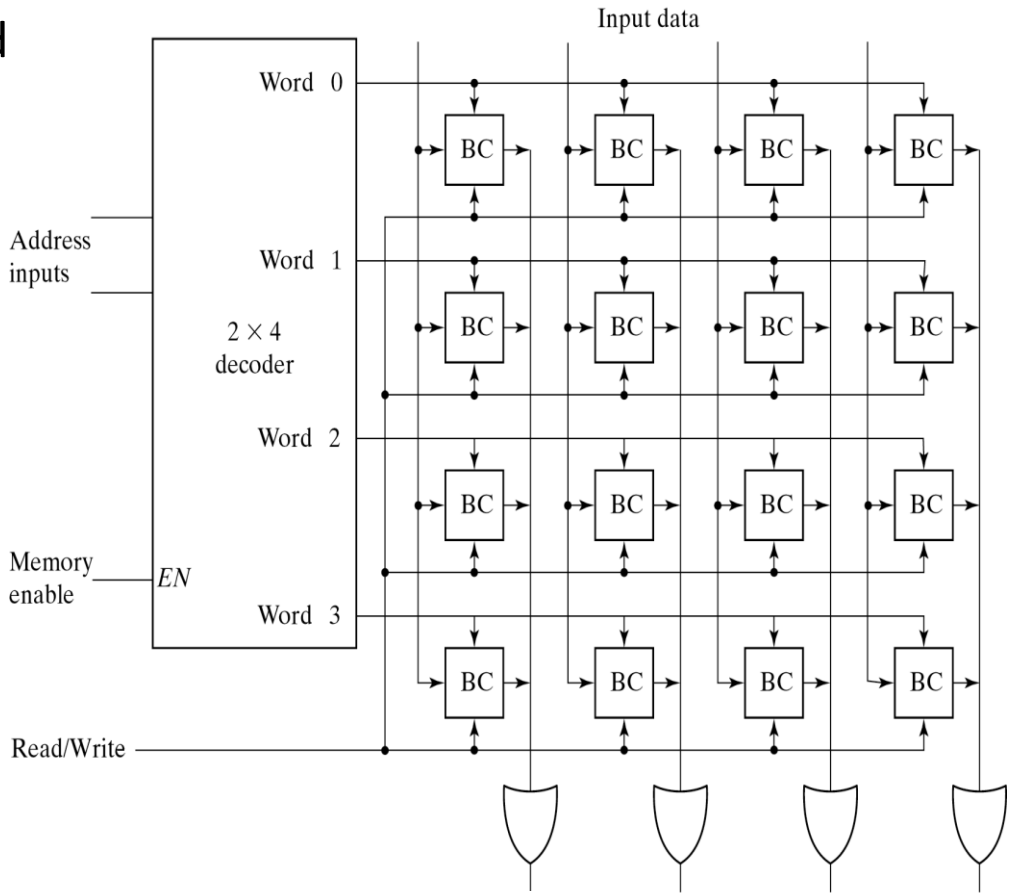
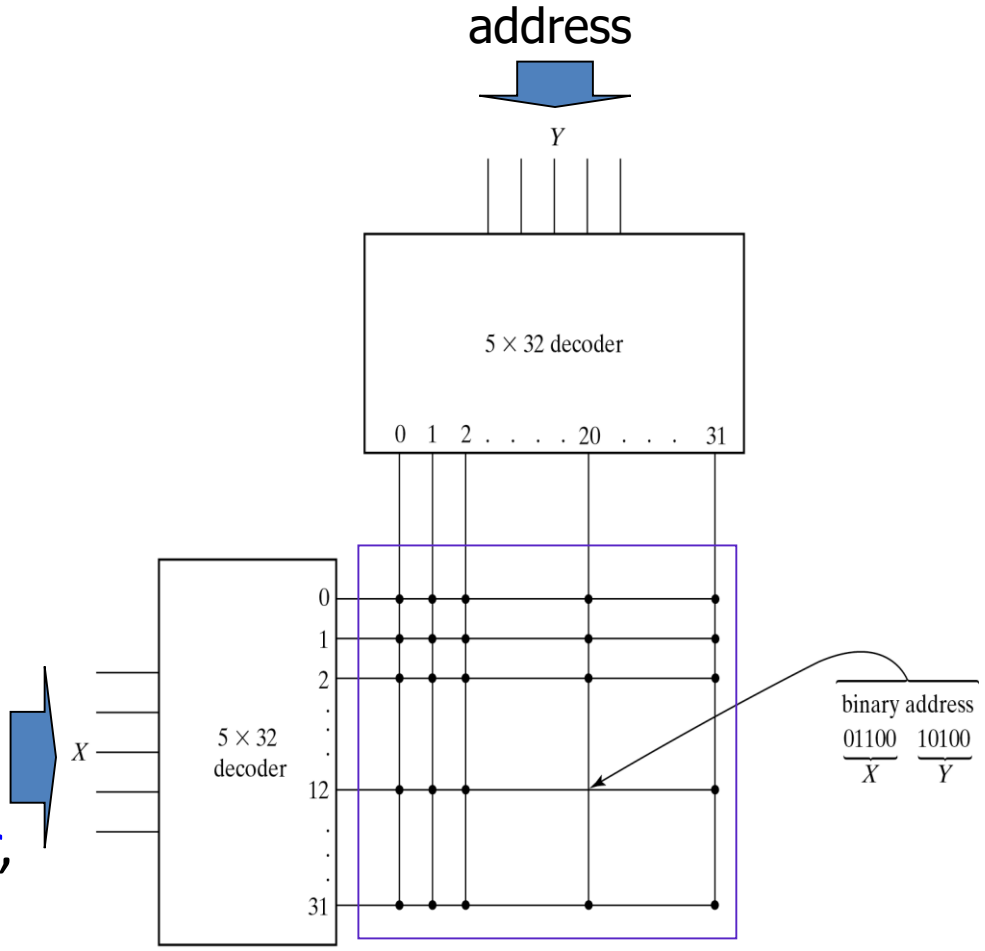


Diagram of a 4×4 RAM

- A memory with 2^k words of n bits per word requires k address lines that go into $kx2^k$ decoder.

Coincident decoding

- A decoder with k inputs and 2^k outputs requires 2^k AND gates with k inputs per gate.
- Two decoding in a two-dimensional selection scheme can reduce the number of inputs per gate.
- 1K-word memory, instead of using a single 10X1024 decoder, we use two 5X32 decoders.



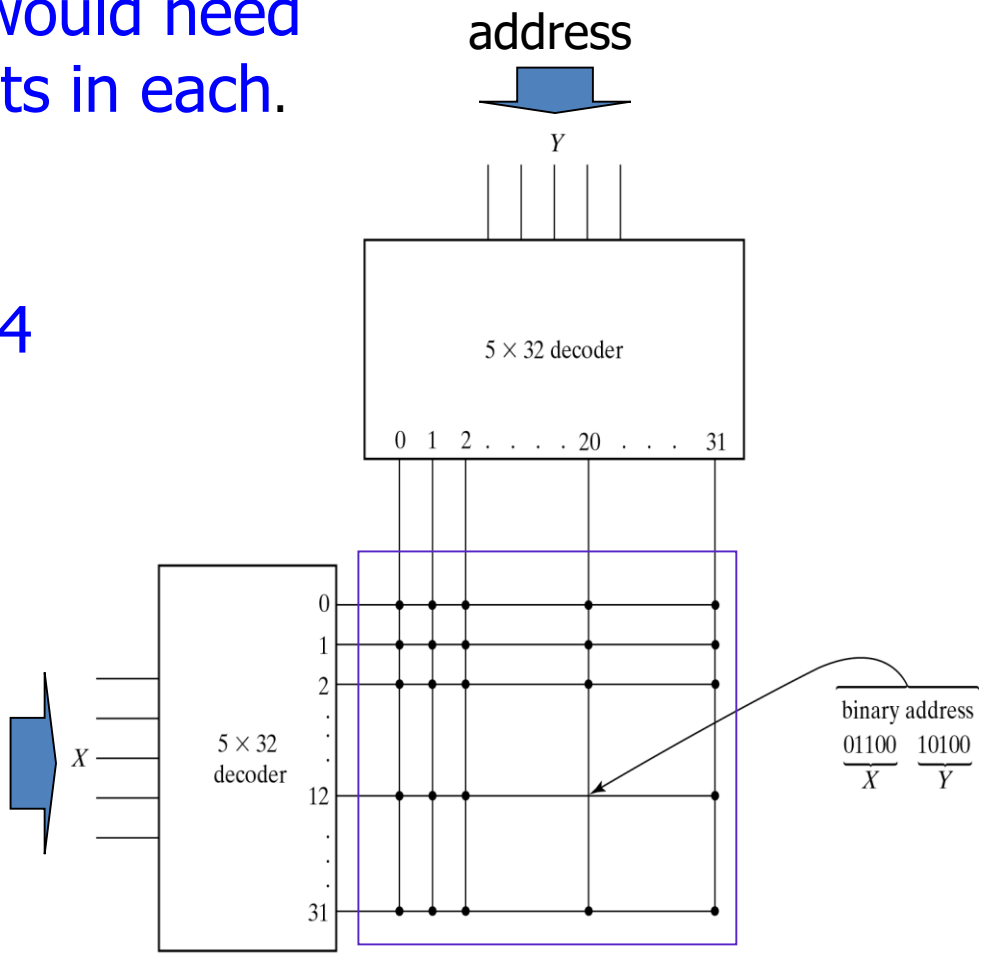
Two-dimensional decoding structure for a 1K-word memory

Coincident decoding

- With the single decoder, we would need 1,024 AND gates with 10 inputs in each.

- In the two-decoder case, we need 64 AND gates with 5 inputs in each.

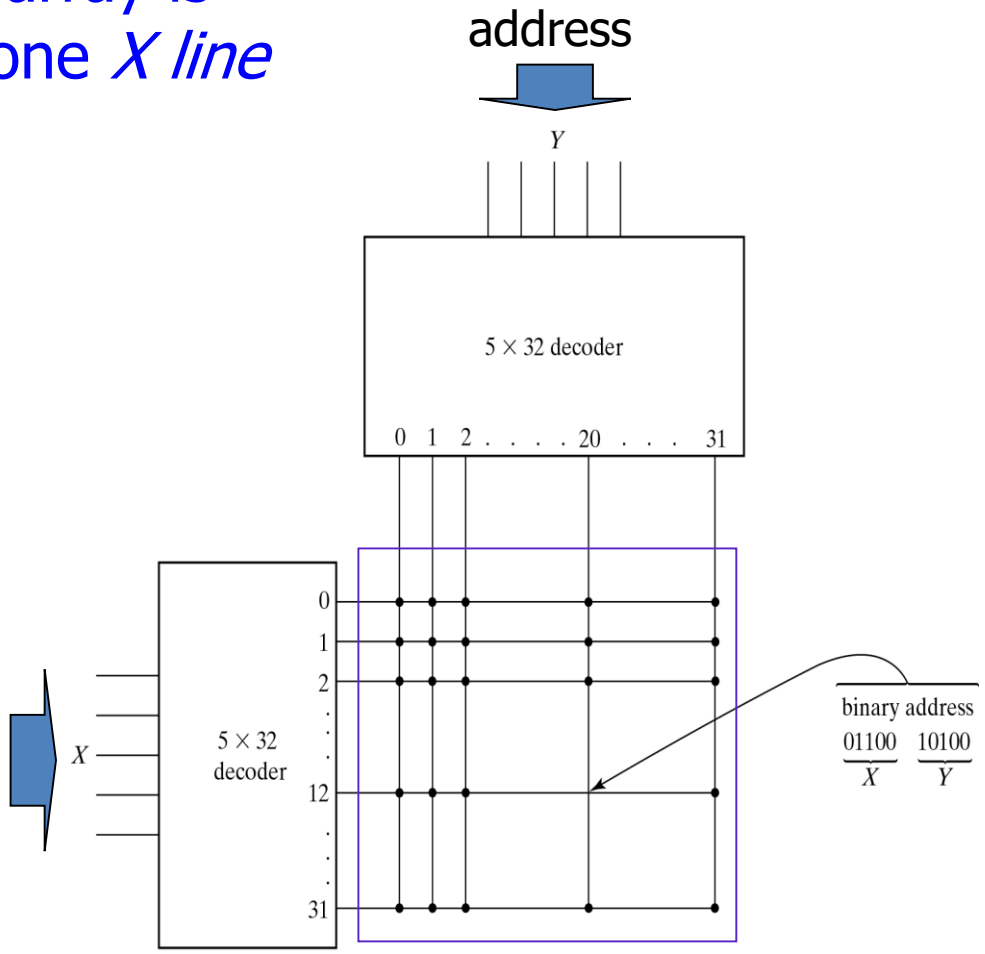
- The five most significant bits of the address go to input *X and the five least significant bits go to input Y.*



Two-dimensional decoding structure for a 1K-word memory

Coincident decoding

- Each word within the memory array is selected by the coincidence of one *X line and one Y* line.
- Thus, each word in memory is selected by the coincidence between 1 of 32 rows and 1 of 32 columns, for a total of 1,024 words.
- each intersection represents a word that may have any number of bits.



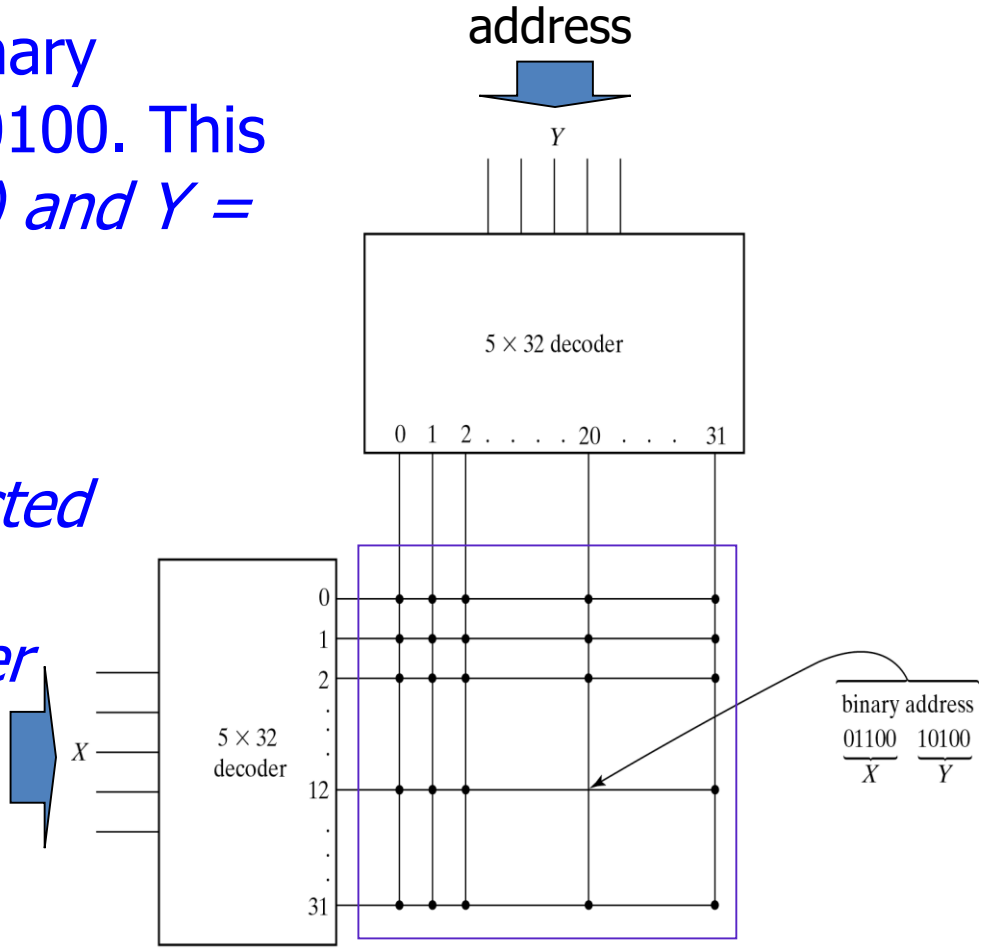
Two-dimensional decoding structure for a 1K-word memory

Coincident decoding

- As an example, consider the word whose address is 404. The 10-bit binary equivalent of 404 is 01100 10100. This makes *X = 01100 (binary 12) and Y = 10100 (binary 20).*

- The *n -bit word that is selected lies in the X decoder output number 12 and the Y decoder* output number 20.

- All the bits of the word are selected for reading or writing.



Two-dimensional decoding structure for a 1K-word memory