Digital Logic Design

Lecture 13:

Multiplexers: (Data Selector)

A digital multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line

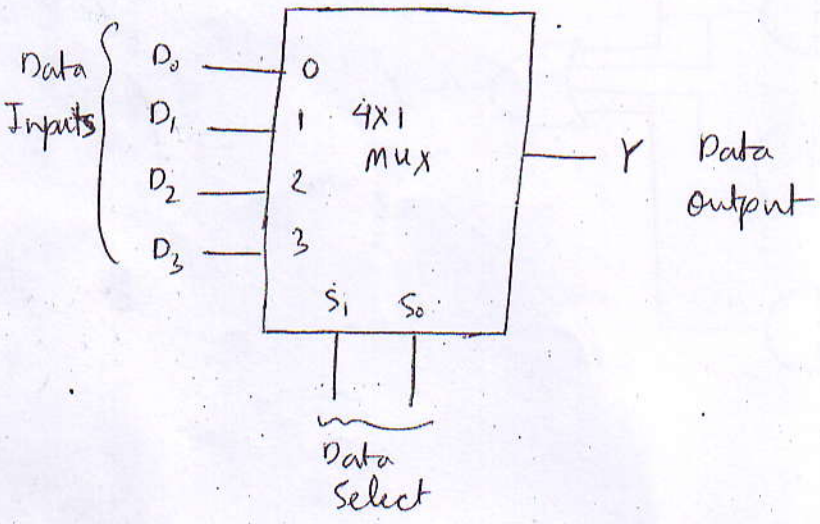


Fig: Logic symbol for a 1-of-4 multiplexer

Data-select Inputs		output
S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

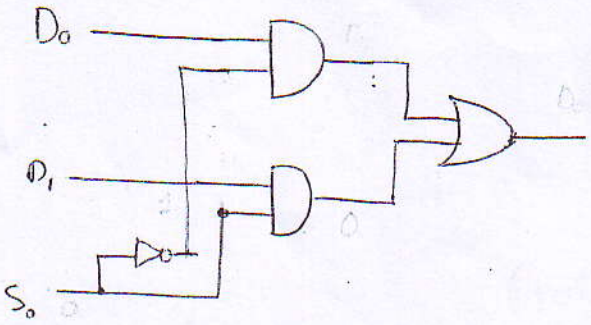


Fig: Logic diagram of a 1-of-2 multiplexer

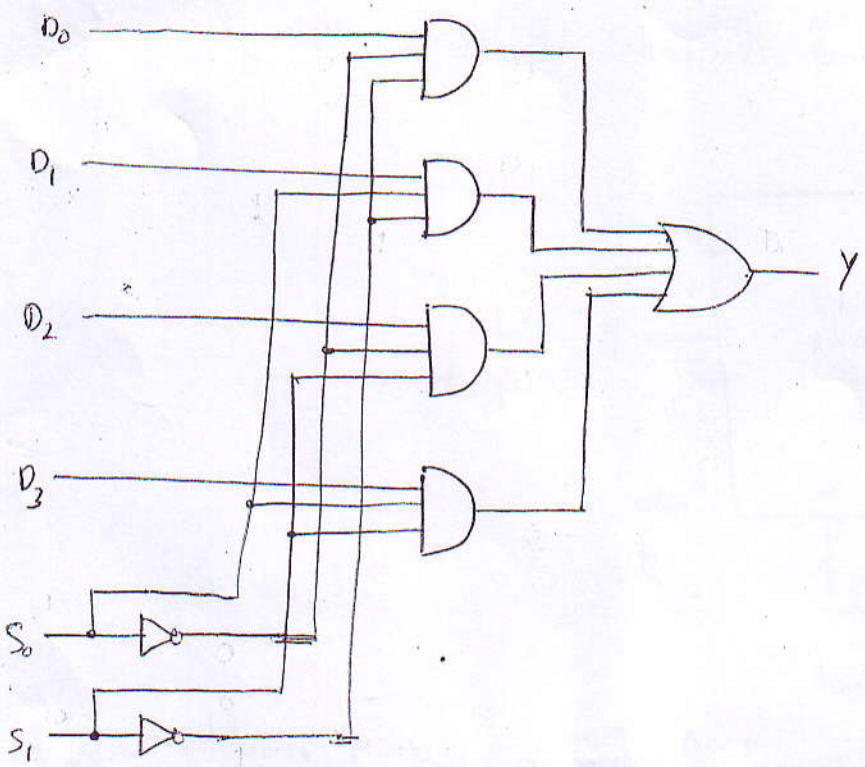


Fig: Logic diagram for a 1-of-4 multiplexer

Quadruple 2-Input Data Selector / multiplexer

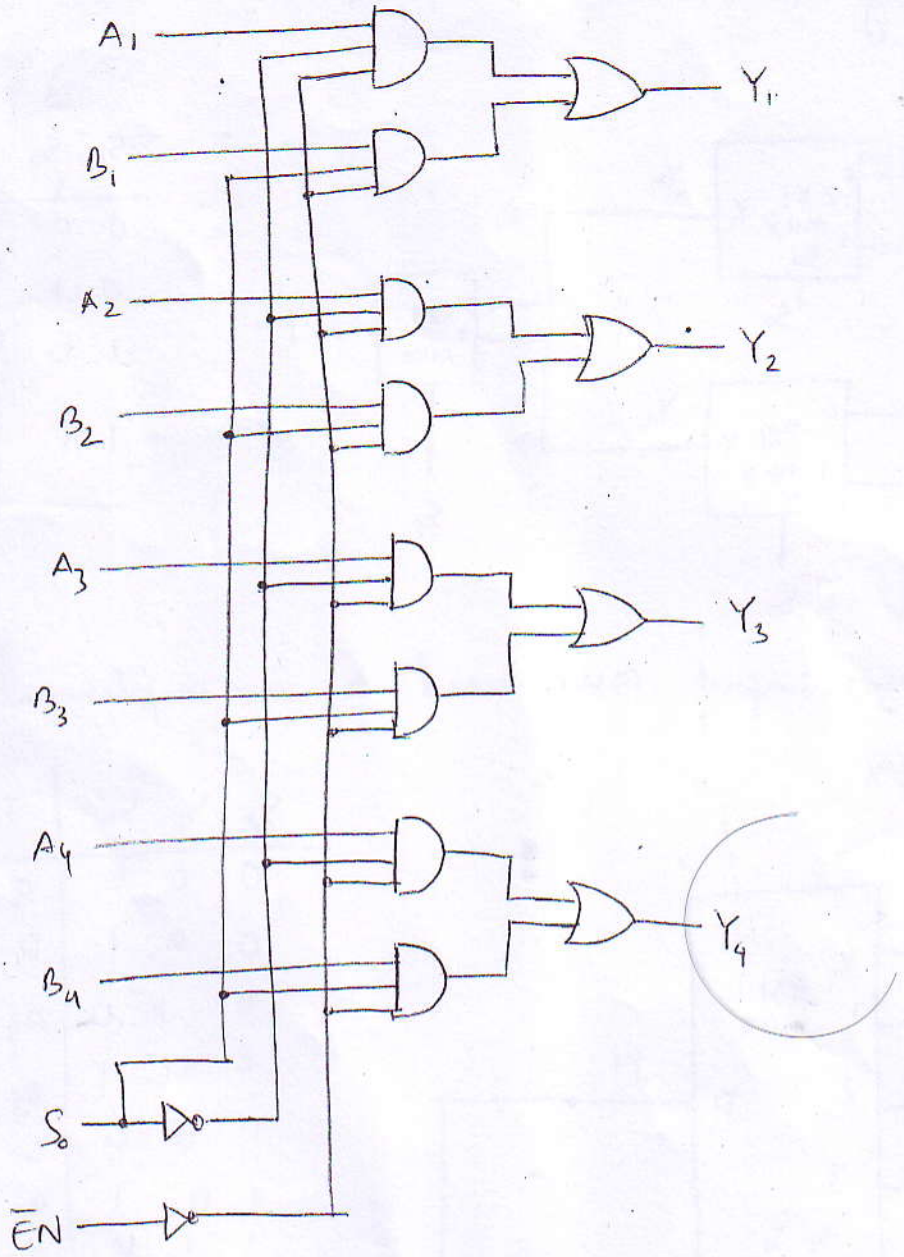


Fig: quadruple 2-input data selector/multiplexer

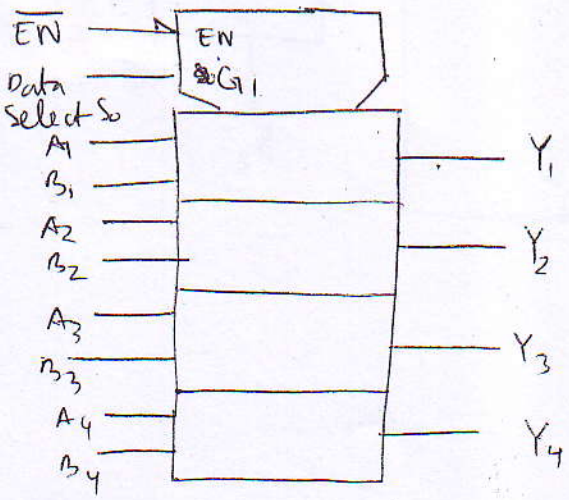
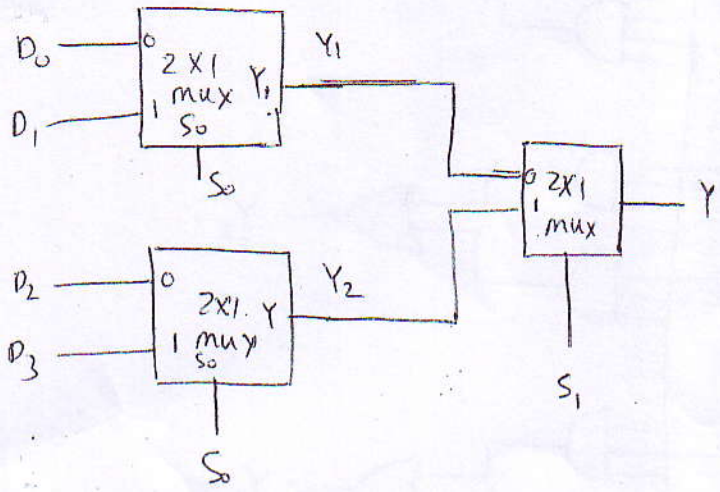


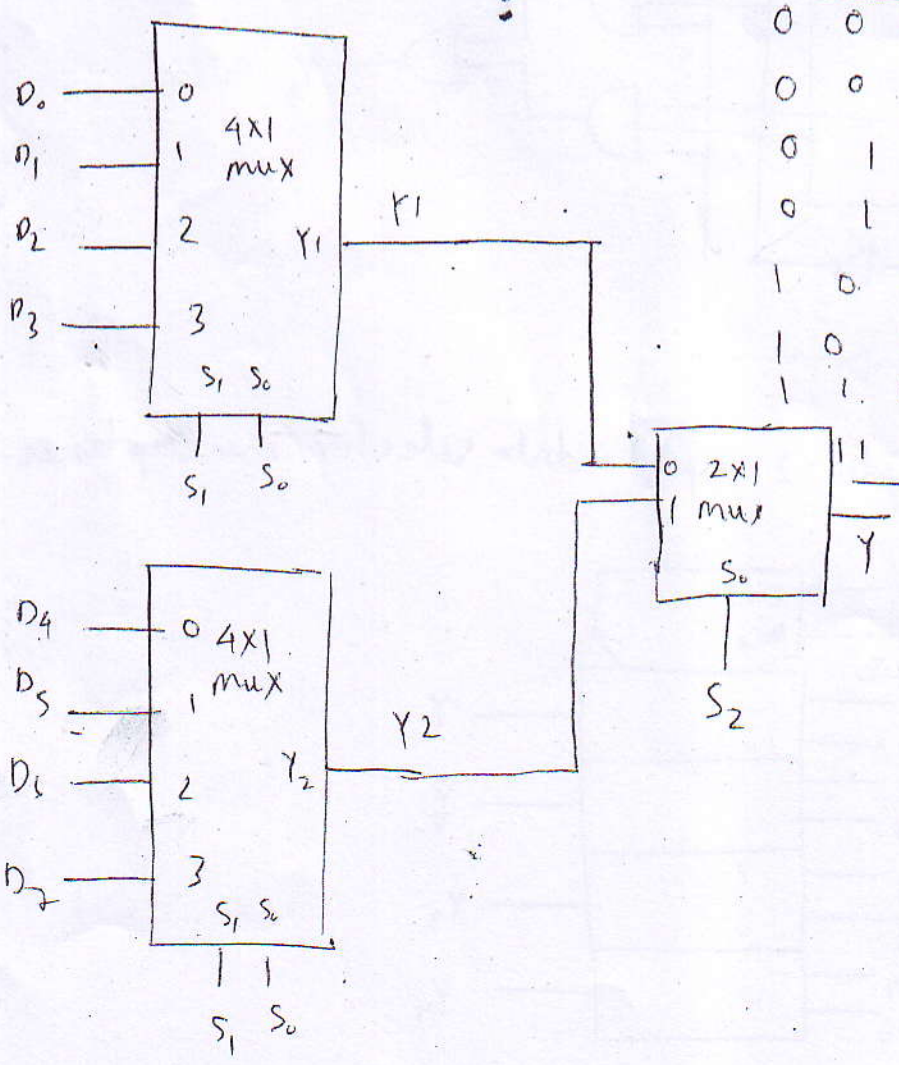
Fig: Logic symbol

Cascading data selector/ multiplexer :



S_1	S_0	Y_1	Y_2	Y
0	0	D_0	D_2	D_0
0	1	D_1	D_3	D_1
1	0	D_0	D_2	D_2
1	1	D_1	D_3	D_3

Fig: 3, 2-input mux used to ~~m~~ implement a 4-input mux



S_2	S_1	S_0	Y_1	Y_2	Y
0	0	0	D_0	D_4	D_0
0	0	1	D_1	D_5	D_1
0	1	0	D_2	D_6	D_2
0	1	1	D_3	D_7	D_3
1	0	0	D_0	D_4	D_4
1	0	1	D_1	D_5	D_5
1	1	0	D_2	D_6	D_6
1	1	1	D_3	D_7	D_7

Fig: 8-input data selector / mux

Boolean Function Implementation using MUX

It is possible to generate any function of (n+1) variables with $2^n - 1$ multiplexer

Implement the function $f(A,B,C) = \sum 2,3,4,6$ using multiplexer

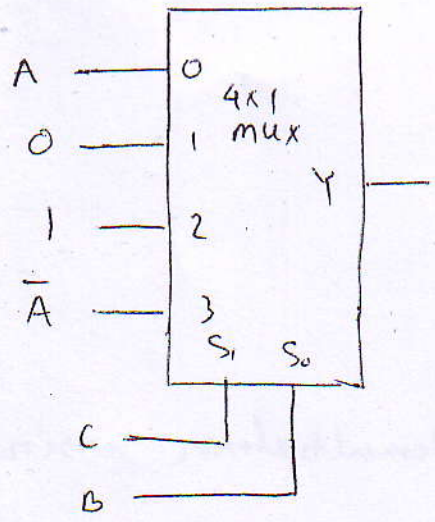
minterms	A	B	C	F
0	0	0	0	0
1	0	0	1	0
2	0	1	0	1
3	0	1	1	1
4	1	0	0	1
5	1	0	1	0
6	1	1	0	1
7	1	1	1	0

$BC = 00$, $F = A$

$BC = 01$, $F = 0$

$BC = 10$, $F = 1$

$BC = 11$, $F = \bar{A}$



Demultiplexers:

A demultiplexer (DEMUX) takes data from one line and distribute them to a given number of output lines.

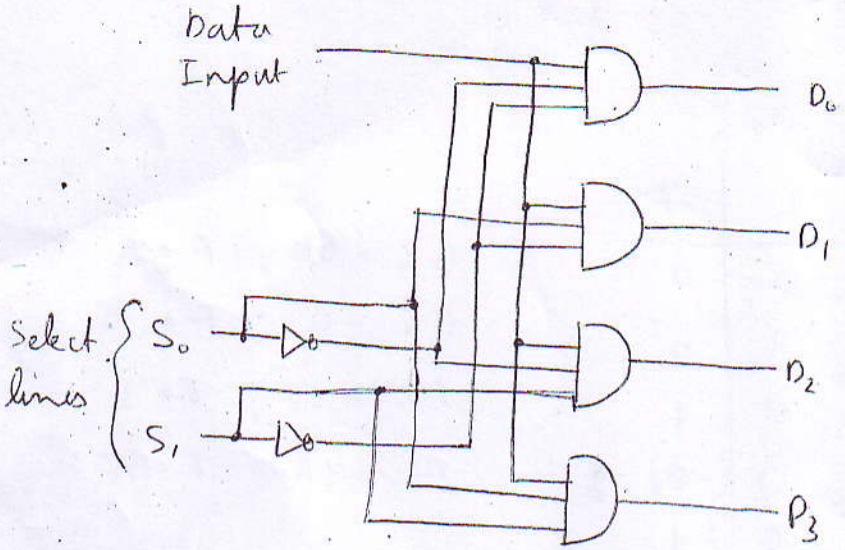
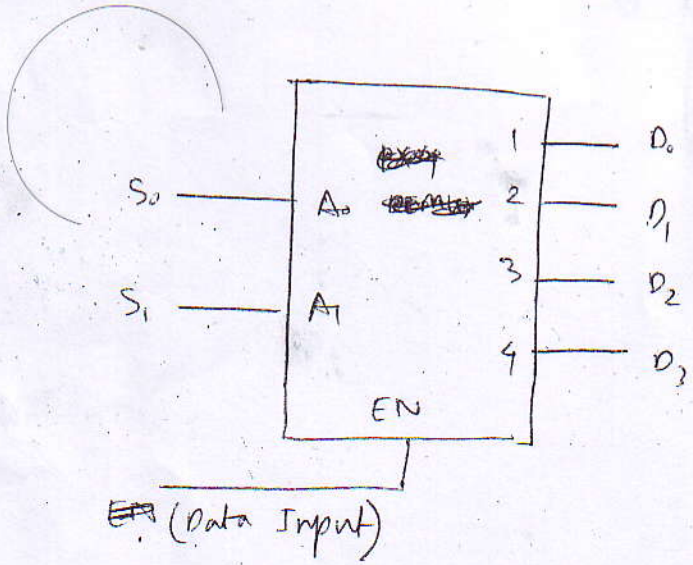


Fig: A 1-to-4 line demultiplexer

Decoders can be used as demultiplexers



* Design a 1 to 8 line Demultiplexer using a 3 line-to-8 line Decoder