



CSE231 Lab | Digital Logic Design

Class Time (Sec-10): Monday(M) 11:20 AM - 02:20 PM

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Course Description:

This course provides an introduction to logic design and basic tools for the design of digital logic systems. A basic idea of number systems will be provided, followed by a discussion on combinational logic: logic gates, Boolean algebra, minimization techniques, arithmetic circuits (adders, subtractors), basic digital circuits (decoders, encoders, multiplexers, shift registers), programmable logic devices (PROM, PAL, PLA). The course will then cover sequential circuits: flip-flops, state transition tables and diagrams, state minimization, state machines, design of synchronous/asynchronous counters, RAM/ROM design. An introduction to programmable logic will also be provided.

Mark Distribution:

Class Attendance:	10%
Lab Quiz:	20%
Report(average):	20%
Midterm Exam:	25%
Final Exam:	25%

Experiments:

Lab 1: Digital Logic Gates and Boolean Functions
Lab 2: Universal Logic Gates
Lab 3: Combinational Logic Design (Canonical Form)
Lab 4: Combinational Logic Design (K Maps)
Lab 5: Binary Arithmetic
Midterm Exam
Lab 6: Mux and decoder
Lab 7A: Flip-Flops - Registers
Lab 7B: Seven Segment Display
Lab 8: Synchronous Sequential Circuits
Final Exam