

Digital Logic Design :-

Lecture 18

UP/DOWN synchronous counter :

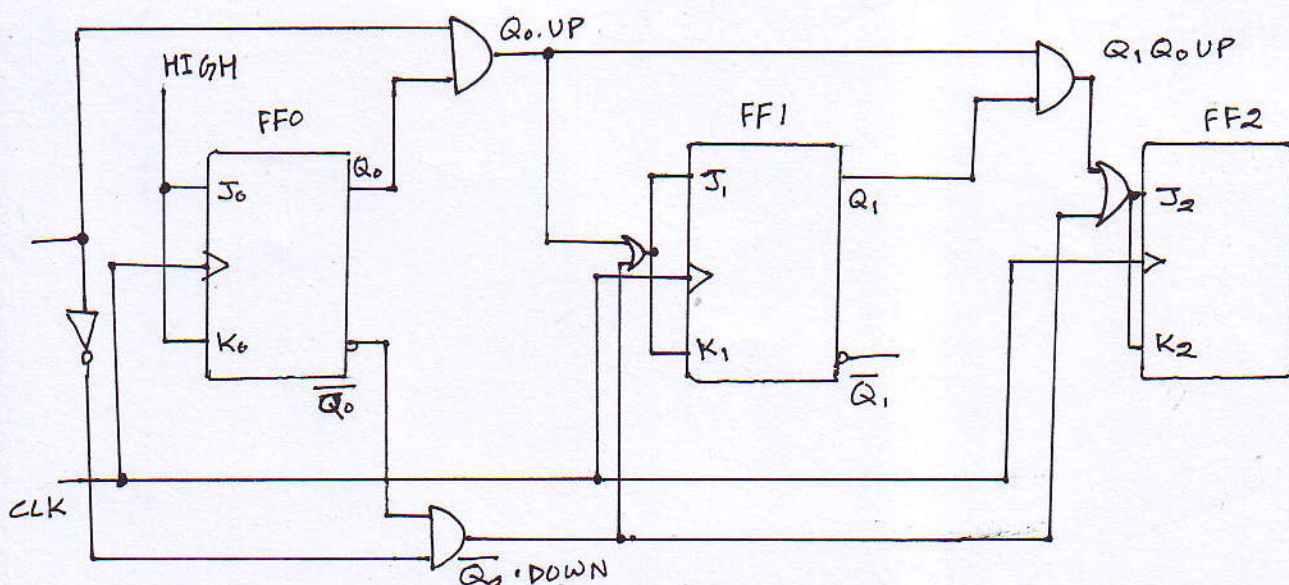
UP/DOWN sequence for a 3-bit binary counter.

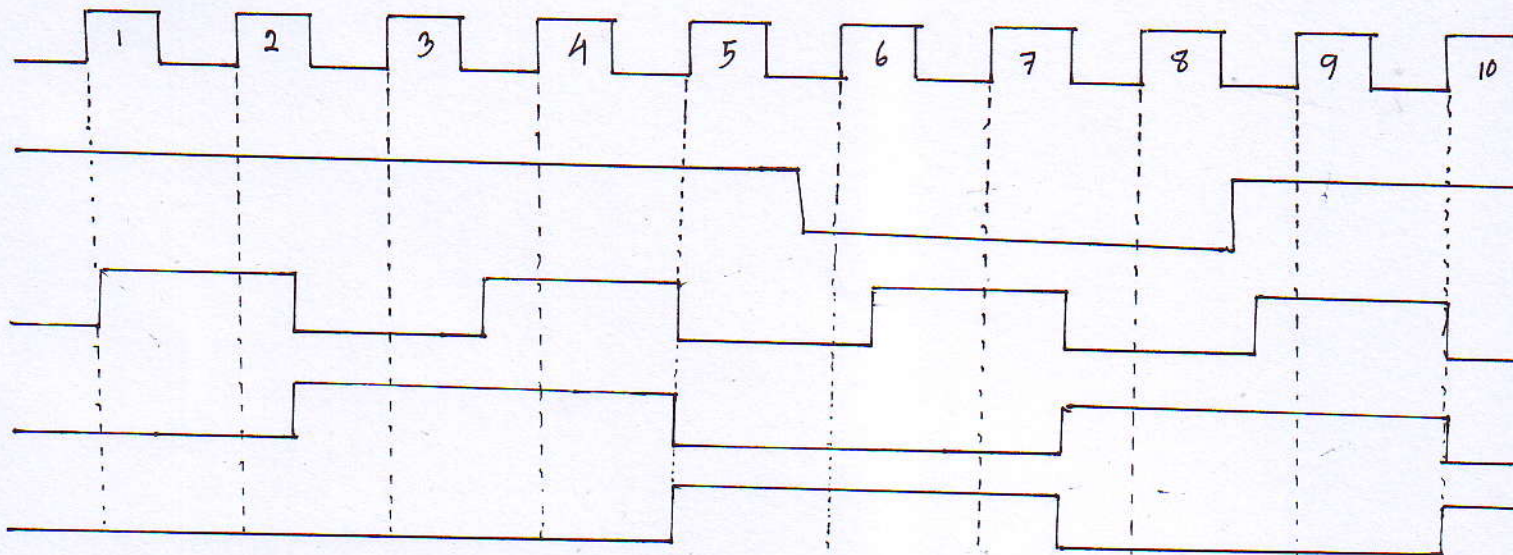
Clock pulse	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0

$$J_0 = K_0 = 1$$

$$J_1 = K_1 = Q_0 \cdot \text{UP} + \bar{Q}_0 \cdot \text{DOWN}$$

$$J_2 = K_2 = Q_1 \cdot Q_0 \cdot \text{UP} + \bar{Q}_1 \cdot \bar{Q}_0 \cdot \text{DOWN}$$

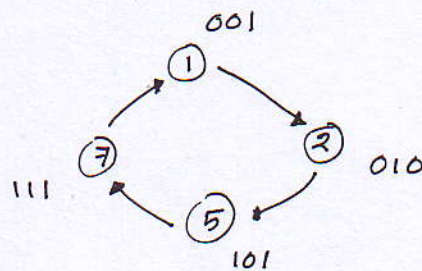




Counter With Irregular Count Sequence :

using JK Flip Flop design a counter with count sequence

Step 1 :



Flip-Flops required = 3

Step 2 :

Next state table :

All other states are don't care

	Present State			Next State		
	Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
1	0	0	1	0	1	0
2	0	1	0	1	0	1
5	1	0	1	1	1	1
7	1	1	1	0	0	1

J_2	K_2	J_1	K_1	J_0	K_0
0	x	1	x	x	1
1	x	x	1	1	x
x	0	1	x	x	0
x	1	x	1	x	0

Step : 3

Transition table for J-K Flip Flop

Q_N	Q_{N+1}	Flip-Flop Inputs	
		J	K
0	→ 1	0	x
0	→ 0	1	x
1	→ 0	x	1
1	→ 1	x	0

Step : 4

$Q_2 Q_1$ Q_0 J_0 Map

	0	1
00	x ₀	x ₁
01	1 ₂	x ₃
11	x ₆	x ₇
10	x ₄	x ₅

$$J_0 = 1$$

$Q_2 Q_1$ Q_0 K_0 Map

	0	1
00	x	1
01	x	x
11	x	0
10	x	0

$$K_0 = \bar{Q}_2$$

$Q_2 Q_1$ Q_0 J_1 Map

	0	1
00	x	1
01	x	x
11	x	x
10	x	1

$$J_1 = 1$$

$Q_2 Q_1$ Q_0 K_1 Map

	0	1
00	x	x
01	1	x
11	x	1
10	x	x

$$K_1 = 1$$

$Q_2 Q_1$ Q_0 J_2 Map

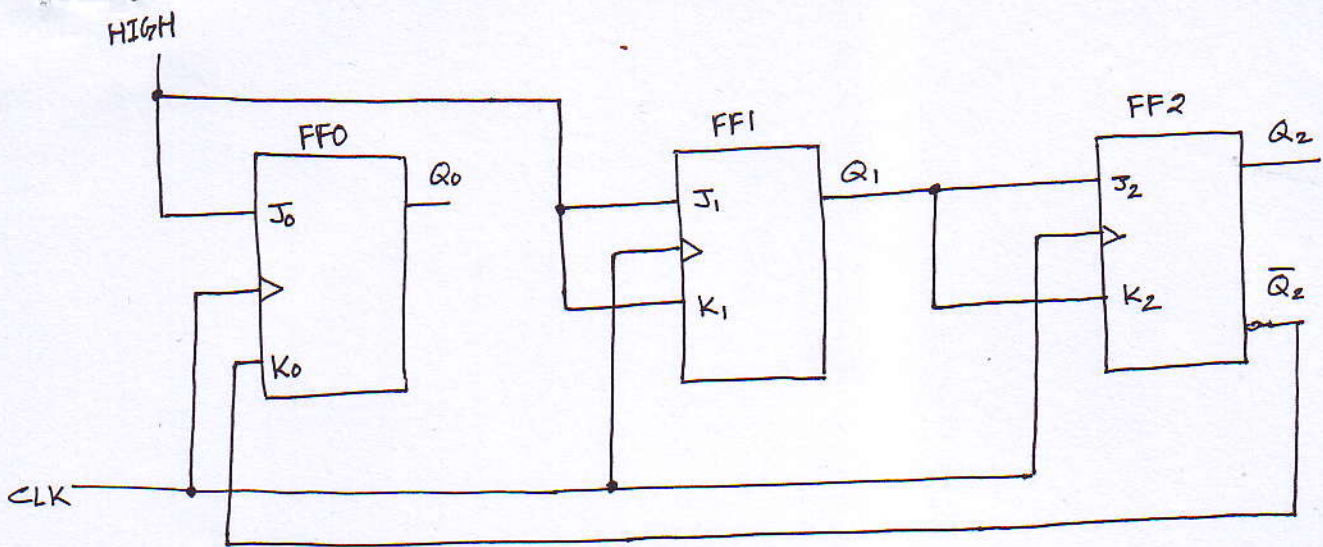
	0	1
00	x	0
01	1	x
11	x	x
10	x	x

$$J_2 = Q_1$$

$Q_2 Q_1$ Q_0 K_2 Map

	0	1
00	x	x
01	x	x
11	x	1
10	x	0

$$K_2 = Q_1$$



Counter Decoding :

Decode 6 from 3 bit Asynchronous Counter
 $(6)_{10} = (110)_2$

