Lab 1: Digital Logic Gates and Boolean Functions

F. Data Sheet

F.1 Introduction to Basic Logic Gates

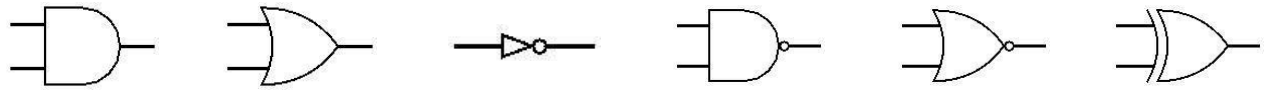


Figure F.1.1: Pin configurations of gates in ICs

Input	AND	OR	NAND	XOR	NOR
0 0	0	0	1	0	1
0 1	0	1	1	1	0
1 0	0	1	1	1	0
1 1	1	1	0	0	0

Input	NOT
0	1
1	0

Table F.1.1: Truth Table of Logic Gates

F.2 Constructing 3-input AND & OR gates from 2-input AND & OR gates

A B C	F = ABC	F = A+B+C
0 0 0	0	0
0 0 1	0	1
0 1 0	0	1
0 1 1	0	1
1 0 0	0	1
1 0 1	0	1
1 1 0	0	1
1 1 1	1	1

Table F.2.1: Truth Tables for 3-input AND and OR

$F = ABC = \quad A(BC) = (AB)C$
$F = A+B+C = A+(B+C) = (A+B)+C$

Table F.2.2: Expressing 3-input gates as 2-input gates using associative law.

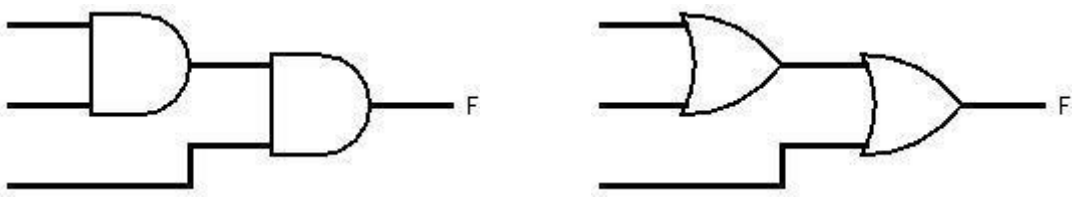


Figure F.2.1: Extension of inputs of AND and OR gates

F.3 Implementation of Boolean Functions

A B C	$I_1 = A'C$	$I_2 = AB'$	$I_3 = BC$	$F = I_1 + I_2 + I_3$
0 0 0	0	0	0	0
0 0 1	1	0	0	1
0 1 0	0	0	0	0
0 1 1	1	0	1	1
1 0 0	0	1	0	1
1 0 1	0	1	0	1
1 1 0	0	0	0	0
1 1 1	0	0	1	1

Figure F.3.1: Truth Table for the given Boolean Function

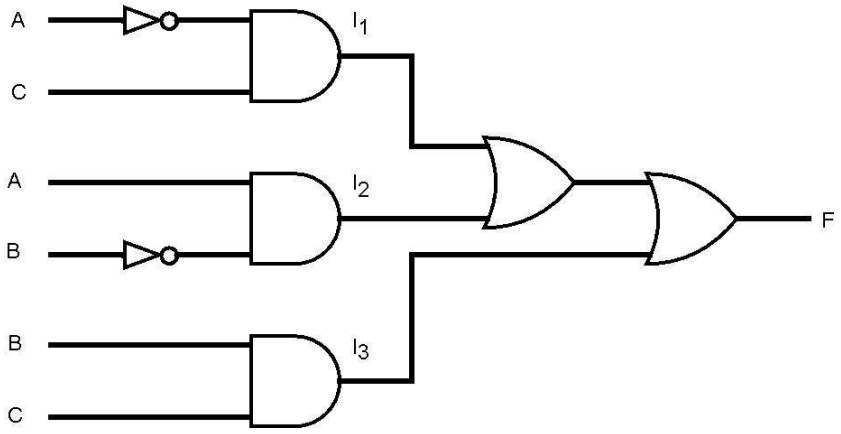
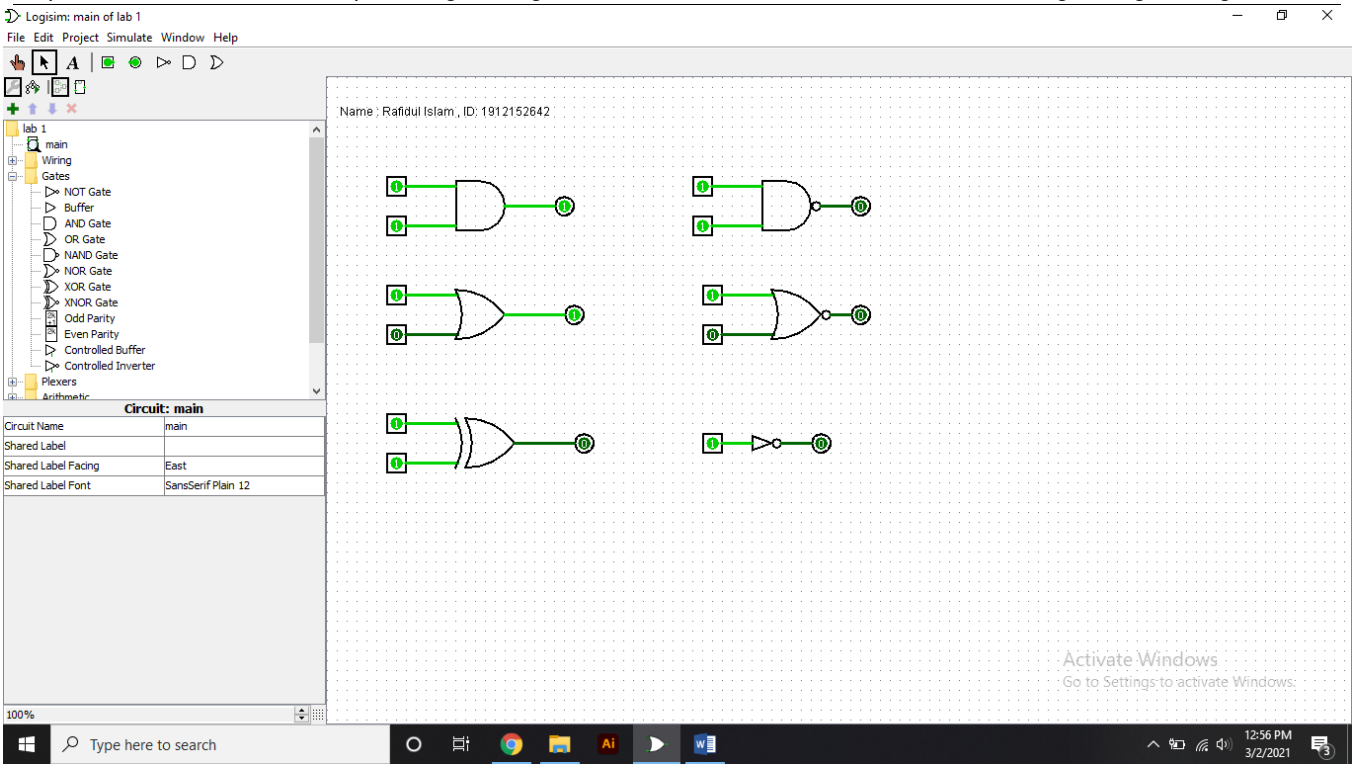


Figure F.3.1: Logic Diagram for the given Boolean Function

Attachment:

1. Attach the screenshots /image of the simulations below
2. Attach the required logic Diagrams with proper figure name and labeling below.


Logisim: main of lab 1
File Edit Project Simulate Window Help
lab 1
main
Wiring
Gates
NOT Gate
Buffer
AND Gate
OR Gate
NAND Gate
NOR Gate
XOR Gate
XNOR Gate
Odd Parity
Even Parity
Controlled Buffer
Controlled Inverter
Plexers
Arithmetic
Circuit: main
Circuit Name main
Shared Label
Shared Label Facing East
Shared Label Font SansSerif Plain 12
Name : Rafidul Islam , ID: 1912152642
100%
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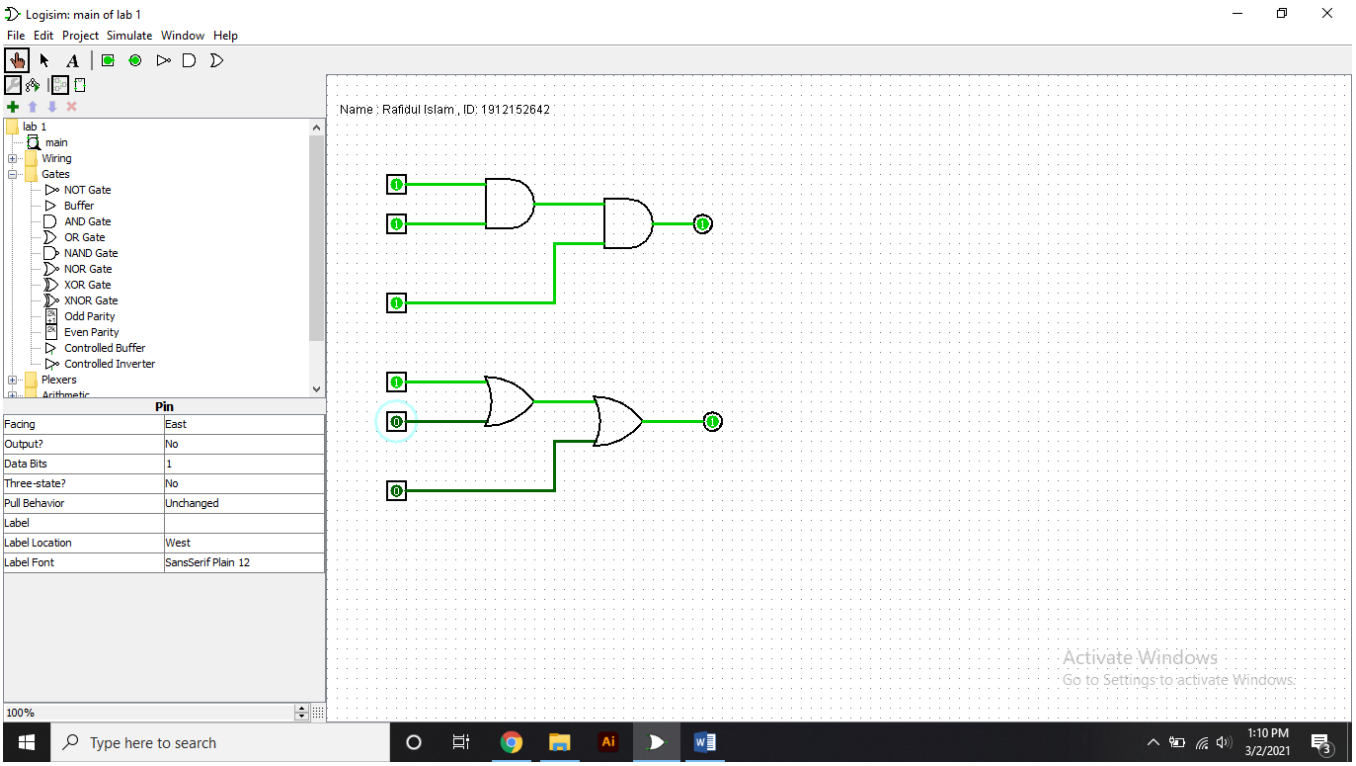
12:56 PM
3/2/2021

F.1.1


Logisim: main of lab 1
File Edit Project Simulate Window Help
lab 1
main
Wiring
Gates
NOT Gate
Buffer
AND Gate
OR Gate
NAND Gate
NOR Gate
XOR Gate
XNOR Gate
Odd Parity
Even Parity
Controlled Buffer
Controlled Inverter
Plexers
Arithmetic
Pin
Facing East
Output? No
Data Bits 1
Three-state? No
Pull Behavior Unchanged
Label
Label Location West
Label Font SansSerif Plain 12
Name : Rafidul Islam , ID: 1912152642
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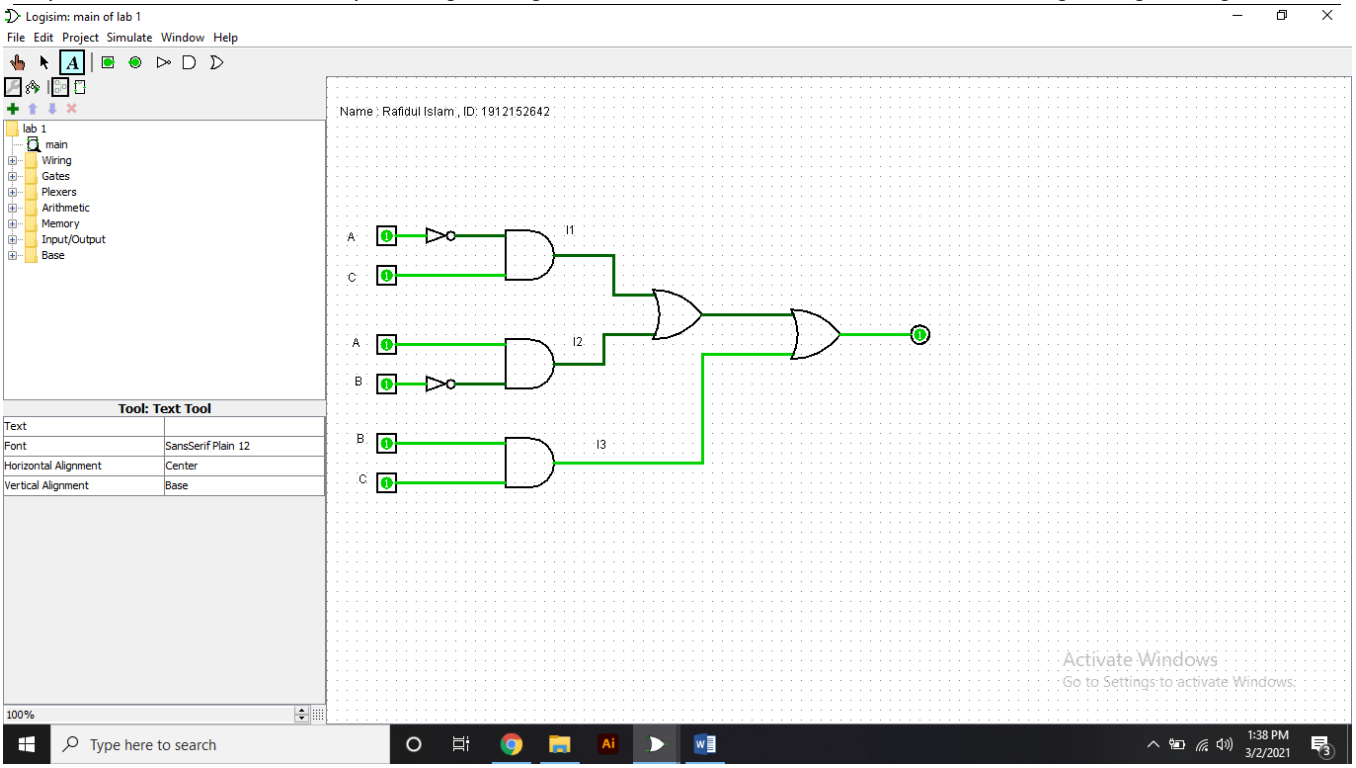
F.2.1


Logisim: main of lab 1
File Edit Project Simulate Window Help
lab 1
main
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Tool: Text Tool
Text
Font
SansSerif Plain 12
Horizontal Alignment
Center
Vertical Alignment
Base
100%
Name : Rafidul Islam , ID: 1912152642
A
C
A
B
B
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I1
I2
I3
Activate Windows
Go to Settings to activate Windows.
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F.3.1