North South University

Department of Electrical and Computer Engineering

LAB REPORT-06

Course name: Digital Logic Design Lab

Course Code: 231.L

Experiment Number: 06

Experiment name: BCD to seven segment decoder.

Experiment Date: 13th April, 2021

Report Submission Date: 20th April, 2021

Section: 06

Group no: 04

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Remarks:	**Score:**

OBJECTIVES:

- Familiarize with the analysis of Seven Segment Decoder circuits.
- Learn the implementation of Seven Segment Decoder using Display.
- Verify the Seven Segment Decoder with the logic

THEORY:

A Digital Decoder IC, is a device which converts one digital format into another and one of the most commonly used devices for doing this is called the Binary Coded Decimal (BCD) to 7-Segment Display Decoder.

7-segment LED (Light Emitting Diode) or LCD (Liquid Crystal Display) type displays, provide a very convenient way of displaying information or digital data in the form of numbers, letters or even alpha-numerical characters.

Typically, 7-segment displays consist of seven individual colored LED's (called the segments), within one single display package. In order to produce the required numbers or HEX characters from 0 to 9 and A to F respectively, on the display the correct combination of LED segments need to be illuminated and BCD to 7-segment Display Decoders. Each element (a, b, c, d, e, f, g) of the seven segment display is turned on when a logic low is applied to its corresponding input pin.

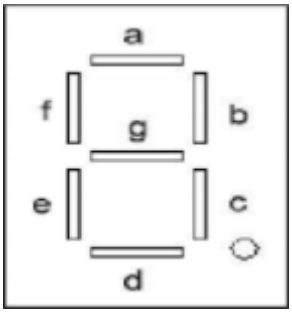

Figure: 7 segment display

EQUIPMENT LIST:

- Trainer Board
- 1 x IC 7447 Decoder
- 1 x Seven Segment Display
- 7 x Resistors

CIRCUIT DIAGRAM:

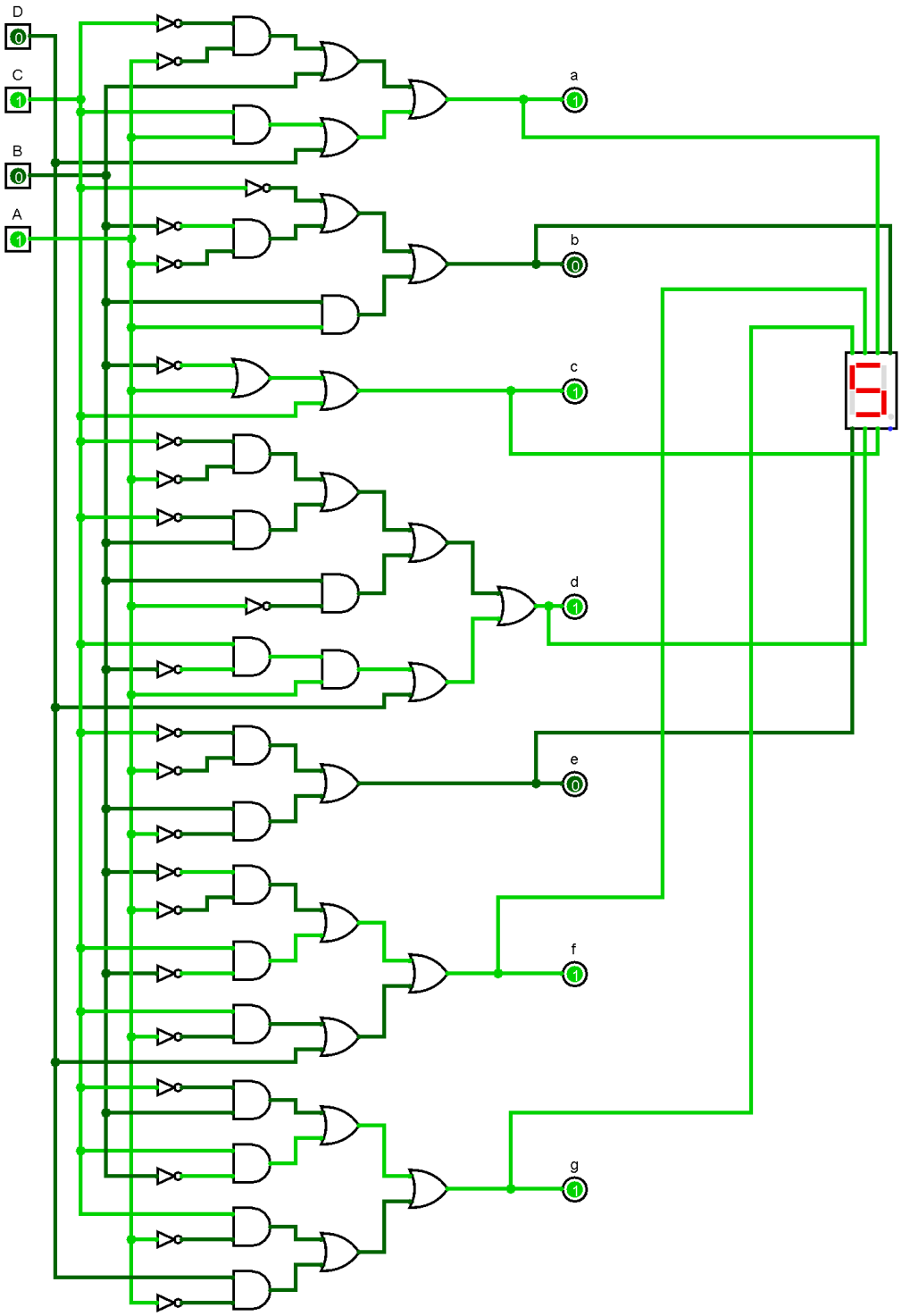

Fig - 02: Circuit for BCD to 7 segment display

Figure : Circuit for BCD to 7 Segment display

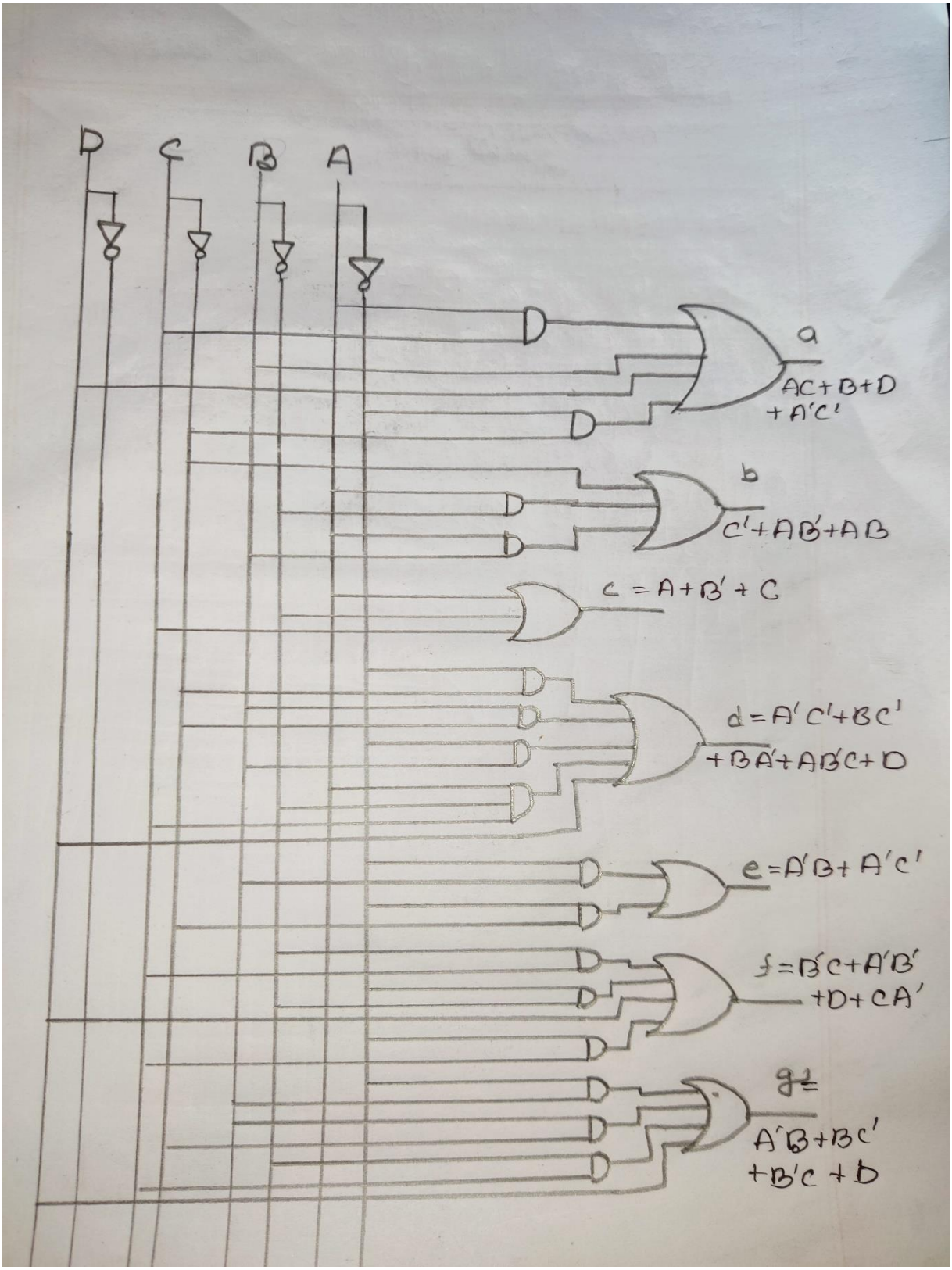

Figure : Combinational Circuit

DATA & TABLE:

Decimal	Inputs				Outputs						
	D	**C**	**B**	**A**	**a**	**b**	**c**	**d**	**e**	**f**	**g**
1	0	0	0	0	1	1	1	1	1	1	0
2	0	0	0	1	0	1	1	0	0	0	0
3	0	0	1	0	1	1	0	1	1	0	1
4	0	0	1	1	1	1	1	1	0	0	1
5	0	1	0	0	0	1	1	0	0	1	1
6	0	1	0	1	1	0	1	1	0	1	1
7	0	1	1	0	1	0	1	1	1	1	1
8	0	1	1	1	1	1	1	0	0	0	0
9	1	0	0	0	1	1	1	1	1	1	1

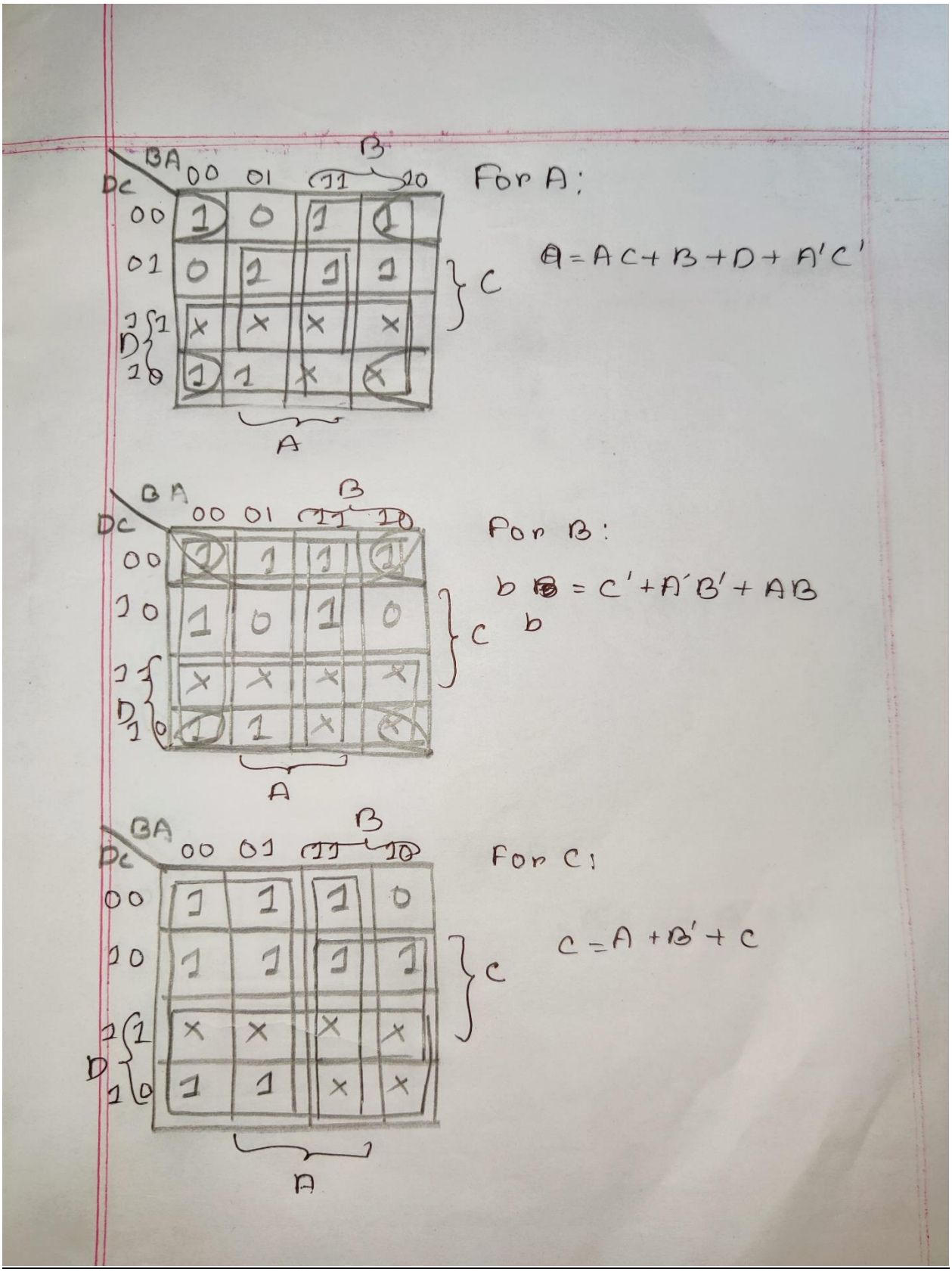

Figure : K map for a,b,c

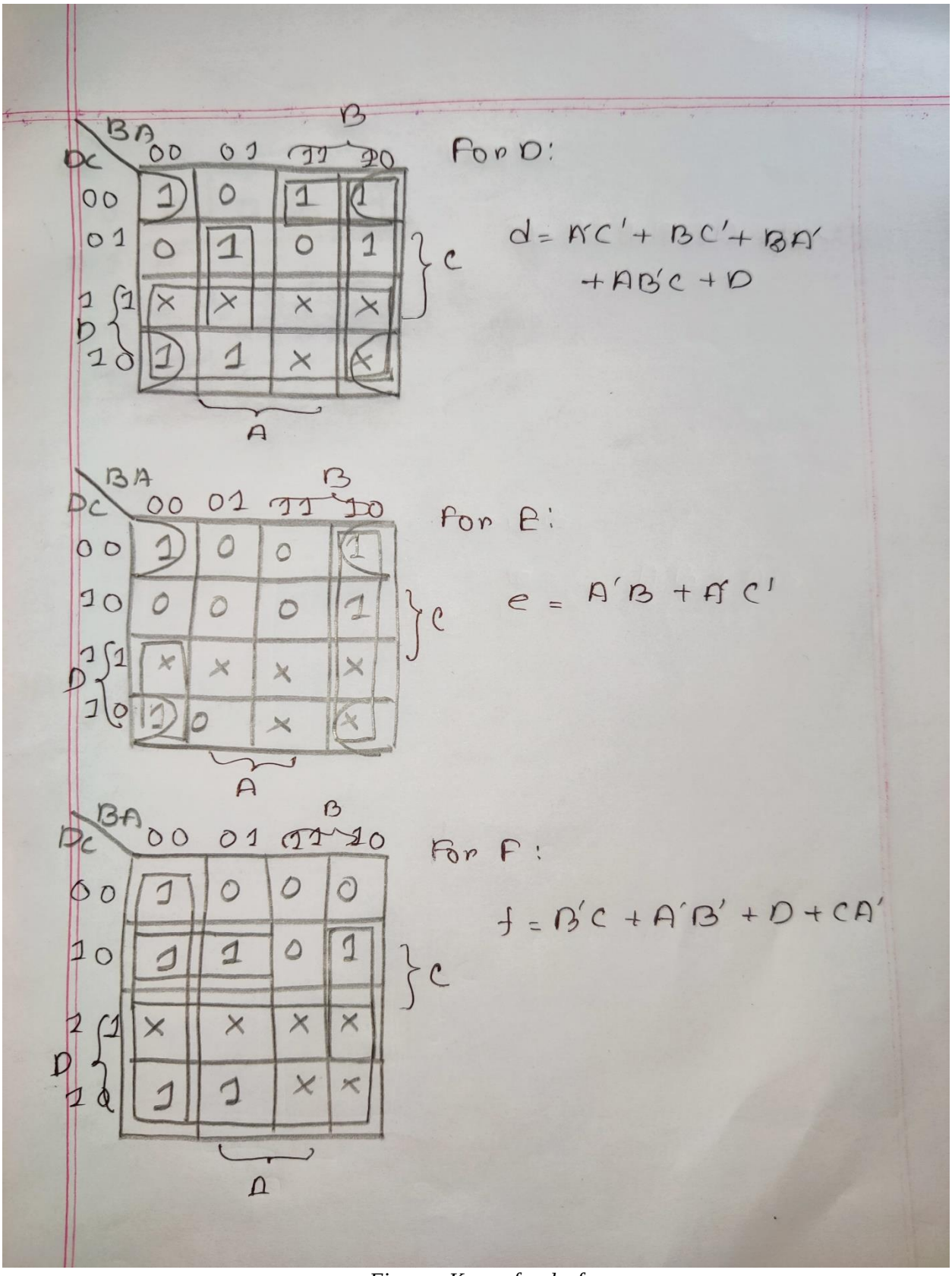

Figure : K map for d,e,f

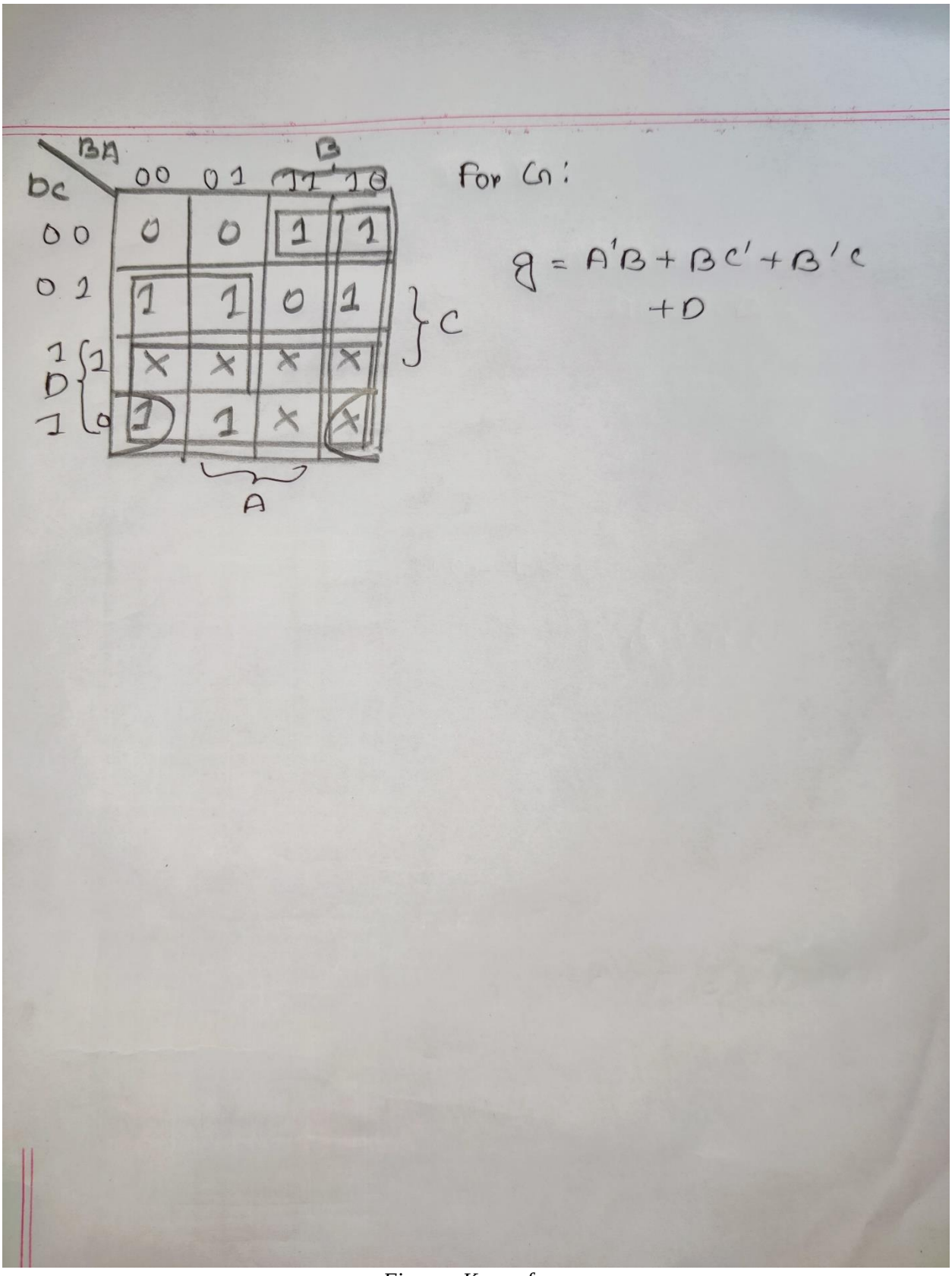

Figure : K map for g

Result analysis and Discussion:

The overall lab experiment was about the construction of BCD to Seven Segment Decoder. This will show 0 to 9. At the beginning of the experiment, we had to complete the data table with the values of input lines D, C, B, A and output lines a, b, c, d, e, f, g.

Then for every output line, I had to find out the Boolean function using Karnaugh map.

With the help of AND and OR logic gates, we designed the logic circuits for BCD to Seven Segment Decoder as well as IC diagram. This decoder worked properly and showed the outputs perfectly. During experiment, Logisim worked perfectly.

From the experiment, we learned about the internal structure of the seven segment display.

Contribution

Name	Contribution in
Khalid Bin Shafiq	**Circuit Diagram**
Rafidul Islam	**Result Analysis and Discussion**
Rashiqur Rahman Rifat	**Theory**
Towsif Muhtadi Khan	**Data & table, Coordinator(Writer)**

Class Assignment 06

10 Marks

1. Complete the tables and attach the k-map simplification
2. Attach the drawing of logic diagram
3. Attach the simulation part

Truth Table:

Decimal	Inputs				Outputs						
	D	**C**	**B**	**A**	**a**	**b**	**c**	**d**	**e**	**f**	**g**
0	0	0	0	0	**1**	**1**	**1**	**1**	**1**	**1**	**0**
1	0	0	0	1	**0**	**1**	**1**	**0**	**0**	**0**	**0**
2	0	0	1	0	**1**	**1**	**0**	**1**	**1**	**0**	**1**
3	0	0	1	1	**1**	**1**	**1**	**1**	**0**	**0**	**1**
4	0	1	0	0	**0**	**1**	**1**	**0**	**0**	**1**	**1**
5	0	1	0	1	**1**	**0**	**1**	**1**	**0**	**1**	**1**
6	0	1	1	0	**1**	**0**	**1**	**1**	**1**	**1**	**1**
7	0	1	1	1	**1**	**1**	**1**	**0**	**0**	**0**	**0**
8	1	0	0	0	**1**	**1**	**1**	**1**	**1**	**1**	**1**
9	1	0	0	1	**1**	**1**	**1**	**1**	**0**	**1**	**1**

Ans 2

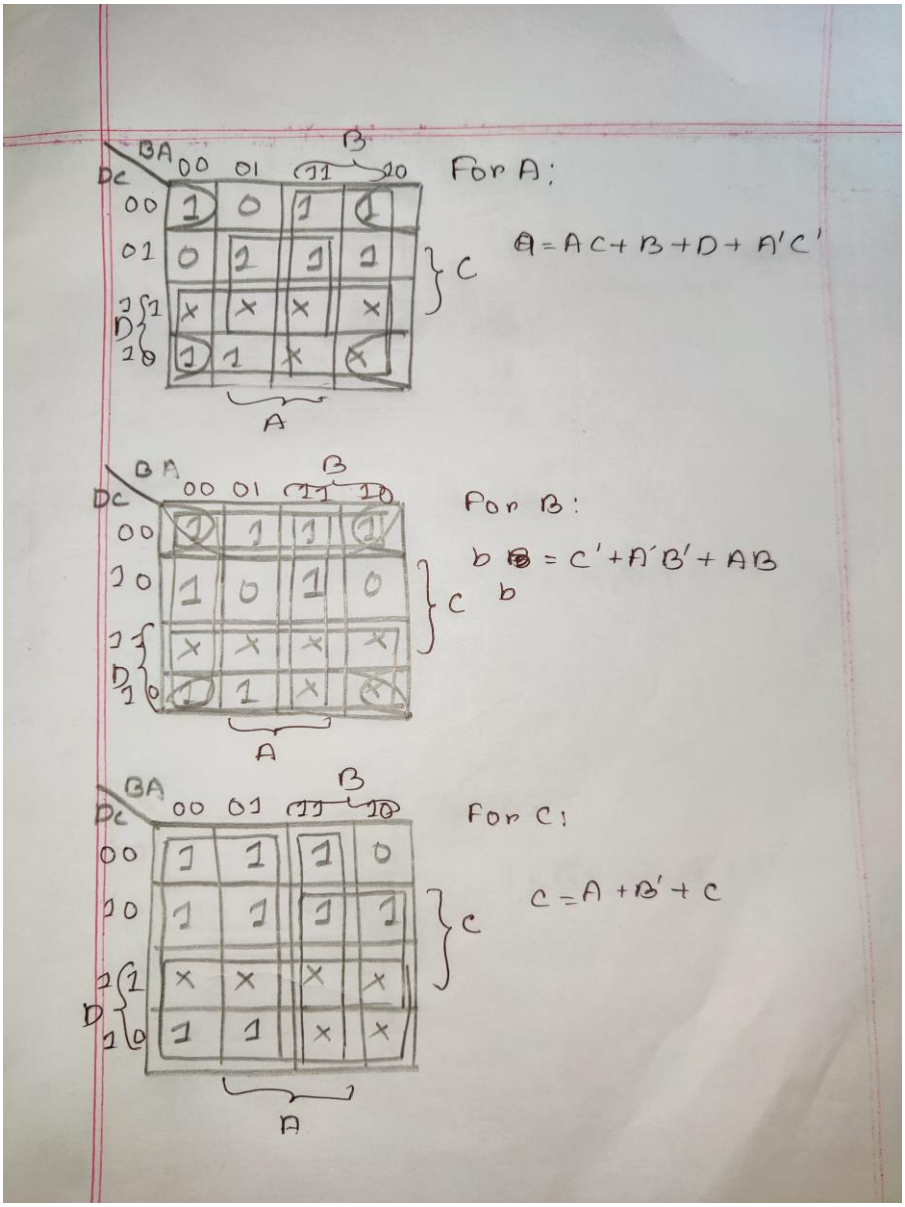

Figure: *K map for a,b,c*

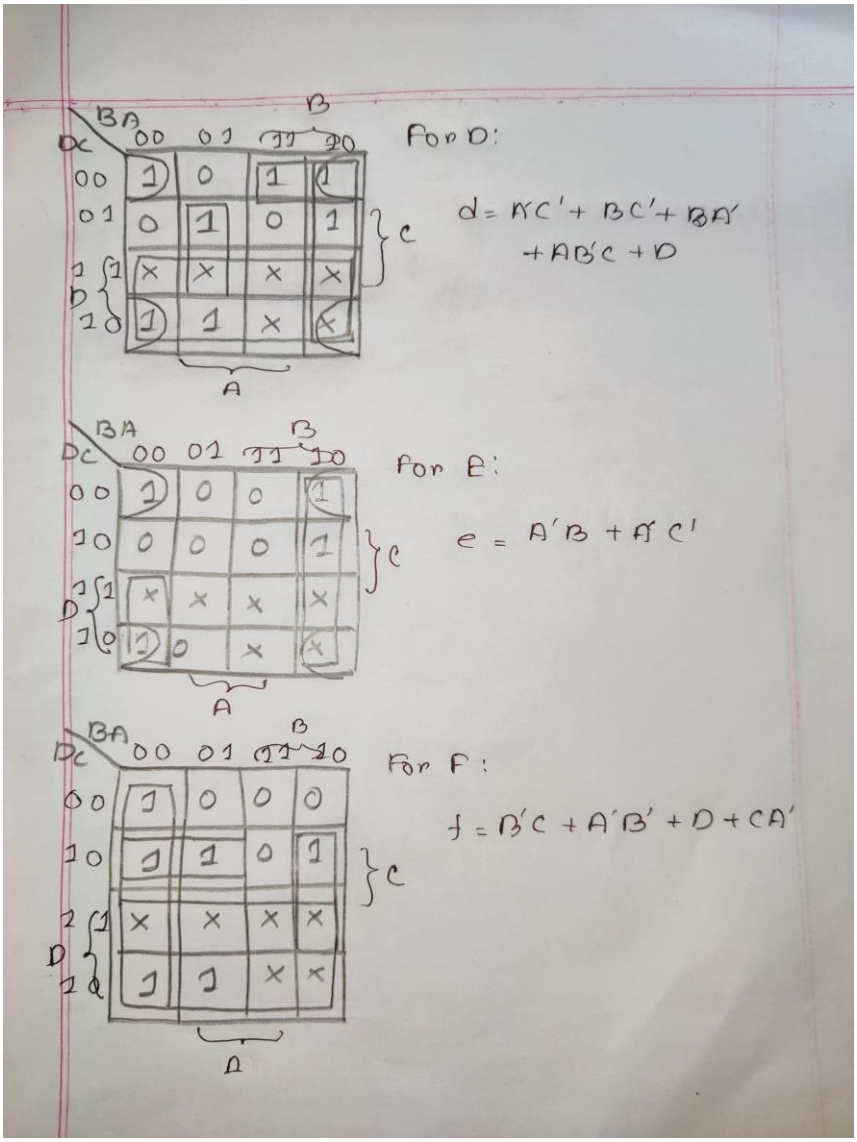

Figure: *K map for d,e,f*

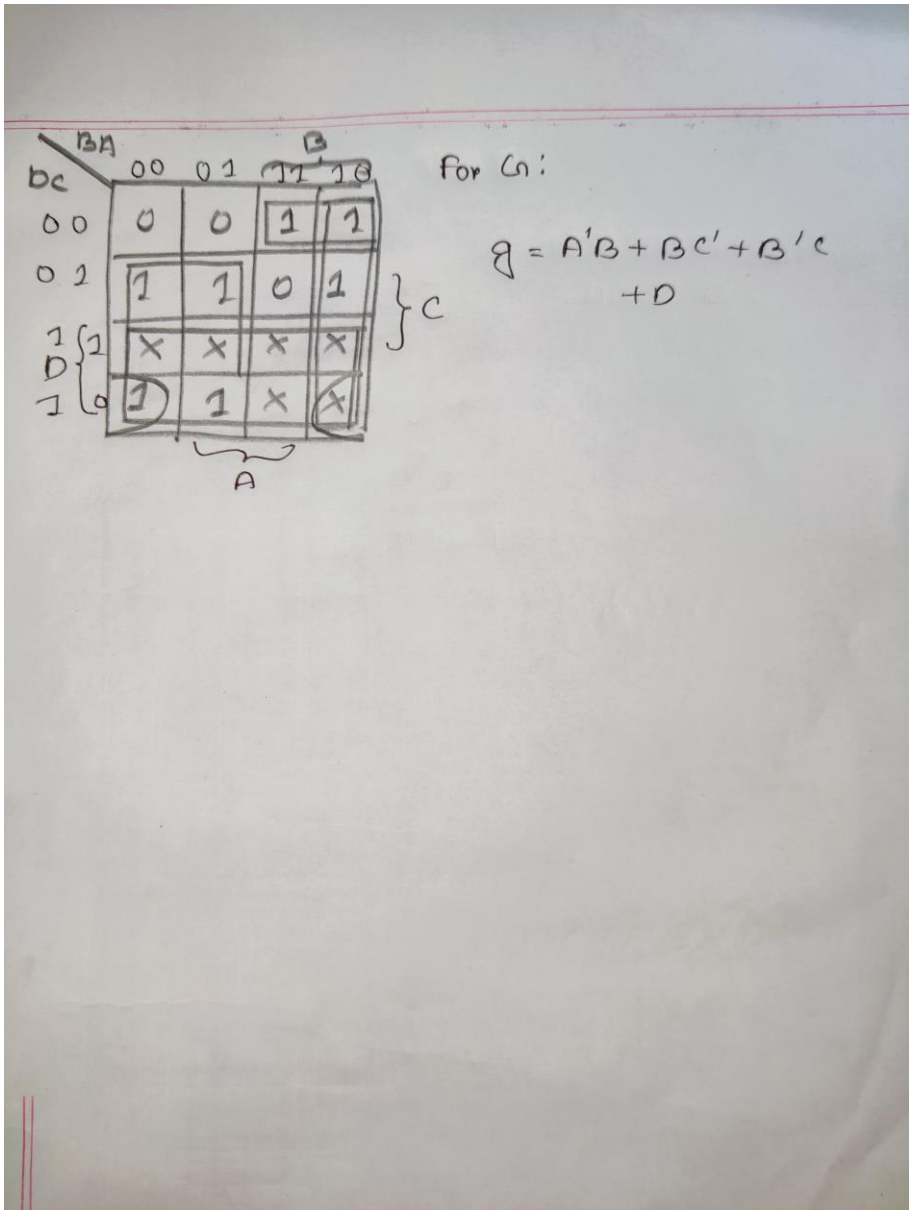

Figure: *K map for g*

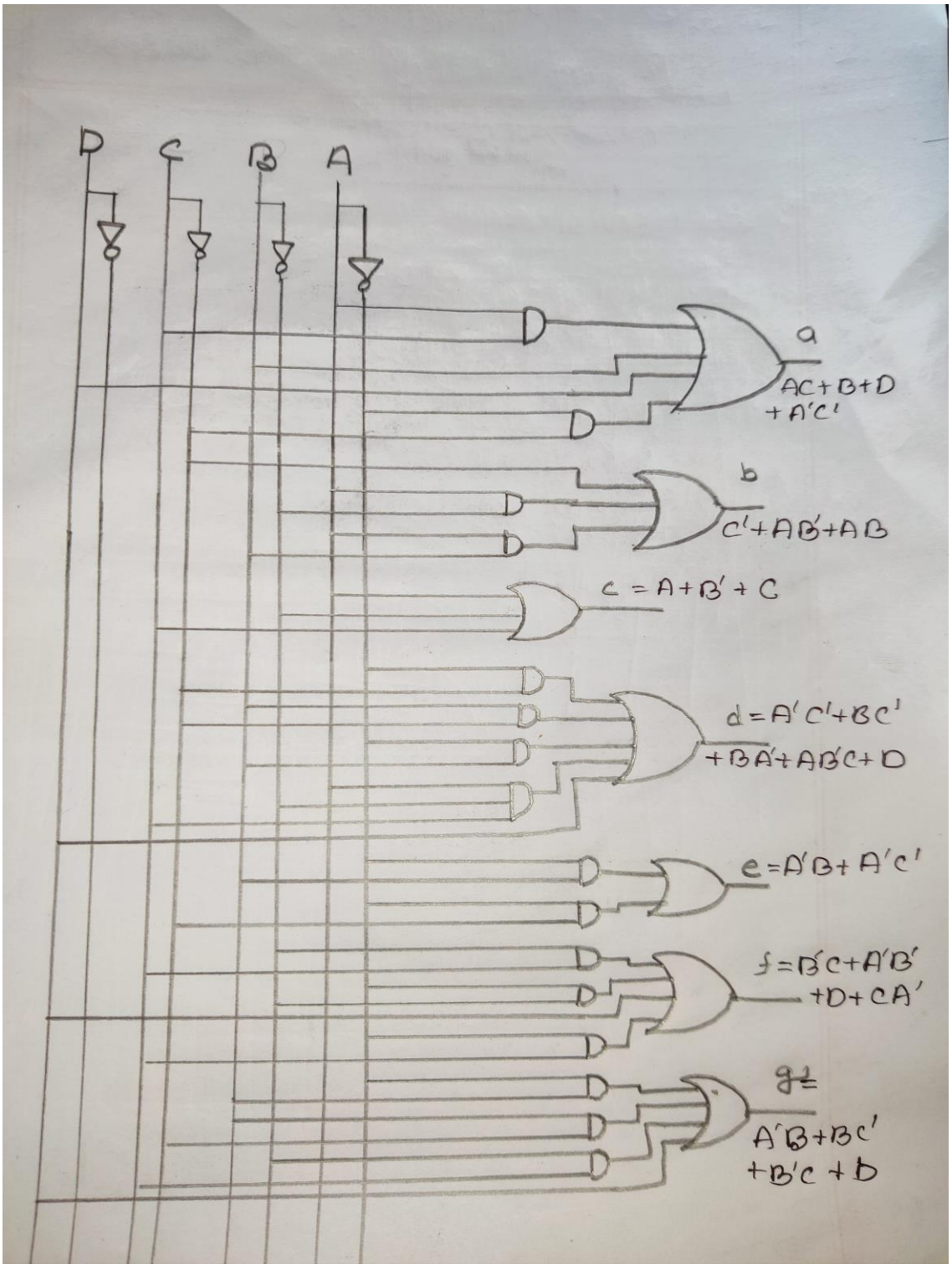

Figure: *Combinational Circuit*

Ans 3

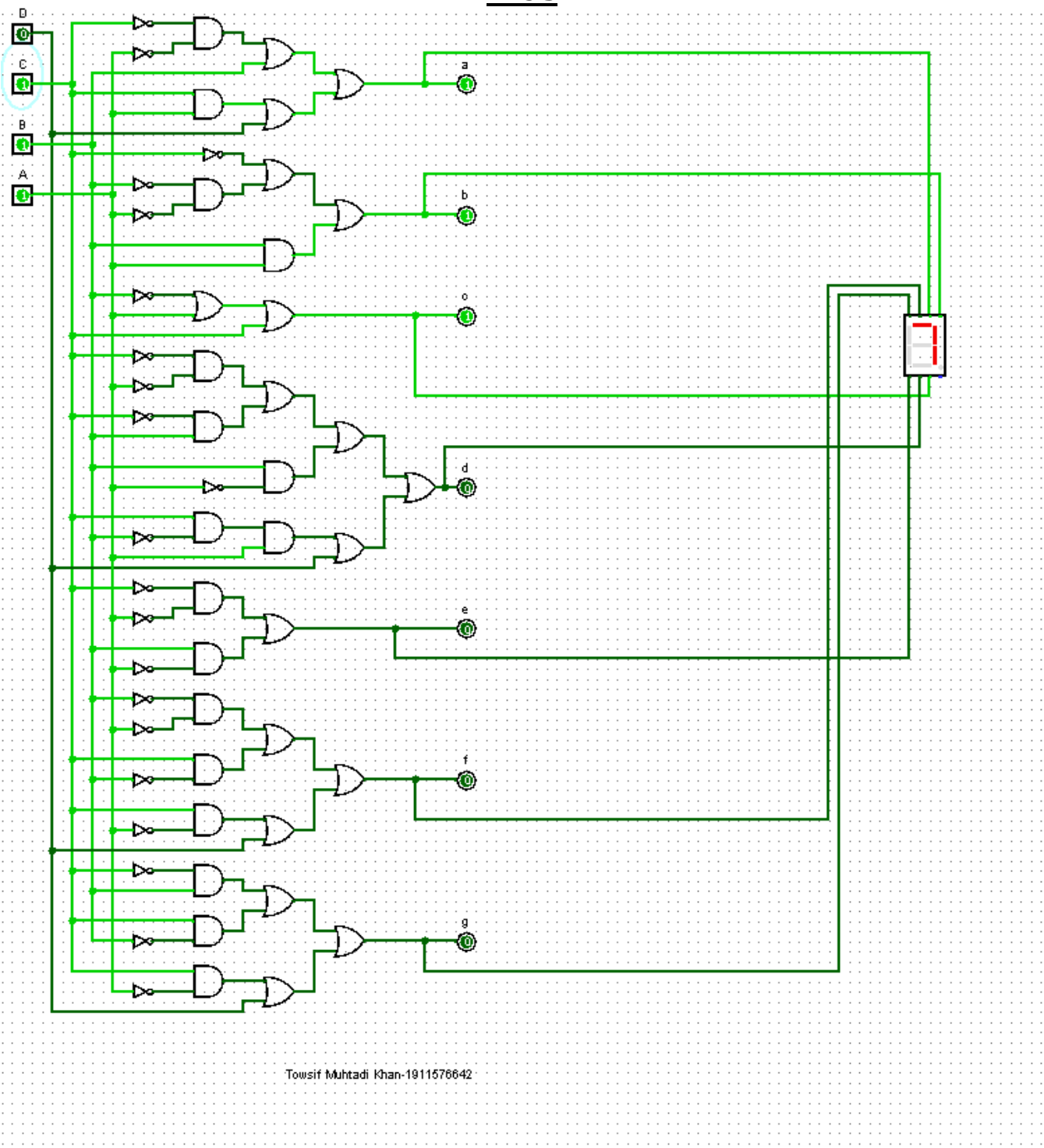

Figure : *Simulation Part*

Towsif Muhtadi Khan-1911576642