North South University

Department of Electrical and Computer Engineering

LAB REPORT-02

Digital Logic Design

CSE 231.L

Experiment Number: 02

Experiment name: Universal Gates

Experiment Date: 9th March, 2021

Report Submission Date: 15th March, 2021

Section: 06

Group no: 04

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Remarks:	**Score:**

OBJECTIVES

- Understand the concept of Universal Gates (NAND & NOR)
- Implement the basic logic gates using universal gates
- Implement boolean functions using universal gates
- Understand gate level minimization

THEORY

Universal Gates:

A universal gate is a gate which can implement any Boolean function without need to use any other gate type. NAND and NOR gates are universal gates. These two gates can build all the basic gates: AND, OR, NOR, NOT, XOR & XNOR. In practice, this is advantageous since NAND and NOR gates are economical and easier to fabricate and are the basic gates used in all IC digital logic families. Using NAND and NOR gates and De Morgan's Theorems different basic gates & EX-OR gates are realized. NAND gate is the AND gate connected to the inverter. Also, the NOR gate is the OR gate connected to the inverter.

Figure C1 shows the implementation of NOT, AND & OR gates using only NAND gates

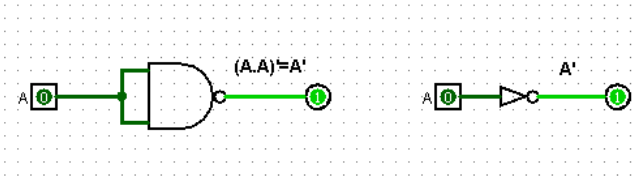


Fig: Implementation of NOT gate using NAND gate

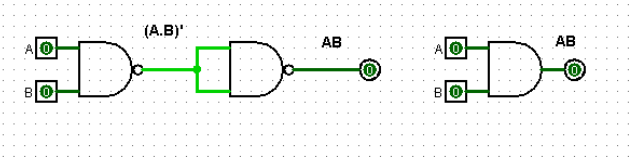


Fig: Implementation of AND gate using NAND gate

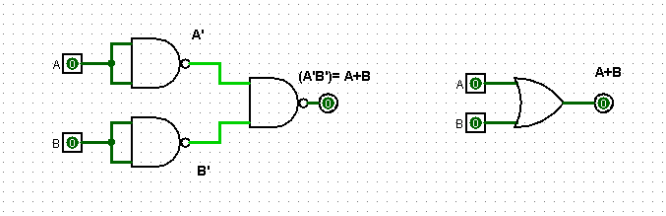


Fig: Implementation of OR gate using NAND gate

***Figure C1**: NAND as a universal gate*

EQUIPMENT LIST

- Trainer Board
- IC 7400 Quadruple 2-input NAND gates
- IC 7402 Quadruple 2-input NOR gates

CIRCUIT DIAGRAM

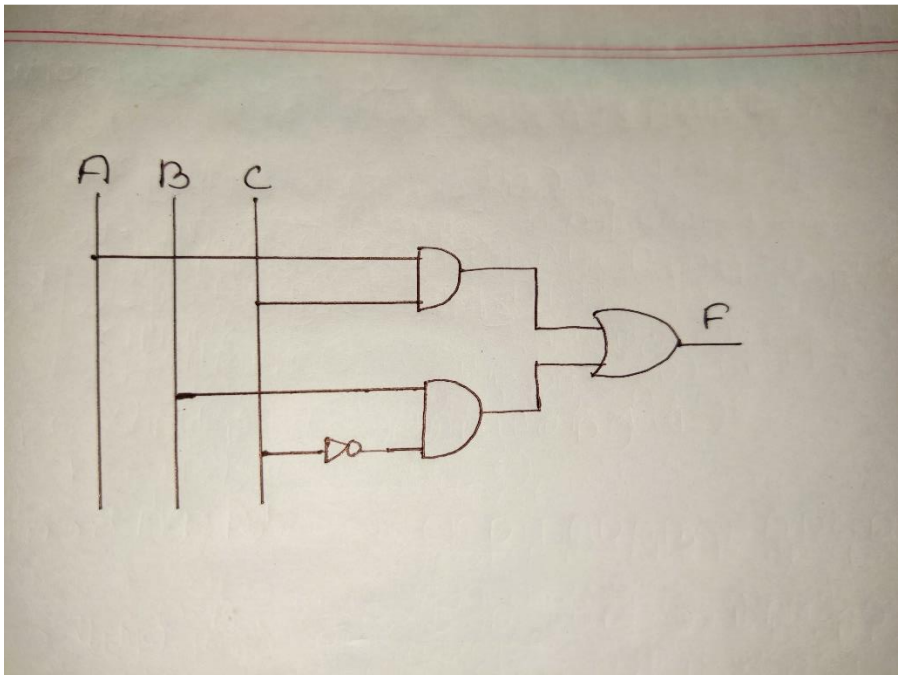
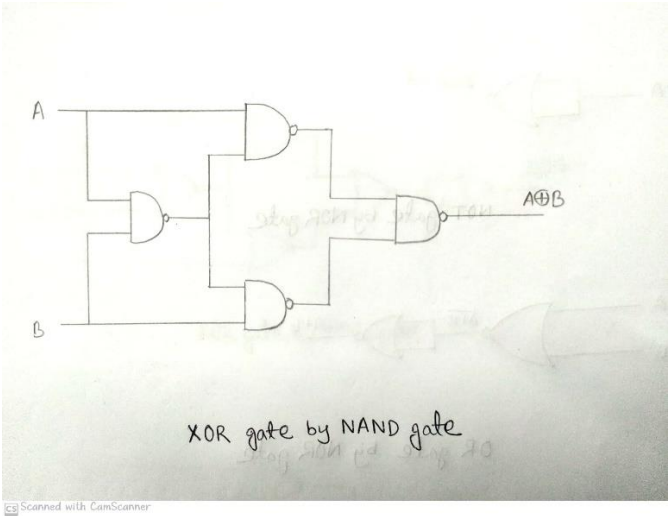
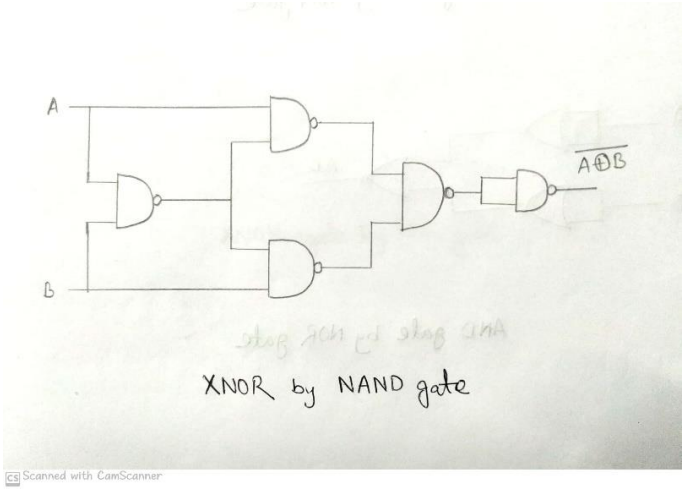


Figure D2: *A combinational circuit*

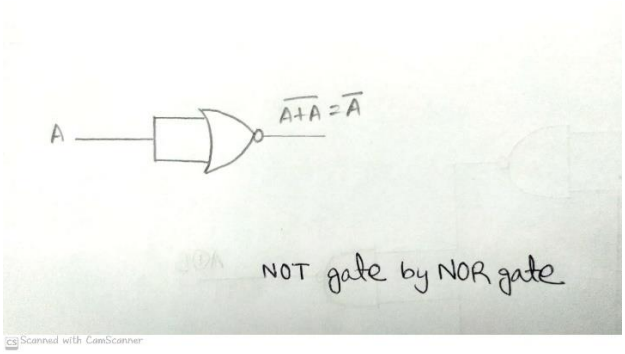


XOR GATE USING NAND GATES

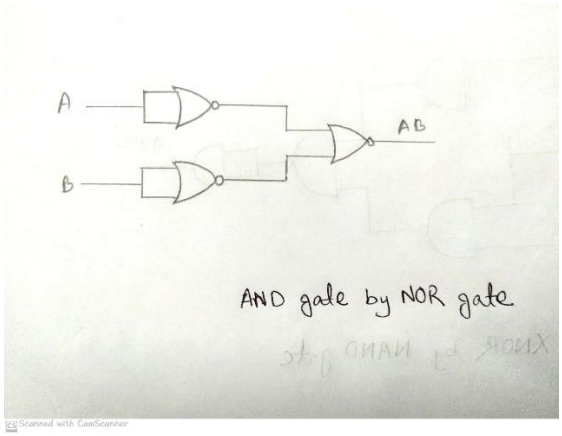


XNOR GATE USING NAND GATES

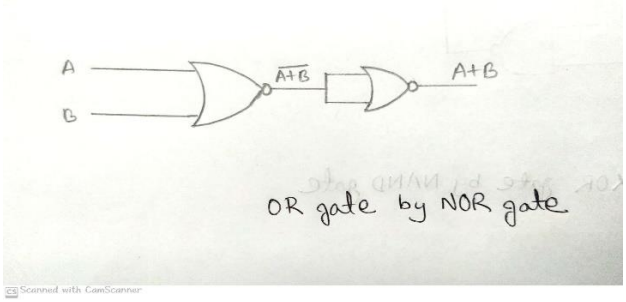
***Figure F1**: Implementation of XOR and XNOR using NAND gates*



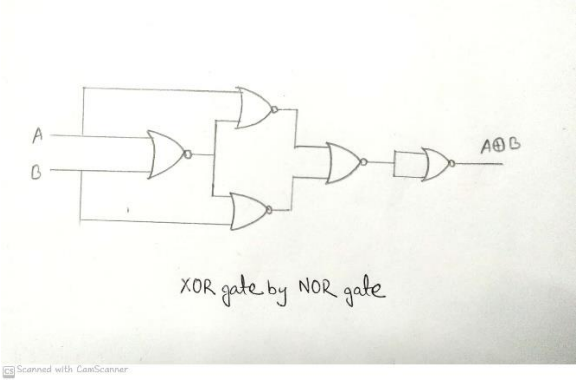
NOT Gate using Nor Gate



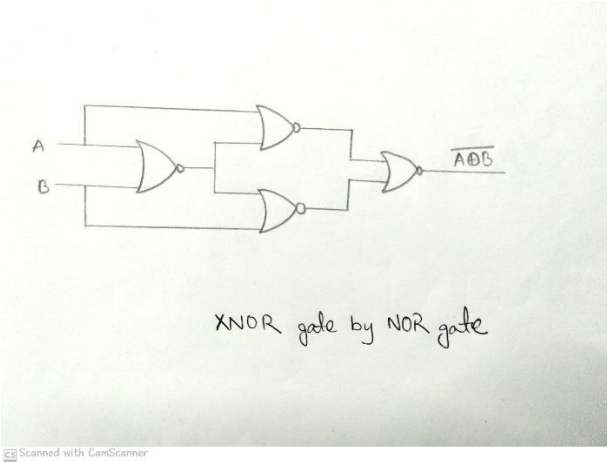
AND Gate using NOR Gate



OR gate using NOR Gate



XOR gate using NOR Gate



XNOR gate using NOR Gate

Figure F2: *Implementation of NOT, AND, OR, XOR and XNOR using NOR gates*

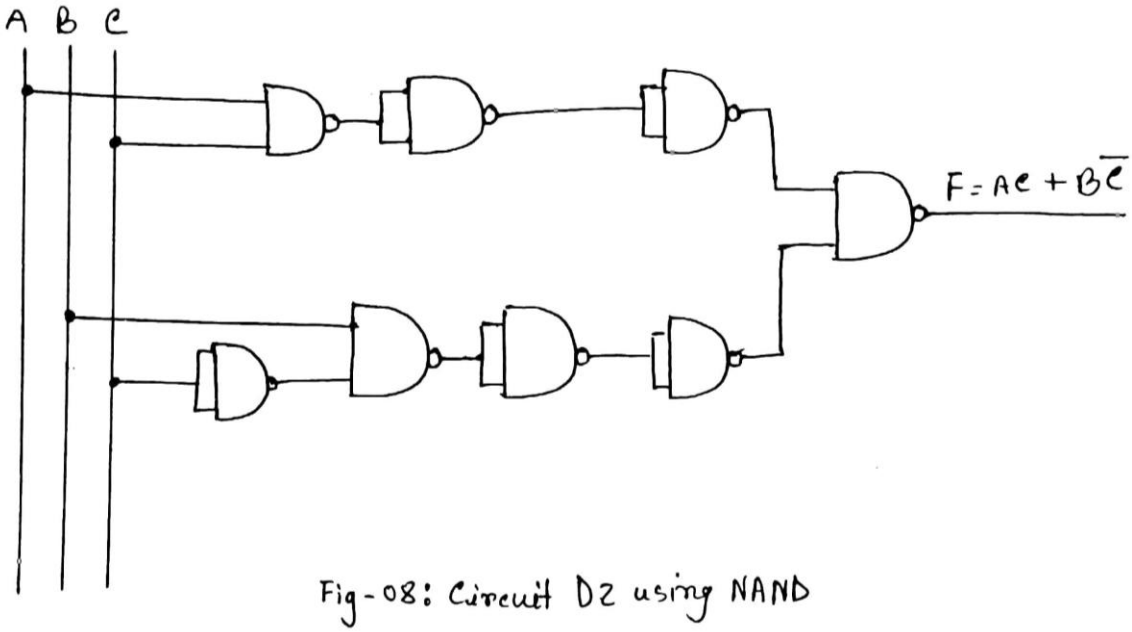


Figure3.1*-Part-1: Replaced by Nand Gate*

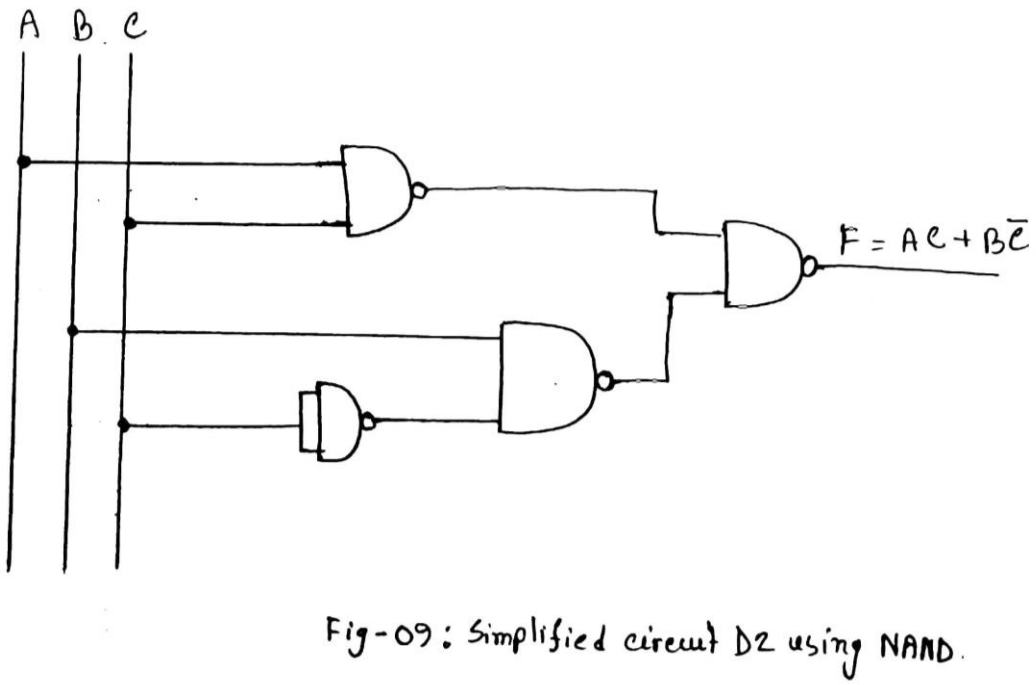


***Figure3.2**-Part-2 : Simplified Circuit using NAND gates*

***Figure F3:** Universal (NAND) gate implementation of the circuit of Figure D2*

DATA & TABLE

A	B	C	I_1=AC	I_2=BC'	F= I_1 + I_2
0	0	0	0	0	**0**
0	0	1	0	0	**0**
0	1	0	0	1	**1**
0	1	1	0	0	**0**
1	0	0	0	0	**0**
1	0	1	1	0	**1**
1	1	0	0	1	**1**
1	1	1	1	0	**1**

Table F1: Truth table of combinational circuit in Figure B2

Result Analysis and Discussion

In this experiment our goal of the experiment is to understand the concepts of universal gate. We know that Nand gate and Nor gate are universal gate.AT first we implement Xor and Xnor gate by using nand gate and after that we implement xor and xnor gate by using Nor gate. we learned about how to implement all the logic gates using universal logic gate. we had to build a combinational circuit and replace each of the gate with its Nand equivalent gate. Then we simplify it. We also did a truth table for F= AC+BC', for truth table we use basic formula of different gates.

Contribution

Name	Contribution In
Khalid Bin Shafiq	Figure F3, Data Table
Rafidul Islam	Figure F1, F2
Rashiqur Rahman Rifat	Theory, Result Analysis & Discussion
Towsif Muhtadi Khan	Figure C1, Figure D2, (Writer)

Lab 2: Universal Logic Gates

Tasks to do:

1. Complete all the tables & figures (F1. to F3.)

2. Attach the relevant screenshots of simulated circuits.

F. Experimental Data

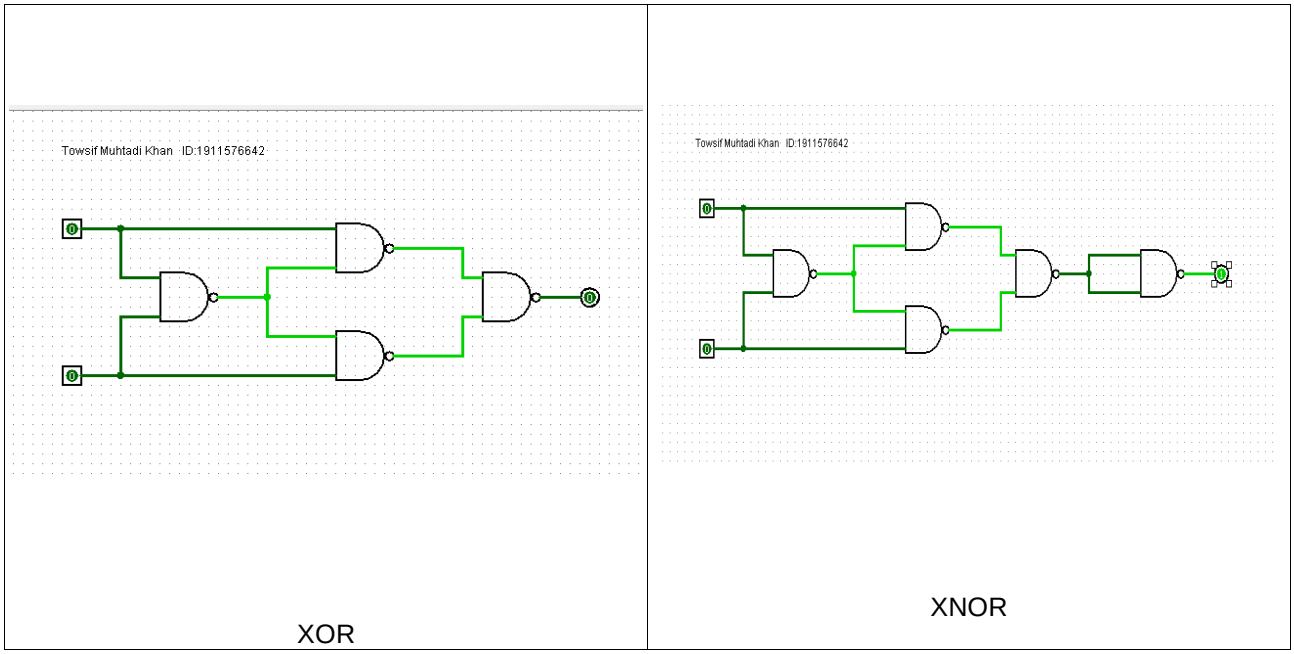
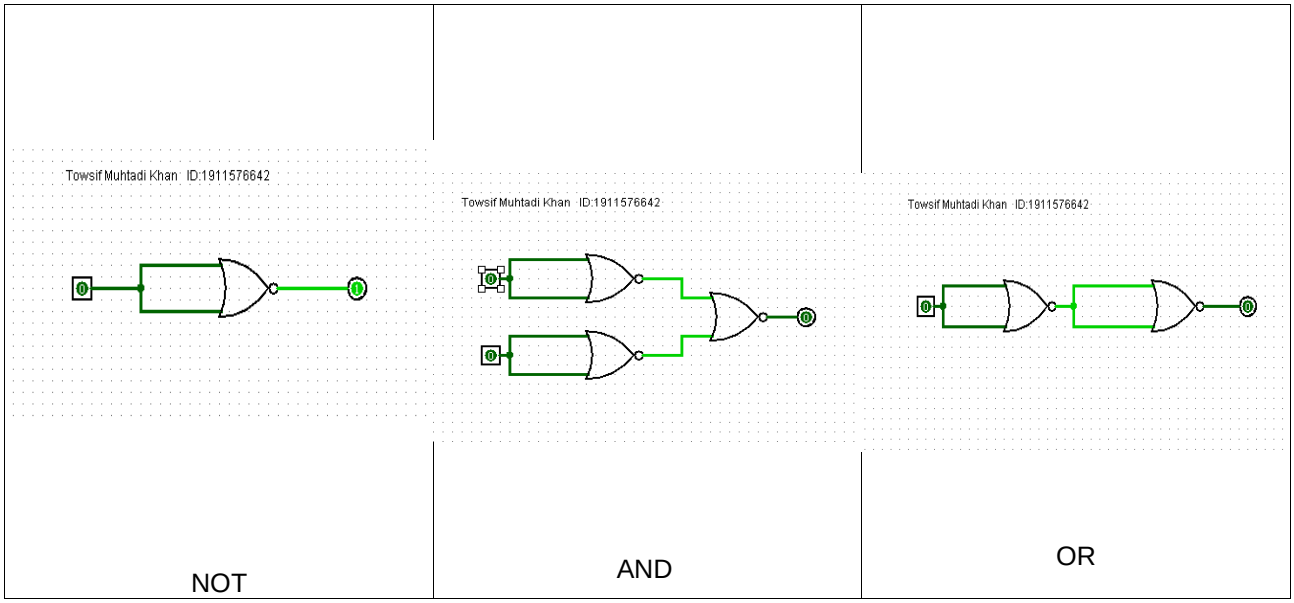


Figure F1: Implementation of XOR and XNOR using NAND gates



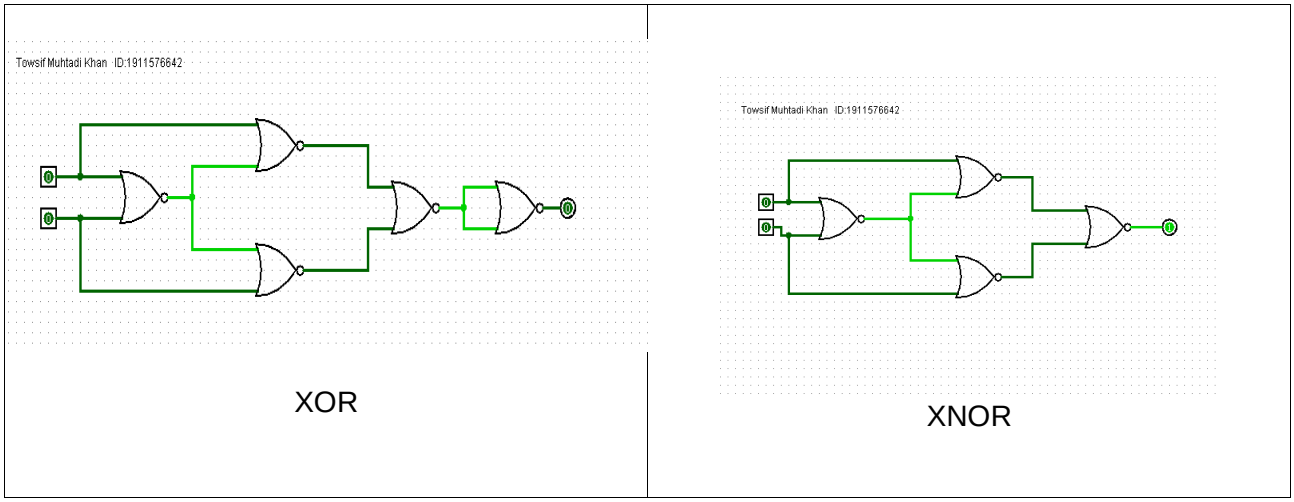
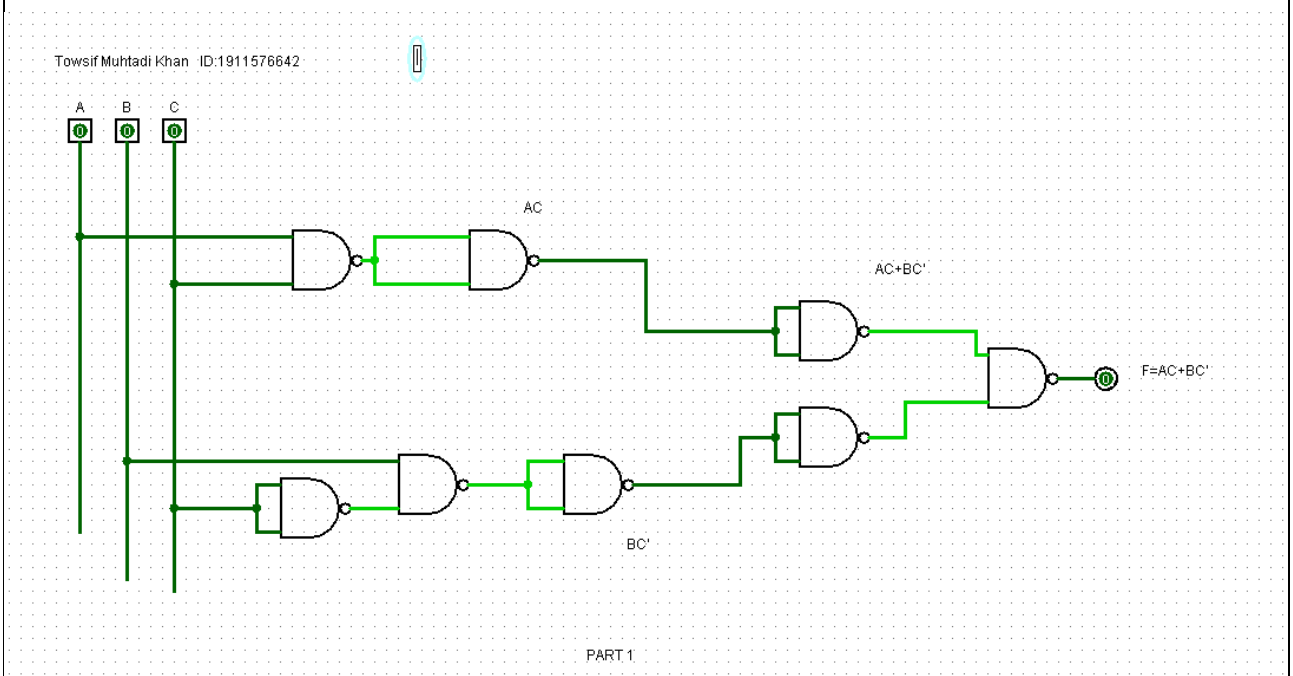


Figure F2: Implementation of NOT, AND, OR, XOR and XNOR using NOR gates

A B C	I_1 = AC	I_2 = BC'	**F** = $I_1 + I_2$
0 0 0	0	0	0
0 0 1	0	0	0
0 1 0	0	1	1
0 1 1	0	0	0
1 0 0	0	0	0
1 0 1	1	0	1
1 1 0	0	1	1
1 1 1	1	0	1

Table F1: Truth table of combinational circuit in Figure B2

Part 1


Towsif Muhtadi Khan ID:1911576642
A
B
C
AC
AC+BC'
F=AC+BC'
BC'
PART 1

Part 2

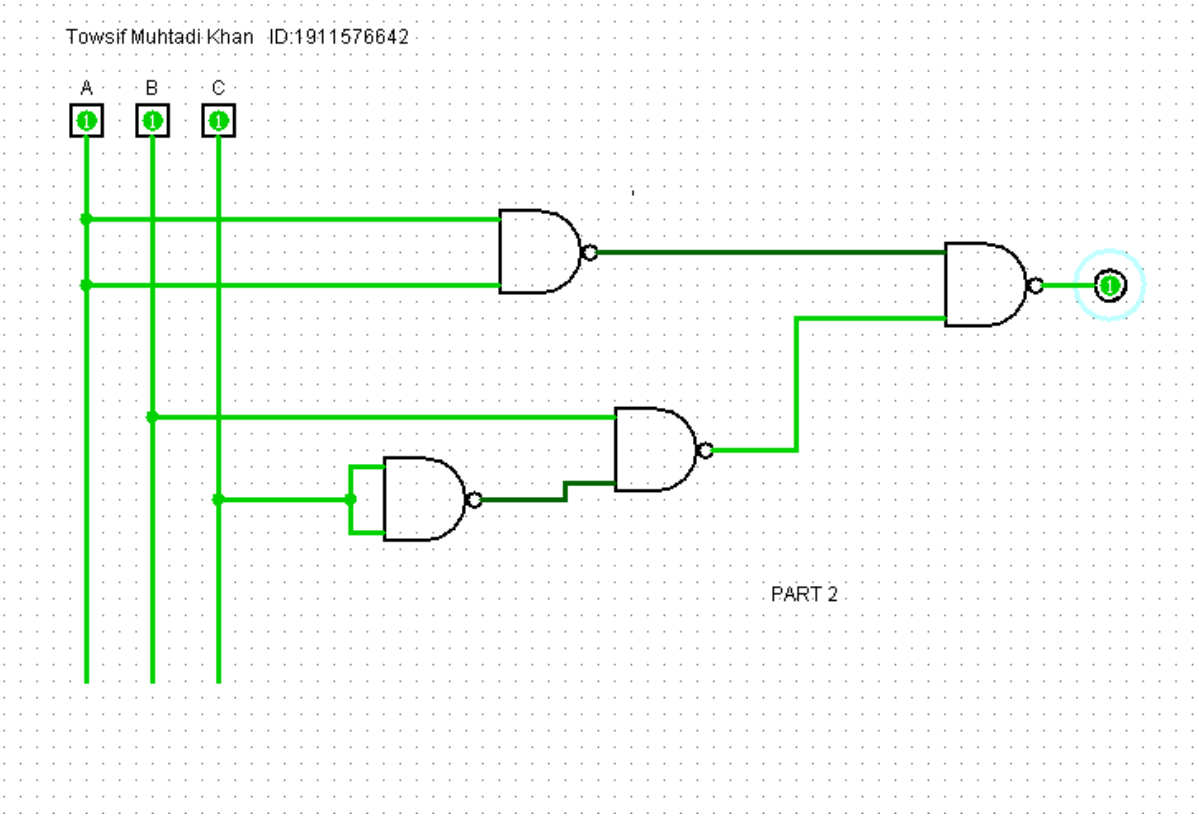

Towsif Muhtadi Khan ID:1911576642
A
B
C
PART 2

Figure F3: Universal (NAND) gate implementation of the circuit of Figure D2

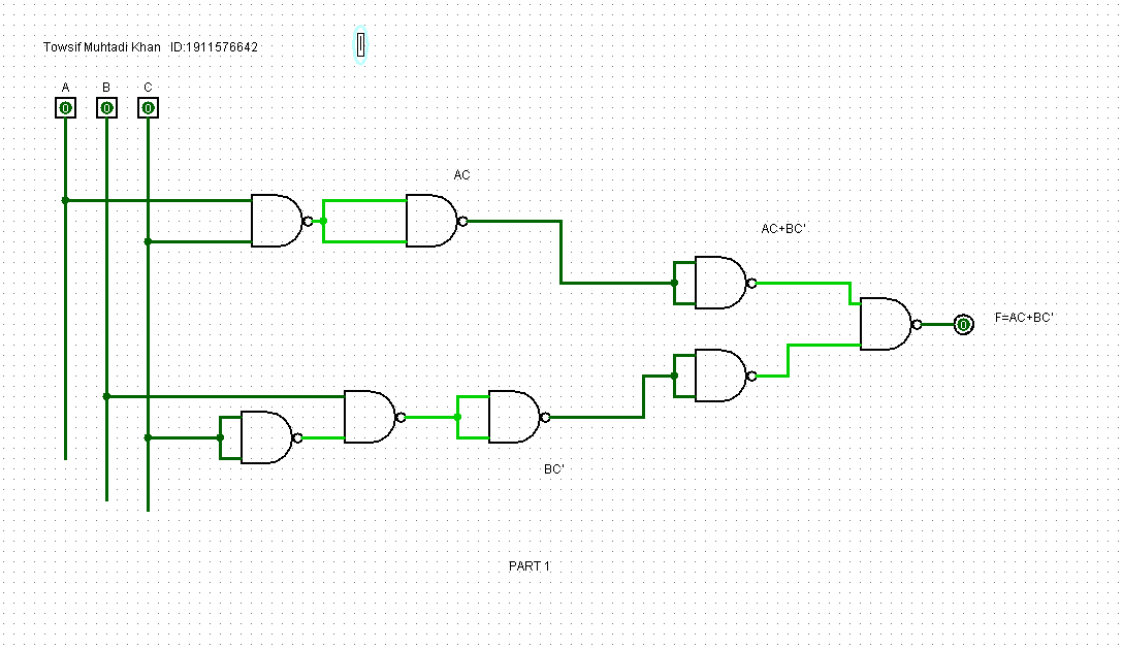


Figure3.1-Part-1: Replaced by Nand Gate

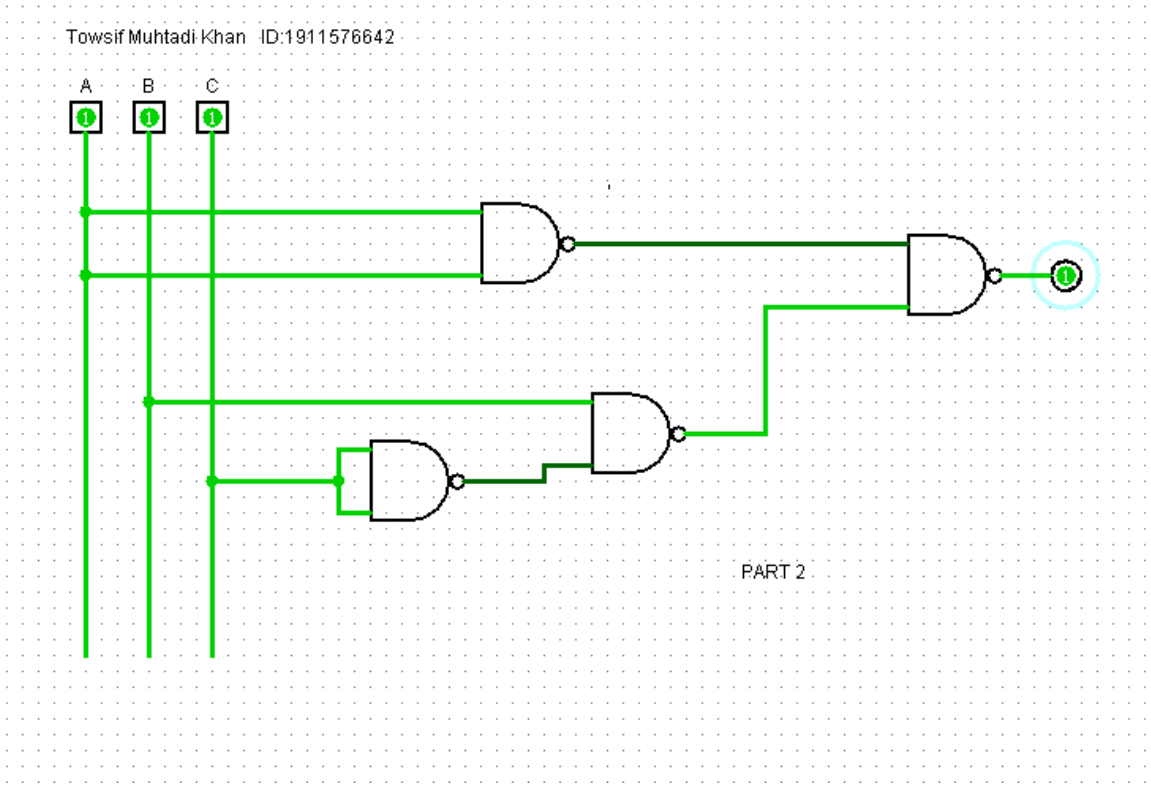


Figure3.2-Part-2:

Towsif Muhtadi Khan -1911576642