North South University

Department of Computer Science and Engineering

Final, Summer-2021

Course No: **CSE231** Course Title: **Digital Logic Design**

Full Marks: 60 Time: 1hr 10 min

	Guidelines for Final Examinations-Summer Semester 2021 1. Clearly write your name and id on top of your first page. You will be deducted 5 (five) points if it is not done. 2. Use pen (pencil only for diagram) and paper for answering questions. 3. Use camscanner if possible to take pictures. 4. Create a single PDF file and rename your file name with your name. submit one file only. If multiple files/images are submitted, all copies will be deleted. 5. Any scripts that are identified as submitted late will be penalized by 1 point per min. 6. Student must not take help from anyone, web resources, books etc. It is strictly prohibited. Failing to do so could result in disqualification. 7. There are a good mixture of questions of different difficulty level. Use your knowledge in answering questions that you are capable of answering by yourself. **8. If plagarism is detected (of any form) you will be given zero in final exam and an "F" grade in the course. No makeup/viva or any form of alternatives will be provided** **9. Students who were involved in plagiarism (provider/receiver) will have the same fate** **10. If anyone is suspected of violating the above-mentioned rules, he/she will be called for a Viva. The syllabus for Viva will include all chapters covered throughout the semester.**	
1	Design a circuit that can detect 4 consecutive 1's.	1

. Draw state diagram & State Table

Write down Boolean functions 5

2. a. Draw the circuit of a 4 bit Ripple Counter. write down the output of counter for the first 4 clock cycles. Assume initial value of the register is 0010 10

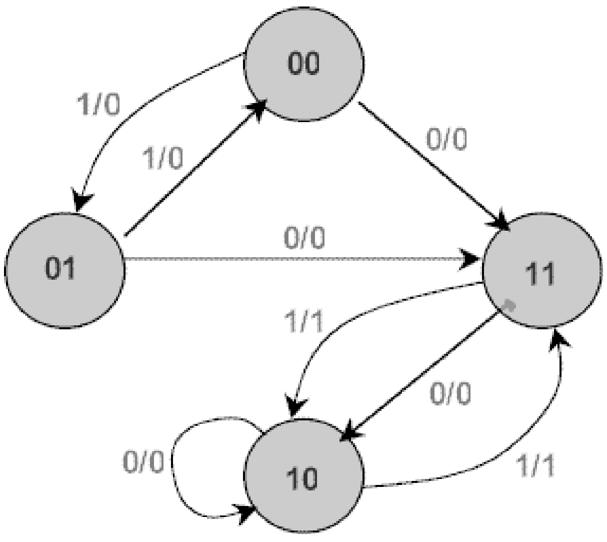
b. Design a 8x4 ROM (using decoder) with the following contents.

Address	Data
000	0001
001	0001
010	1110
011	0000
100	0111
101	0110
110	1111
111	0101

3. Consider a sequential circuit that can detect the following pattern 0101. You need to draw the state diagram (optimum) only. The sequence may repeat and the last value of a sequence can be considered as the starting of a new sequence. 10

4. a. Draw the state table based on the following state diagram. 15

b. Extend the state table for the input of T types of flip flop



5.	Consider the following piece of code and implement it using digital circuit.
	
	i=10,
	
	while (i>0)
	
	{
	  If (A[i]<B[i])
	    Sum[i] = A[i] + B[i]
	    else
	    Sum[i] = A[i] x 2
	
	i--
	}
	
	Use only functional block to solve the program. The design must be fully operational.
	Explain the operation of the proposed solution
	Each array contains 4 bit data
		15

6.	Reduce the number of state in the following ***state table, tabulate the reduced table, and draw the state diagram***.	10

Present State	Next State		Output	
	x = 0	x = 1	x = 0	x = 1
a	*f*	*b*	0	0
b	*d*	*c*	0	1
c	*f*	*e*	1	0
d	*g*	*a*	0	1
e	*d*	*c*	0	1
f	*f*	*b*	0	0
g	*g*	*h*	0	0
h	*g*	*h*	0	0
