North South University

Department of Electrical and Computer Engineering

LAB REPORT-05

Course name: Digital Logic Design Lab

Course Code: 231.L

Experiment Number: 05

Experiment name: Binary Arithmetic

Experiment Date: 6th April, 2021

Report Submission Date: 13th April, 2021

Section: 06

Group no: 04

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Remarks:	**Score:**

OBJECTIVES:

- Understand the concept of binary addition and subtraction.
- Learn about half and full binary adders.
- Perform binary addition and subtraction using IC7483.
- Understand the concept of BCD addition and implement a BCD adder using IC7483.

THEORY:

Binary arithmetic is used in digital systems mainly because the numbers (decimal and floating-point numbers) are stored in binary format in most computer systems. All arithmetic operations such as addition, subtraction, multiplication, and division are done in binary representation of numbers.

In Digital Circuits, A Binary Adder-Subtractor is one which is capable of both addition and subtraction of binary numbers in one circuit itself. The operation being performed depends upon the binary value the control signal holds. It is one of the components of the ALU (Arithmetic Logic Unit). This Circuit Requires prerequisite knowledge of Ex-OR Gate, Binary Addition and Subtraction, Full Adder.

Let's consider two 4-bit binary numbers A and B as inputs to the Digital Circuit for the operation with digits A0, A1, A2, A3 for A and B0, B1, B2, B3 for B. The circuit consists of 4 full adders since we are performing operation on 4-bit numbers. There is a control line K that holds a binary value of either 0 or 1 which determines that the operation being carried out is addition or subtraction.

EQUIPMENT LIST:

- Trainer board
- 1 x IC 7483 4-bit binary adder
- 1 x IC 7486 quadruple 2-Input XOR gates
- 2 x IC 7483 4-bit binary adder
- 2 x IC 7483 4-bit binary adder
- 1 x IC 7408 quadruple 2-Input AND gates
- 1 x IC 7432 quadruple 2-Input OR gates

CIRCUIT DIAGRAM:

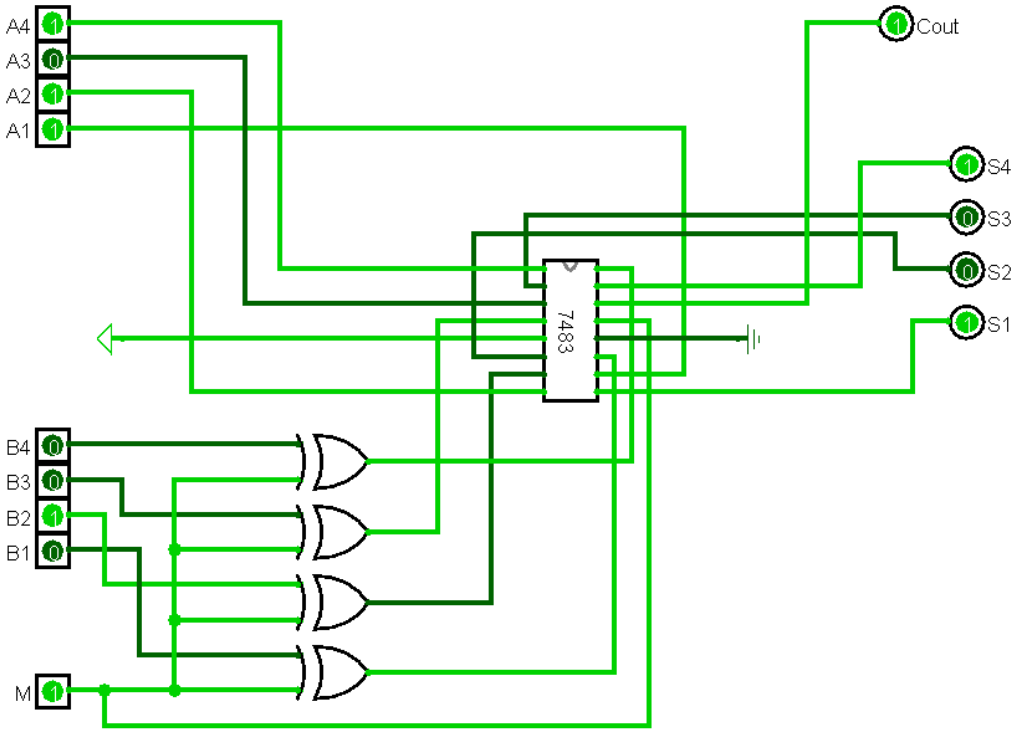

Fig-F.1: Circuit for Binary Adder-Subtractor

FIG – F.1: CIRCUIT FOR BINARY ADDED SUBTRACTOR

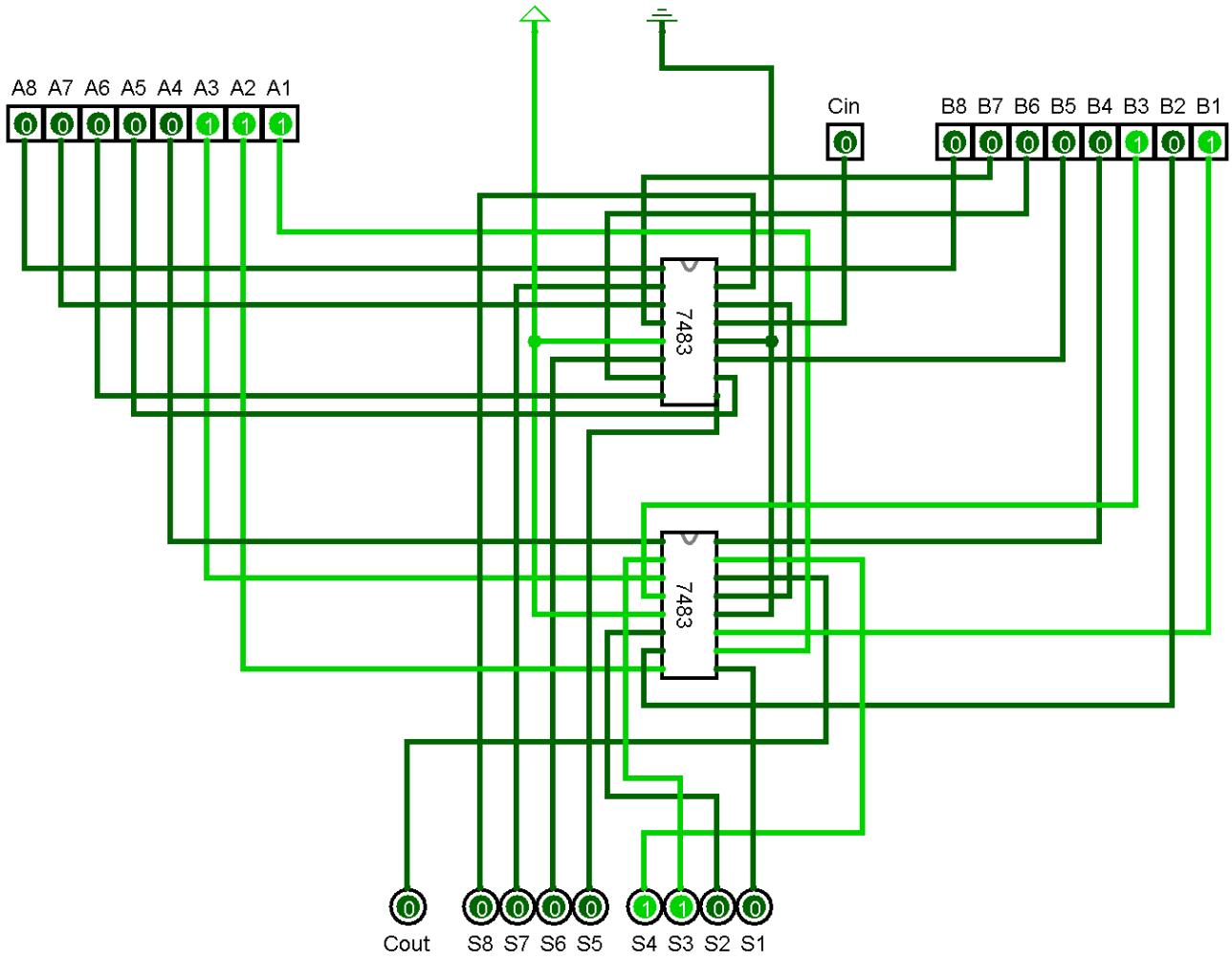

FIG – F.2: RIPPLE-THROUGH-CARRY-ADDER

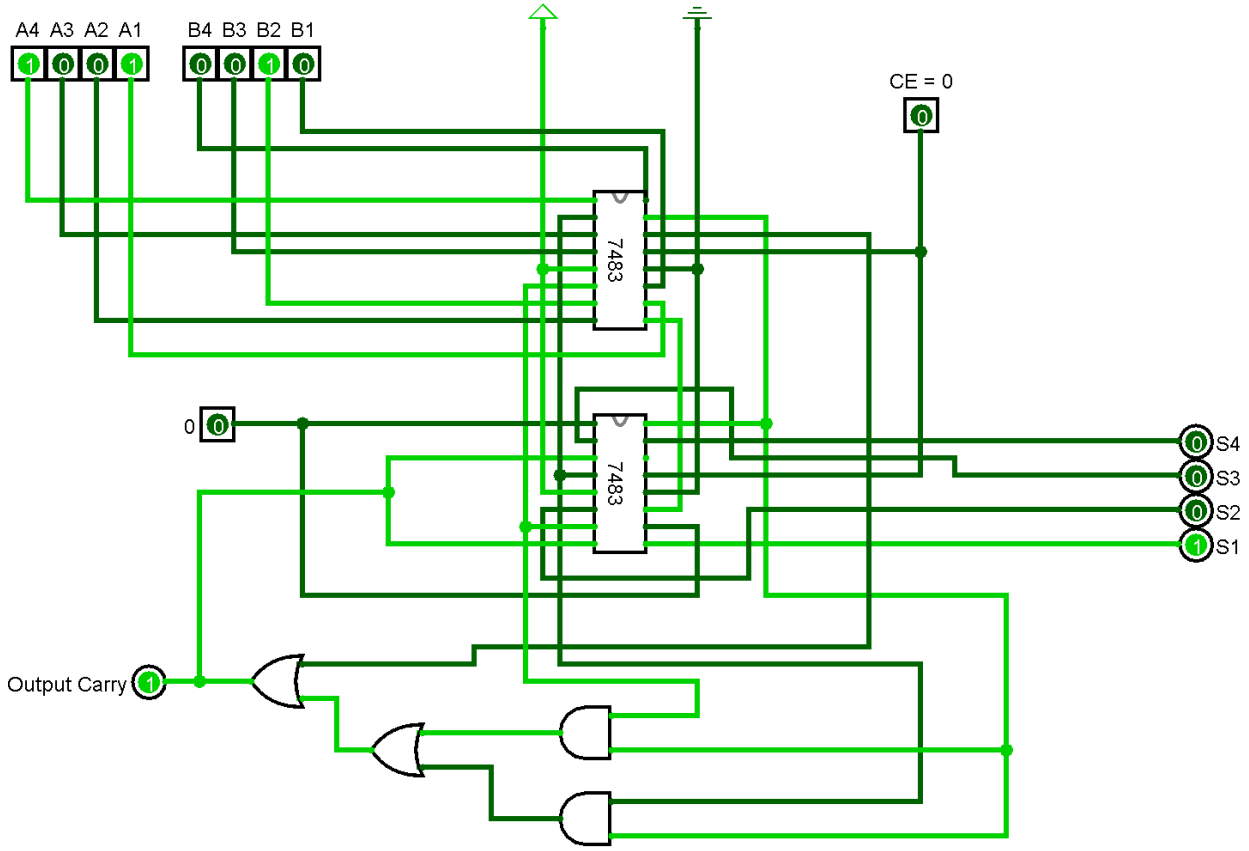

FIG – F.3: BCD ADDER

DATA & TABLE:

F.1 *Experimental Data (Binary Adder-Subtractor):*

Operation	M	A	B	C4	S4 S3 S2 S1
7 + 5	0	0111	0101	0	1100
4 + 6	0	0100	0110	0	1010
9 + 11	0	1001	1011	1	0100
15 + 15	0	1111	1111	1	1110
7 – 5	1	0111	0101	1	0010
4 – 6	1	0100	0110	0	1110
11 – 2	1	1011	0010	1	1001
15 – 15	1	1111	1111	1	0000

Table F.1.1

F.2 *Experimental Data (Ripple-Through-Carry Adder):*

Operation	A	B	Overflow Carry	Sum
7 + 5	00000111	00000101	0	00001100
18 + 19	00010010	00010011	0	00100101
72 + 83	01001000	01010011	0	10011011
129 + 255	10000001	11111111	1	10000000

TableF.2.1

F.3 *Experimental Data (BCD Adder):*

Decimal	Binary Sum						BCD Sum			
Value	**K**	**Z_3**	**Z_2**	**Z_1**	**Z_0**	**C**	**S_3**	**S_2**	**S_1**	**S_0**
0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	1
2	0	0	0	1	0	0	0	0	1	0
3	0	0	0	1	1	0	0	0	1	1
4	0	0	1	0	0	0	0	1	0	0
5	0	0	1	0	1	0	0	1	0	1
6	0	0	1	1	0	0	0	1	1	0
7	0	0	1	1	1	0	0	1	1	1
8	0	1	0	0	0	0	1	0	0	0
9	0	1	0	0	1	0	1	0	0	1
10	0	1	0	1	0	1	0	0	0	0
11	0	1	0	1	1	1	0	0	0	1
12	0	1	1	0	0	1	0	0	1	0
13	0	1	1	0	1	1	0	0	1	1
14	0	1	1	1	0	1	0	1	0	0
15	0	1	1	1	1	1	0	1	0	1
16	1	0	0	0	0	1	0	1	1	0
17	1	0	0	0	1	1	0	1	1	1
18	1	0	0	1	0	1	1	0	0	0
19	1	0	0	1	1	1	1	0	0	1

Table F.3.1

Operation	A	B	Overflow Carry	Sum
9 + 0	1001	0000	0	1001
9 + 1	1001	0001	1	0000
9 + 2	1001	0010	1	0001
9 + 3	1001	0011	1	0010
9 + 4	1001	0100	1	0011
9 + 5	1001	0101	1	0100
9 + 6	1001	0110	1	0101
9 + 7	1001	0111	1	0110
9 + 8	1001	1000	1	0111
9 + 9	1001	1001	1	1000

Table F.3.2

RESULT ANALYSIS AND DISCUSSION:

The title of the LAB 05 is “Binary Arithmetic”. From the objectives of the experiment, we can say that, in this experiment we have done binary addition and subtraction, half and full binary adders, BCD addition and have implemented a BCD adder using IC7483.
The overall lab experiment was about the various implementations of 4-bit Binary Adder.
At the beginning of experiment, we built the logic circuit as well as IC diagram for 4-bit Adder. Then we used the IC diagram to implement Binary Adder-Subtractor, 8-bit ripple carry adder and BCD Adder.
For implementation of Binary Adder-Subtractor, we had to use one 4-bit Binary Adder and 4 XOR gates.
For implementation of 8-bit ripple carry adder, we had to use two 4-bit Binary Adders.
For implementation of BCD Adder, we had to use two 4-bit Binary Adders, two 2-input AND gates and one 2-input OR gate.
From the experiment, we learned about the working process of Binary Adder-Subtractor, 8-bit ripple carry adder and BCD Adder and their implementations by using 4-bit binary Adder.

CONTRIBUTION

NAME	CONTRIBUTION IN
Khalid Bin Shafiq	**CIRCUIT DIAGRAM**
Rafidul Islam	**RESULT ANALYSIS AND DISCUSSION**
Rashiqur Rahman Rifat	**THEORY**
Towsif Muhtadi Khan	**DATA & TABLE, COORDINATOR**

Class Assignment 05

Task-1: Complete the data tables.

Task -2: Attach the Simulation Part

F.1 Experimental Data (Binary Adder-Subtractor):

Operation	M	A	B	C4	S4 S3 S2 S1
7 + 5	0	**0111**	**0101**	**0**	**1100**
4 + 6	0	**0100**	**0110**	**0**	**1010**
9 + 11	0	**1001**	**1011**	**1**	**0100**
15 + 15	0	**1111**	**1111**	**1**	**1110**
7 – 5	1	**0111**	**0101**	**1**	**0010**
4 – 6	1	**0100**	**0110**	**0**	**1110**
11 – 2	1	**1011**	**0010**	**1**	**1001**
15 – 15	1	**1111**	**1111**	**1**	**0000**

TableF.1.1

F.2 Experimental Data (Ripple-Through-Carry Adder):

Operation	A	B	Overflow Carry	Sum
7 + 5	**00000111**	**00000101**	**0**	**00001100**
18 + 19	**00010010**	**00010011**	**0**	**00100101**
72 + 83	**01001000**	**01010011**	**0**	**10011011**
129 + 255	**10000001**	**11111111**	**1**	**10000000**

Table F.2.1

F.3 Experimental Data (BCD Adder):

Decimal Value	Binary Sum					BCD Sum				
	K	Z_3	Z_2	Z_1	Z_0	C	S_3	S_2	S_1	S_0
0	0	0	0	0	0	**0**	**0**	**0**	**0**	**0**
1	0	0	0	0	1	**0**	**0**	**0**	**0**	**1**
2	0	0	0	1	0	**0**	**0**	**0**	**1**	**0**
3	0	0	0	1	1	**0**	**0**	**0**	**1**	**1**
4	0	0	1	0	0	**0**	**0**	**1**	**0**	**0**
5	0	0	1	0	1	**0**	**0**	**1**	**0**	**1**
6	0	0	1	1	0	**0**	**0**	**1**	**1**	**0**
7	0	0	1	1	1	**0**	**0**	**1**	**1**	**1**
8	0	1	0	0	0	**0**	**1**	**0**	**0**	**0**
9	0	1	0	0	1	**0**	**1**	**0**	**0**	**1**
10	0	1	0	1	0	**1**	**0**	**0**	**0**	**0**

11	0	1	0	1	1	**1**	**0**	**0**	**0**	**1**
12	0	1	1	0	0	**1**	**0**	**0**	**1**	**0**
13	0	1	1	0	1	**1**	**0**	**0**	**1**	**1**
14	0	1	1	1	0	**1**	**0**	**1**	**0**	**0**
15	0	1	1	1	1	**1**	**0**	**1**	**0**	**1**
16	1	0	0	0	0	**1**	**0**	**1**	**1**	**0**
17	1	0	0	0	1	**1**	**0**	**1**	**1**	**1**
18	1	0	0	1	0	**1**	**1**	**0**	**0**	**0**
19	1	0	0	1	1	**1**	**1**	**0**	**0**	**1**

Table F.3.1

Operation	**A**	**B**	**Overflow Carry**	**Sum**
9 + 0				
9 + 1				
9 + 2				
9 + 3				
9 + 4				
9 + 5				
9 + 6				
9 + 7				
9 + 8				
9 + 9				

Table F.

Class Assignment 05

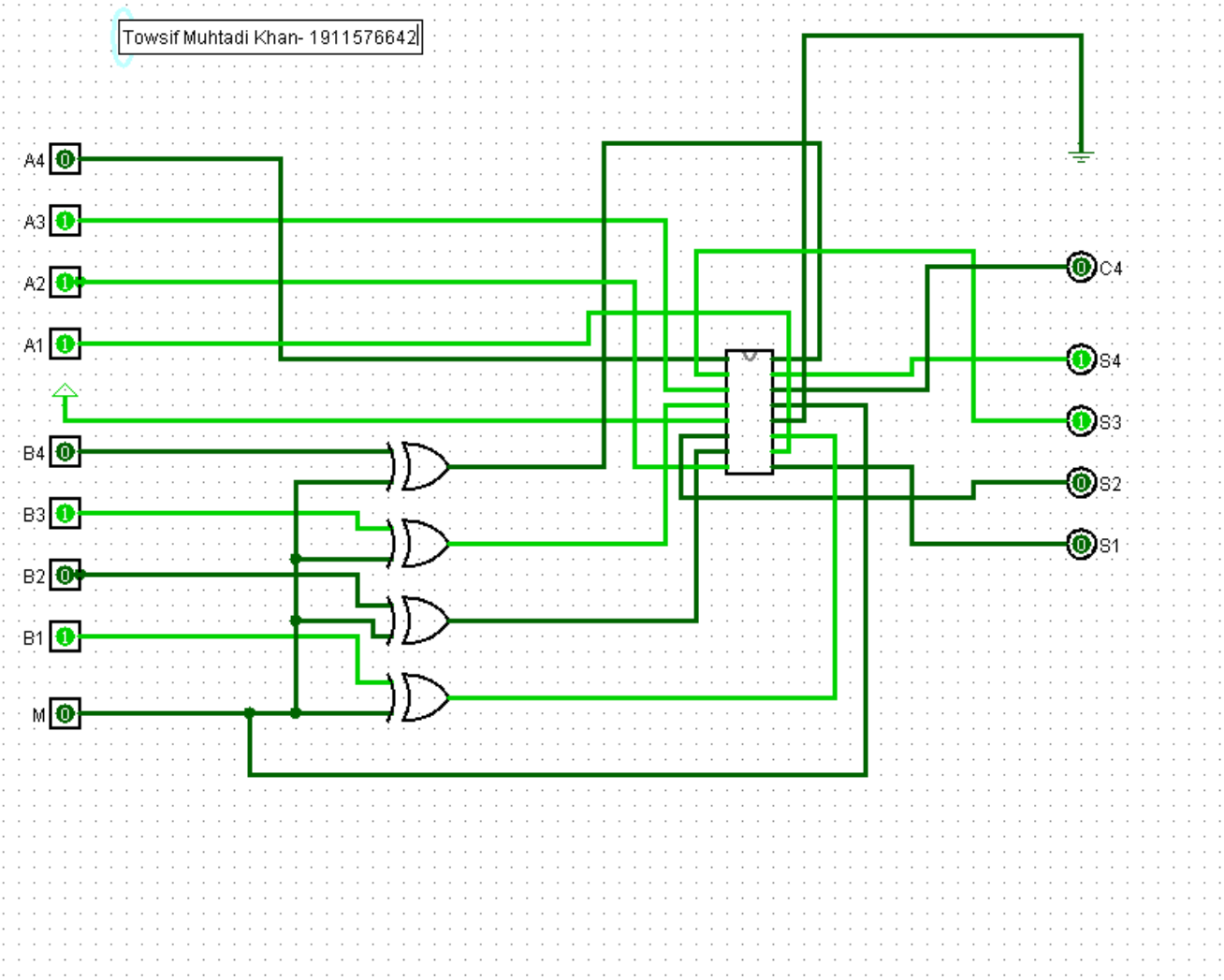

Figure: **Binary adder Subtractor**

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