The aim of the project is to assess the students' ability to tie in theoretical and experimental knowledge from CSE 231 to complete a practical project as a future Computer Science Engineer, and to work in a team. Information on groups and Team Leaders is outlined in Sec. 1.

The project consists of three phases. Each phase consists of an individual deadline that are summarized in Sec. 2. It is imperative that you meet all deadlines in order to complete the full project in due time. The mark distribution for the project is summarized in Sec. 3. The project description is given in Sec. 4. Objectives or tasks for each phase of the project are described in Sec. 5.

1 Groups

Each group must assign a responsible Team Leader. The responsibilities of the team leader include (but are not limited to) the following:

- Hold meeting with group and decide on design.
- Hold regular meetings with group to ensure project is on track.
- Delegate tasks and deadlines to individual group members.
- Ensure group members complete their assigned tasks.
- Ensure project deadlines are met.
- Keep track of project budget, or assign another group member to do so.

The group leaders must send me an email stating the name and Id of the group members by 1st December. The subject must be 183_CSE231.7_groupXX_project. Here, XX should be replaced by your group number. All future emails regarding the project should be sent as a reply to this email.

2 Deadlines

Combinational Circuit Design (Basic and Universal Logic Gates.)	3rd December
Combinational Circuit Design (Mux, Encoder/ Decoder)	3rd December
Sequential Circuit Design	8th December
Combinational Circuit Implementation	11th December
Sequential Circuit Implementation & Viva Presentation	**TBA**

3 Mark Distributions

Mark distribution for the project is outlined below.

Combinational Circuit Design	25
Combinational Circuit Implementation	10
Sequential Circuit Design	25
Sequential Circuit Implementation	25
Viva Presentation	15
Total	**100**

Final marks will only be confirmed upon satisfactory completion of the project. Marks will be given at the discretion of the faculty member considering the group is capable of the work submitted based on their overall performance.

3.1 Late Submission

Failure to meet each deadline will result in a deduction of 20% for each deadline missed.

Failure to complete the project by the final deadline will result in an award of **0 mark**.

3.2 Plagiarism

Plagiarism will **NOT** be tolerated. Any form of plagiarism will result in an immediate award of **0 mark** to the group for the entire project. Same applies to the hardware implementation. If multiple reports are found as copies, an immediate award of **0 mark** shall be awarded to **ALL** parties without further deliberation.

4 Project Description

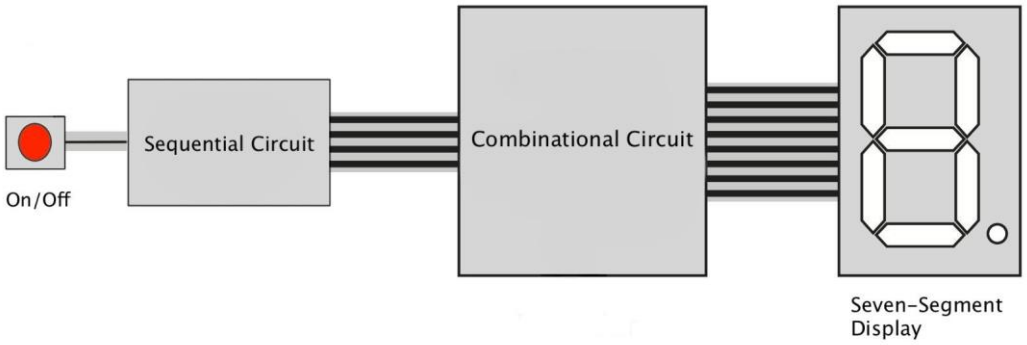

Figure 1: Circuit block diagram. Sequential circuit produces a sequence of codes. Code from sequential circuit is decoded by combinational circuit to light up corresponding segments of a seven-segment display.

Consider the digital system shown in Fig. 1. Switching on the circuit results in the string of characters **"CSE231.7GX$_1$X$_2$ProJ"** being displayed on the seven-segment display one character at a time at a set time interval of 2-3 seconds. Here, "**X$_1$X$_2$**" represents your **group no**. At the end of the sequence, the string is repeated.

The sequential logic circuit produces a sequence of codes that are required to represent the string of characters **"CSE231.7GX$_1$X$_2$ProJ".** The sequential logic circuit is connected to an active high or active low seven-segment display via a combinational logic circuit. The latter decodes the input codes from the sequential logic circuit in order to drive the individual segments of the seven-segment display to show each character 'C', 'S', 'E' ,'2', '3', '1', '.' , '7' , 'G', 'X$_1$' , 'X$_2$' , 'P' , 'r' , 'o' , 'J' as dictated by the sequence.

NOTE: Only **ONE** seven-segment display is to be used and the display will show one character at a time based on the sequence.

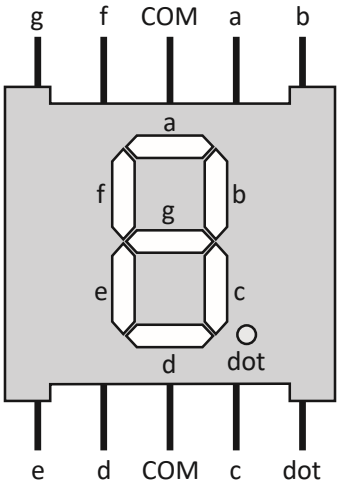

Figure 2: Segment and pin configuration of a seven-segment display. For an active high display, each segment (a – g and dot) light up when a logic high is applied to its corresponding input pin.

Fig. 2 shows the schematic of seven-segment display with its segments and corresponding input pins labelled (a – g). The COM ports are for V_{CC} *(for Common Anode)* and *Gnd (for Common Cathode)*.

5 Objectives

1. **Combinational Circuit Design**

Design the combinational logic part of the system described in Sec. 4, that is, the circuit to display the characters of the string **"CSE231.7GX$_1$X$_2$ProJ"** on a seven segment display. Groups will show their group no. instead of **X$_1$X$_2$**

All the groups need to design the Combinational Circuit Using:

1. Basic Logic Gates
2. Universal Logic Gates
3. Multiplexer
4. Decoder or Encoder

   Please note that you will get four different designs for the same output using this four types of IC's. And if you wish, you may design it based on programmable logic also.

The group must complete a working schematic of the four circuit designs using Logisim and submit a soft-copy of it, on or before the deadline via electronic mail.

2. **Combinational Circuit Implementation**

It is at the discretion of the group to opt for their choice of implementation - minimal logic, universal logic, decoder, multiplexer or programmable logic. However, the group must be able to provide rationale for their design choice and it must be using relevant material covered in the course.

The group must implement and demonstrate the combinational circuit to display the required characters on a seven-segment display.

3. **Sequential Circuit Design**

Design the sequential logic part of the system described in Sec. 4, that is, the sequence generator for the string of characters **"CSE231.7GX$_1$X$_2$ProJ"**

There should be an extra input control bit. If the control bit is 0, the string should be **"CSE231.7GX$_1$X$_2$ProJ".** However, if the control bit is 1, the string should skip the next three digits and show the fourth digit when the next clock pulse arrives. For example, let's say that the control bit is initially 0. So, the seven segment display would show C. Now if we change the control bit to 1 after "C" the circuit should show "3" and skip **S,E,2** then "G" then "r" and so on. The string would be "**C3GrS1X$_1$oE.X$_2$J27P**" and repeat "**C3GrS1X$_1$oE.X$_2$J27P**" as long as the control input is kept to 1.

You should provide three different designs using J-K, T and D flip flop. The group must complete a working schematic of the three circuit designs using Logisim and submit a soft-copy of it, on or before the deadline via electronic mail.

4. **Sequential Circuit Implementation & Viva Presentation**

It is at the discretion of the group to opt for their choice of implementation –J-K, T or D filp-flop. However, the group must be able to provide rationale for their design choice and it must be using relevant material covered in the course.

Students must provide a presentation and a report describing their project.

The presentation and report both must contain important project details such as budget, project photos, truth tables, state diagram etc.

Important note: The clock pulses should be automatically provided using IC 555.