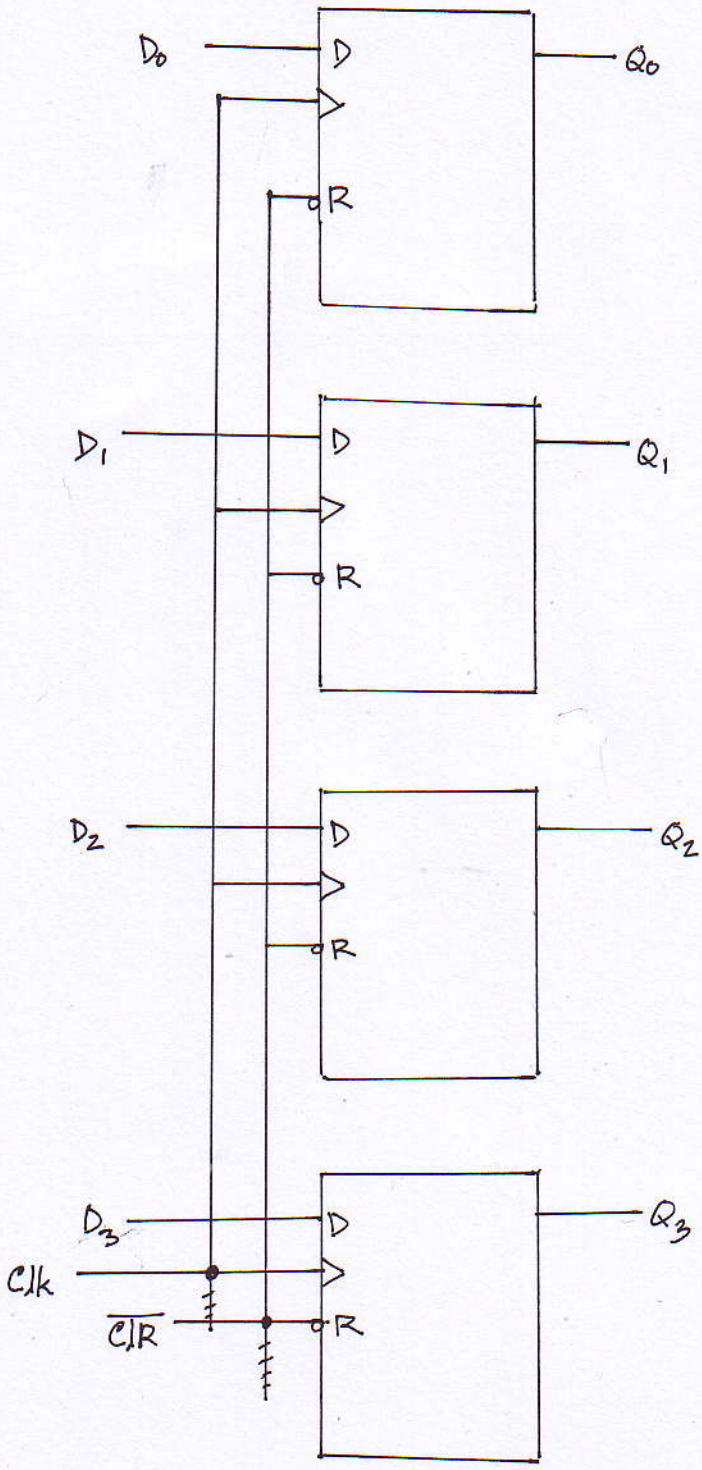
Digital Logic Design :

Lecture 16

Flip Flop Applications :

Parallel Data Storage



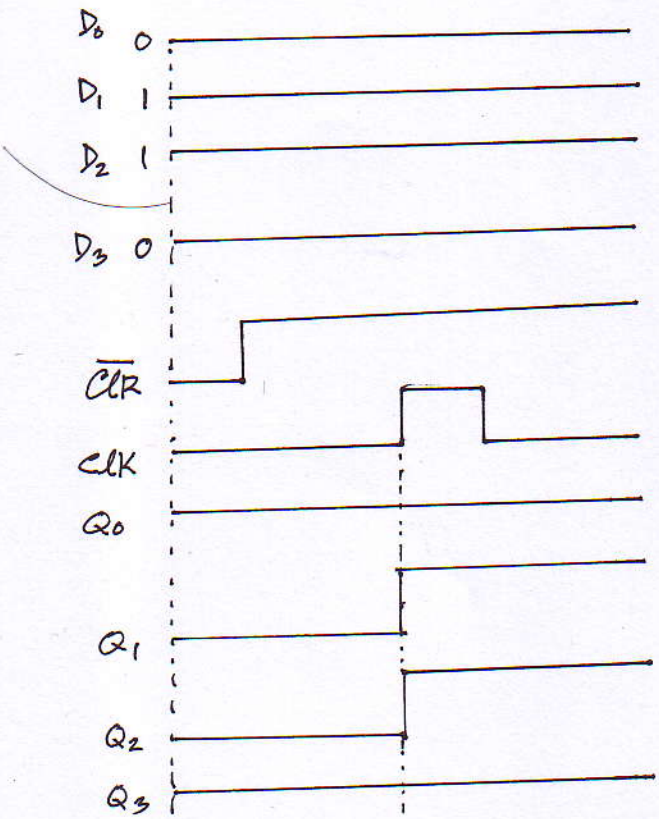
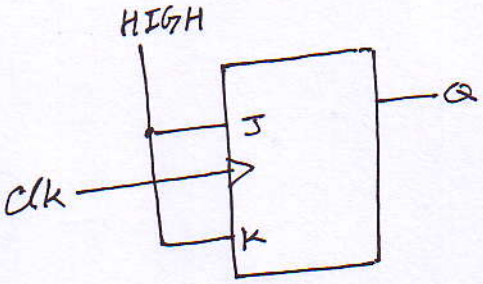
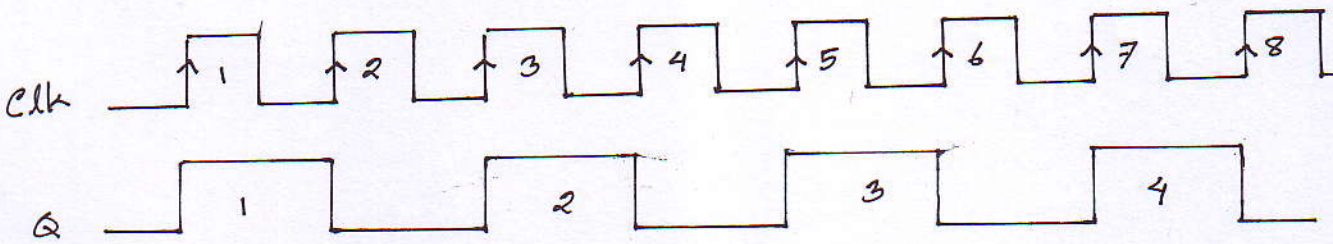


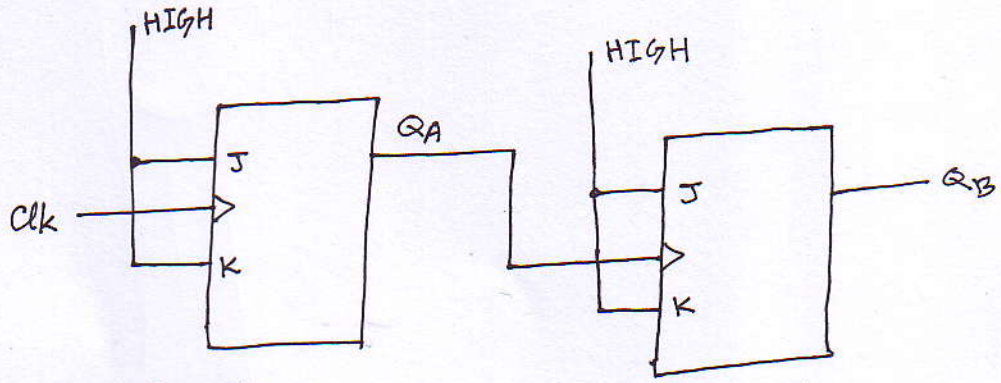
Fig : Flip Flops used for parallel data storage

Frequency Division :

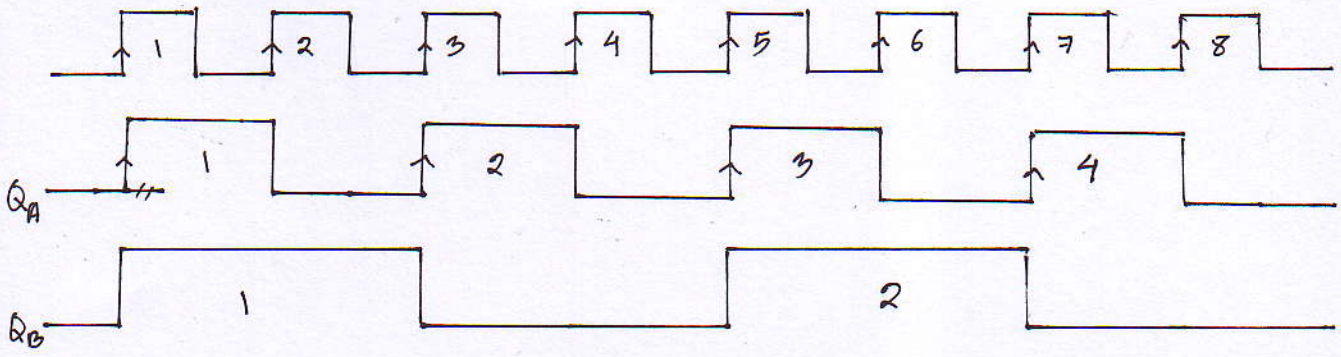
A J-K flip-flop can be used to devide the frequency of a clock by 2 when connected to toggle (J = K = ∅)



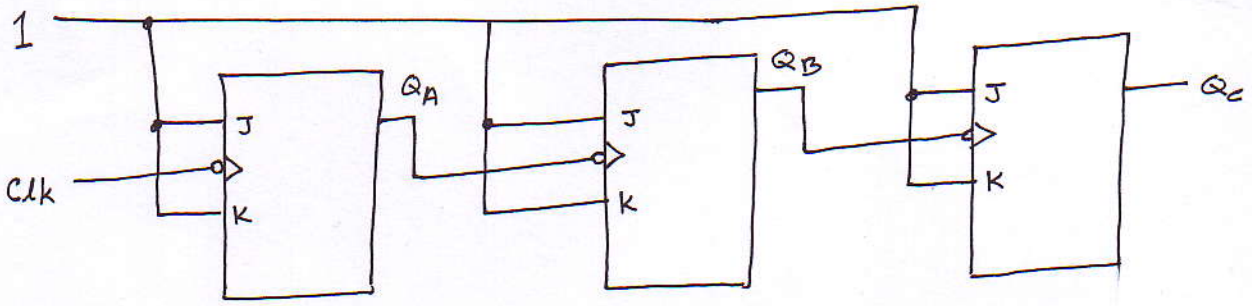


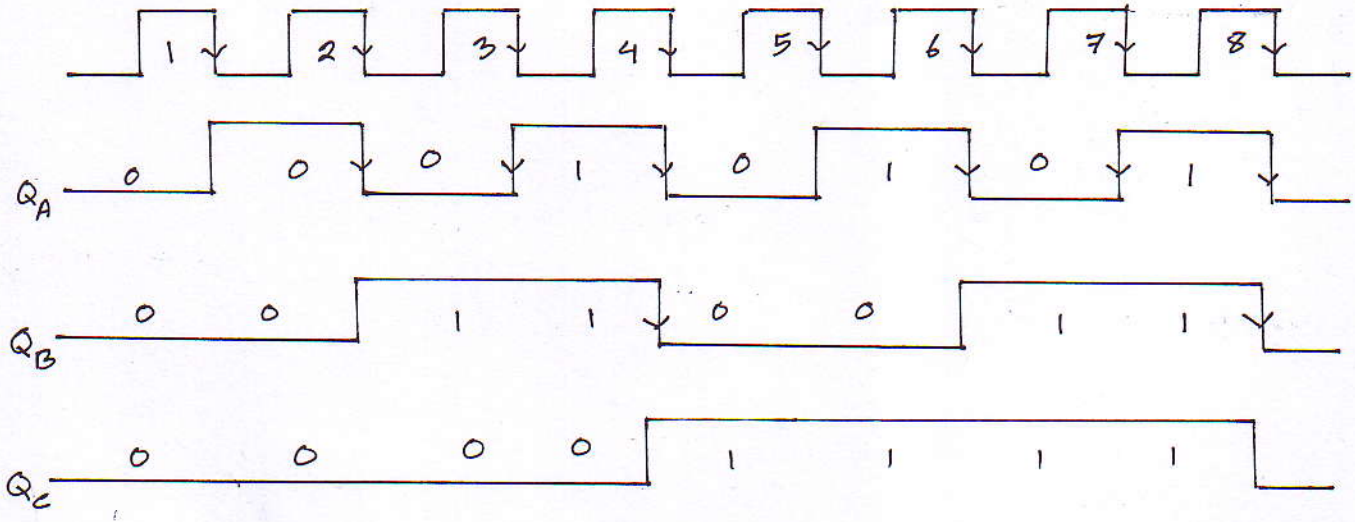


flip-flop A flip-flop B



Counting :





	Q_C	Q_B	Q_A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1

A synchronous Counter Operation :

A 2-Bit # Asynchronous Binary Counter

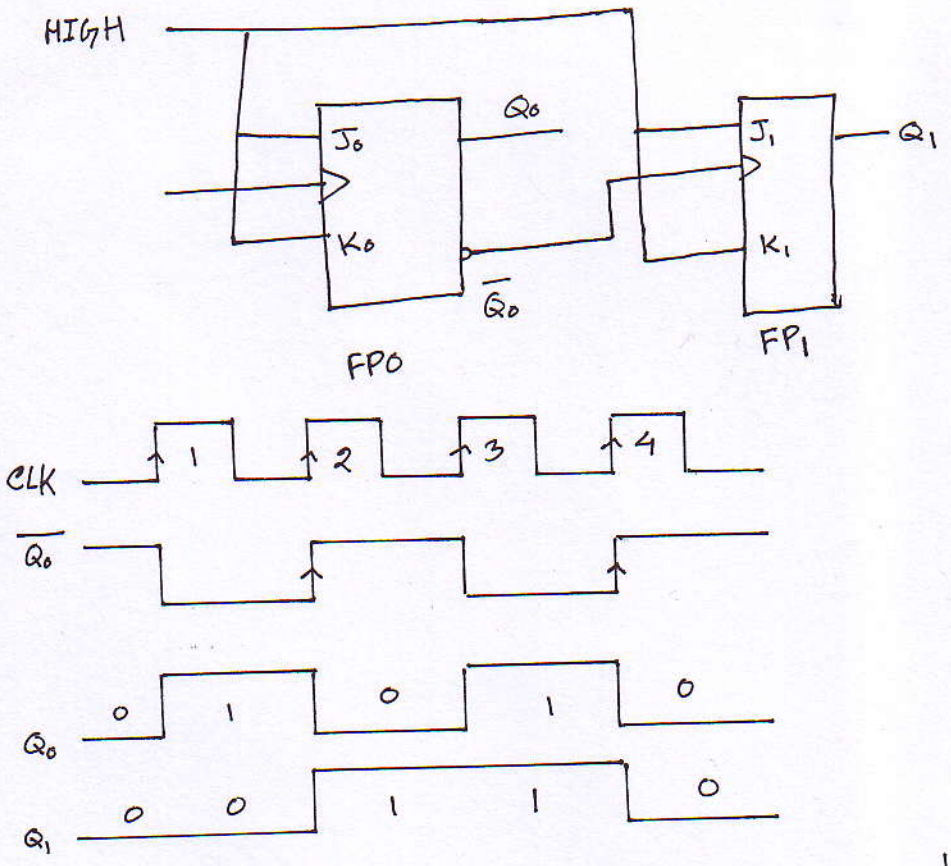
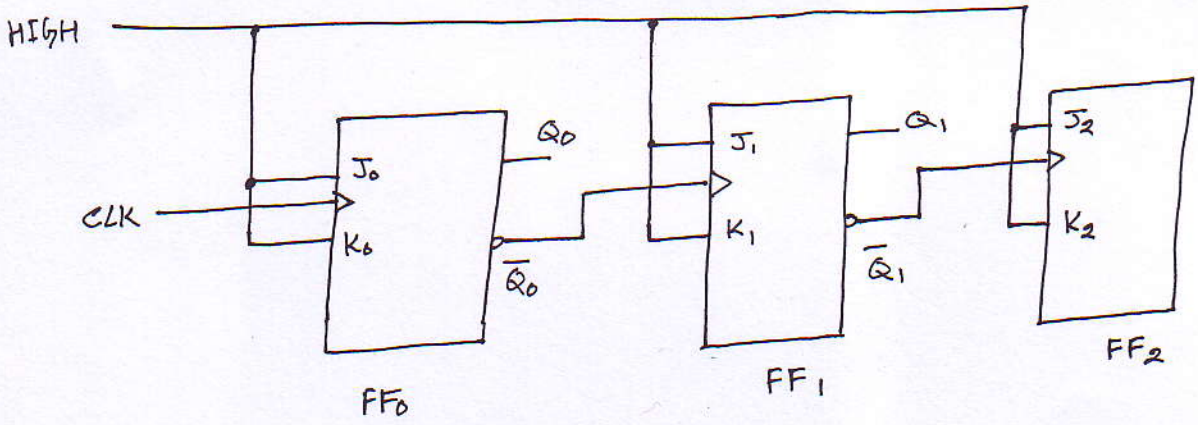


Fig : Timing diagram for the counter

Clock pulse	Q_1	Q_0
Initially	0	0
1	0	1
2	1	0
3	1	1
4 (recycles)	0	0

Table : State sequence for a 2-stage binary counter

A 3-Bit Asynchronous Binary Counter



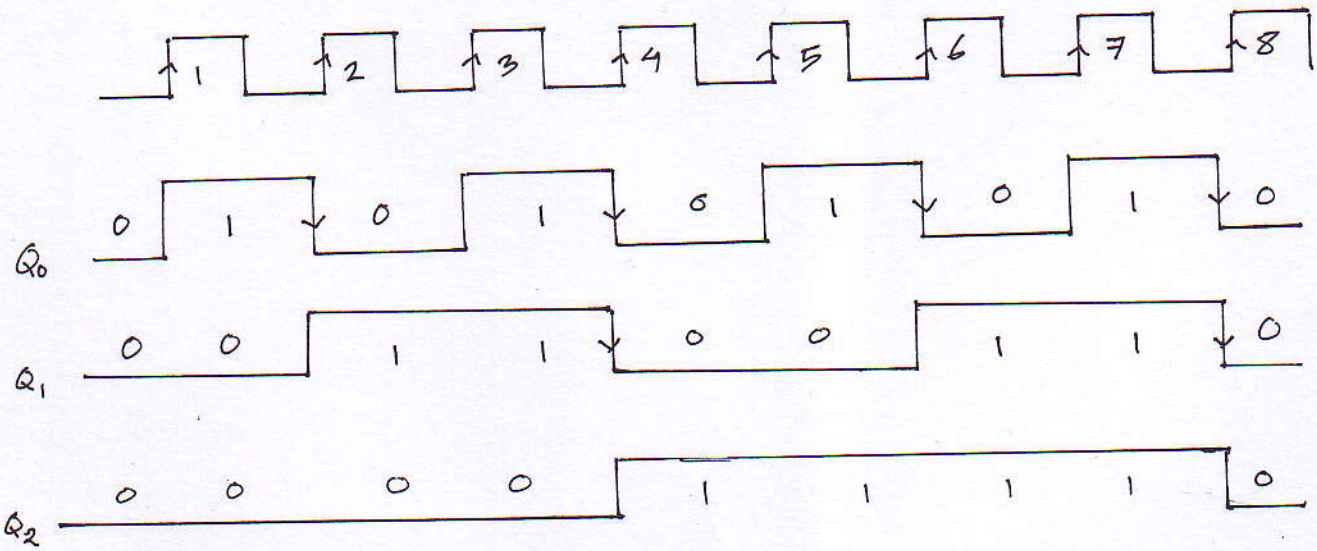
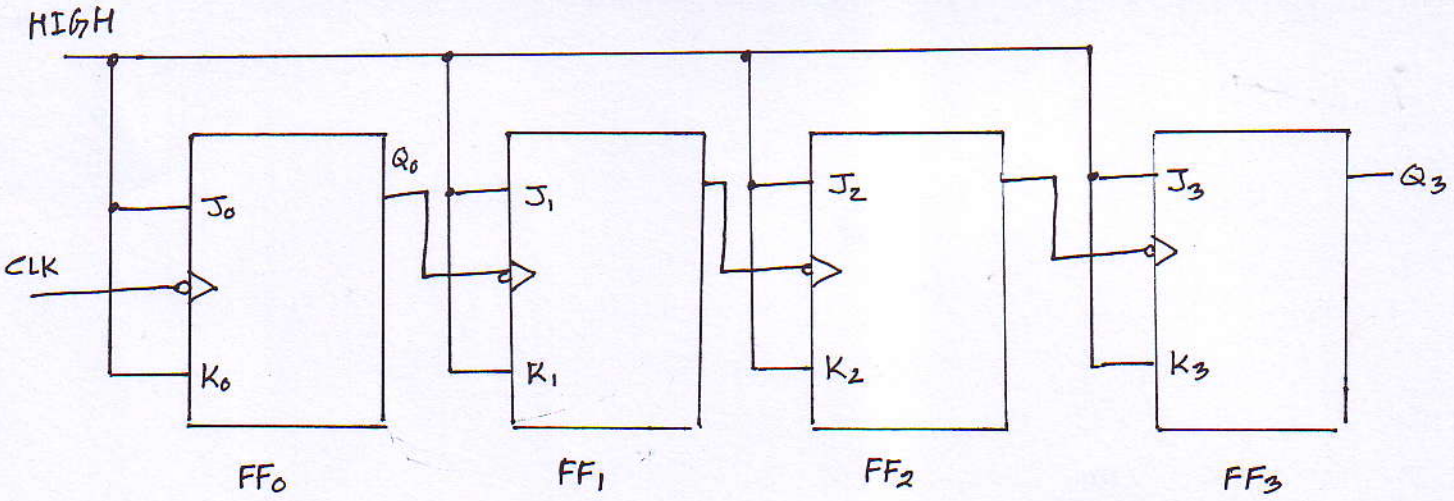


Fig : Timing diagram

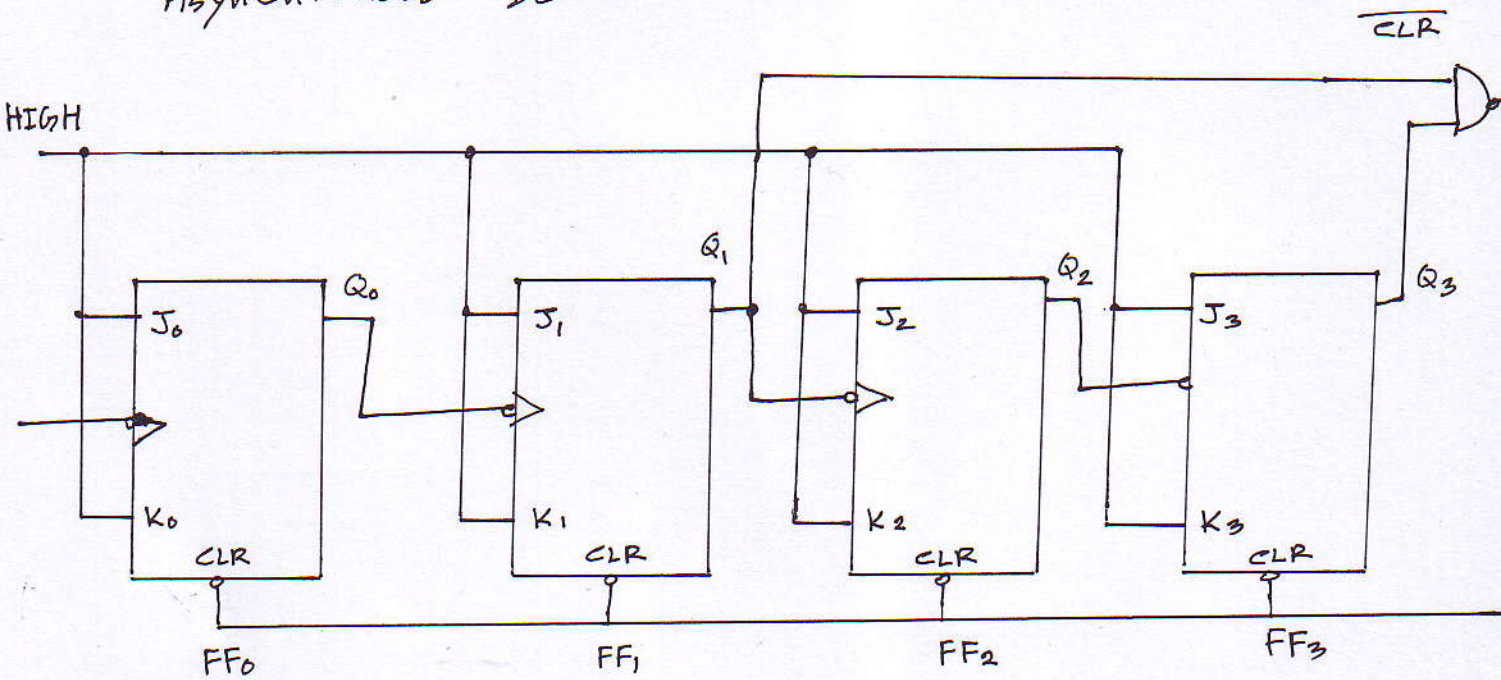
Clock pulse	Q_2	Q_1	Q_0
Initially	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8 (recycles)	0	0	0

Fig : State sequence for a 3-stage binary counter

A four bit Asynchronous binary counter :



Asynchronous Decode Counter



State sequence for an asynchronous decode counter

Clock pulse	Q_3	Q_2	Q_1	Q_0	
Initially	0	0	0	0	
1	0	0	0	1	
2	0	0	1	0	
3	0	0	1	1	
4	0	1	0	0	
5	0	1	0	1	
6	0	1	1	0	
7	0	1	1	1	
8	1	0	0	0	
9	1	0	0	1	
10	1	0	1	0	→ Decode & reset to 0000