North South University
Department of Electrical and Computer Engineering
CSE 231L: Digital Logic Design Lab

Lab instructor: Abdullah Al Noman
Lab time: R 2.40 pm - 5.50 pm (CSE231 Section 07)
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Office Location: LIB 600 (C1 and C4)
Office hours: **R** 11.20 am - 2.30 pm **A** 11.20 am - 2.30 pm **T** 11.20 am – 4.10 pm

Lab Experiments:

Experiment 1- Introduction to Digital Logic Gates and Boolean Function.

Experiment 2- Introduction to Universal Logic gates and Boolean Function Implementation.

Experiment 3- Combinational Logic Design Using Canonical Form.

Experiment 4- Combinational Logic Design Minimization and Implementation using Karnaugh maps.

Experiment 5- Logic Design and Implementation of Binary Arithmetic Circuit.

Experiment 6- Introduction to Multiplexers and Decoders.

Experiment 7- Introduction to Flip-Flops.

Experiment 8- Synchronous and Asynchronous Sequential Logic Design and Implementation.

Experiment 9- Introduction to Registers.

Marks Distribution:

- Attendance = 00%
- Class Performance = 15%
- Quiz = 20%
- Lab Reports = 15%
- Viva = 10%
- Set Up = 10%
- Final Written Test = 30%

Detailed Schedule:

Week	Exp. No.	TOPIC	DUE
1	0	How to use breadboard, trainer board and ICS	
2	1	Introduction to Digital Logic Gates and Boolean Functions	
3	2	Introduction to Universal Logic Gates and Boolean Function Implementation	
4	3	Combinational Logic Design (Canonical Form)	Lab Report-1
5	4	Combinational Logic Design (K-maps)	Lab Report-2
6	5	Logic Design and Implementation of Binary Arithmetic Circuit	Lab Report-3
7	6	Introduction to Multiplexers and Decoders	Lab Report-4, ***Quiz-1***
8	7	Introduction to Flip-Flops	Lab Report-5
9	8	Synchronous and Asynchronous Sequential Logic Design and Implementation	Lab Report-6
10	9	Introduction to Registers	Lab Report-7, ***Quiz-2***
11			Lab Report-8
12		SETUP EXAM	