Digital Logic Design :

Lecture 17

* Asynchronous clocked modulous-12 counter with asynchronous recycling.

On the 12th clock pulse the counter is to be forced to count from '0'. This can be done by decoding 1100.

State sequence :

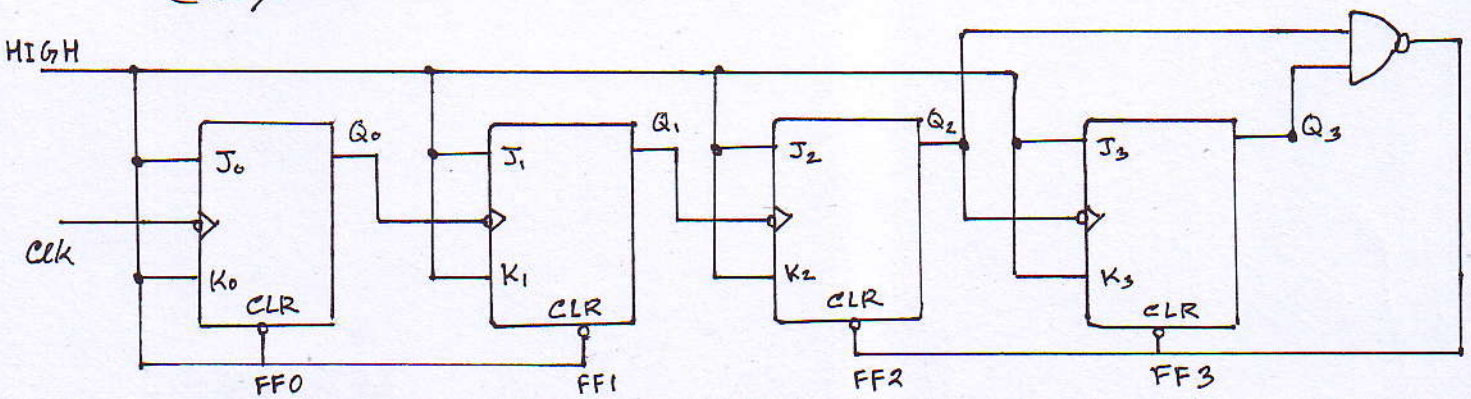
Clock pulse	Q_3	Q_2	Q_1	Q_0
Initially	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12 (recycles)	✗→0	✗→0	0	0

$J_0 = K_0 = 1$

$J_1 = K_1 = Q_0$

$J_2 = K_2 = Q_0 Q_1 \bar{Q}_3$

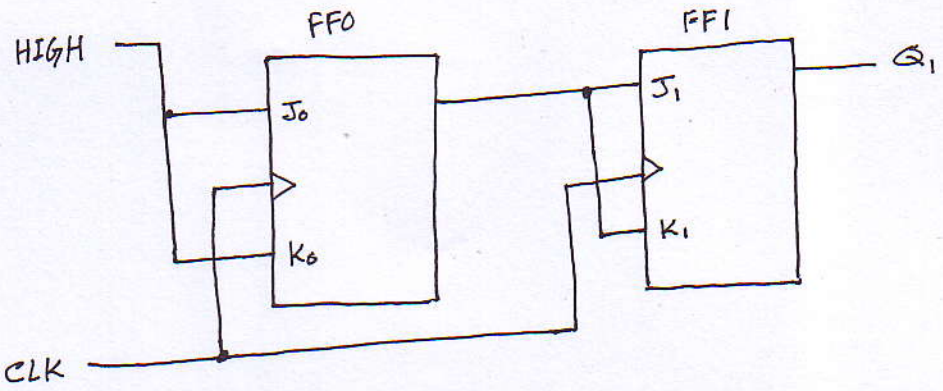
$J_3 = K_3 = Q_0 Q_1 Q_2 + Q_0 Q_1 Q_3$



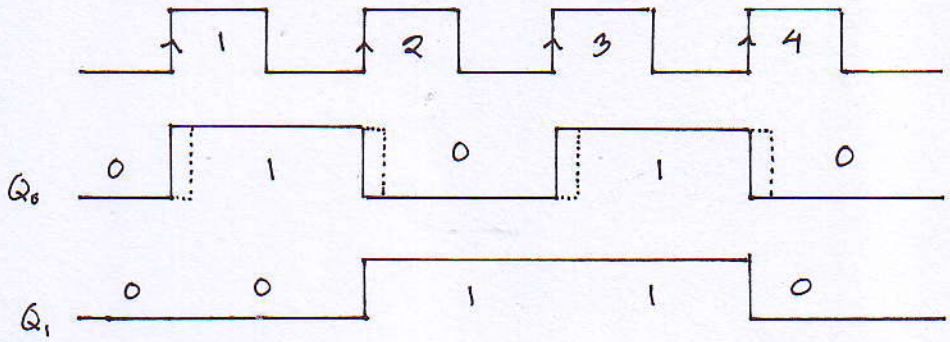
Synchronous Counter :

The flip flops within synchronous counter are all clocked at the same time by a common clock pulse.

A 2 Bit synchronous Binary Counter :



Timing diagram :



State : sequence

Clock pulse	Q_1	Q_0
Initially	0	0
1	0	1
2	1	0
3	1	1
4 (recycles)	0	0

A 3-Bit Synchronous Binary Counter :

state sequency :

clock pulse	Q_2	Q_1	Q_0
Initially	0	0	0
1	0	0	1 ✓
2	0	1	0
3	0	1	1 ✓
4	1	0	0
5	1	0	1 ✓
6	1	1	0
7	1	1	1 ✓
8 (recycles)	0	0	0

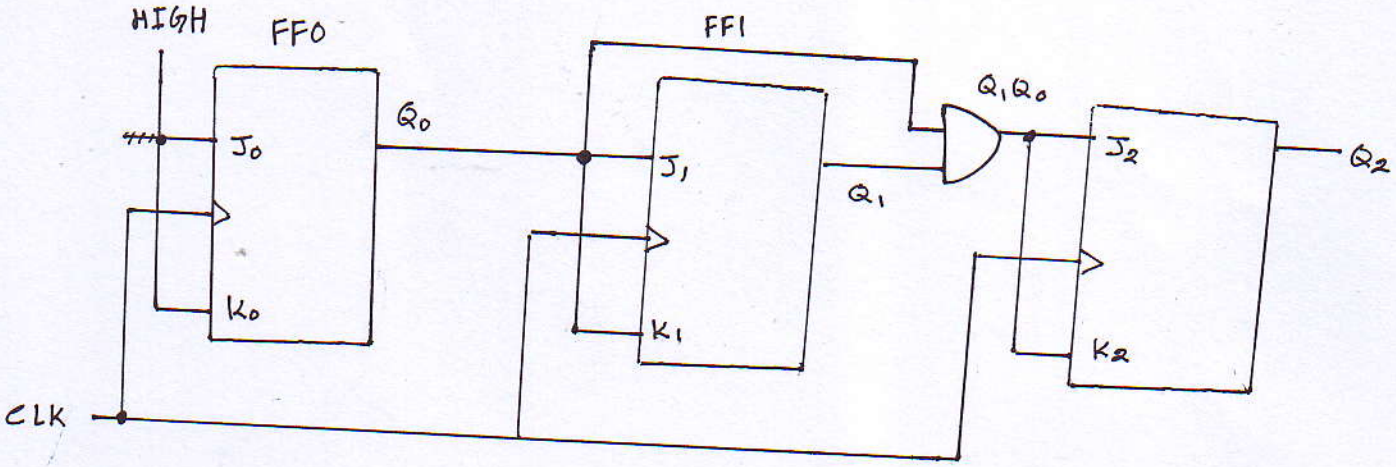


Fig : a 3-bit synchronous binary counter

$J_1 = K_1 = Q_0$

$J_2 = K_2 = Q_1Q_0$

A 4-Bit Synchronous Binary Counter

State sequence :

Clock pulse	Q_3	Q_2	Q_1	Q_0
Initially	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
16 (recycles)	0	0	0	0

$J_1 = K_1 = Q_0$

$J_2 = K_2 = Q_1 Q_0$

$J_3 = K_3 = Q_2 (Q_1 Q_0)$

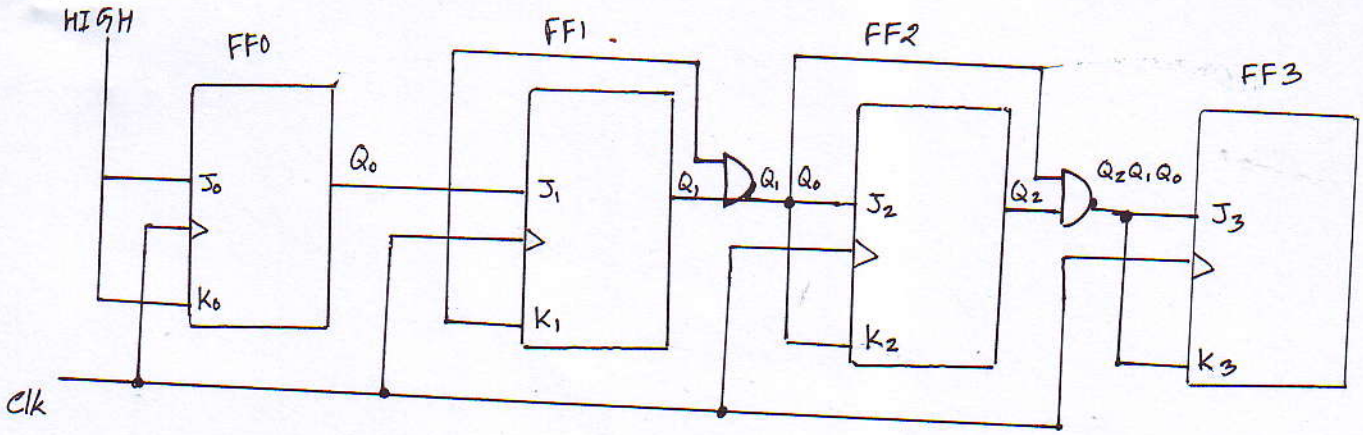


Fig : Synchronous 4-Bit Binary counter

synchronous decode counters :

state sequence :

Clock pulse	Q_3	Q_2	Q_1	Q_0
Initially	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10 (recycles)	0	0	0	0

$J_0 = K_0 = 1$

$J_1 = K_1 = Q_0\overline{Q_3}$

$J_2 = K_2 = Q_1Q_0$

$J_3 = K_3 = Q_2Q_1Q_0 + Q_3Q_0$

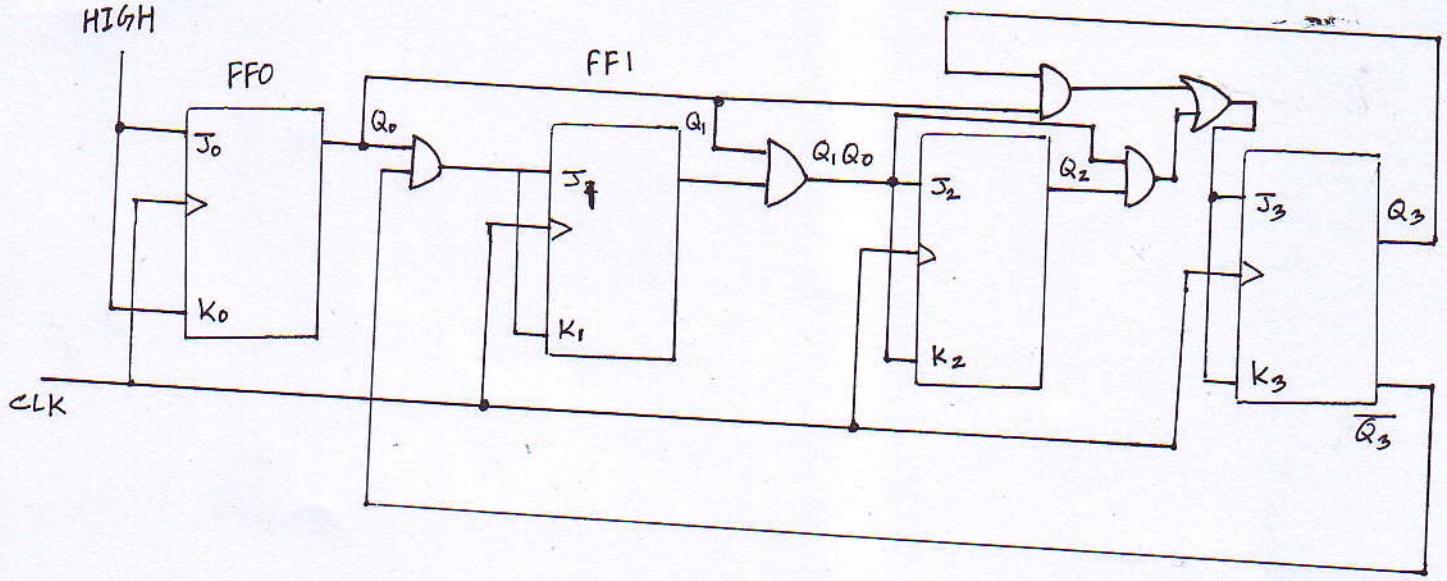


Fig : A synchronous BCD decode counter

Modulus - 12 synchronous counter

State sequence :

Clock pulse	Q_3	Q_2	Q_1	Q_0
Initially	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12 (recycles)	0	0	0	0

$J_0 = K_0 = 1$

$J_1 = K_1 = Q_0$

$J_2 = K_2 = \overline{Q_3} Q_1 Q_0$

$J_3 = K_3 = Q_2 Q_1 Q_0 + Q_3 Q_1 Q_0$