North South University

Department of Computer Science and Engineering

Quiz-3, Section –3, Summer-2021

Course No: **CSE 231** Course Title: **Digital Logic Design**

Time: 20 min Full Marks: 10

Draw the output F for the following D flip flop (falling edge type) input Q. You can assume the initial value of F =0 3

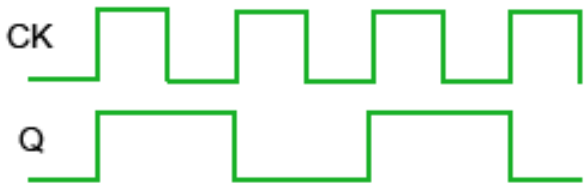

Figure 1 : Timing Diagram

2. Check Figure 2 and answer the following : 7

a. Identify the number of states, inputs and outputs

b. Write down the state equations (Flip Flop Outputs)

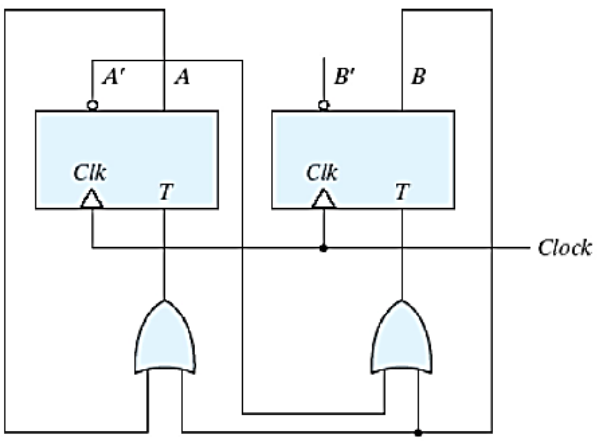

Figure 2 : Sequential Circuit