Lab 6: Introduction to Multiplexers and Decoders

A. Objectives

- Understand the concept of multiplexing in the context of digital logic circuits.
- Learn about the internal logic of digital multiplexers.
- Implement digital logic functions using multiplexers.
- Observe and analyze the operations of the 3 to 8 Line Decoder

B. Theory

Multiplexers: A multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line. The selection of a particular input line is controlled by a set of selection lines. Normally, there are 2^n input lines and n selection lines whose bit combinations determine which input is selected.

A block diagram and truth table for a 4:1 Multiplexer (4 inputs and 1 output) is given below.

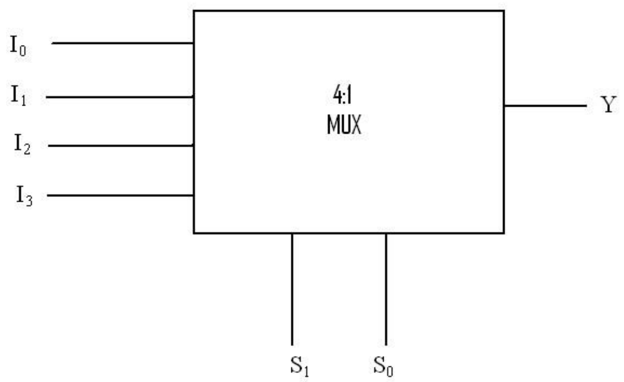

Figure B.1: Block Diagram of a 4:1 Multiplexer

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3
Output Equation: **$Y = I_0S_1'S_0' + I_1S_1'S_2 + I_2S_1S_2' + I_3S_1S_2$**		

Table B.1: Truth Table for a 4:1 Multiplexer

Decoders: A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^n output lines.
Figure B2 shows the block diagram for a 3 to 8 line decoder. Here, x, y and z are the inputs and the combination of their values determines which output line becomes active. Setting all the input values to zero activates the first output line (0), setting x and y to zero and z to 1 activates the second output line (1) and this pattern continues till all the inputs are 1 at which point the eighth output line (7) is activated.

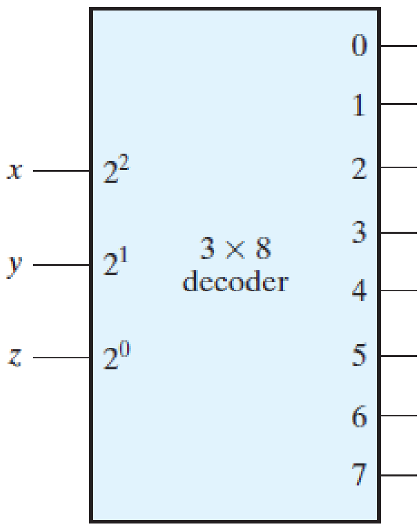

Figure B.2: Block diagram of a 3 to 8 line decoder

New Apparatus:

IC 74151 (8:1 Multiplexer):

The 74151 is a 16 pin IC which requires a Ground connection at pin 8 and V_{CC} at pin 16. Pins 4, 3, 2, 1 and 15, 14, 13, 12 are the inputs, pins 9, 10 and 11 are used to select a particular input and pin 5 is the output. Pin 6 is provides the inverse of the output at pin 5. An input at pin 7 is used to Enable the IC.

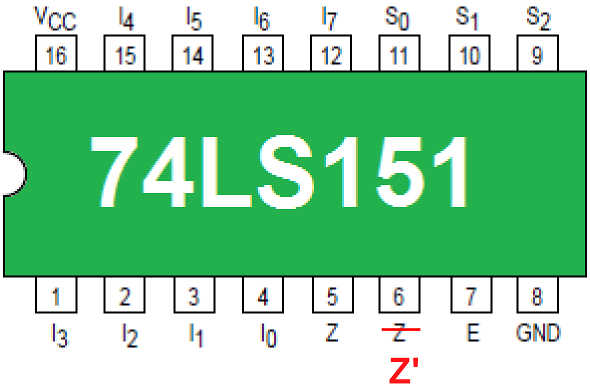

Figure B.3: Pinout of IC74151

IC 74138 (3 to 8 Line Decoder):

The 74138 is also a 16 pin IC which requires Ground at pin 8 and VCC at pin 16. Pins 15, 14, 13, 12, 11, 10, 9 and 7 are used as the outputs and pins 3, 2 and 1 are used to take input. A combination of the inputs at pins 6, 4 and 5 is used to enable the device. In order for the IC to function as intended, pin 6 (G1) must have a high value and both pins 4 and 5 (G2A and G2B) must have low values.

Unlike some of the other ICs used so far, the outputs of the 74138 IC are ACTIVE-LOW which means that they provide a 0 or LOW output when they are activated and a 1 or High output when they are inactive.

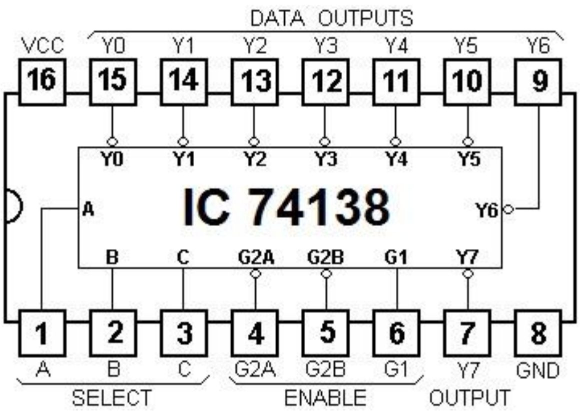

Figure B.4: Pinout of IC74138

Experiment 1: Constructing a 4:1 Multiplexer using basic Logic Gates

C.1 Apparatus

- Trainer Board
- 1 x IC 7404 Hex Inverter (NOT gates)
- 2 x IC 4073 3-input AND gates
- 1 x IC 7432 2-input OR gates

D.1 Procedure

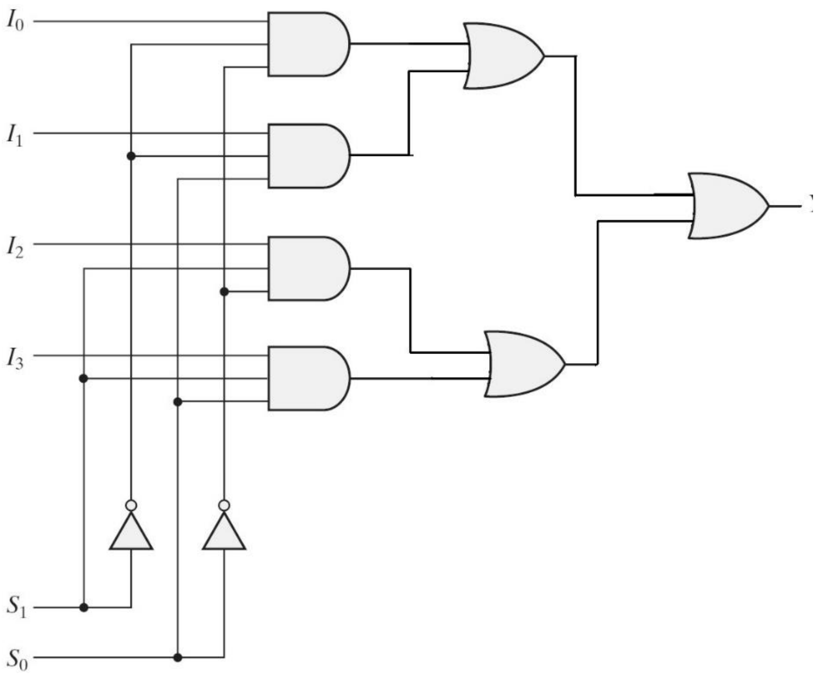

Figure D.1.1: 4:1 Multiplexer

1. Construct the circuit for the 4:1 MUX shown in **Figure D.1.1**.
2. Complete the Theoretical column of the truth table (**Table F.1.1**) for the following function:
   - $F(A, B, C) = \Sigma\,(0, 2, 3, 6)$
3. Now determine the inputs you need to provide to each data input line (I_0, I_1, I_2, I_3) of the MUX if you use A and B as the selection inputs, S_1 and S_0 respectively. Write down the values in the Data Inputs column.
4. Physically implement the function using the 4:1 MUX circuit you constructed.
5. Now complete the Practical column of the truth table.

E.1 Questions

1. Simulate the circuit you built for the 4:1 Multiplexer (**Figure D.1.1**) using Logisim. Include a screenshot of the circuit with your report.

Experiment 2: Using an 8:1 Multiplexer to implement a Boolean function

C.2 Apparatus

- Trainer board
- 1 x IC 74151 (8:1 Multiplexer)

D.2 Procedure

1. Complete the Theoretical column of the truth table (**Table F.2.1**) for the following function:
   - $F(A, B, C, D) = \Sigma\ (0, 1, 3, 7, 9, 10, 14, 15)$
2. Now determine the inputs you need to provide to each data input line (I_0 - I_7) of the MUX if you use A, B and C as the selection inputs, S2, S1 and S0 respectively. Note down the values in the Data Inputs column.
3. Draw the IC diagram (**Figure F.2.1**) for the implementation of the function using the provided 8:1 MUX (IC 74151). Clearly label the inputs and outputs that you will use.
4. Implement the function using the 8:1 MUX.
5. Now complete the Practical column of the truth table.

E.2 Questions

1. Draw the IC diagram (with input values) for the implementation of the following function using IC 74151
   - $F(A, B, C, D) = \Sigma\ (1, 2, 3, 6, 9, 12, 13)$

Experiment 3: Analyzing the behavior of a 3 to 8 Line Decoder (IC74138)

C.3 Apparatus

- Trainer board
- 1 x IC 74138 (3:8 Line Decoder)

D.3 Procedure

1) Wire up the IC 74183 using the diagram in Figure B3 as your reference.
   a) Set the Enable inputs to the appropriate values. G1 should be set to High and both G2A and G2B should be set to Low.
   b) The 3 select inputs (C B A) should be connected to 3 binary switches and the 8 outputs should be connected to individual LEDs. Note that ‘C’ is the highest order bit and ‘A’ is the lowest.
2) Now change the values of the select inputs (C B A) to every combination from LLL to HHH and complete the truth table in Table F.3.1. In this table, use “L” to record a 0 and “H” to record a 1.

E.3 Questions

1. Explain the difference between an active-high and an active-low device.

F. Data Sheet:

Instructor's Signature: ....

Group:	Date:
Section:	Report:

F.1 Experimental Data (Implementing a Boolean function using a 4:1 MUX):

A	B	C	F (Theoretical)	Data Inputs	F (Practical)
0	0	0		I_0 =	
0	0	1			
0	1	0		I_1 =	
0	1	1			
1	0	0		I_2 =	
1	0	1			
1	1	0		I_3 =	
1	1	1			

Table F.1.1

F.2 Experimental Data (Implementing a Boolean function using an 8:1 MUX IC):

A	B	C	D	F (Theoretical)	Data Inputs	F (Practical)
0	0	0	0		I_0 =	
0	0	0	1			
0	0	1	0		I_1 =	
0	0	1	1			
0	1	0	0		I_2 =	
0	1	0	1			
0	1	1	0		I_3 =	
0	1	1	1			
1	0	0	0		I_4 =	
1	0	0	1			
1	0	1	0		I_5 =	
1	0	1	1			
1	1	0	0		I_6 =	
1	1	0	1			
1	1	1	0		I_7 =	
1	1	1	1			

Table F.2.1

Figure F.2.1

F.3 Experimental Data (3 to 8 Line Decoder):

Enable Inputs		Select Inputs			Outputs							
G1	**G2**	**C**	**B**	**A**	**Y_0**	**Y_1**	**Y_2**	**Y_3**	**Y_4**	**Y_5**	**Y_6**	**Y_7**
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L								
H	L	L	L	H								
H	L	L	H	L								
H	L	L	H	H								
H	L	H	L	L								
H	L	H	L	H								
H	L	H	H	L								
H	L	H	H	H								

Table F.3.1