

Lab 8: Synchronous Sequential Circuits

A. Objectives

- Gain a practical understanding of State Diagrams and State Tables.
- Understand the concept of designing Sequential Circuits using Flip-Flops.
- Design and implement a Synchronous Sequential Circuit given a State Diagram.

B. Theory

Synchronous Sequential Circuits: A sequential circuit, as shown in **Figure B1**, consists of a combinational circuit to which storage elements are connected to form a feedback path. The storage elements (usually Flip-Flops) are devices capable of storing binary information. The binary information stored in these elements at any given time defines the state of the sequential circuit at that time. The sequential circuit receives binary information from external inputs that, together with the present state of the storage elements, determine the binary value of the outputs. The next state of the storage elements is a function of external inputs and the present state. Thus, a sequential circuit is specified by a time sequence of inputs, outputs, and internal states. In contrast, the outputs of combinational logic depend only on the present values of the inputs.

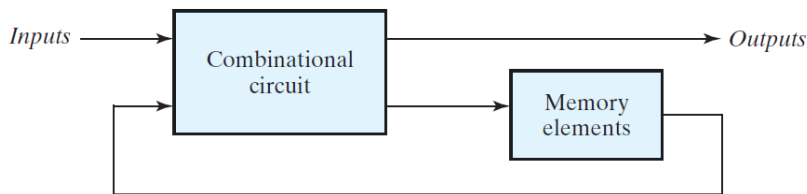


Figure B1: Sequential Circuit: Block Diagram

There are two main types of sequential circuits, and their classification is a function of the timing of their signals. A synchronous sequential circuit is a system whose behavior can be defined from the knowledge of its signals at discrete instants of time. The behavior of an asynchronous sequential circuit depends upon the input signals at any instant of time and the order in which the inputs change.

A synchronous sequential circuit (outlined in **Figure B2**) employs signals that affect the storage elements at only discrete instants of time. Synchronization is achieved by a timing device called a clock generator, which provides a clock signal having the form of a periodic train of clock pulses. The clock signal is commonly denoted by the identifiers clock and clk. The clock pulses are distributed throughout the system in such a way that storage elements are affected only with the arrival of each pulse.

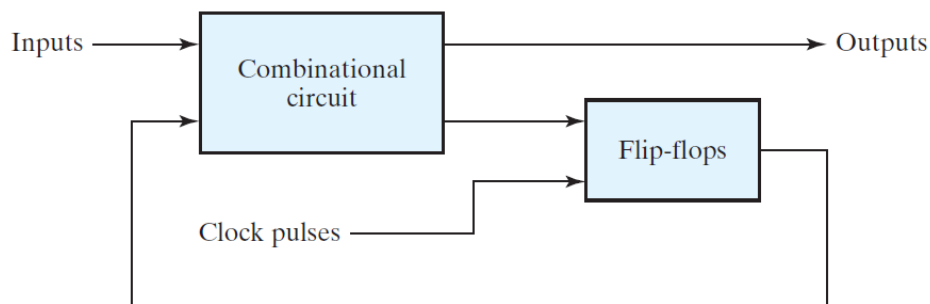


Figure B2: Synchronous Sequential Circuit: Block Diagram

In order to analyze and design Synchronous Sequential Circuits, we need to use State Tables and State Diagrams. The **State Table** (or Transition Table) shows how the state and output of the sequential circuit changes with respect to the current state and input. **State Diagrams** are simply graphical forms of the State Tables. In this type of diagram, a state is represented by a circle, and the (clock-triggered) transitions between states are indicated by directed lines connecting the circles. The binary number inside each circle identifies the state of the flip-flops. The directed lines are labeled with two binary numbers separated by a slash. The input value during the present state is labeled first, and the number after the slash gives the output during the present state with the given input.

Figure B3 shows the State Table and State Diagram for a Sequential Circuit.

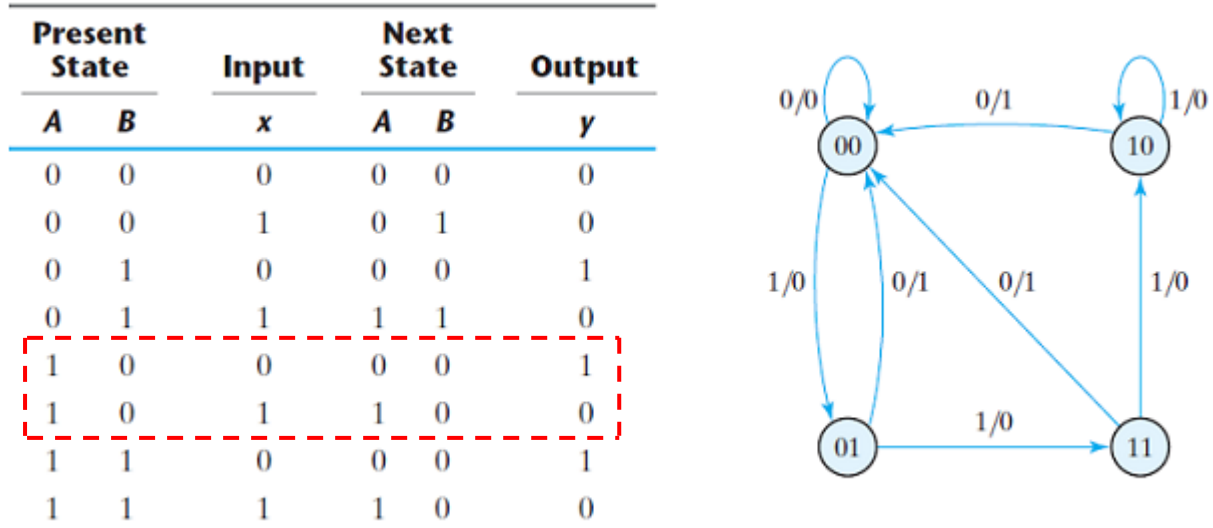
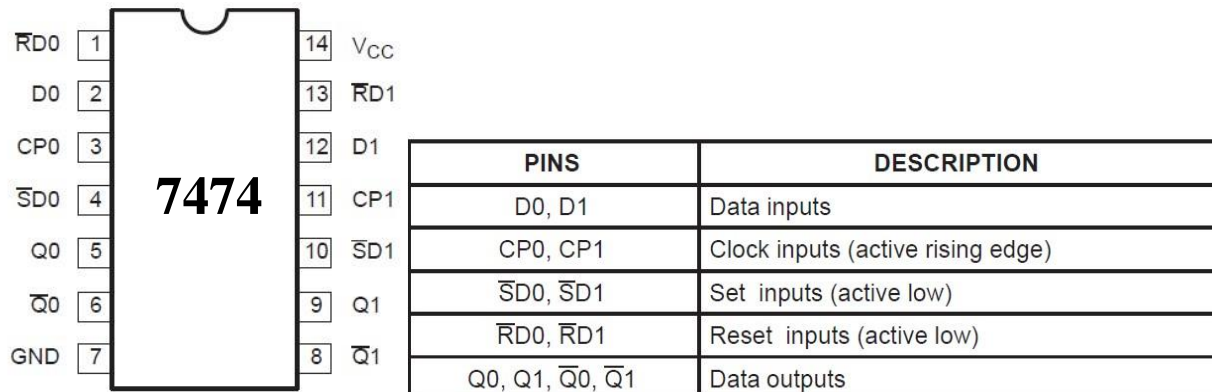


Figure B3: State Table and Diagram Example

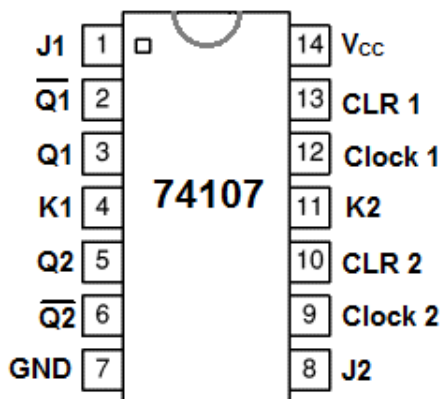
Let's take a look at the State '10' ($A = 1$ and $B = 0$; top right circle in the state diagram) to understand how the State Table and Diagram works. When '10' is the Present State, an input value of 0 will cause the output to become 1 ($x = 0$, $y = 1$ in the table; the arrow going left from circle '10' toward circle '00' in the diagram). This will also cause the state to change to '00'.

Alternately, an input of 1 in this state ('10') will cause the output to become 0 ($x = 1$, $y = 0$ in the table; the arrow looping from '10' back to '10' in the diagram). However, the state will remain unchanged.

All the other state transitions can be analyzed in this way.

New Apparatus:**IC 7474 (Dual D Flip-Flops):****Figure B4:** Pinout of IC7474

The 7474 is a 14 pin IC which requires a Ground connection at pin 7 and V_{CC} at pin 14. Pins 2 and 12 serve as the inputs for the two Flip-Flops and pins 5 and 9 act as the corresponding outputs. Pins 6 and 8 provide the inverse of the outputs. Pin 3 is the clock input for the first Flip-Flop and pin 11 is the clock input for the second Flip-Flop. The set and reset inputs for each Flip-Flop (pin 4, pin 1 and pin 10, pin 13) all have to be supplied a logic 1 in order for the Flip-Flops to work.

IC 74107 (Dual JK Flip-Flops):

The 74107 is a 14 pin IC which requires a Ground connection at pin 7 and V_{CC} at pin 14. Pins 1 and 4 serve as the J and K inputs for the first Flip-Flop and pins 8 and 11 act as the J and K inputs for the second Flip-Flop. Pins 2 and 5 are the outputs of Flip-Flop 1 and Flip-Flop 2 respectively. Pin 12 is the clock input for the first Flip-Flop and pin 9 is the clock input for the second Flip-Flop. The CLR 1 and CLR 2 inputs (pin 13 and pin 10, respectively) have to be supplied with logic 1 or 0 depending on the internal implementation of the particular IC.

Figure B5: Pinout of IC74107

Experiment 1: Constructing a Sequential Circuit using JK Flip-Flops

C.1 Apparatus

- Trainer board
- 1 x IC 74107 JK Flip-Flop
- 1 x IC 7408 2-input AND gates
- 1 x IC 7404 Hex inverters (NOT gates)

D.1 Procedure

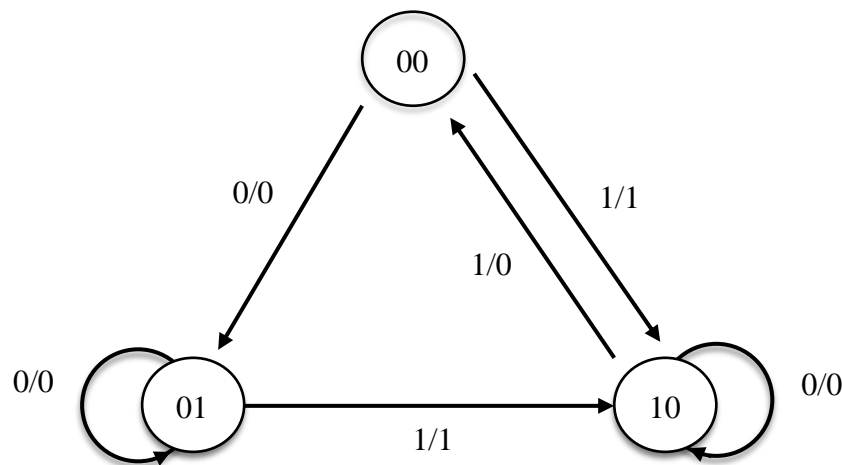


Figure D.1.1 State Diagram for a Synchronous Sequential Circuit

The given State Diagram represents a circuit that has two Flip-Flops (A and B), one input (X) and one output (Y). The unused states should be treated as don't-care conditions.

1. Complete the **Next State** and **Output** columns of the State Table (**Table F.1.1**).
2. Now, use the Excitation Table of the JK Flip-Flop (Table D.1.1) to determine the inputs for the two Flip-Flops (J_A , J_B and K_A , K_B) for each state transition.

Q	Q _{next}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Table D.1.1: JK flip-flop: Excitation Table

3. Use Karnaugh Maps to minimize the functions of the combinational circuit for each Flip-Flop input (J_A , K_A , J_B and K_B) as well as the combinational circuit for the output (Y).
4. Draw the diagram for the Synchronous Sequential Circuit using JK Flip-Flops and the minimized equations.
5. Construct the circuit using the given ICs.
6. Verify that the state transitions and outputs of your completed circuit match those in the State Table (**Table F.1.1**) you prepared earlier.

E.1 Report

1. Simulate the sequential circuit you built (**Figure F.1.1**) using Logisim. Include a screenshot of the circuit with your report.

Experiment 2: Constructing a Sequential Circuit using T Flip-Flops

C.2 Apparatus

- Trainer board
- 1 x IC 74107 JK Flip-Flop
- 1 x IC 7408 2-input AND gates
- 1 x IC 7432 2-input OR gates
- 1 x IC 7404 Hex Inverter (NOT gates)

D.2 Procedure

This time, you need to create the same sequential circuit using T Flip-Flops in place of JK Flip-Flops.

1. Complete the **Next State** and **Output** columns of the State Table (**Table F.2.1**).
2. Now, use the Excitation Table of the T Flip-Flop (**Table D.2.1**) to determine the inputs for the two Flip-Flops (T_A and T_B) for each state transition.

Q	Q_{next}	T
0	0	0
0	1	1
1	0	1
1	1	0

Table D.2.1: T flip-flop: Excitation Table

3. Use Karnaugh Maps to minimize the functions of the combinational circuit for each Flip-Flop input (T_A and T_B) as well as the combinational circuit for the output (Y).
4. Draw the diagram for the Synchronous Sequential Circuit using T Flip-Flops and the minimized equations.
5. Construct the circuit using the given ICs. Use the diagram in **Figure D.2.1** to construct a T Flip-Flop using the given JK Flip-Flop IC 74107.
6. Verify that the state transitions and outputs of your completed circuit match those in the State Table (**Table F.2.1**) you prepared earlier.

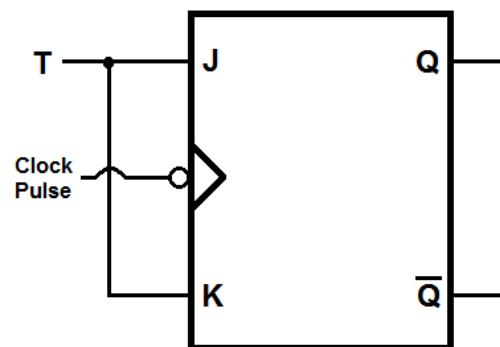


Figure D.2.1: T flip-flop constructed using JK flip-flop

E.2 Report

1. Is the output equation (Y) of this circuit the same as the equation in the JK Flip-Flop circuit? Explain why.

Experiment 3: Constructing a Sequential Circuit using D Flip-Flops

C.3 Apparatus

- Trainer board
- 1 x IC 7474 Dual D Flip-Flops
- 1 x IC 7408 2-input AND gates
- 1 x IC 7432 2-input OR gates
- 1 x IC 7404 Hex Inverter (NOT gates)

D.3 Procedure

Now, you need to create the same sequential circuit using D Flip-Flops in place of T Flip-Flops.

1. Complete the **Next State** and **Output** columns of the State Table (**Table F.3.1**).
2. Now, use the Excitation Table of the D Flip-Flop (**Table D.3.1**) to determine the inputs for the two Flip-Flops (D_A and D_B) for each state transition.

Q	Q_{next}	D
0	0	0
0	1	1
1	0	0
1	1	1

Table D.3.1: D flip-flop: Excitation Table

3. Use Karnaugh Maps to minimize the functions of the combinational circuit for each Flip-Flop input (D_A and D_B) as well as the combinational circuit for the output (Y).
4. Draw the diagram for the Synchronous Sequential Circuit using D Flip-Flops and the minimized equations.
5. Construct the circuit using the given ICs. You will use the D Flip-Flops in IC 7474.
6. Verify that the state transitions and outputs of your completed circuit match those in the State Table (**Table F.3.1**) you prepared earlier.

E.3 Report

1. Draw the IC diagram for the logic circuit in **Figure F.3.1**

Instructor's Signature:

Group:	Date:
Section:	Report:

Present state		Input	Next state		Output	Flip-flop input functions			
A	B	X	A	B	Y	J _A	K _A	J _B	K _B
0	0	0	0	1	0	0	X	1	X
0	0	1	1	0	1	1	X	0	X
0	1	0							
0	1	1							
1	0	0							
1	0	1							
1	1	0							
1	1	1							

Table F.1.1: State Table for circuit using JK Flip-Flops

$$J_B =$$

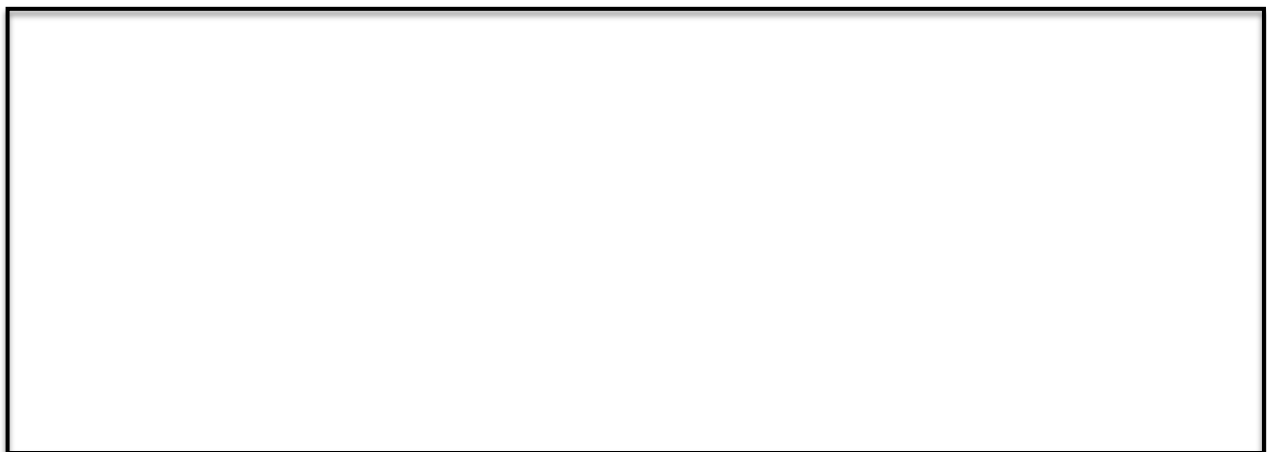
$$Y =$$


Figure F.1.1: Circuit Diagram

F.2 Experimental Data: Constructing a Sequential Circuit using T Flip-Flops

Present state		Input	Next state		Output	Flip-flop input functions	
A	B	X	A	B	Y	T _A	T _B
0	0	0	0	1	0	0	1
0	0	1	1	0	1	1	0
0	1	0					
0	1	1					
1	0	0					
1	0	1					
1	1	0					
1	1	1					

Table F.2.1: State Table for circuit using T Flip-Flops

T_A =

T_B =

Y =**Figure F.2.1:** Circuit Diagram

F.3 Experimental Data: Constructing a Sequential Circuit using D Flip-Flops

Present state		Input	Next state		Output	Flip-flop input functions	
A	B	X	A	B	Y	D _A	D _B
0	0	0	0	1	0	0	1
0	0	1	1	0	1	1	0
0	1	0					
0	1	1					
1	0	0					
1	0	1					
1	1	0					
1	1	1					

Table F.3.1: State Table for circuit using D Flip-Flops

D_A =

D_B =

Y =**Figure F.3.1:** Circuit Diagram