

North South University
Department of Electrical & Computer Engineering

Course Code: CSE231L

Course Title: Digital Logic Design

Faculty: DR. M ABDUR RAZZAK

**Project Report of “Design a Combinational Logic
Circuit to display “IUBFALL” in a Seven Segment
Display**

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Section: 07

Group Number:02

Submitted To: MD. AL – AMIN BHUIYAN

Submitted By

S.N.	Student Name	ID
9	Al Zammee	2021648642
12	Umme Suraia Haque Setu	2031278642
18	Humayra Rahman Nipa	2121128642
24	Saif Mohammed	2121913642
35	Afra Saiara Saima	2132242642

CSE231 Lab Project Report

2. Executive Summary

This project is about displaying the English letters “IUBFALL” with the help of seven segment device. We built MUX Expression forms to indicate the letters for the combinational circuit. We will use a cathode seven-segment display using combinational and sequential circuits in this project. We created a Truth Table to determine what pins need to be active for each letter. After completing that, we implemented the Boolean function using K-Map and designed our combinational circuits accordingly. We applied the simplified expressions for each form and determined which circuit design was the most efficient in terms of cost and power consumption.

3. Background

We need this seven-segment display project to understand how to design logic through combinational and sequential circuits. We can also become familiar with the Boolean Algebra, K- Map through this project. In a digital logic design project, a seven-segment display is used as part of the overall system design to display numerical information to the user. For example, a digital clock may use a seven-segment display to show the current time, or a calculator may use a seven-segment display to show the calculation result. So, we need this project to implement digital logic and practically design it. And also know to minimize costs in design.

The project is developed based on Boolean functions, MUX expression form, logic gates and a seven-segment display. So, to develop the project, we need to understand these concepts first and then apply them practically using ICs on the trainer board.

The project is being proposed on MUX. There are several reasons why MUXes are helpful in digital design:

- MUXes can reduce the number of connections and gates needed in a circuit, which makes it easier to design and debug.
- MUXes can implement logical functions such as AND, OR, and NOT, often used in digital circuits.
- MUXes can be used to implement arithmetic functions such as addition and subtraction, which are also commonly used in digital circuits.

- MUXes can be used to implement state machines, which control the behaviour of digital circuits.
- MUXes can implement memory elements such as registers and flip-flops, which store data in digital circuits.

Overall, MUXes are a versatile and essential component of digital design, and they are used in a wide variety of applications.

4. Objective of the Project

The objectives of the seven-segment display project are:

- Implementation of the Boolean logic operation and Boolean Algebra: In this project, we apply Boolean logic and algebra to find the MUX form and show the letters in the display.
- Implementing Boolean Algebra and K-maps to realize two-level minimal/optimal combinational circuits: We need Boolean algebra and K-Map for the minimal combinational circuit to build a sequential circuit.
- The design process of combinational and sequential circuits: We must design combinational and sequential circuits using logic gates. Such as NOT, OR, and NAND.
- The operation of latches and flip-flops: We need to use J-K Flip flop to build sequential circuits for the combinational part.
- The simulation tool for digital system design: For this project, we use Logisim simulation software for the theoretical part.
- Displaying numerical or alphanumeric information: In this project, we show seven alphabets “IUBFALL” one by one on seven segment display.
- Learning about electronics and programming: By doing this project, we are learning about digital electronics and how to design it with logical expression and build programming knowledge.

5. Project Work Plan and Human Resources

• Truth Table

Letters	Inputs			Outputs						
	A	B	C	a	b	c	d	e	f	g
I	0	0	0	0	0	0	0	1	1	0
U	0	0	1	0	1	1	1	1	1	0
B	0	1	0	1	1	1	1	1	1	1
F	0	1	1	1	0	0	0	1	1	1
A	1	0	0	1	1	1	0	1	1	1
L	1	0	1	0	0	0	1	1	1	0
L	1	1	0	0	0	0	1	1	1	0
	1	1	1	X	X	X	X	X	X	X

Truth Table: "TUBFALL"

Letters	A	Data Select		Inputs								Outputs							
		B(s ₁)	C(s ₂)	a	b	c	d	e	f	g	Minterms	a	b	c	d	e	f	g	
I	0	0	0	0	0	0	0	1	1	0	I ₀	\bar{A}	A	A	0			\bar{A}	$a = I_0 \bar{s}_1 \bar{s}_0 + I_1 \bar{s}_1 \bar{s}_0 + I_2 \bar{s}_1 \bar{s}_0 + I_3 \bar{s}_1 \bar{s}_0$
U	0	0	1	0	1	1	1	1	1	0									
B	0	1	0	1	1	1	1	1	1	1	I ₁	\bar{A}	\bar{A}	\bar{A}	A			\bar{A}	$b = I_0 \bar{s}_1 \bar{s}_0 + I_1 \bar{s}_1 \bar{s}_0 + I_2 \bar{s}_1 \bar{s}_0 + I_3 \bar{s}_1 \bar{s}_0$
F	0	1	1	1	0	0	0	1	1	1							1	1	
A	1	0	0	1	1	1	0	1	1	1	I ₂	0	\bar{A}	\bar{A}	A			0	$c = I_0 \bar{s}_1 \bar{s}_0 + I_1 \bar{s}_1 \bar{s}_0 + I_2 \bar{s}_1 \bar{s}_0 + I_3 \bar{s}_1 \bar{s}_0$
L	1	0	1	0	0	0	1	1	1	0									
L	1	1	0	0	0	0	1	1	1	0	I ₃	A	0	0	A			A	$d = I_0 \bar{s}_1 \bar{s}_0 + I_1 \bar{s}_1 \bar{s}_0 + I_2 \bar{s}_1 \bar{s}_0 + I_3 \bar{s}_1 \bar{s}_0$
	1	1	1	X	X	X	X	X	X	X									
																			$e = 1$
																			$f = 1$
																			$g = I_0 \bar{s}_1 \bar{s}_0 + I_1 \bar{s}_1 \bar{s}_0 + I_2 \bar{s}_1 \bar{s}_0 + I_3 \bar{s}_1 \bar{s}_0$

Table: 4:1 MUX

- State Diagram

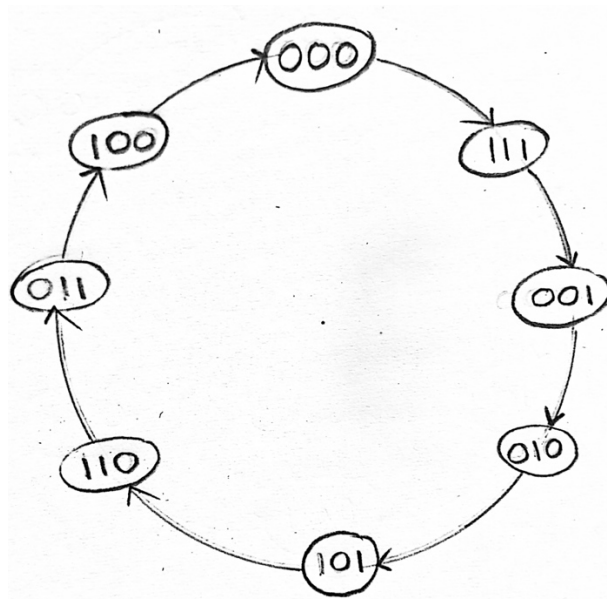


Figure: State Diagram of “TUBFALL”

- State Table

Output			Inputs					
Present State Q _A Q _B Q _C	Next State Q _A [*] Q _B [*] Q _C [*]		J _A K _A	J _B K _B	J _C K _C			
000	111		1 x	1 x	1 x			
111	001		x 1	x 1	x 0			
001	010		0 x	1 x	x 1			
010	101		1 x	x 1	1 x			
101	010		x 0	1 x	x 1			
110	011		x 1	x 0	1 x			
011	100		1 x x	x 1	x 1			
100	000		x 1 1	0 x	0 x			

- K-Map

K-Map for J_A

Q_C	$\overline{Q_C}$	Q_C
$\overline{Q_A}\overline{Q_B}$	1	0
$\overline{Q_A}Q_B$	1	1
$Q_A\overline{Q_B}$	x	x
Q_AQ_B	x	x

$$J_A = \overline{Q_C} + Q_B$$

K-map for K_A

Q_C	$\overline{Q_C}$	Q_C
$\overline{Q_A}\overline{Q_B}$	x	0
$\overline{Q_A}Q_B$	x	x
$Q_A\overline{Q_B}$	1	1
Q_AQ_B	1	0

$$K_A = \overline{Q_C} + Q_B$$

K-Map for J_B

Q_C	$\overline{Q_C}$	Q_C
$\overline{Q_A}\overline{Q_B}$	1	1
$\overline{Q_A}Q_B$	x	x
$Q_A\overline{Q_B}$	x	x
Q_AQ_B	0	1

$$J_B = Q_C + \overline{Q_A}$$

K-Map for K_B

Q_C	$\overline{Q_C}$	Q_C
$\overline{Q_A}\overline{Q_B}$	x	x
$\overline{Q_A}Q_B$	1	1
$Q_A\overline{Q_B}$	0	1
Q_AQ_B	x	x

$$K_B = Q_C + \overline{Q_A}$$

K-Map for J_C

	$\overline{Q_C}$	Q_C
$\overline{Q_A}\overline{Q_B}$	1	x
$\overline{Q_A}Q_B$	1	x
$Q_A\overline{Q_B}$	1	x
Q_AQ_B	0	x

$$J_C = \overline{Q_A} + Q_B$$

K-Map for K_C

Q_C	$\overline{Q_C}$	Q_C
$\overline{Q_A}\overline{Q_B}$	x	1
$\overline{Q_A}Q_B$	x	1
$Q_A\overline{Q_B}$	x	0
Q_AQ_B	x	1

$$K_C = \overline{Q_A} + Q_B$$

K-Map: Sequential Part (J-K Flip Flop)

- **Circuit Diagram**

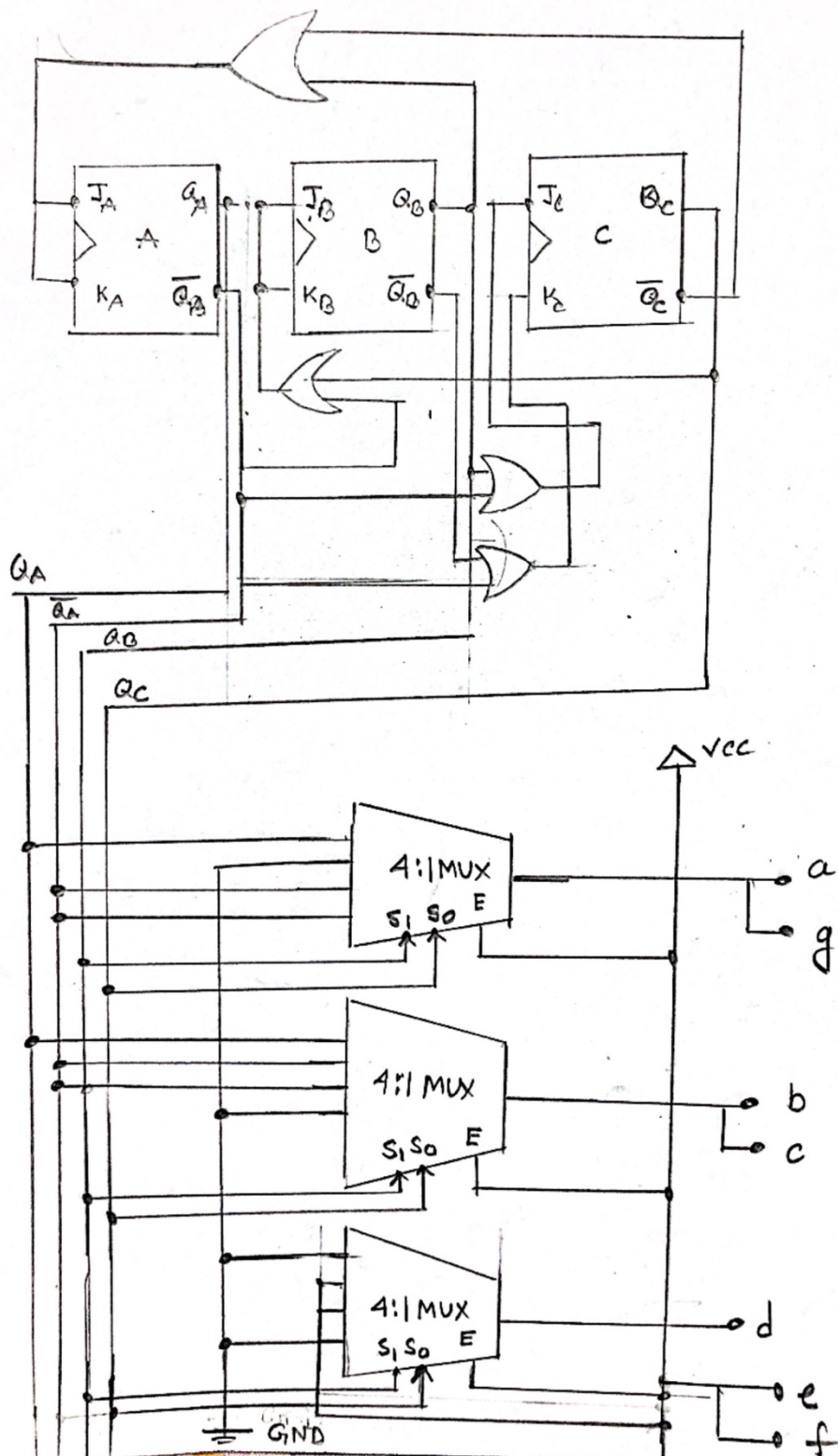
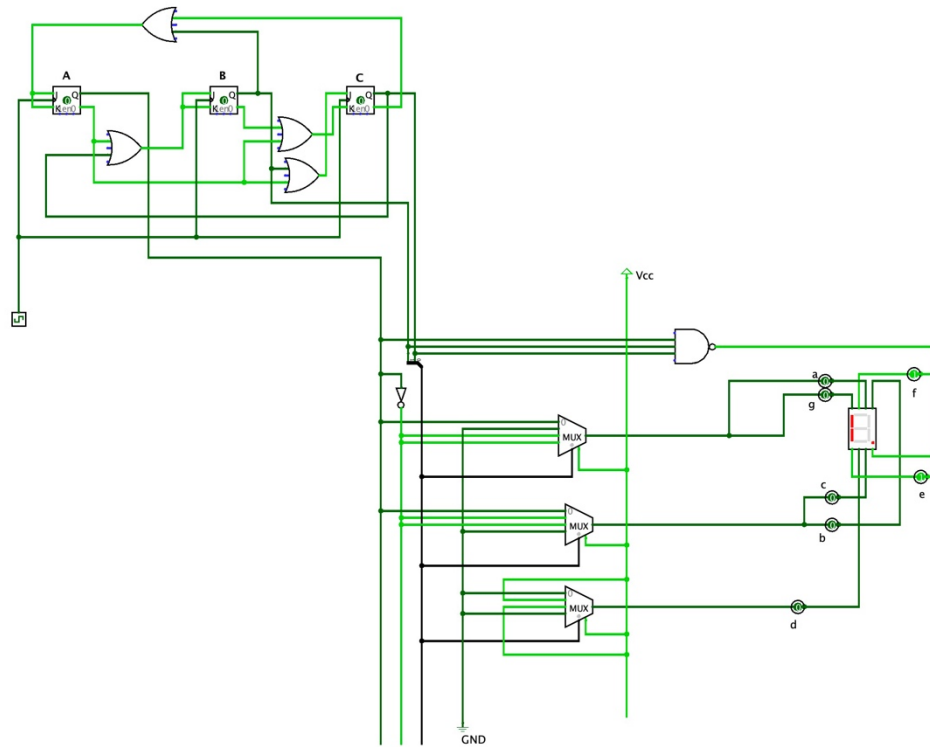
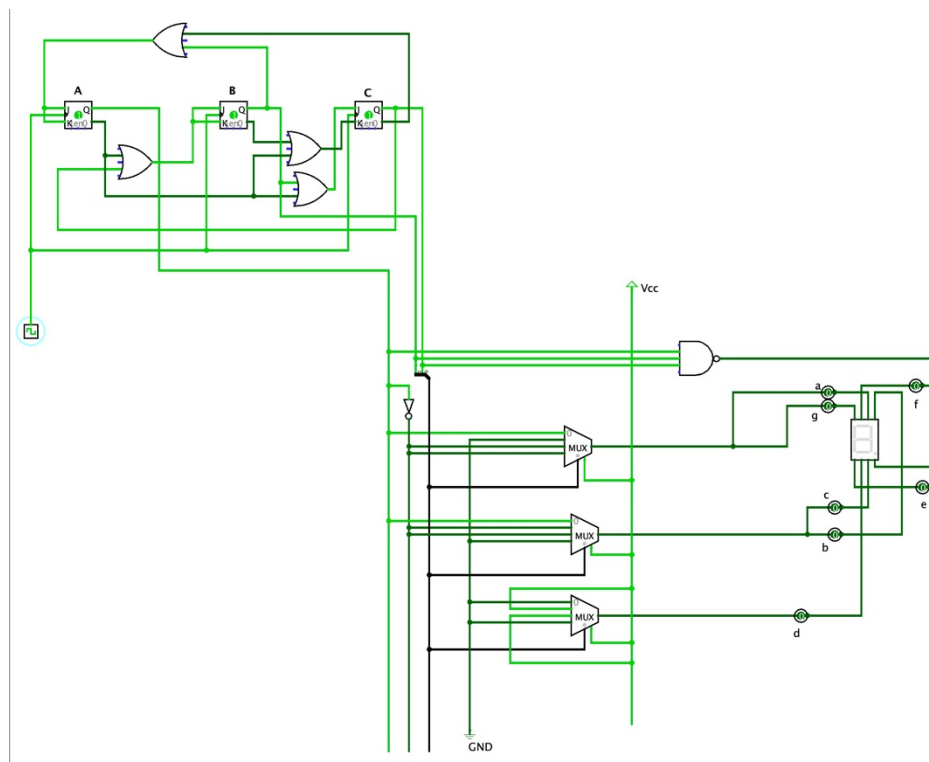


Figure: Circuit Diagram Combinational and Sequential part

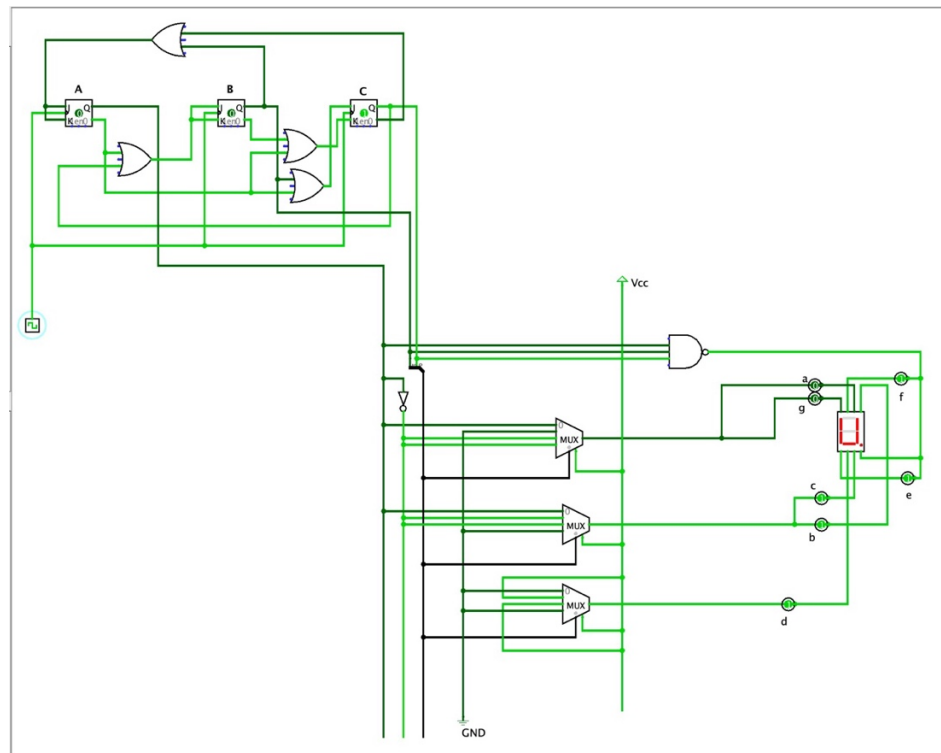
Logisim Simulation



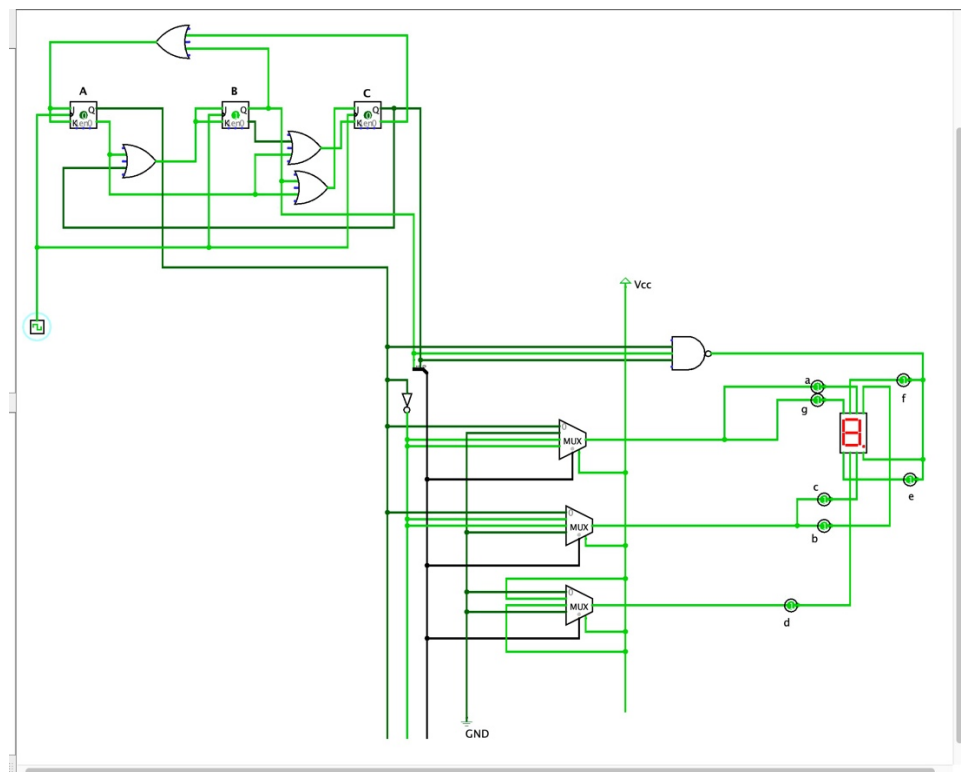
Screenshot 1: State – 000 – Letter – “I”



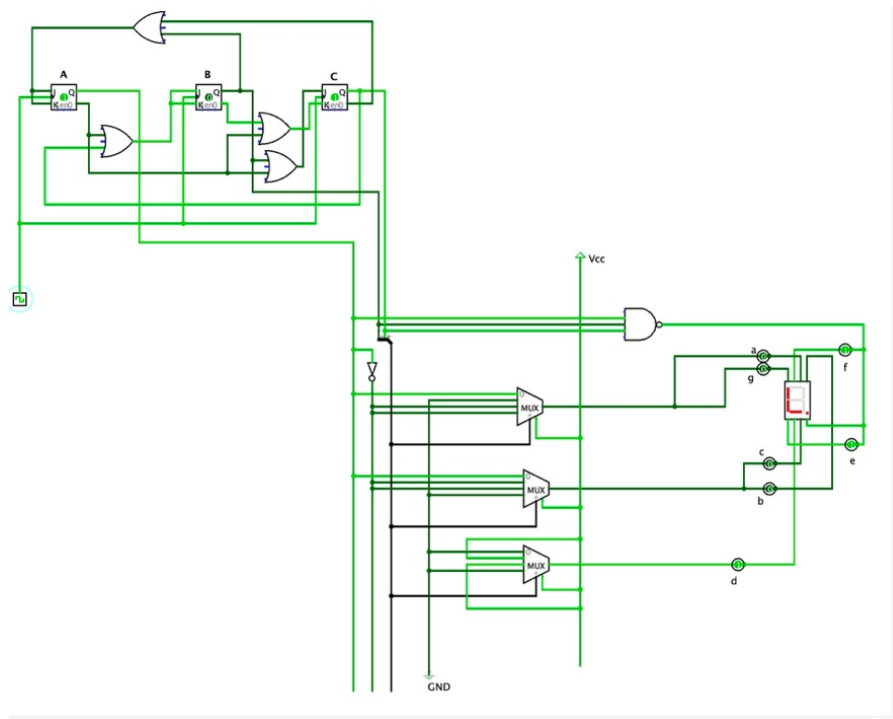
Screenshot 2: State – 111 – Letter – “Blank”



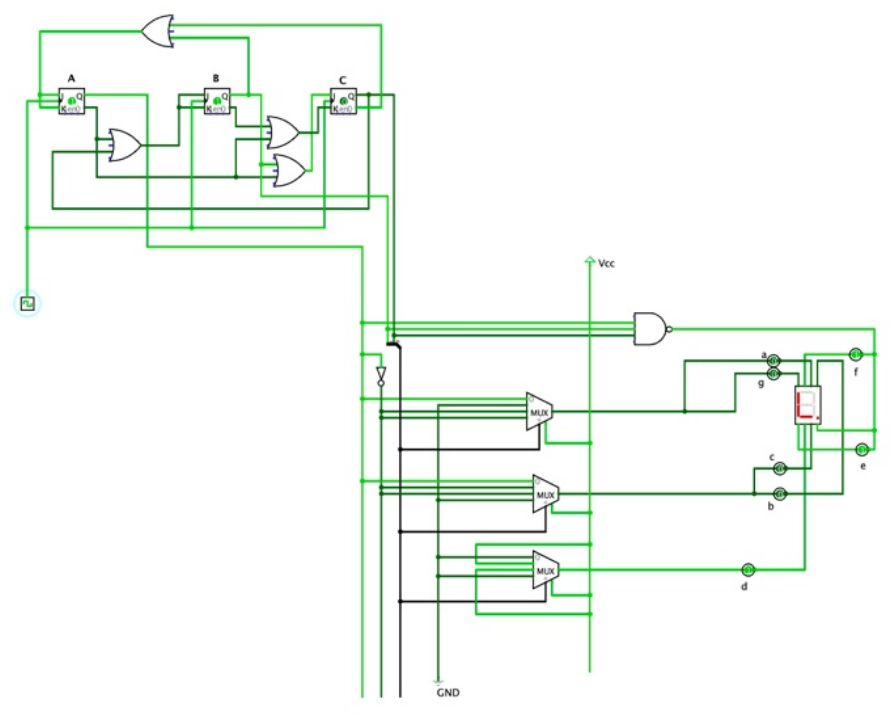
Screenshot 3: State – 001 – Letter – “U”



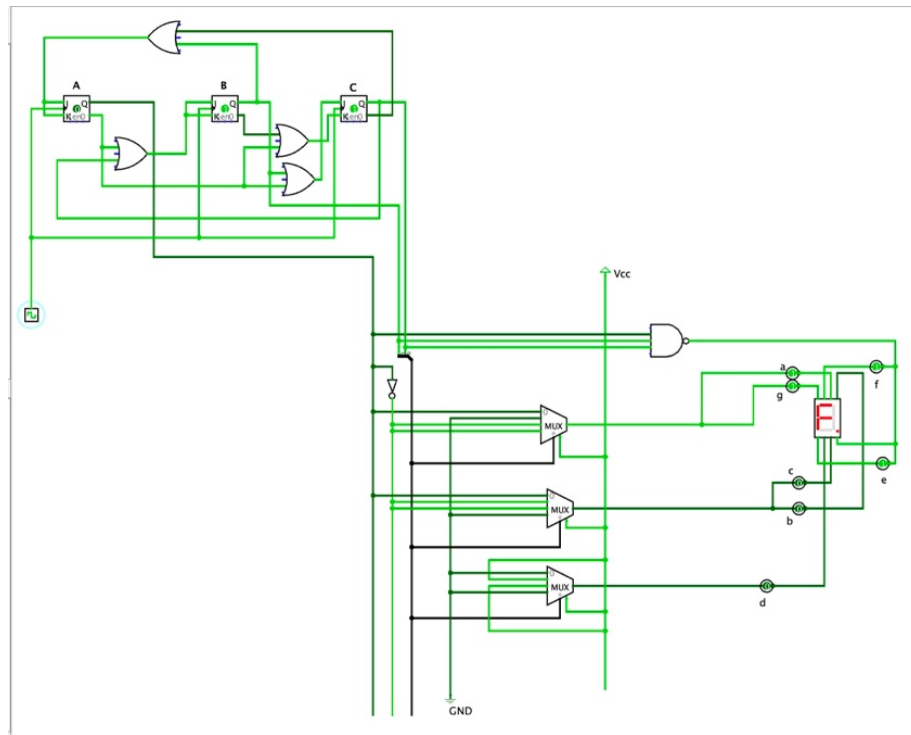
Screenshot 4: State – 010 – Letter – “B”



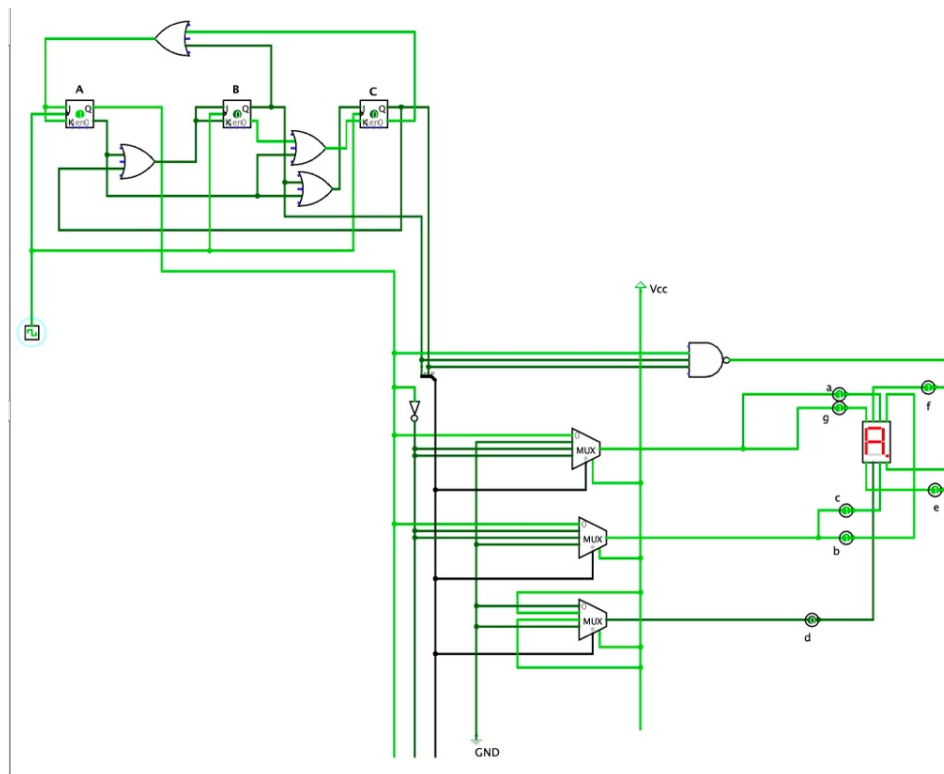
Screenshot 5: State – 101 – Letter – “L”



Screenshot 6: State – 110 – Letter – “L”



Screenshot 7: State – 011 – Letter – “F”



Screenshot 8: State – 100 – Letter – “A”

In this project, we apply Boolean logic and algebra to find the MUX form and show the letters in the display which satisfy the Implementation of the Boolean logic operation and Boolean Algebra objective. Then, we build K- Map for the minimal combinational circuit to build a sequential circuit. It satisfies the implementation of Boolean Algebra and K-maps to realize two-level minimal/optimal combinational circuits. After that, we design combinational and sequential circuits using logic gates. Such as NOT, OR, and NAND. It satisfies the objective design process of combinational and sequential circuits. We have used J-K Flip flop to build sequential circuits for the combinational part, which fulfils the operation of latches and flip-flops. For this project, we use Logisim simulation software for the theoretical part, which satisfies the simulation tool for the digital system design objective. Then we show seven alphabets “IUBFALL” one by one on seven segment display which helps display numerical or alphanumeric information.

At the end of the project, we are learning about digital electronics and how to design it with logical expression and build programming knowledge.

- **Human Resource**

Work Distribution (Topics)	Work done by
1. Logisim Simultaltion 2. MUX Table	Saif Mohammed 2121913642 (Coordinator)
1. Circuit Diagram	Al Zammee 2021648642
1. Truth table	Humayra Rahman Nipa 2121128642
1. State Table	Umme Suraia Haque Setu 2031278642
1. K-Map	Afra Saiara Saima 2132242642

6. Proposed Budget

As we are using Multiplexer to display “IUBFALL” letters, we need

2-IC 74LS153 (4:1 MUX) cost= 90 Tk

1-IC 7400 (2-input NAND gate) cost = 30 Tk

1-IC 7404 (2-input NOT gate) cost = 30 TK

3-Breadboard cost = 450 Tk

1-9V Battery cost = 100 TK

1-IC 7805 (Register) = 15 Tk

Wires Set cost = 180 Tk

1-Cathode 7 Segment Display = 15 Tk

2-IC 4027 (Dual J-k Flip-Flop) = 60 TK

1- IC 7432 (2-input OR gate) = 30 TK

1-IC 555 = 20 TK

Total cost = 930 Tk

So, the proposed budget for the project is 930 Tk.

7. Conclusion

Overall, this muxed 7-segment display project can be a valuable tool for displaying large amounts of information in a limited space. With the proper hardware and software, we can use it to create a wide variety of interactive displays and projects within a short time and at a minimum cost.