8-bit ALU using VHDL and implement on FPGA and evaluate power and timing performance.

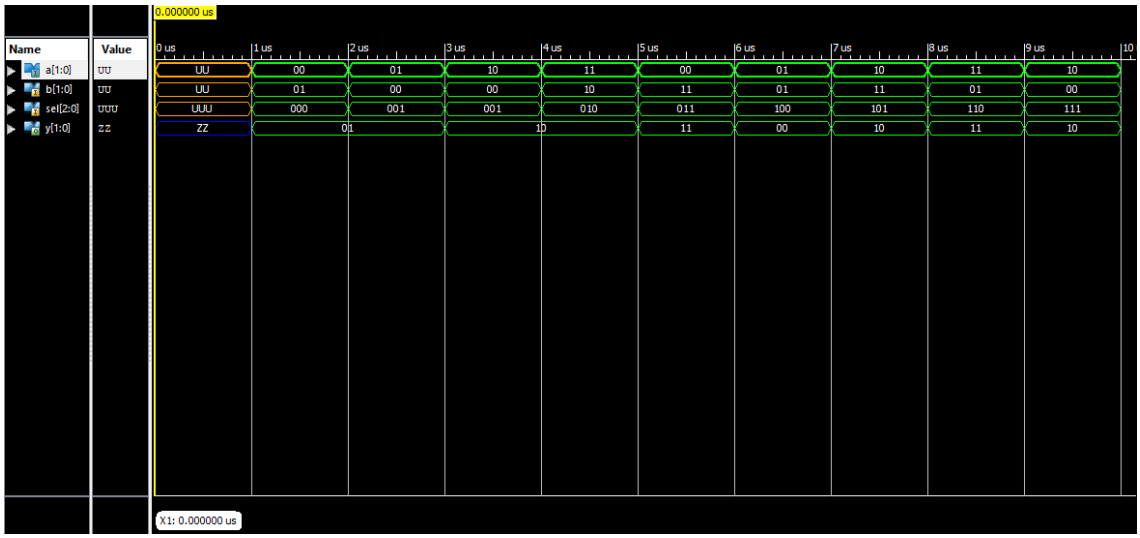
Program:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity Expt_1b is
   Port ( A : in  STD_LOGIC_VECTOR(1 downto 0);
          B : in  STD_LOGIC_VECTOR(1 downto 0);
          sel : in  STD_LOGIC_VECTOR(2 downto 0);
          Y : out  STD_LOGIC_VECTOR(1 downto 0));
end Expt_1b;

architecture Behavioral of Expt_1b is
begin
process(A,B,sel)
  begin
    case sel is
 when "000" => Y <=A+B;
 when "001" => Y <=A-B;
 when "010" => Y <=A AND B;
 when "011" => Y <=A NAND B;
 when "100" => Y <=A XOR B;
 when "101" => Y <=A XNOR B;
 when "110" => Y <=A OR B;
 when "111" => Y <=A;
 when others => Y <="ZZ";
   end case;
end process;
end Behavioral;
```

UCF (User Constraint File):

```
Net"A<0>"LOC="A10";
Net"A<1>"LOC="D14";
Net"B<0>"LOC="C14";
Net"B<1>"LOC="P15";
Net"sel<0>"LOC="P12";
Net"sel<1>"LOC="R5";
Net"sel<2>"LOC="T5";
Net"Y<0>"LOC="U18";
Net"Y<1>"LOC="M14";
```


0.000000 us
Name
Value
a[1:0]
b[1:0]
sel[2:0]
y[1:0]
UU
UU
UUU
ZZ
0 us
1 us
2 us
3 us
4 us
5 us
6 us
7 us
8 us
9 us
10
00 01 10 11 00 01 10 11 10
01 00 00 10 11 01 11 01 00
000 001 001 010 011 100 101 110 111
01 10 11 00 10 11 10
X1: 0.000000 us

Implementation on FPGA Board: