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Part 1

① a. Data hazard - when a planned instruction cannot execute in the proper clock cycle b/c data that's needed to execute the instruction is not yet available

b. Control hazard - when the proper instruction can't execute in the proper pipeline clock cycle b/c the instruction that was fetched is not the one that's needed

c. structural hazard - a planned instruction can't execute in the proper clock cycle b/c the hardware does not support the combination of instructions

② a. forwarding (or bypassing)
b. branch prediction

③ a. true
b. false
c. true
d. false

④ 1. Instruction fetch - during this, the next instruction is fetched from instruction memory. The right half of IM is shaded to depict that the memory is read
2. Instruction decode - the instruction's fields are converted into datapath control signals, and simultaneously the register file is read
3. Execute - the ALU is used to perform the instructions operation or to compute an address
4. Data memory access - the data memory may be read or written
5. Write back - the register file may be written by certain instructions (like R-type instructions)

(5) a. clock cycle

b. instruction fetch stage

c.